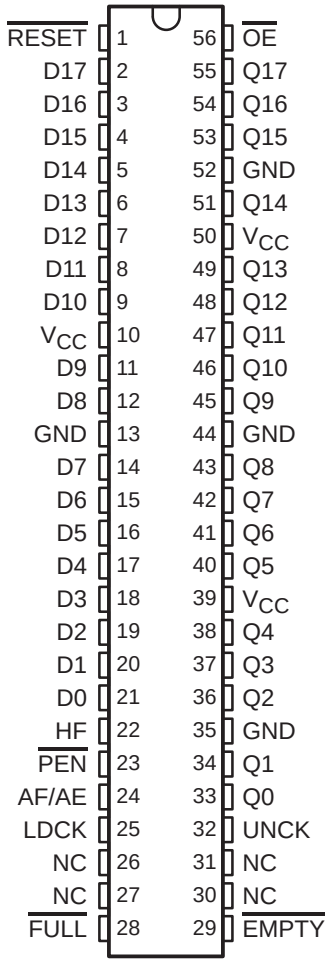
- **Member of the Texas Instruments Widebus™ Family**
- **Low-Power Advanced CMOS Technology**
- **Operates From 3-V to 3.6-V V_{CC}**
- **Load Clock and Unload Clock Can Be Asynchronous or Coincident**
- **Full, Empty, and Half-Full Flags**
- **Programmable Almost-Full/Almost-Empty Flag**
- **Fast Access Times of 18 ns With a 50-pF Load and All Data Outputs Switching Simultaneously**
- **Data Rates up to 40 MHz**
- **3-State Outputs**
- **Pin-to-Pin Compatible With SN74ACT7804, SN74ACT7806, and SN74ACT7814**
- **Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing**

DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN74ALVC7806 is an 18-bit FIFO with high speed and fast access times. Data is processed at rates up to 40 MHz with access times of 18 ns in a bit-parallel format. These memories are designed for 3-V to 3.6-V V_{CC} operation.

Data is written into memory on a low-to-high transition of the load clock (LDCK) and is read out on a low-to-high transition of the unload clock (UNCK). The memory is full when the number of words clocked in exceeds the number of words clocked out by 256. When the memory is full, LDCK has no effect on the data residing in memory. When the memory is empty, UNCK has no effect.

Status of the FIFO memory is monitored by the full ($\overline{FULL}$), empty ($\overline{EMPTY}$), half-full (HF), and almost-full/almost-empty (AF/AE) flags. The $\overline{FULL}$ output is low when the memory is full and high when the memory is not full. The $\overline{EMPTY}$ output is low when the memory is empty and high when it is not empty. The HF output is high whenever the FIFO contains 128 or more words and low when it contains 127 or fewer words. The AF/AE status flag is a programmable flag. The first one or two low-to-high transitions of LDCK after reset are used to program the almost-empty offset value (X) and the almost-full offset value (Y) if program enable ($\overline{PEN}$) is low. The AF/AE flag is high when the FIFO contains X or fewer words or (256 – Y) or more words. The AF/AE flag is low when the FIFO contains between (X + 1) and (255 – Y) words.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

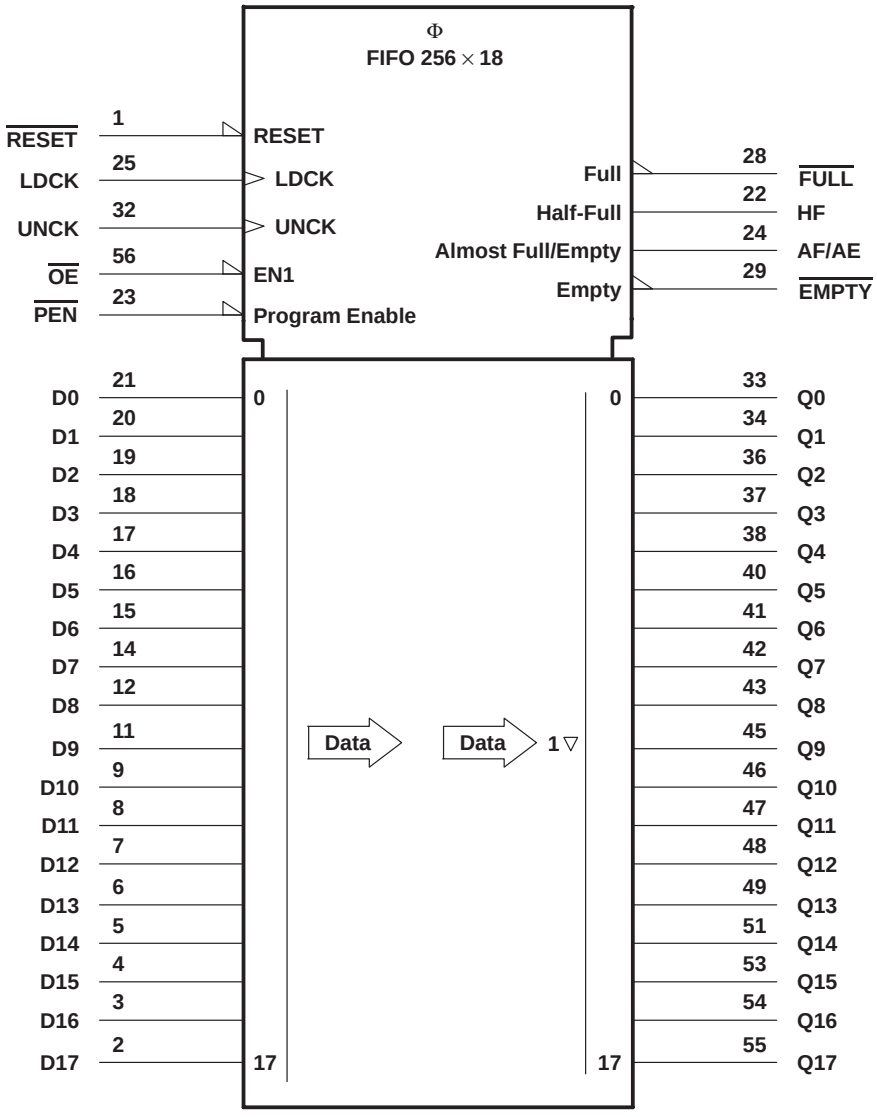
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description (continued)

A low level on the reset ($\overline{\text{RESET}}$) resets the internal stack pointers and sets $\overline{\text{FULL}}$ high, AF/AE high, HF low, and $\overline{\text{EMPTY}}$ low. The Q outputs are not reset to any specific logic level. The FIFO must be reset on power up. The first word loaded into empty memory causes $\overline{\text{EMPTY}}$ to go high and the data to appear on the Q outputs. The data outputs are in the high-impedance state when the output-enable ($\overline{\text{OE}}$) is high.

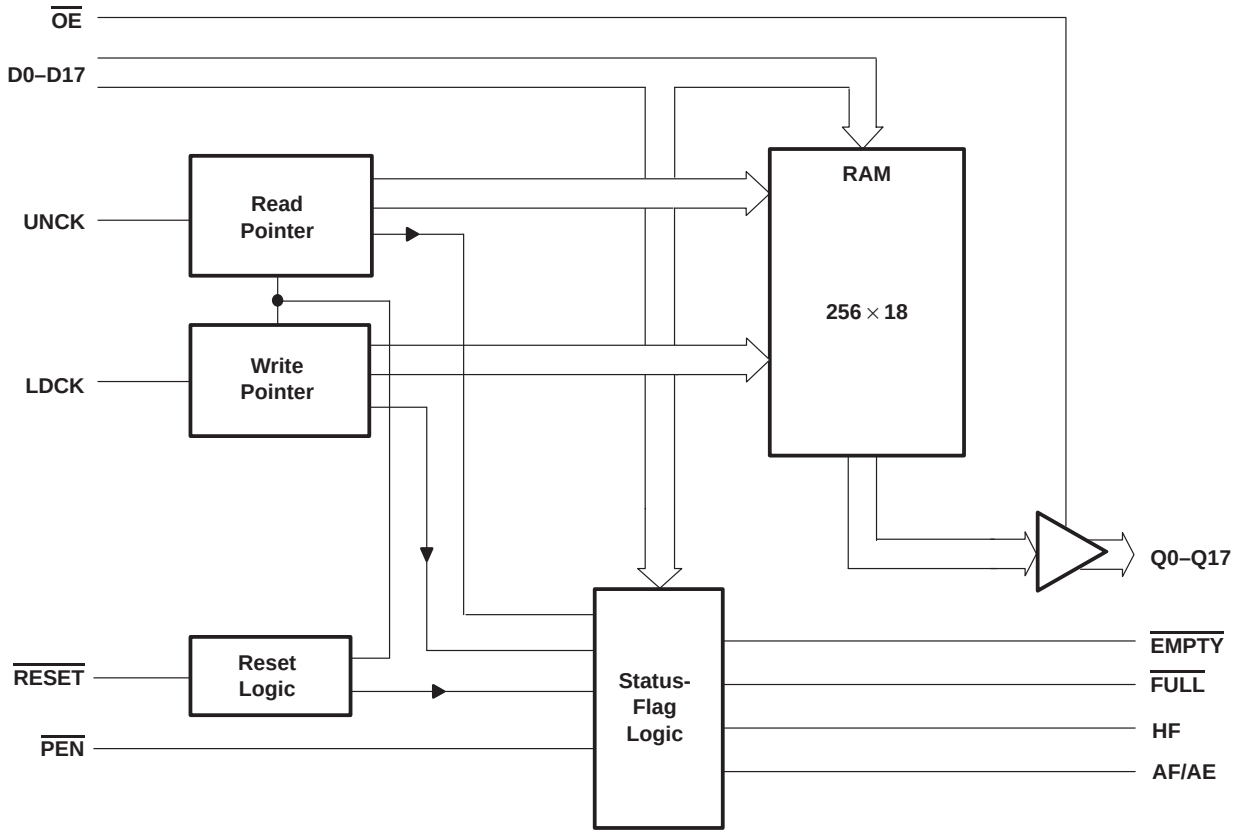
The SN74ALVC7806 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AF/AE	24	O	Almost full/almost empty flag. Depth-offset values can be programmed for this flag or the default value of 64 can be used for both the almost empty offset (X) and the almost full offset (Y). AF/AE is high when memory contains X or fewer words or (256 – Y) or more words. AF/AE is high after reset.
D0–D17	2–9, 11–12, 14–21	I	18-bit data input port
$\overline{\text{EMPTY}}$	29	O	Empty flag. $\overline{\text{EMPTY}}$ is low when the FIFO is empty. A FIFO reset also causes $\overline{\text{EMPTY}}$ to go low.
$\overline{\text{FULL}}$	28	O	Full flag. $\overline{\text{FULL}}$ is low when the FIFO is full. A FIFO reset causes $\overline{\text{FULL}}$ to go high.
HF	22	O	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
LDCK	25	I	Load clock. Data is written to the FIFO on the rising edge of LDCK when $\overline{\text{FULL}}$ is high.
$\overline{\text{OE}}$	56	I	Output enable. When $\overline{\text{OE}}$ is high, the data outputs are in the high-impedance state.
$\overline{\text{PEN}}$	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D7 is latched as an AF/AE offset value when $\overline{\text{PEN}}$ is low and WRTCLK is high.
Q0–Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	O	18-bit data output port
$\overline{\text{RESET}}$	1	I	Reset. A low level on $\overline{\text{RESET}}$ resets the FIFO and drives AF/AE and $\overline{\text{FULL}}$ high and HF and $\overline{\text{EMPTY}}$ low.
UNCK	32	I	Unload clock. Data is read from the FIFO on the rising edge of UNCK when $\overline{\text{EMPTY}}$ is high.

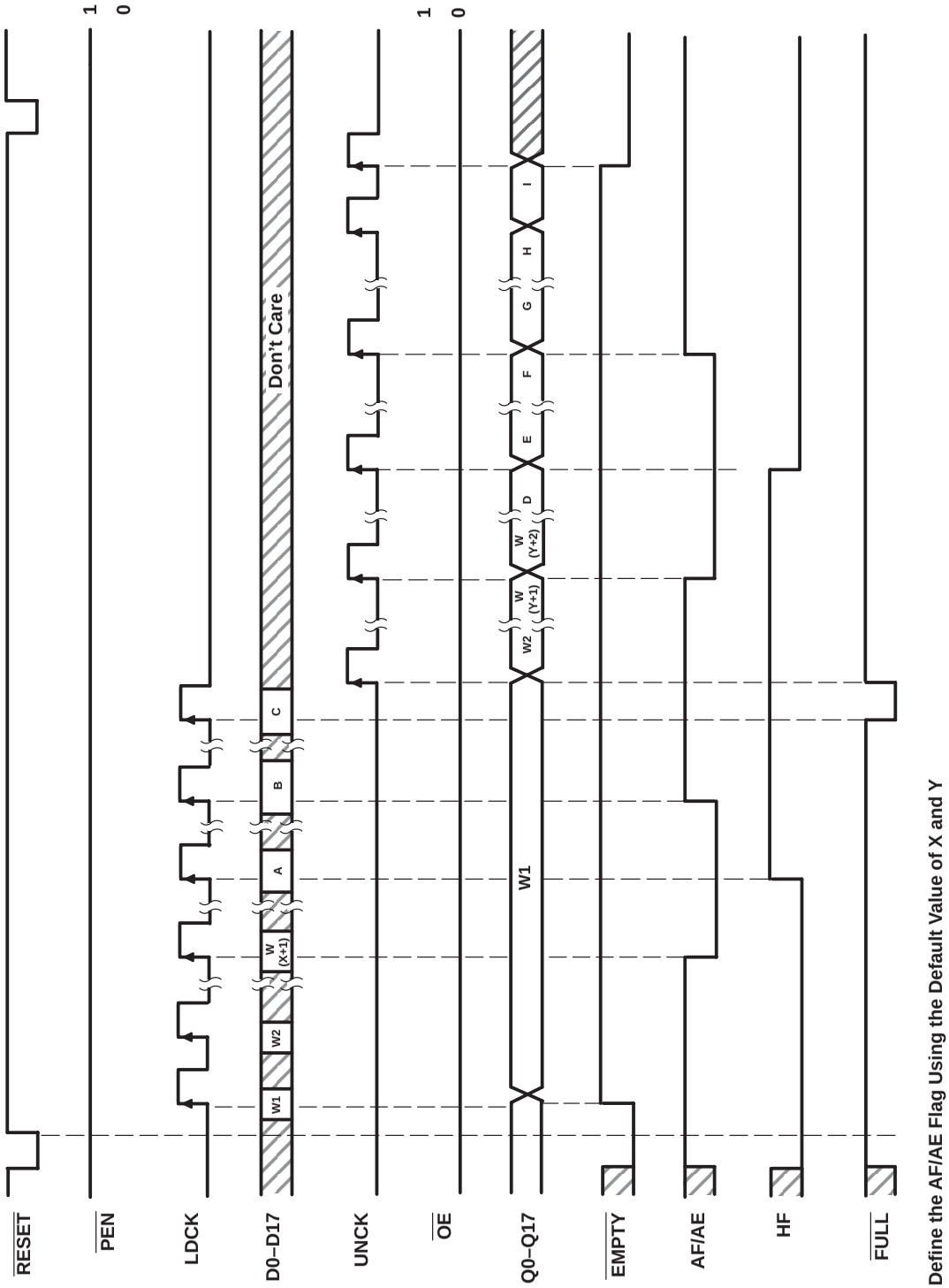


Figure 1. Write, Read, and Flag Timing Reference

Define the AF/AE Flag Using the Default Value of X and Y

DATA-WORD NUMBERS FOR FLAG TRANSITIONS

DEVICE	TRANSITION WORD								
	A	B	C	D	E	F	G	H	I
SN74ALVC7806	W128	W(256 – Y)	W256	W129	W130	W(256 – X)	W(257 – X)	W255	W256

Figure 1. Write, Read, and Flag Timing Reference (Continued)

offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. The AF/AE flag is high when the FIFO contains X or fewer words or (256 – Y) or more words.

To program the offset values, $\overline{\text{PEN}}$ can be brought low after reset. On the following low-to-high transition of LDCK, the binary value on D0–D7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PEN}}$ low for another low-to-high transition of LDCK reprograms Y to the binary value on D0–D7 at the time of the second LDCK low-to-high transition. Writes to the FIFO memory are disabled while the offsets are programmed. A maximum value of 127 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 32, $\overline{\text{PEN}}$ must be held high.

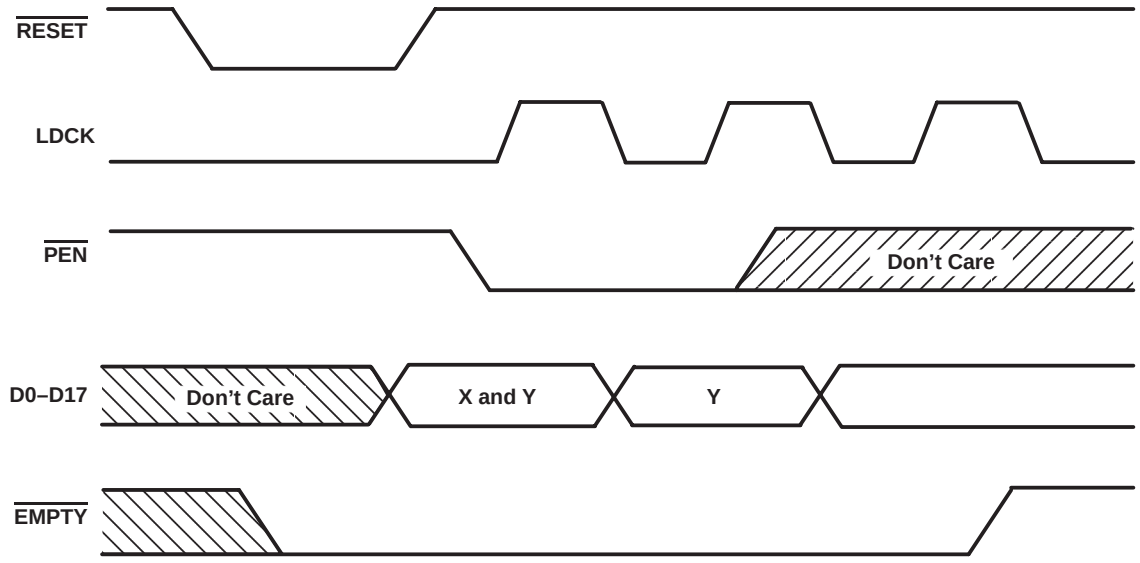


Figure 1. Programming X and Y Separately

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range applied to a disabled 3-state output . . . . . –0.5 V to 3.6 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 74°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

			’ALVC7806-25		’ALVC7806-40		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply Voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current, Q outputs, flags	V_{CC} = 3 V		–8		–8	mA
I_{OL}	Low-level output current, Q outputs, flags	V_{CC} = 3 V		16		16	mA
T_A	Operating free-air temperature		0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	Flags, Q outputs	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3 V,	I_{OH} = –8 mA	2.4			
V_{OL}	Flags, Q outputs	V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA			0.2	V
	Flags	V_{CC} = 3 V,	I_{OL} = 8 mA			0.4	
	Q outputs	V_{CC} = 3 V,	I_{OL} = 16 mA			0.55	
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±5	µA
I_{OZ}		V_{CC} = 3.6 V,	V_O = V_{CC} or GND			±10	µA
I_{CC}		V_{CC} = 3.6 V,	V_I = V_{CC} or GND and I_O = 0			40	µA
ΔI_{CC}§		V_{CC} = 3.6 V, One input at V_{CC}–0.6 V, Other inputs at V_{CC} or GND				500	µA
C_i		V_{CC} = 3.3 V,	V_I = V_{CC} or GND		3		pF
C_o		V_{CC} = 3.3 V,	V_O = V_{CC} or GND		6		pF

‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating conditions (see Figures 1 through 3)

			’ALVC7806-25		’ALVC7806-40		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			40		25	MHz
t_w	Pulse duration	D0–D17 high or low	8		12		ns
		LDCK high or low	8		12		
		UNCK high or low	8		12		
		$\overline{PEN}$ low	8		12		
		$\overline{RESET}$ low	10		12		
t_{su}	Setup time	D0–D17 before LDCK↑	5		5		ns
		LDCK inactive before $\overline{RESET}$ high	6		6		
		$\overline{PEN}$ before LDCK↑	8		8		
t_h	Hold time	D0–D17 after LDCK↑	0		0		ns
		$\overline{PEN}$ high after LDCK low	0		0		
		$\overline{PEN}$ low after LDCK↑	3		3		
		LDCK inactive after $\overline{RESET}$ high	6		6		

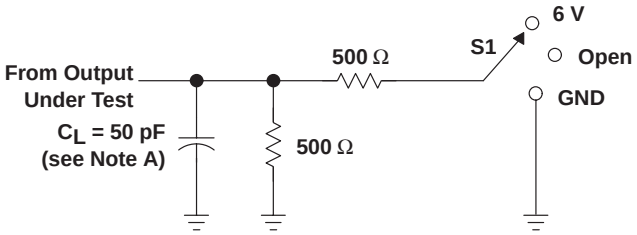
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	’ALVC7806-25		’ALVC7806-40		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	LDCK or UNCK		40		25		MHz
t_{pd}	LDCK↑	Any Q	9	22	9	24	ns
	UNCK↑		6	18	6	20	
t_{PLH}	LDCK↑	$\overline{EMPTY}$	6	17	6	19	ns
t_{PHL}	UNCK↑	$\overline{EMPTY}$	6	17	6	19	ns
	$\overline{RESET}$ low		4	18	4	20	
	LDCK↑	$\overline{FULL}$	6	17	6	19	
t_{PLH}	UNCK↑	$\overline{FULL}$	6	17	6	19	ns
	$\overline{RESET}$ low		4	20	4	22	
t_{pd}	LDCK↑	AF/AE	7	20	7	22	ns
	UNCK↑		7	20	7	22	
t_{PLH}	$\overline{RESET}$ low	AF/AE	2	12	2	14	ns
	LDCK↑	HF	5	20	5	22	
t_{PHL}	UNCK↑	HF	7	20	7	22	ns
	$\overline{RESET}$ low		3	14	3	16	
t_{en}	$\overline{OE}$	Any Q	2	10	2	11	ns
t_{dis}	$\overline{OE}$	Any Q	2	11	2	12	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

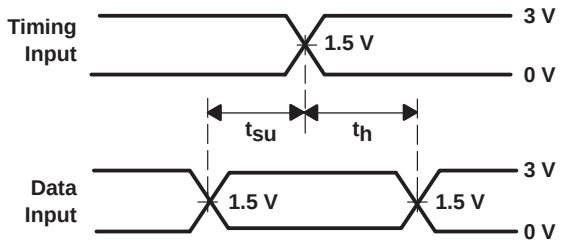
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per FIFO channel	Outputs enabled	C_L = 50 pF, f = 5 MHz	53	pF

PARAMETER MEASUREMENT INFORMATION

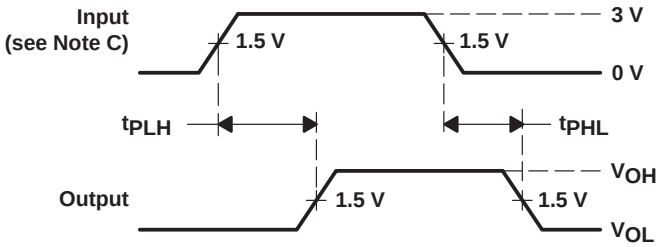


LOAD CIRCUIT FOR OUTPUTS

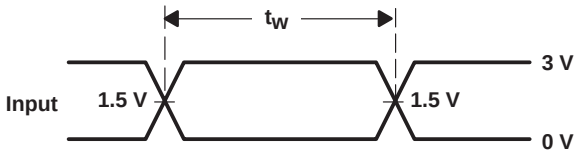
PARAMETER		S1
t_{en}	t_{PZH}	GND
	t_{PZL}	6 V
t_{dis}	t_{PHZ}	GND
	t_{PLZ}	6 V
t_{pd}	t_{PLH}/t_{PHL}	Open



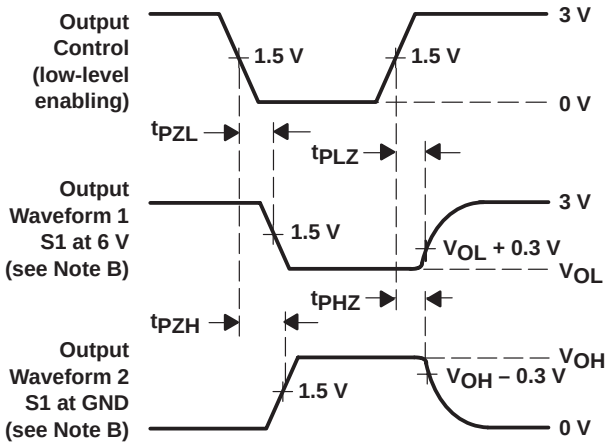
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 2. Standard CMOS Outputs (FULL, EMPTY, HF, AF/AE)

TYPICAL CHARACTERISTICS

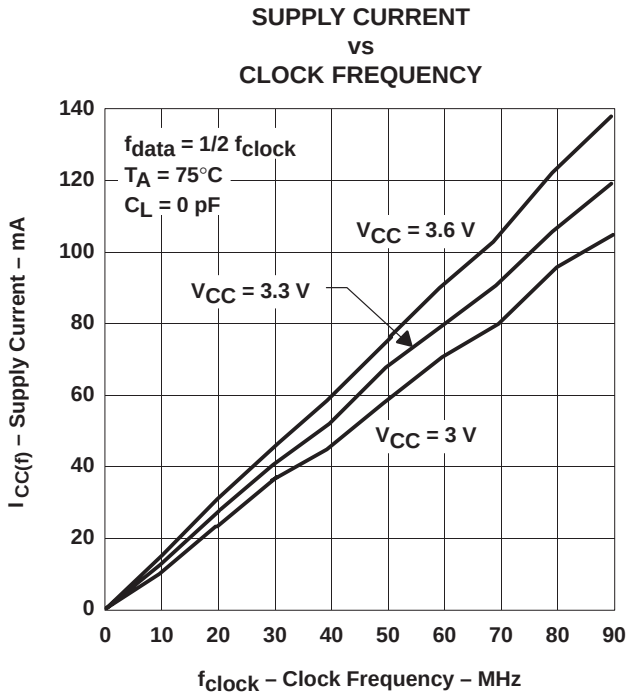


Figure 3

APPLICATION INFORMATION

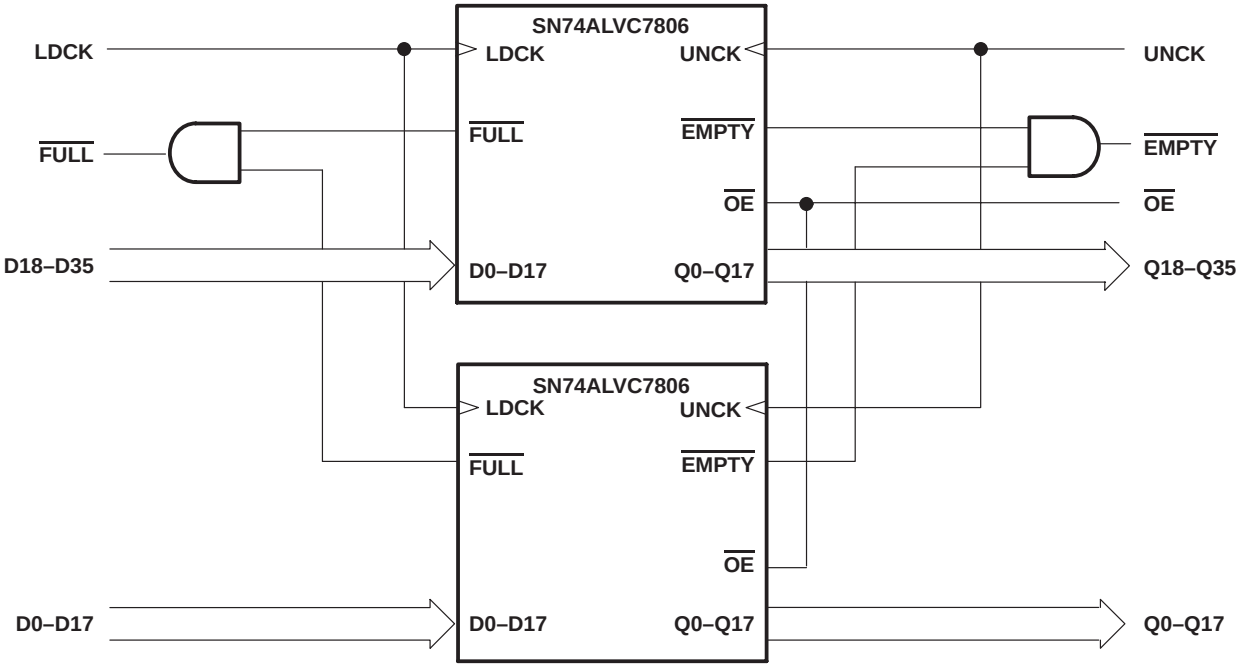


Figure 4. Word-Width Expansion: 256 × 36 Bits

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVC7806-25DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALVC7806-25
SN74ALVC7806-25DL.A	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALVC7806-25
SN74ALVC7806-40DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALVC7806-40
SN74ALVC7806-40DL.A	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALVC7806-40

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

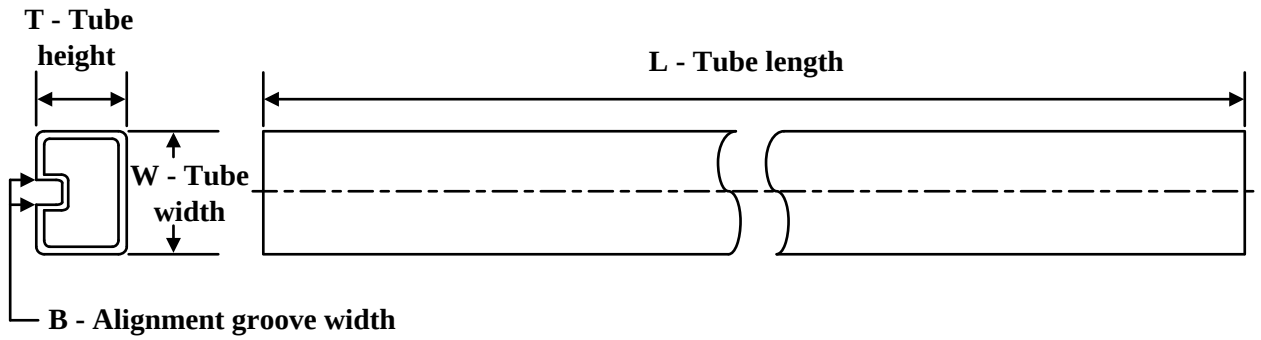
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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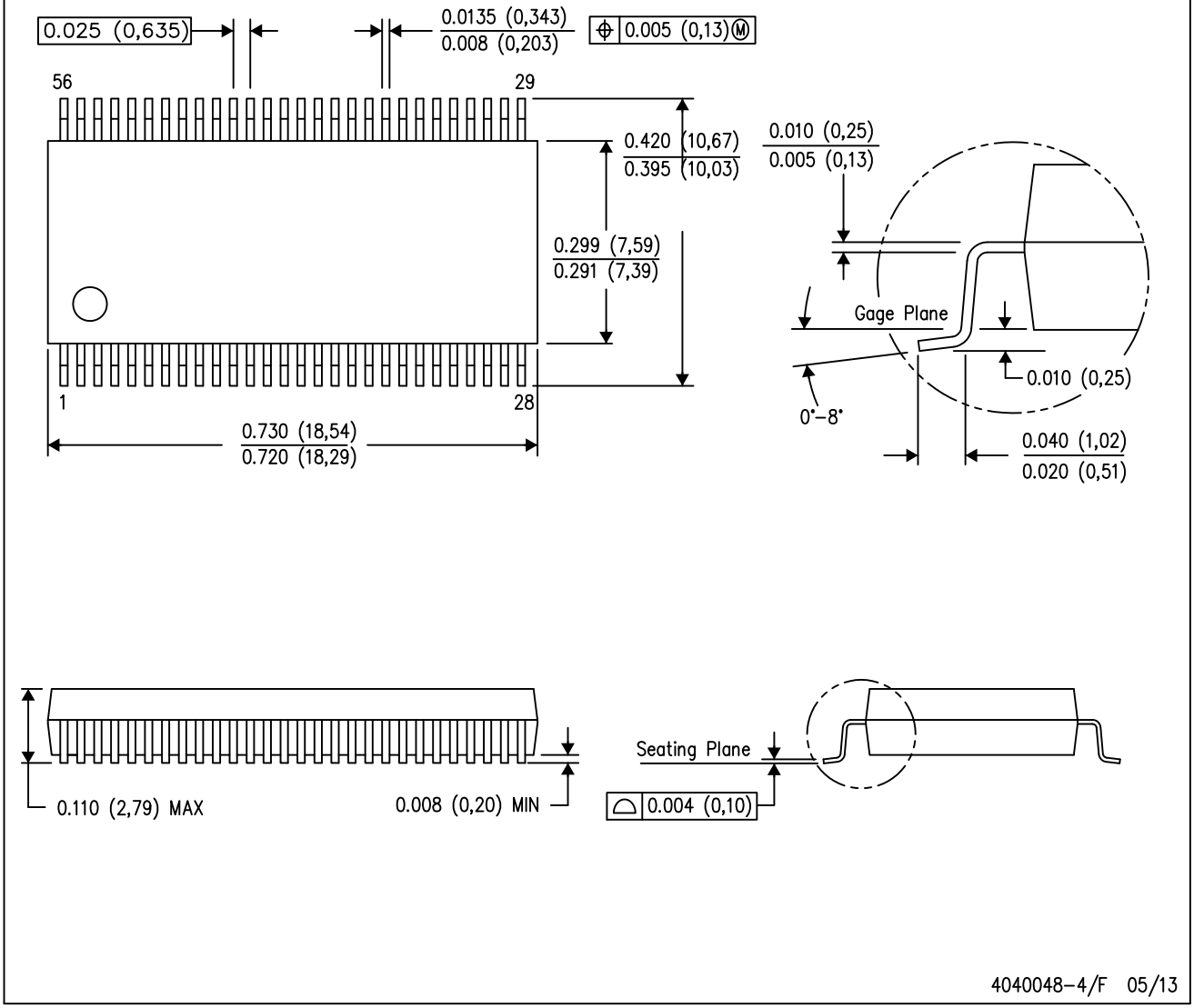
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALVC7806-25DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ALVC7806-25DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ALVC7806-40DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ALVC7806-40DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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