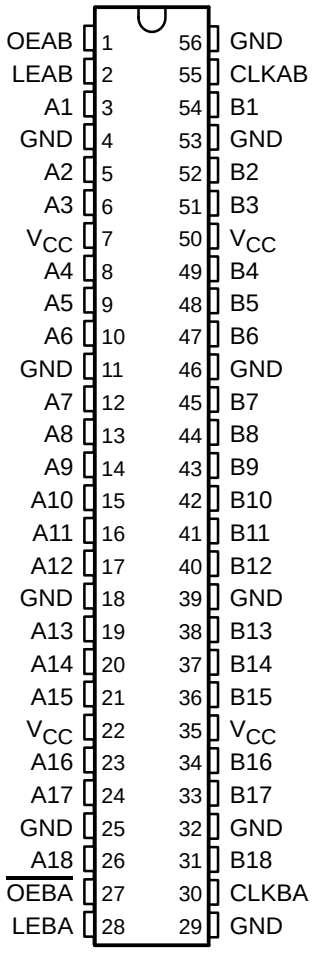
- **Member of the Texas Instruments Widebus™ Family**
- **Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Sub 1-V Operable**
- **Max t_{pd} of 2 ns at 1.8 V**
- **Low Power Consumption, 10 μA at 1.8 V**
- **±8-mA Output Drive at 1.8 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DGV PACKAGE
(TOP VIEW)



description/ordering information

This 18-bit universal bus transceiver is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses $\overline{OEBA}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AUC16501DGGR	AUC16501
	TVSOP – DGV	Tape and reel	SN74AUC16501DGVR	MH501
	VFBGA – GQL	Tape and reel	SN74AUC16501GQLR	MH501

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

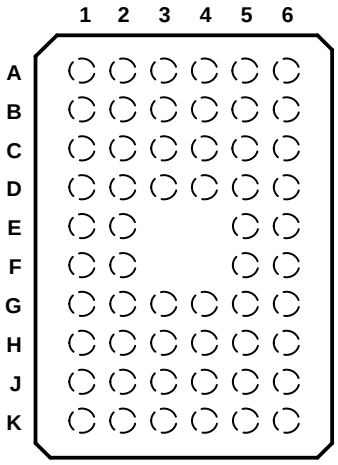
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description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor, and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQL PACKAGE
(TOP VIEW)



terminal assignments

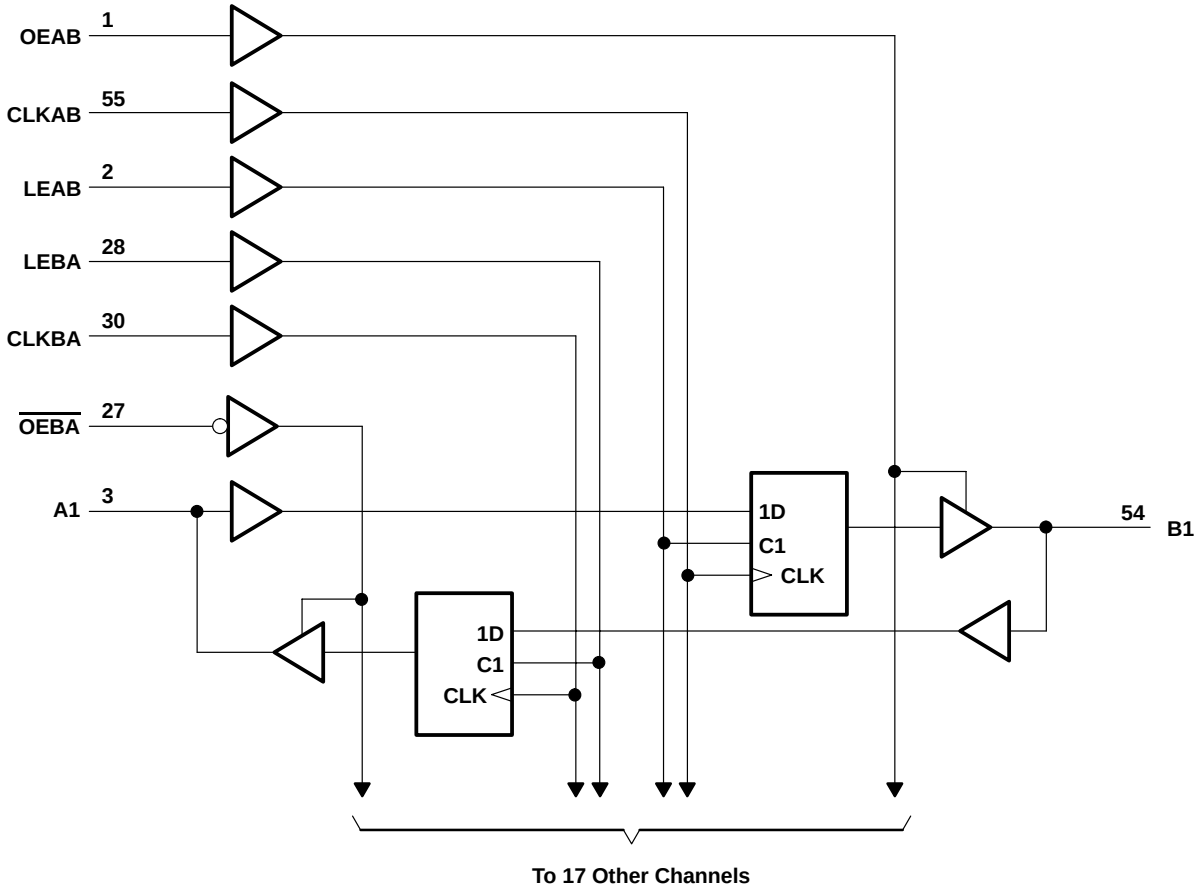
	1	2	3	4	5	6
A	A1	LEAB	OEAB	GND	CLKAB	B1
B	A3	A2	GND	GND	B2	B3
C	A5	A4	V_{CC}	V_{CC}	B4	B5
D	A7	A6	GND	GND	B6	B7
E	A9	A8			B8	B9
F	A10	A11			B11	B10
G	A12	A13	GND	GND	B13	B12
H	A14	A15	V_{CC}	V_{CC}	B15	B14
J	A16	A17	GND	GND	B17	B16
K	A18	$\overline{OEBA}$	LEBA	GND	CLKBA	B18

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

† A-to-B data flow is shown; B-to-A flow is similar, but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low
§ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 3.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 3.6 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±20 mA
Continuous current through V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 64°C/W
DGV package . . . . . 48°C/W
GQL package . . . . . 42°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	$0.65 \times V_{CC}$		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	
		V_{CC} = 2.3 V to 2.7 V		0.7	
V_I	Input voltage		0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–0.7	mA
		V_{CC} = 1.1 V		–3	
		V_{CC} = 1.4 V		–5	
		V_{CC} = 1.65 V		–8	
		V_{CC} = 2.3 V		–9	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		0.7	mA
		V_{CC} = 1.1 V		3	
		V_{CC} = 1.4 V		5	
		V_{CC} = 1.65 V		8	
		V_{CC} = 2.3 V		9	
$\Delta t/\Delta v$	Input transition rise or fall rate			20	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		0.8 V to 2.7 V	V_{CC}–0.1			V
		I_{OH} = –0.7 mA		0.8 V		0.55		
		I_{OH} = –3 mA		1.1 V	0.8			
		I_{OH} = –5 mA		1.4 V	1			
		I_{OH} = –8 mA		1.65 V	1.2			
		I_{OH} = –9 mA		2.3 V	1.8			
V_{OL}		I_{OL} = 100 μA		0.8 V to 2.7 V			0.2	V
		I_{OL} = 0.7 mA		0.8 V		0.25		
		I_{OL} = 3 mA		1.1 V			0.3	
		I_{OL} = 5 mA		1.4 V			0.4	
		I_{OL} = 8 mA		1.65 V			0.45	
		I_{OL} = 9 mA		2.3 V			0.6	
I_I	Control inputs	$V_I = V_{CC}$ or GND		0.8 V to 2.7 V			±5	μA
I_{off}		V_I or V_O = 2.7 V		0			±10	μA
I_{OZ}‡		$V_O = V_{CC}$ or GND		2.7 V			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	0.8 V to 2.7 V			20	μA
C_i		$V_I = V_{CC}$ or GND		2.5 V		3.5	4.5	pF
C_{io}		$V_O = V_{CC}$ or GND		2.5 V		6	7.5	pF

† All typical values are at T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			85		150		250		300		350	MHz
t_w	Pulse duration	LE high		5.8	4		1.7		1.5		1.5		ns
		CLK high or low		5.8	4		1.7		1.5		1.5		
t_{su}	Setup time	Data before CLK↑		0.2	0.6		0.6		0.6		0.6		ns
		Data before LE↓	CLK high	0.1	0.4		0.4		0.3		0.3		
			CLK low	0.1	0.4		0.4		0.3		0.3		
t_h	Hold time	Data after CLK↑		0.3	1.2		1.1		0.9		0.9		ns
		Data after LE↓	CLK high or low	1.3	1.5		1.3		1.2		1.2		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f_{max}			85		150		250			300		350	MHz
t_{pd}	A or B	B or A	8.5	0.9	4	1	2.8	0.3	2	2.8	0.1	2.3	ns
t_{pd}	LE	A or B	9.8	1.6	6.3	1	4.1	0.9	2.5	3.8	0.7	3	ns
t_{pd}	CLK		9.2	1.5	3.8	0.7	3.1	0.9	2.2	3.3	0.6	2.7	ns
t_{en}	OEAB	B	9.7	1.6	3	1.1	3.2	1	1.8	3.4	0.8	2.8	ns
t_{dis}			15	3.6	5.3	0.9	5.7	1.7	2.4	3.2	1	3.1	ns
t_{en}	$\overline{OEBA}$	A	11	1.7	5.7	1	3.7	1	2.2	3.7	0.7	3	ns
t_{dis}			18	3.5	7.5	1.4	5.4	2	3.5	5.2	0.9	3	ns

operating characteristics for transparent mode, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pd}† (each bit)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f_{data} = 10 MHz, f_{clk} = V_{CC} or GND, 1 f_{out} = 10 MHz, $\overline{OEAB}$ = V_{CC}, $\overline{OEBA}$ = GND, LE = V_{CC}, C_L = 0 pF	30	31	33	36	44	pF
C_{pd} (each bit)	Power dissipation capacitance	Outputs disabled	1 f_{data} = 10 MHz, f_{clk} = V_{CC} or GND, 1 f_{out} = not switching, $\overline{OEAB}$ = GND, $\overline{OEBA}$ = V_{CC}, LE = V_{CC}, C_L = 0 pF	9	9	10	12	16	pF

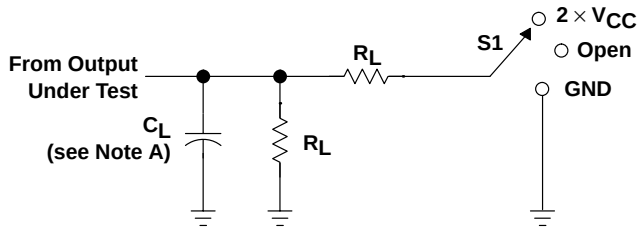
† C_{pd} (each output) is the C_{pd} for each data bit (input and output circuitry) as it operates at 5 MHz (the clock is operating at 10 MHz in this test, but its I_{CC} component has been subtracted out).

operating characteristics for clocked mode, $T_A = 25°C$†

PARAMETER			TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pd}‡ (each bit)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f_{data} = 5 MHz, 1 f_{clk} = 10 MHz, 1 f_{out} = 5 MHz, $\overline{OEAB}$ = V_{CC}, $\overline{OEBA}$ = GND, LE = GND, C_L = 0 pF	29	30	31	35	43	pF
C_{pd} (Z)	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 f_{data} = 5 MHz, 1 f_{clk} = 10 MHz, f_{out} = not switching, $\overline{OEAB}$ = GND, $\overline{OEBA}$ = V_{CC}, LE = GND, C_L = 0 pF	8	8	9	10	13	pF
C_{pd}§ (each clock)	Power dissipation capacitance	Outputs disabled, clock only switching	1 f_{data} = 0 MHz, 1 f_{clk} = 10 MHz, f_{out} = not switching, $\overline{OEAB}$ = GND, $\overline{OEBA}$ = V_{CC}, LE = GND, C_L = 0 pF	31	32	32	34	39	pF

† Total device C_{pd} for multiple (n) outputs switching and (y) clocks inputs switching = {n * C_{pd} (each output)} + {y * C_{pd} (each clock)}
‡ C_{pd} (each bit) is the C_{pd} for each data bit (input and output circuitry) as it operates at 5 MHz (the clock is operating at 10 MHz in this test, but its I_{CC} component has been subtracted out).
§ C_{pd} (each clock) is the C_{pd} for the clock circuitry only as it operates at 10 MHz.

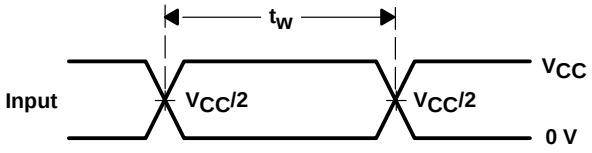
PARAMETER MEASUREMENT INFORMATION



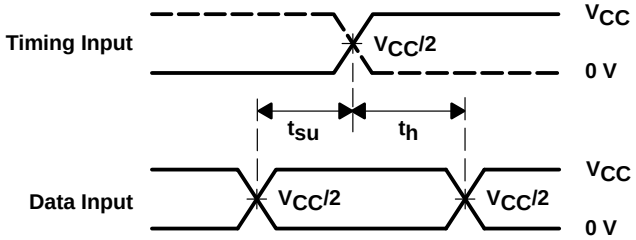
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

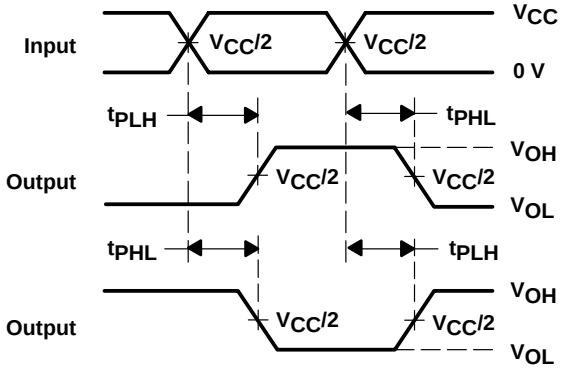
V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



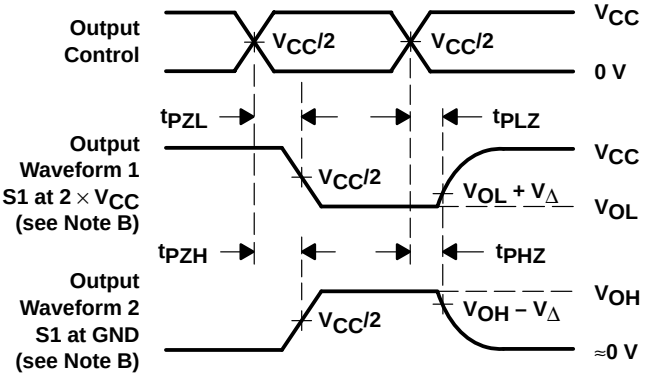
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



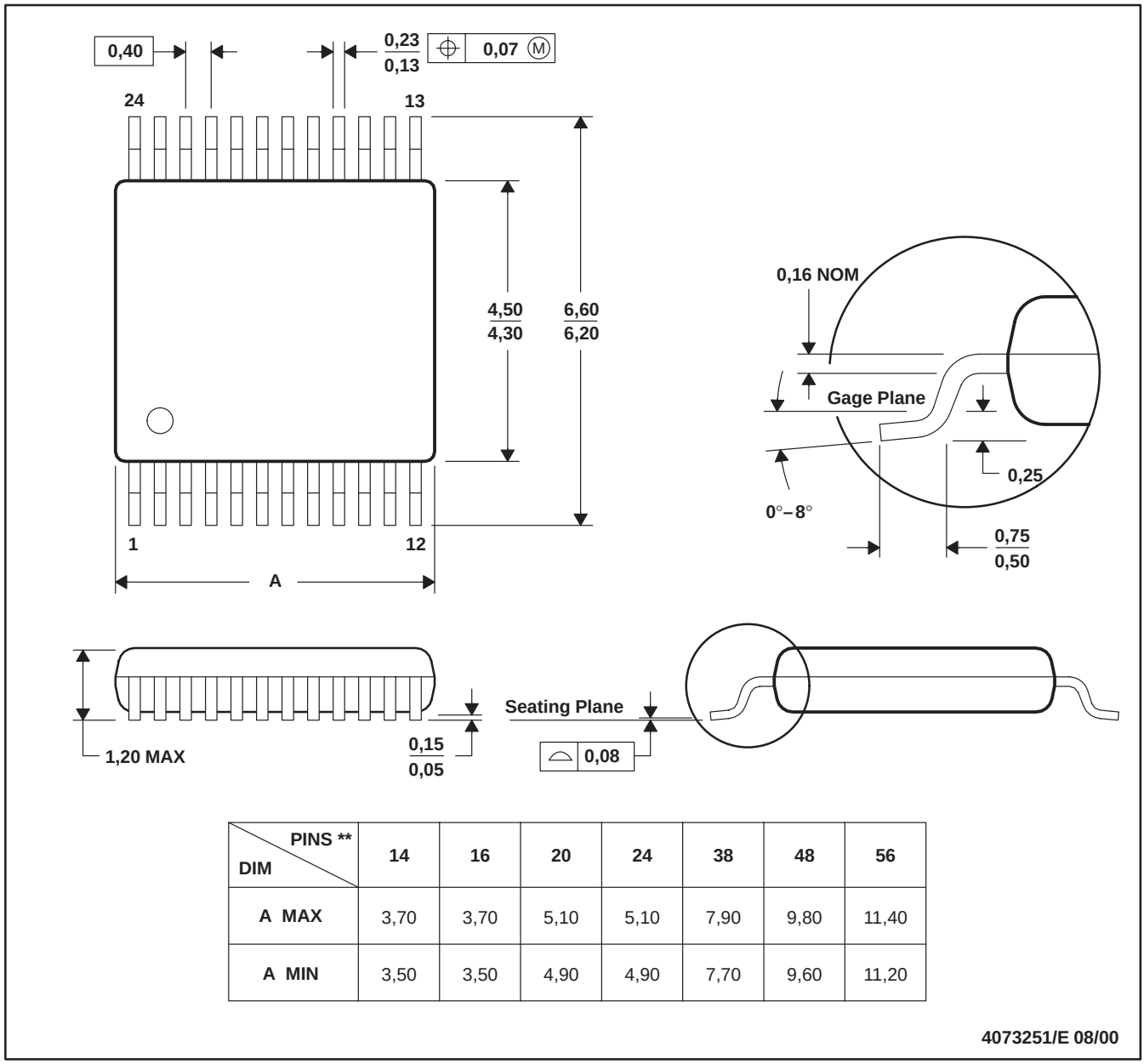
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

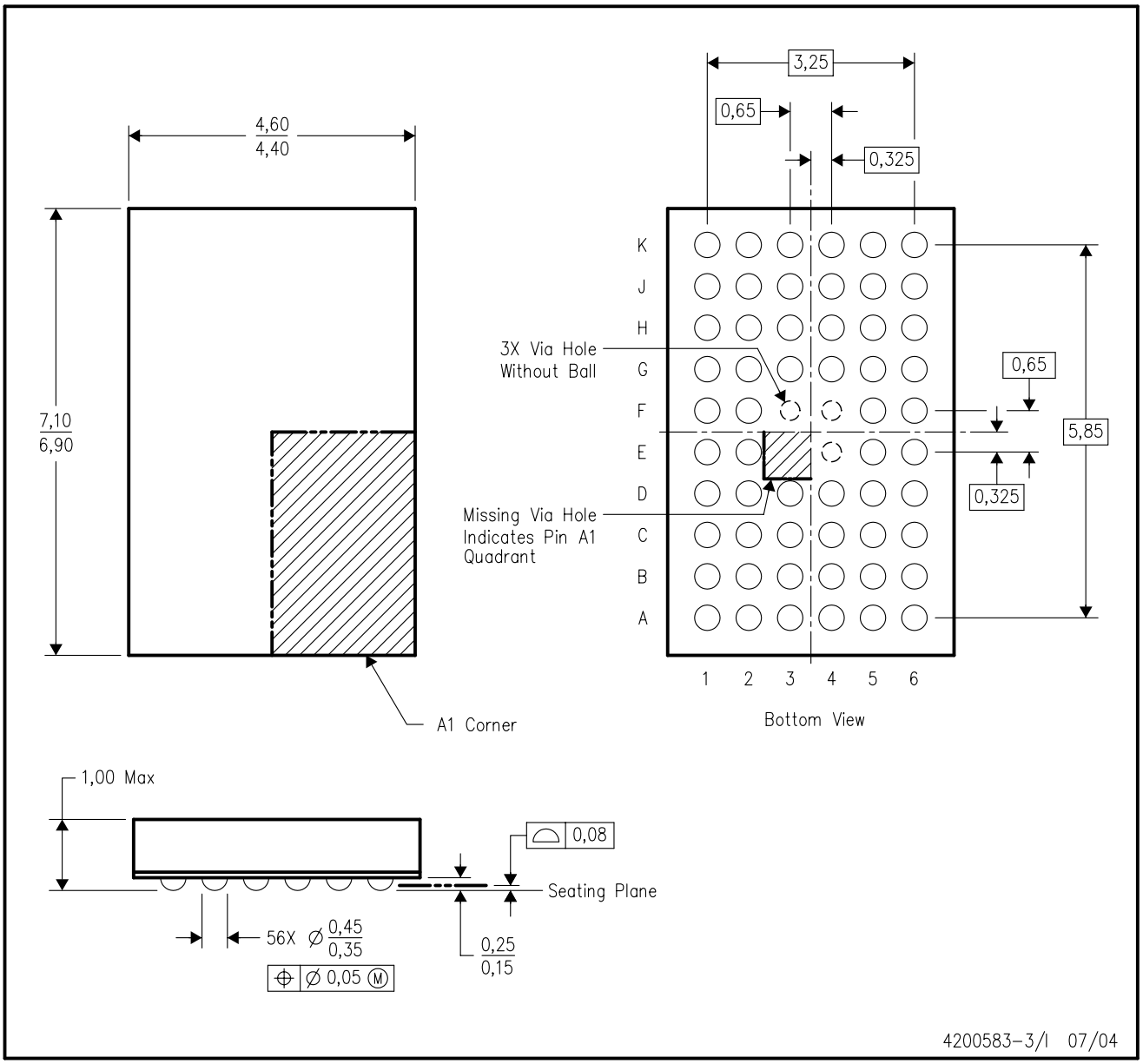


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY

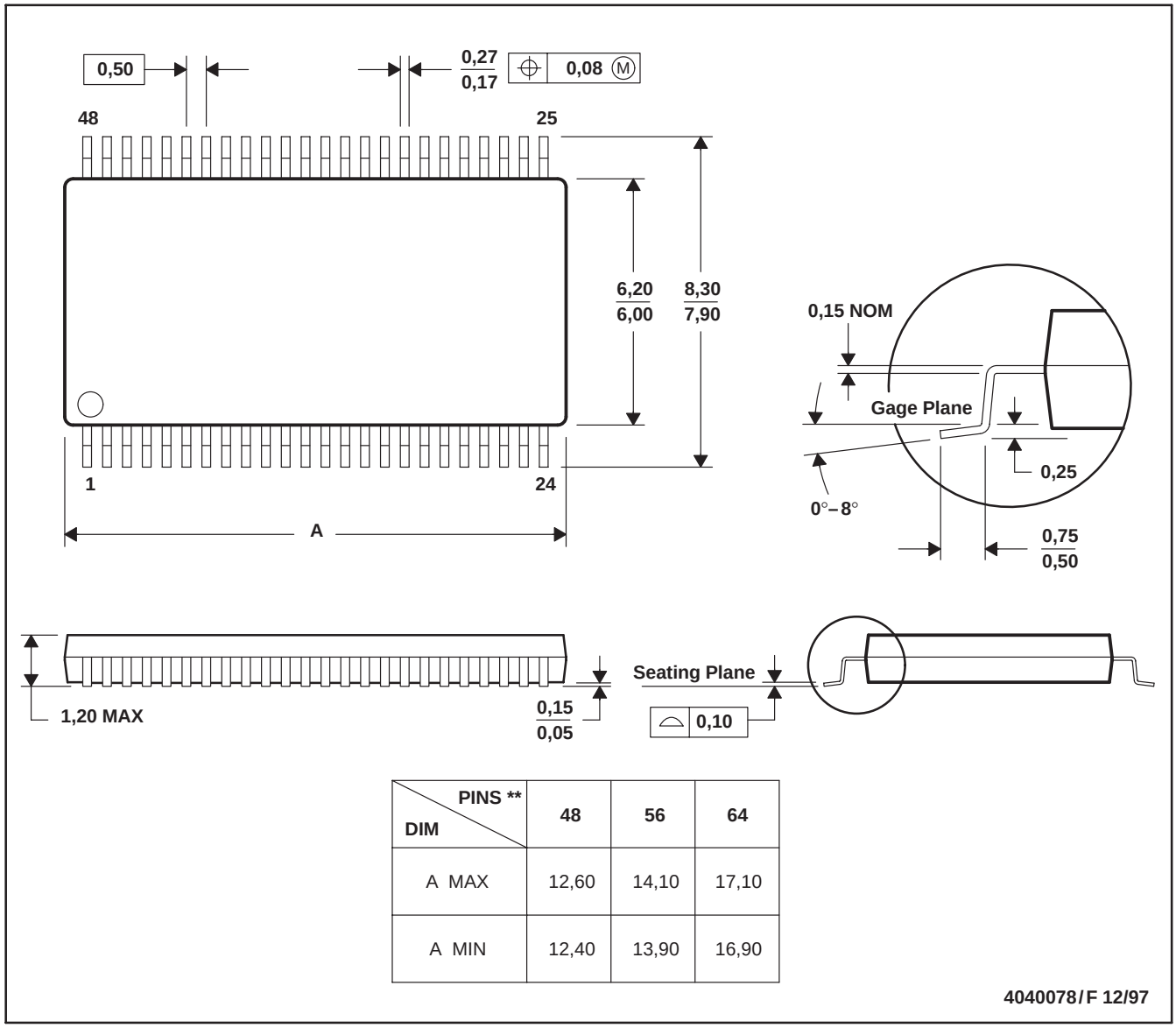


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BA.
D. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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