# SN74AUP1G06 Low-Power Single Inverter With Open-Drain Outputs

## 1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC}$ = 0.9 µA Maximum)
- Low Dynamic-Power Consumption ($C_{pd}$ = 1 pF Typical at 3.3 V)
- Low Input Capacitance ($C_i$ = 1.5 pF Typical)
- Low Noise – Overshoot and Undershoot <10% of $V_{CC}$
- $I_{off}$ Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys}$ = 250 mV Typical at 3.3 V)
- Wide Operating $V_{CC}$ Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd}$ = 3.6 ns Maximum at 3.3 V
- Suitable for Point-to-Point Applications

## 2 Applications

- AV Receivers
- Smartphones
- Blu-ray Players and Home Theaters
- Desktop or Notebook PCs
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable

## 3 Description

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire $V_{CC}$ range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see

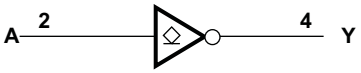
*AUP – The Lowest-Power Family* and *Excellent Signal Integrity*).

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74AUP1G06DBV | SOT-23 (5) | 2.90 mm × 1.60 mm |
| SN74AUP1G06DCK | SC70 (5) | 2.00 mm × 1.25 mm |
| SN74AUP1G06DRL | SOT-5X3 (5) | 1.60 mm × 1.20 mm |
| SN74AUP1G06DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74AUP1G06DSF | SON (6) | 1.00 mm x 1.00 mm |
| SN74AUP1G06YFP | DSBGA (4) | 0.76 mm × 0.76 mm |
| SN74AUP1G06DPW | X2SON (5) | 0.80 mm x 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

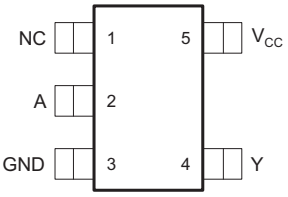
| Changes from Revision D (May 2010) to Revision E | Page |
|---|---|
| • Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Deleted *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information* at the end of the data sheet | 1 |


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# 5 Pin Functions and Configurations

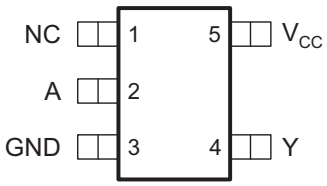
NC – No internal connection

**DBV Package**
**5-Pin SOT-23**
**Top View**

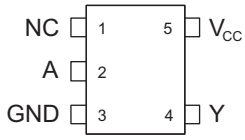



See mechanical drawings for dimensions.

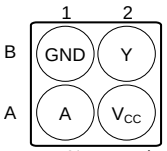
**DCK Package**
**5-Pin SC70**
**Top View**




**DRL Package**
**5-Pin SOT-5X3**
**Top View**

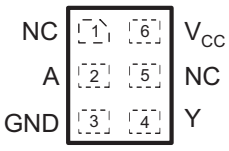



**YFP Package**
**4-Pin DSBGA**
**Bottom View**

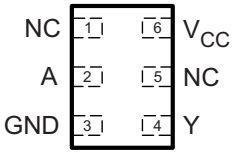



Not to scale

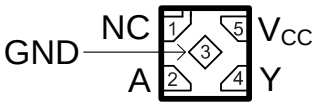
**DRY Package**
**6-Pin SON**
**Top View**




**DSF Package**
**6-Pin SON**
**Top View**




**DPW Package(1)**
**5-Pin X2SON**
**Top View**




**Pin Functions**

| PIN(1) | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DBV, DCK, DRL, DPW | DRY, DSF | YFP | | |
| A | 2 | 2 | A1 | I | Input |
| GND | 3 | 3 | B1 | — | Ground |
| NC(2) | 1 | 1, 5 | — | — | Not connected |
| $V_{CC}$ | 5 | 6 | A2 | — | Positive supply |
| Y | 4 | 4 | B2 | O | Output |

(1) See mechanical drawings for dimensions
(2) NC – No internal connection

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | –0.5 | 4.6 | V |
| Input voltage(2), $V_I$ | | –0.5 | 4.6 | V |
| Voltage range applied to any output in the high-impedance or power-off state(2), $V_O$ | | –0.5 | 4.6 | V |
| Output voltage range in the high or low state(2), $V_O$ | | –0.5 | $V_{CC}$ + 0.5 | V |
| Input clamp current, $I_{IK}$ | $V_I$ < 0 | | –50 | mA |
| Output clamp current, $I_{OK}$ | $V_O$ < 0 | | –50 | mA |
| Continuous output current, $I_O$ | | | ±20 | mA |
| Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| Junction temperature, $T_j$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

See(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0.65 × $V_{CC}$ | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.9 | |
| $V_I$ | Input voltage | | 0 | 3.6 | V |
| $V_O$ | Output voltage | | 0 | 3.6 | V |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.8 V | | 20 | µA |
| | | $V_{CC}$ = 1.1 V | | 1.1 | mA |
| | | $V_{CC}$ = 1.4 V | | 1.7 | |
| | | $V_{CC}$ = 1.65 V | | 1.9 | |
| | | $V_{CC}$ = 2.3 V | | 3.1 | |
| | | $V_{CC}$ = 3 V | | 4 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 0.8 V to 3.6 V | | 200 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.


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## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74AUP1G06 | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRL (SOT-5X3) | DRY (SON) | DPW (X2SON) | DSF (SON) | YFP (DSBGA) | |
| | | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 6 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 230.5 | 303.6 | 295.1 | 342.1 | 504.3 | 377.1 | 179.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 172.7 | 203.8 | 131.0 | 233.1 | 234.9 | 187.7 | 2.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 62.2 | 100.9 | 143.9 | 206.7 | 370.3 | 236.6 | 58.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 49.3 | 76.1 | 14.7 | 63.4 | 44.5 | 29.0 | 1.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 61.6 | 99.3 | 144.4 | 206.7 | 369.7 | 236.3 | 58.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | 165.2 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 20 µA | $T_A$ = 25°C | 0.8 V to 3.6 V | | | 0.1 | V |
| | | | $T_A$ = –40°C to +85°C | | | | 0.1 | |
| | | $I_{OL}$ = 1.1 mA | $T_A$ = 25°C | 1.1 V | | | 0.3 × $V_{CC}$ | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.3 × $V_{CC}$ | |
| | | $I_{OL}$ = 1.7 mA | $T_A$ = 25°C | 1.4 V | | | 0.31 | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.37 | |
| | | $I_{OL}$ = 1.9 mA | $T_A$ = 25°C | 1.65 V | | | 0.31 | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.35 | |
| | | $I_{OL}$ = 2.3 mA | $T_A$ = 25°C | 2.3 V | | | 0.31 | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.33 | |
| | | $I_{OL}$ = 3.1 mA | $T_A$ = 25°C | | | | 0.44 | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.45 | |
| | | $I_{OL}$ = 2.7 mA | $T_A$ = 25°C | 3 V | | | 0.31 | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.33 | |
| | | $I_{OL}$ = 4 mA | $T_A$ = 25°C | | | | 0.44 | |
| | | | $T_A$ = –40°C to +85°C | | | | 0.45 | |
| $I_I$ | Inflection point current | A input: $V_I$ = GND to 3.6 V | $T_A$ = 25°C | 0 V to 3.6 V | | | 0.1 | µA |
| | | | $T_A$ = –40°C to +85°C | | | | 0.5 | |
| $I_{off}$ | Off-state current | $V_I$ or $V_O$ = 0 V to 3.6 V | $T_A$ = 25°C | 0 V | | | 0.2 | µA |
| | | | $T_A$ = –40°C to +85°C | | | | 0.6 | |
| $\Delta I_{off}$ | Off-state current change | $V_I$ or $V_O$ = 0 V to 3.6 V | $T_A$ = 25°C | 0 V to 0.2 V | | | 0.2 | µA |
| | | | $T_A$ = –40°C to +85°C | | | | 0.6 | |
| $I_{CC}$ | Supply current | $V_I$ = GND or $V_{CC}$ to 3.6 V, $I_O$ = 0 | $T_A$ = 25°C | 0.8 V to 3.6 V | | | 0.5 | µA |
| | | | $T_A$ = –40°C to +85°C | | | | 0.9 | |
| $\Delta I_{CC}$ | Supply current change | $V_I$ = $V_{CC}$ – 0.6 V, $I_O$ = 0 | $T_A$ = 25°C | 3.3 V | | | 40 | µA |
| | | | $T_A$ = –40°C to +85°C | | | | 50 | |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND, $T_A$ = 25°C | | 0 V | | 1.5 | | pF |
| | | | | 3.6 V | | 1.7 | | |
| $C_o$ | Output capacitance | $V_O$ = GND, $T_A$ = 25°C | | 0 V | | 1.7 | | pF |

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## 6.6 Switching Characteristics, $C_L$ = 5 pF

over recommended operating free-air temperature range, $C_L$ = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time | A | Y | $V_{CC}$ = 0.8 V | $T_A$ = 25°C | | 12.4 | | ns |
| | | | | $V_{CC}$ = 1.2 V ± 0.1 V | $T_A$ = 25°C | 2.7 | 12 | 9.9 | |
| | | | | | $T_A$ = –40°C to +85°C | 2 | | 12.8 | |
| | | | | $V_{CC}$ = 1.5 V ± 0.1 V | $T_A$ = 25°C | 2.1 | 3.5 | 6.2 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.5 | | 7.6 | |
| | | | | $V_{CC}$ = 1.8 V ± 0.15 V | $T_A$ = 25°C | 2.1 | 3.1 | 4.7 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.2 | | 5.9 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | $T_A$ = 25°C | 1.4 | 2.2 | 3.2 | |
| | | | | | $T_A$ = –40°C to +85°C | 1 | | 3.9 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | $T_A$ = 25°C | 1.3 | 2.2 | 3.3 | |
| | | | | | $T_A$ = –40°C to +85°C | 0.8 | | 3.6 | |

## 6.7 Switching Characteristics, $C_L$ = 10 pF

over recommended operating free-air temperature range, $C_L$ = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time | A | Y | $V_{CC}$ = 0.8 V | $T_A$ = 25°C | | 15.1 | | ns |
| | | | | $V_{CC}$ = 1.2 V ± 0.1 V | $T_A$ = 25°C | 3.6 | 12 | 11.2 | |
| | | | | | $T_A$ = –40°C to +85°C | 2.7 | | 14.1 | |
| | | | | $V_{CC}$ = 1.5 V ± 0.1 V | $T_A$ = 25°C | 2.9 | 4.3 | 7 | |
| | | | | | $T_A$ = –40°C to +85°C | 2.2 | | 8.6 | |
| | | | | $V_{CC}$ = 1.8 V ± 0.15 V | $T_A$ = 25°C | 2.7 | 3.9 | 5.4 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.8 | | 6.7 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.1 | 2.9 | 3.8 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.4 | | 4.5 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | $T_A$ = 25°C | 1.7 | 3 | 4.5 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.2 | | 4.9 | |

## 6.8 Switching Characteristics, $C_L$ = 15 pF

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay time | A | Y | $V_{CC}$ = 0.8 V | $T_A$ = 25°C | | 17.4 | | ns |
| | | | | $V_{CC}$ = 1.2 V ± 0.1 V | $T_A$ = 25°C | 4.9 | 12 | 12.2 | |
| | | | | | $T_A$ = –40°C to +85°C | 3.4 | | 15.2 | |
| | | | | $V_{CC}$ = 1.5 V ± 0.1 V | $T_A$ = 25°C | 3.5 | 5 | 7.7 | |
| | | | | | $T_A$ = –40°C to +85°C | 2.7 | | 9.4 | |
| | | | | $V_{CC}$ = 1.8 V ± 0.15 V | $T_A$ = 25°C | 3.2 | 4.8 | 6.6 | |
| | | | | | $T_A$ = –40°C to +85°C | 2.2 | | 7.3 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.5 | 3.5 | 4.5 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.7 | | 5.1 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | $T_A$ = 25°C | 2 | 3.8 | 6 | |
| | | | | | $T_A$ = –40°C to +85°C | 1.5 | | 6.5 | |


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## 6.9 Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ Propagation delay time | A | Y | $V_{CC}$ = 0.8 V | $T_A$ = 25°C | | 25.3 | | ns |
| | | | $V_{CC}$ = 1.2 V ± 0.1 V | $T_A$ = 25°C | 7.6 | 12 | 16 | |
| | | | | $T_A$ = –40°C to +85°C | 5.6 | | 19.3 | |
| | | | $V_{CC}$ = 1.5 V ± 0.1 V | $T_A$ = 25°C | 5.9 | 7.6 | 10.1 | |
| | | | | $T_A$ = –40°C to +85°C | 4.3 | | 12 | |
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | $T_A$ = 25°C | 4.8 | 7.4 | 10.7 | |
| | | | | $T_A$ = –40°C to +85°C | 3.6 | | 11 | |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | $T_A$ = 25°C | 3.7 | 5.4 | 7.1 | |
| | | | | $T_A$ = –40°C to +85°C | 2.8 | | 7.8 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | $T_A$ = 25°C | 3.2 | 6.5 | 10.5 | |
| | | | | $T_A$ = –40°C to +85°C | 2.5 | | 10.8 | |

## 6.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 0.8 V | 1 | pF |
| | | | 1.2 V ± 0.1 V | 1 | |
| | | | 1.5 V ± 0.1 V | 1 | |
| | | | 1.8 V ± 0.15 V | 1 | |
| | | | 2.5 V ± 0.2 V | 1 | |
| | | | 3.3 V ± 0.3 V | 1 | |

## 6.11 Typical Characteristics

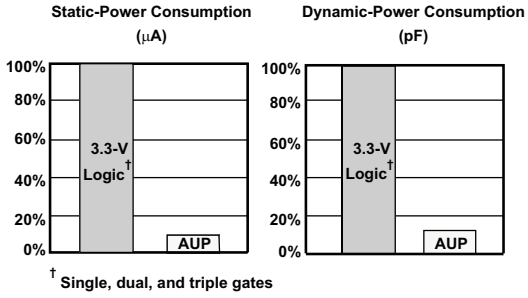



**Figure 1. AUP – The Lowest-Power Family**

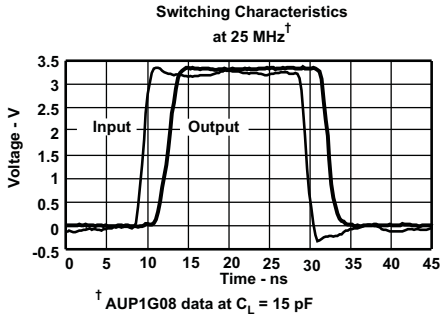
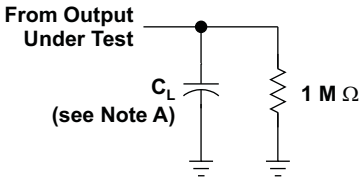


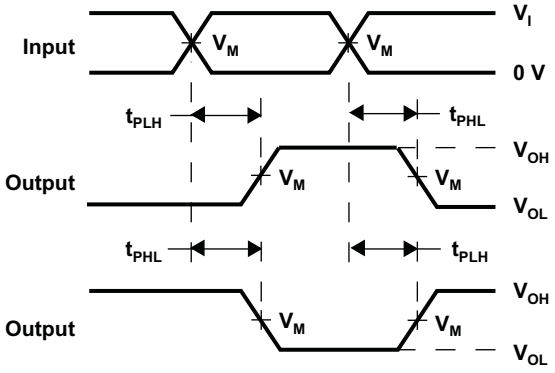

**Figure 2. Excellent Signal Integrity**

# 7 Parameter Measurement Information

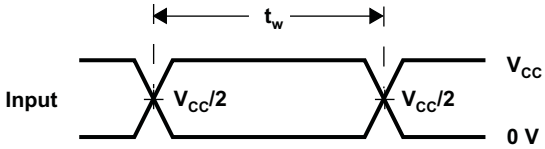



**LOAD CIRCUIT**

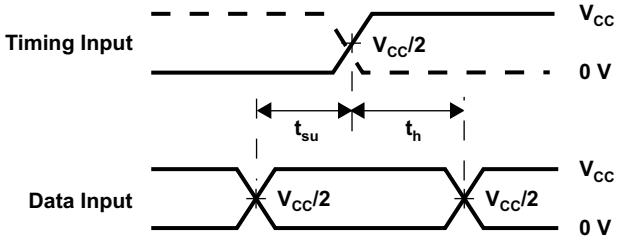
| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**




**VOLTAGE WAVEFORMS**
**PULSE DURATION**



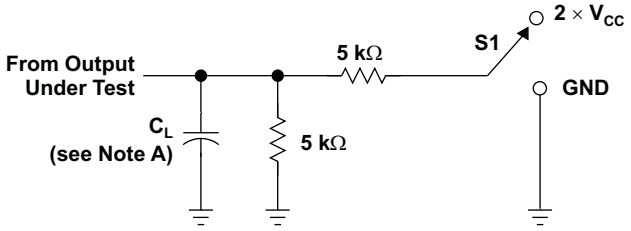

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
E. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit And Voltage Waveforms - Propagation Delays, Setup And Hold Times, And Pulse Width**


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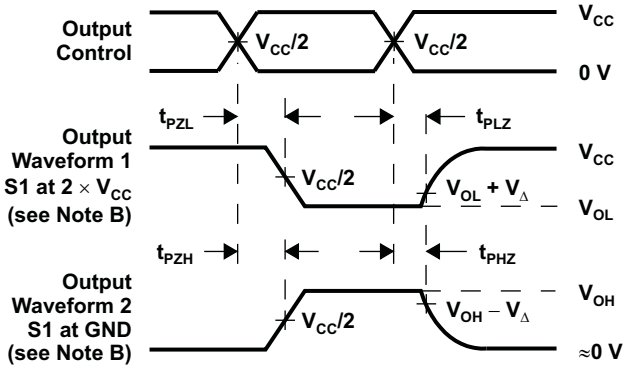
## Parameter Measurement Information (continued)




| TEST | S1 |
|---|---|
| $t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | 2 × $V_{CC}$<br>GND |

LOAD CIRCUIT

| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $V_\Delta$ | 0.1 V | 0.1 V | 0.1 V | 0.15 V | 0.15 V | 0.3 V |




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit And Voltage Waveforms - Enable And Disable Times**

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# 8 Detailed Description

## 8.1 Overview

The output of this single inverter buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

## 8.2 Functional Block Diagram

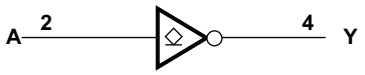



**Figure 5. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

### 8.3.1 CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from VCC. When the output is not actively pulling the line low, it will go into a high impedance state (3-state). This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pullup.

The drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be utilized to condition the input signal prior to the standard CMOS input.


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## Feature Description (continued)

### 8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

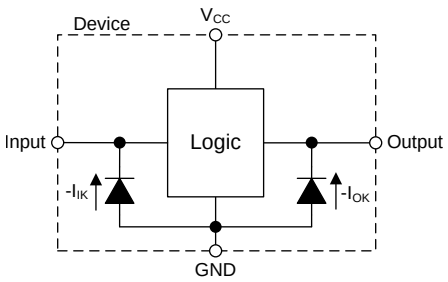



**Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.4 Partial Power Down ($I_{off}$)

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off}$ in the *Electrical Characteristics*.

### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings*.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1G06 device.

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | Hi-Z |

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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

Open-drain devices are very commonly used for voltage level translation. In this application, the SN74AUP1G06 is used to translate a 1.8-V output from device A to a 3.3-V input on device B.

## 9.2 Typical Application

The application schematic shown in Figure 7 includes two generic devices, labeled as "Device A" and "Device B."

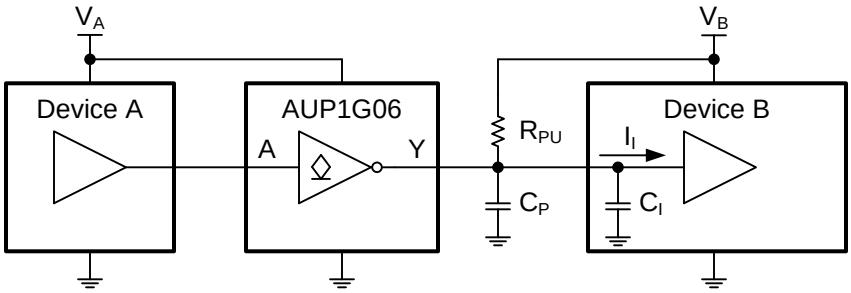



**Figure 7. Application schematic for voltage translation with SN74AUP1G06**

### 9.2.1 Design Requirements

This device has a standard CMOS input, so be careful to avoid slow or floating inputs that might cause oscillation or excessive current. Please see the *Implications of Slow or FLoating CMOS Inputs* Application Report.

This device has an open-drain output, which means that the output enters a high-impedance state when a normal CMOS device would drive the output high. A pull-up resistor must be added to the output for an open-drain device to have a high output. The selection of this pull-up resistor is detailed in the next section.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Electrical Characteristics* table.
   - Inputs are overvoltage tolerant allowing them to go as high as $V_{I(max)}$ in the *Absolute Maximum Ratings* table at any valid $V_{CC}$.
2. Recommended Output Conditions
   - Output voltage must not exceed $V_{O(max)}$ as specified in the *Absolute Maximum Ratings* table.
   - Pull-up resistor (R) selection depends on three primary factors: desired output high voltage ($V_{OH}$), which is directly related to total leakage current into the SN74AUP1G240 and the peripheral device's input ($I_L$), desired 0 to 90% rising edge time ($t_r$), which is directly related to the parasitic line capacitance ($C_P$), and the maximum current during low output ($I_{OL}$), which is directly related to the supply value. These three equations govern pull-up resistor selection:
     - $R \le ( V_{CC} - V_{OH} ) / I_L$
     - $R \le t_r / ( 2.3 * C_P)$
     - $R \ge V_{CC} / I_{OL(max)}$


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## Typical Application (continued)

### 9.2.3 Application Curve

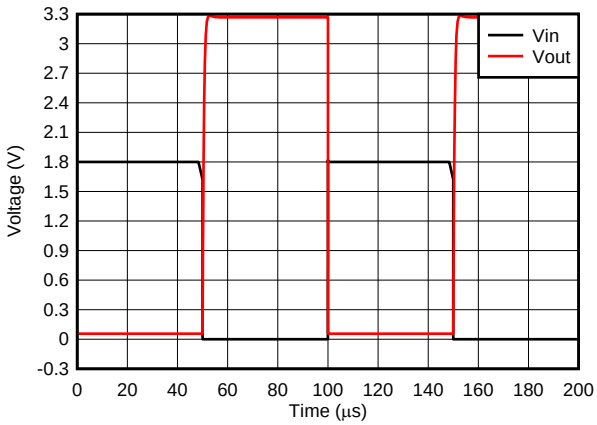



**Figure 8. Simulated up-translation with the SN74AUP1G06**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple $V_{CC}$ pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 10 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

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## 11.2 Layout Example

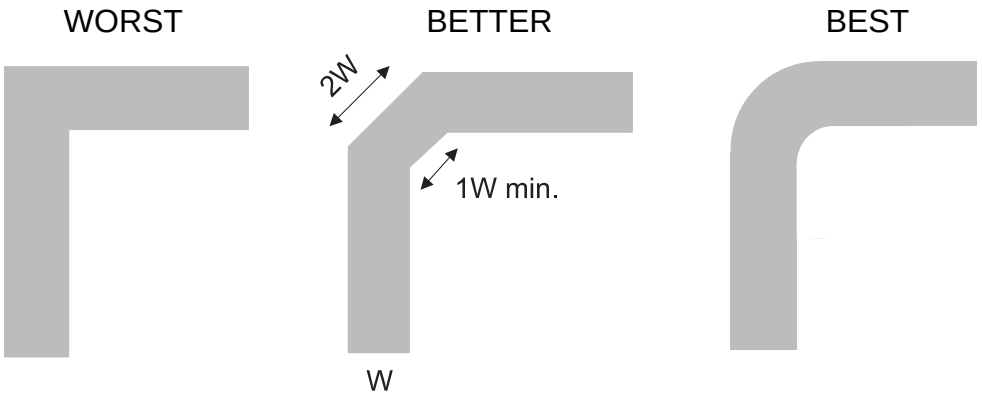



**Figure 9. Trace Example**

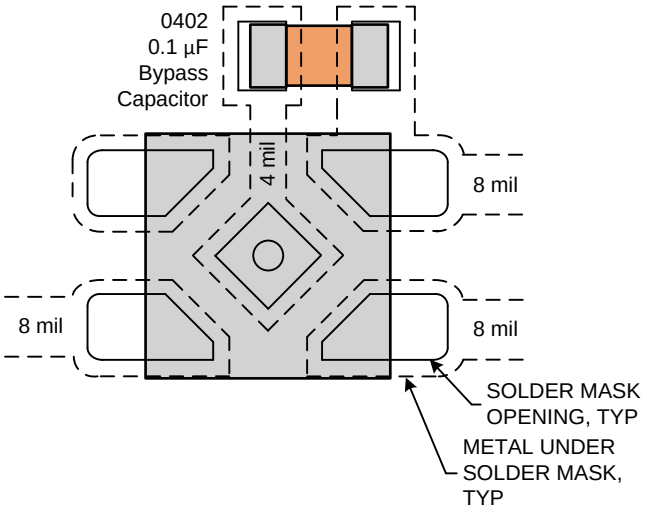



**Figure 10. Example Layout With DPW (X2SON-5) Package**


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Designing and Manufacturing with TI's X2SON Packages* application note
- Texas Instruments, *How to Select Little Logic* application note
- Texas Instruments, *Introduction to Logic* application note
- Texas Instruments, *Understanding Schmitt Triggers* application note
- Texas Instruments, *Semiconductor Packing Material Electrostatic Discharge (ESD) Protection* application note
- Texas Instruments, *Logic Guide* selection & solution suides
- Texas Instruments, *Little Logic Guide 2014* selection & solution guides
- Texas Instruments, *Little Logic Guide 2012* selection & solution guides

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## GENERIC PACKAGE VIEW

**DPW 5** **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

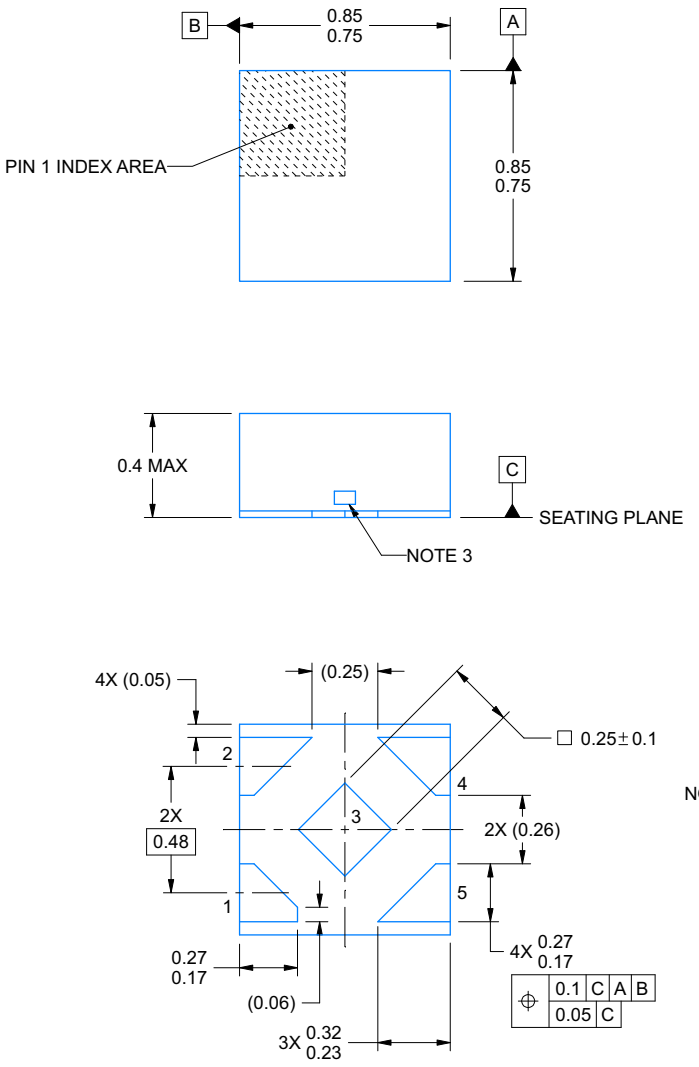
4211218-3/D

# PACKAGE OUTLINE

## DPW0005A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

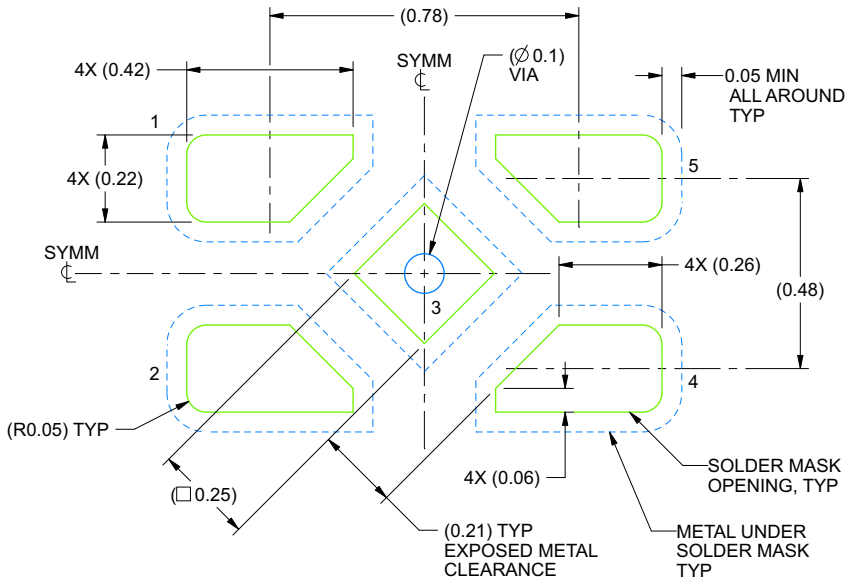

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# EXAMPLE BOARD LAYOUT

## DPW0005A

### X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

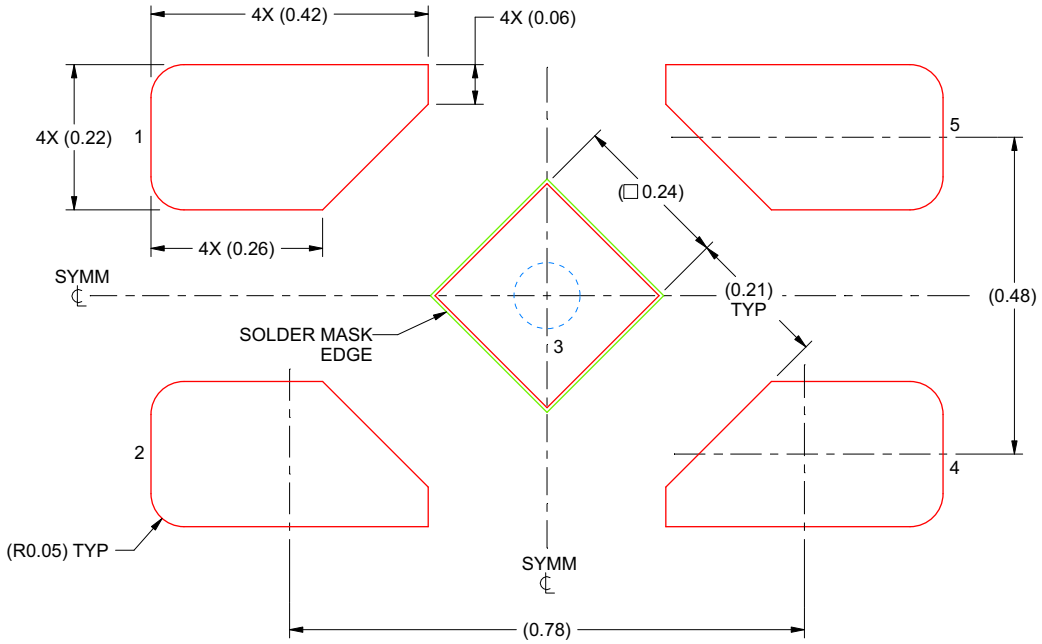
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).


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## EXAMPLE STENCIL DESIGN

**DPW0005A** — **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G06DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H06R |
| SN74AUP1G06DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H06R |
| SN74AUP1G06DBVRE4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H06R |
| SN74AUP1G06DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H06R |
| SN74AUP1G06DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H06R |
| SN74AUP1G06DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H06R |
| SN74AUP1G06DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (HT5, HTF, HTR) |
| SN74AUP1G06DCKR.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | (HT5, HTF, HTR) |
| SN74AUP1G06DCKRG4 | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HT5, HTF, HTR) |
| SN74AUP1G06DCKRG4.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HT5, HTF, HTR) |
| SN74AUP1G06DCKT | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HT5, HTR) |
| SN74AUP1G06DCKT.B | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HT5, HTR) |
| SN74AUP1G06DPWR | Active | Production | X2SON (DPW) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CH |
| SN74AUP1G06DPWR.B | Active | Production | X2SON (DPW) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CH |
| SN74AUP1G06DRLR | Active | Production | SOT-5X3 (DRL) \| 5 | 4000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HT7, HTR) |
| SN74AUP1G06DRLR.B | Active | Production | SOT-5X3 (DRL) \| 5 | 4000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HT7, HTR) |
| SN74AUP1G06DRYR | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DRYR.B | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DSF2 | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DSF2.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DSFR | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DSFR.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DSFRG4 | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06DSFRG4.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT |
| SN74AUP1G06YFPR | Active | Production | DSBGA (YFP) \| 4 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | - | HT<br>N |
| SN74AUP1G06YFPR.B | Active | Production | DSBGA (YFP) \| 4 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HT<br>N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

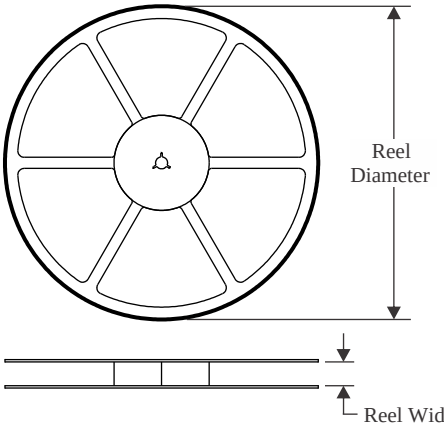
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

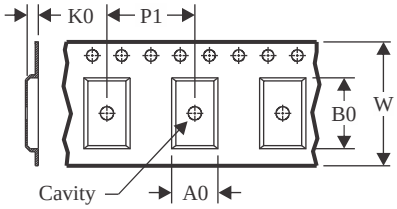
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

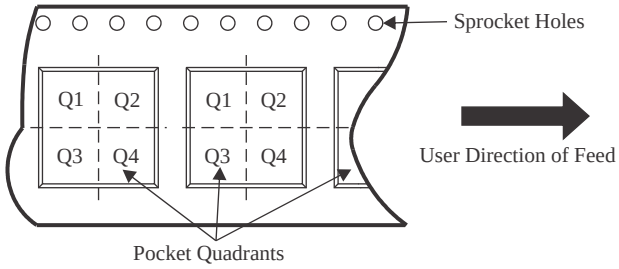



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

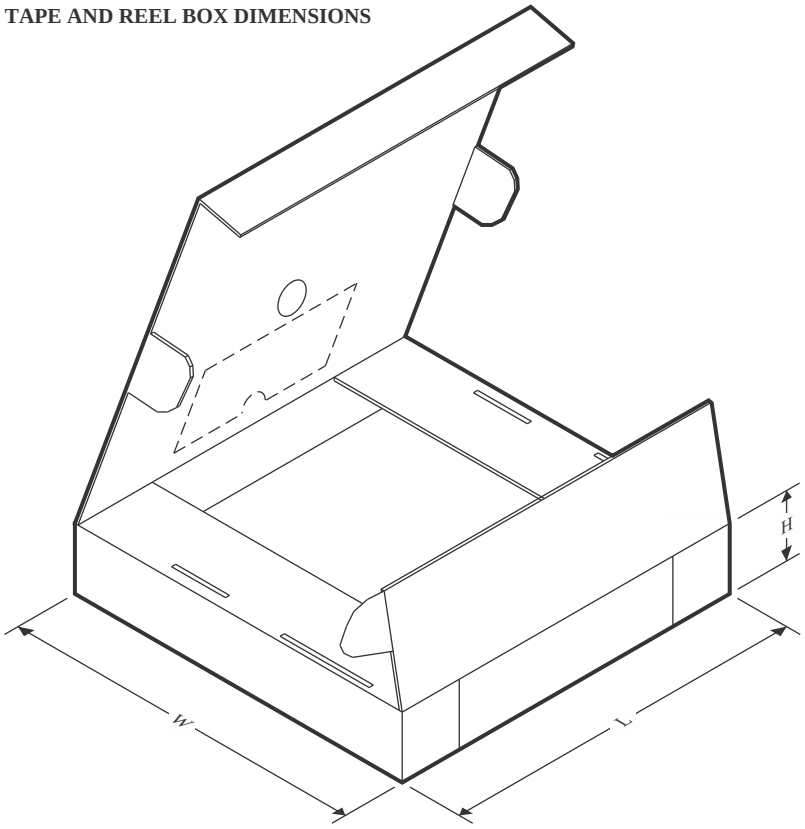



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G06DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74AUP1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G06DRYR | SON | DRY | 6 | 5000 | 180.0 | 8.4 | 1.25 | 1.6 | 0.7 | 4.0 | 8.0 | Q1 |
| SN74AUP1G06DSF2 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G06DSF2 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DSF2 | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| SN74AUP1G06DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.63 | 4.0 | 8.0 | Q2 |
| SN74AUP1G06DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G06DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G06DSFRG4 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G06YFPR | DSBGA | YFP | 4 | 3000 | 178.0 | 9.2 | 0.89 | 0.89 | 0.58 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1G06DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G06DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G06DCKRG4 | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G06DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G06DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AUP1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G06DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G06DRYR | SON | DRY | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DSF2 | SON | DSF | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DSF2 | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G06DSF2 | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |

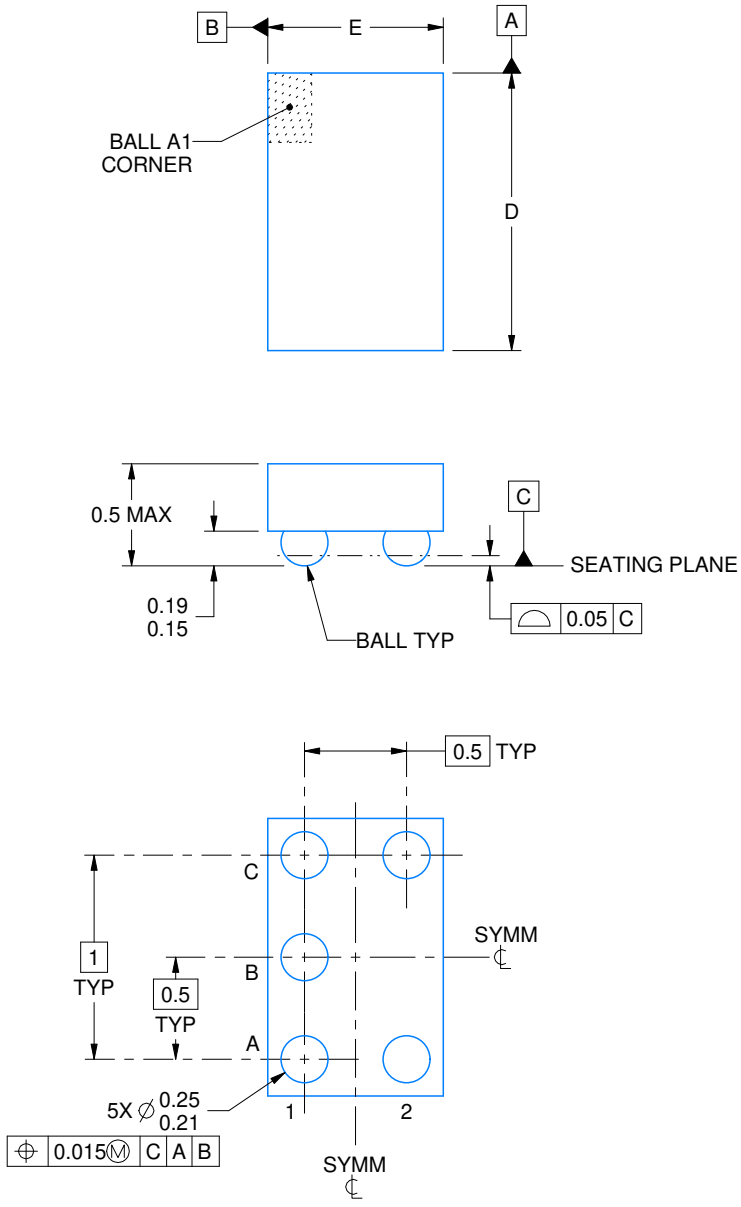
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AUP1G06DSFR | SON | DSF | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G06DSFR | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G06DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G06DSFRG4 | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G06YFPR | DSBGA | YFP | 4 | 3000 | 270.0 | 225.0 | 227.0 |

# PACKAGE OUTLINE

## YZP0005

## DSBGA - 0.5 mm max height

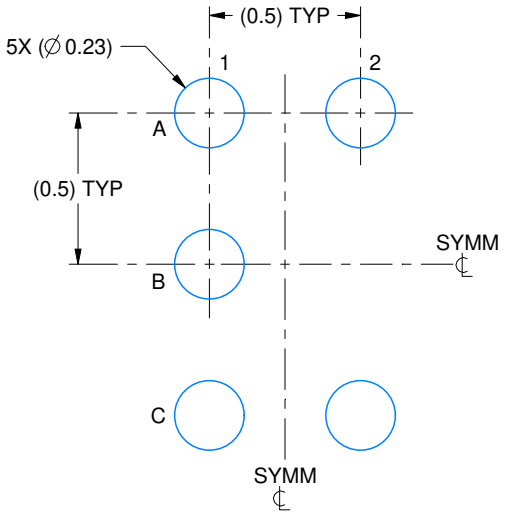
DIE SIZE BALL GRID ARRAY



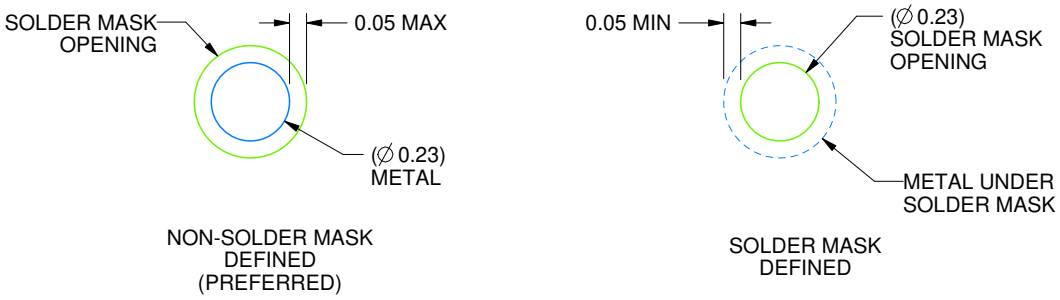

4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

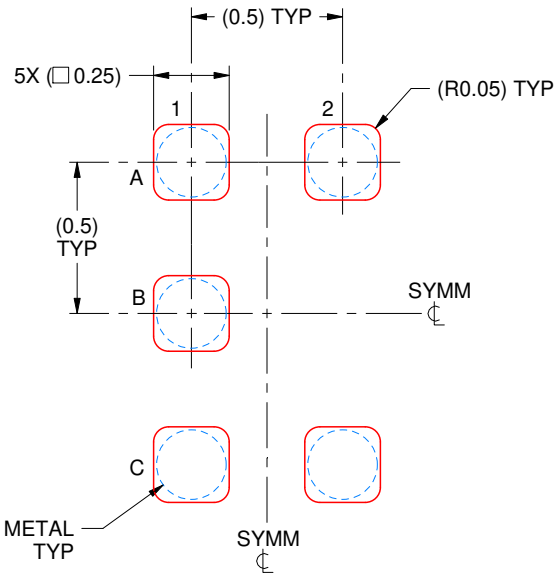



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

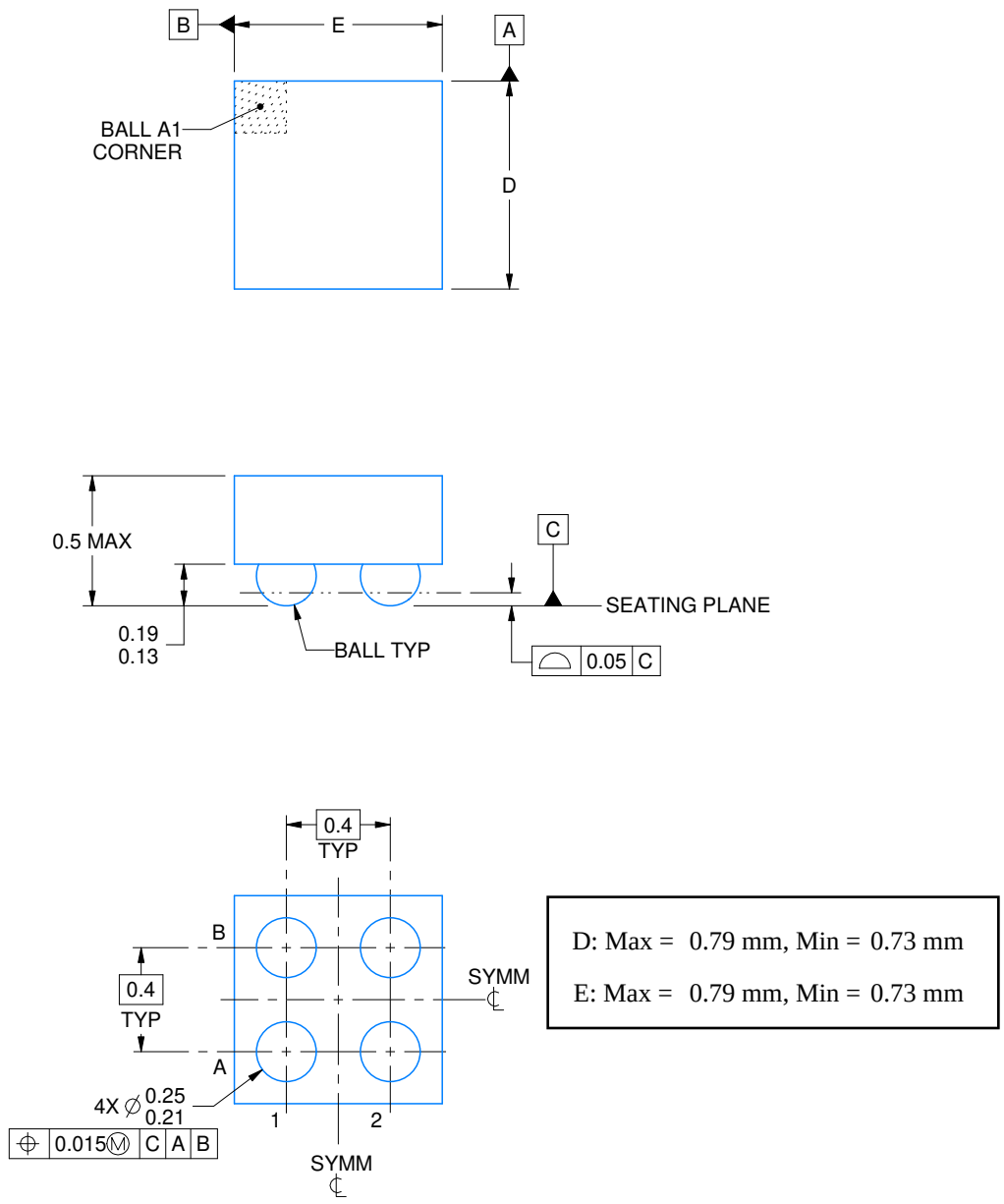
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## YFP0004

## DSBGA - 0.5 mm max height

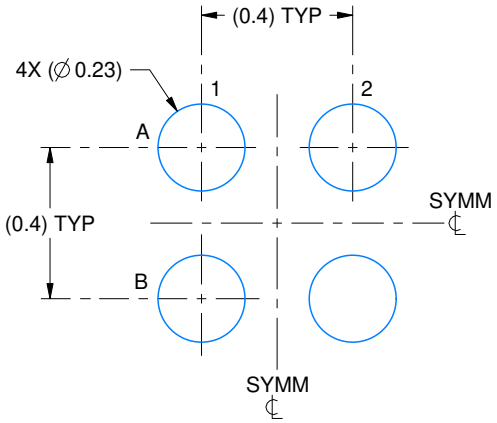
DIE SIZE BALL GRID ARRAY



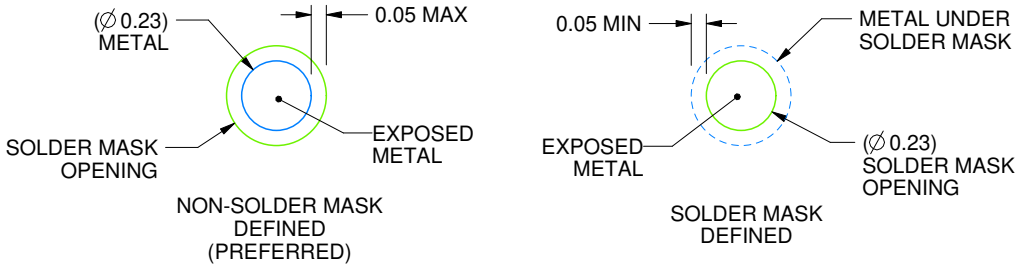

4223507/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X

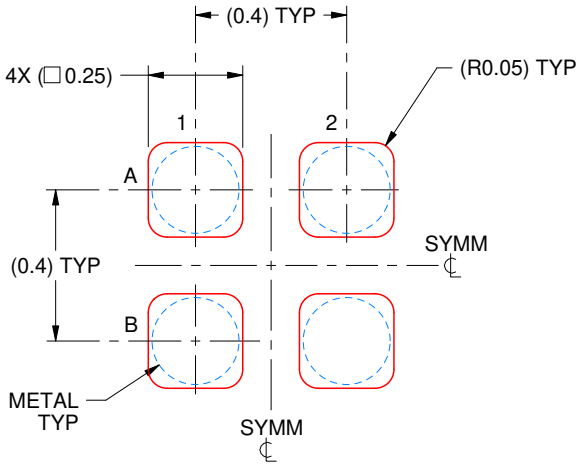



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

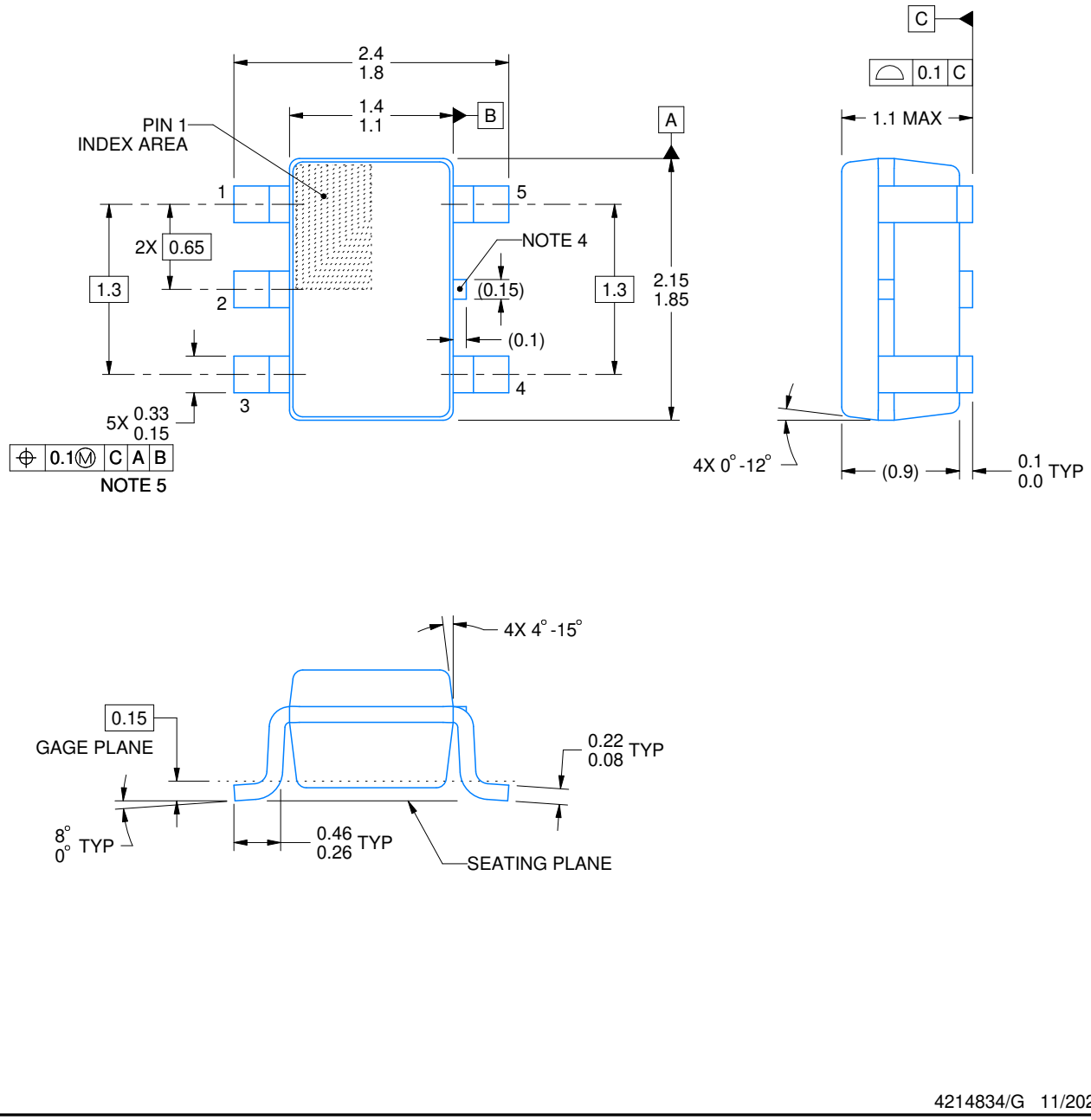
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

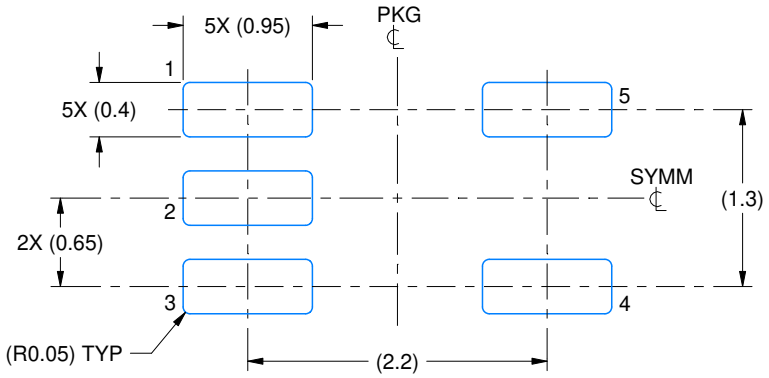
SMALL OUTLINE TRANSISTOR



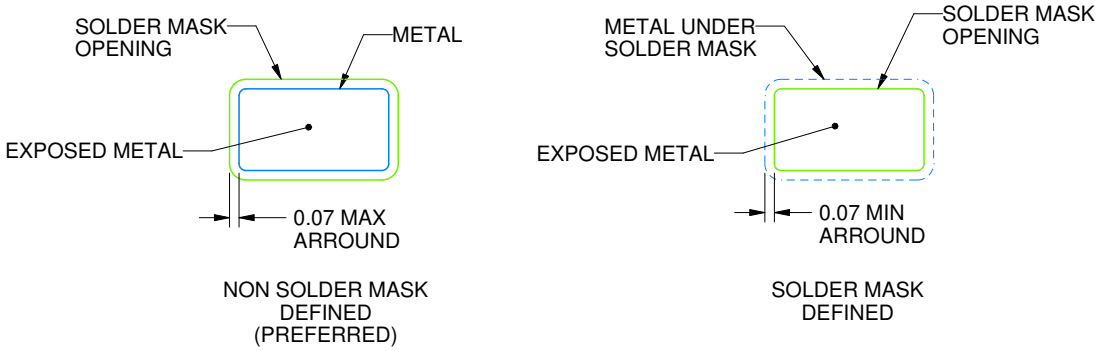

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

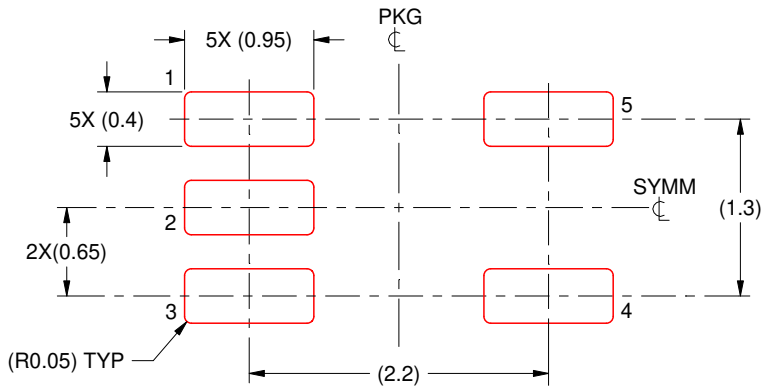



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

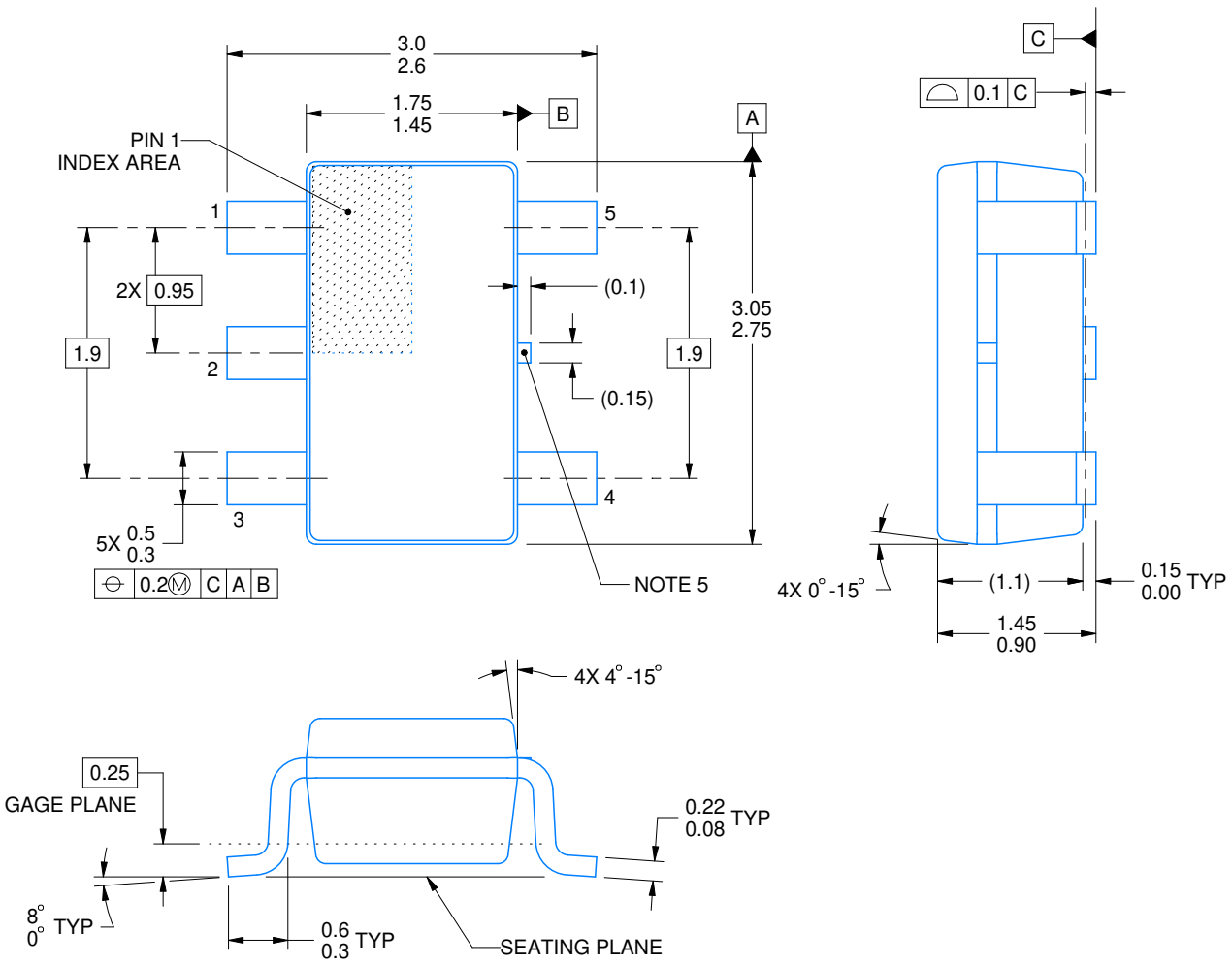
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

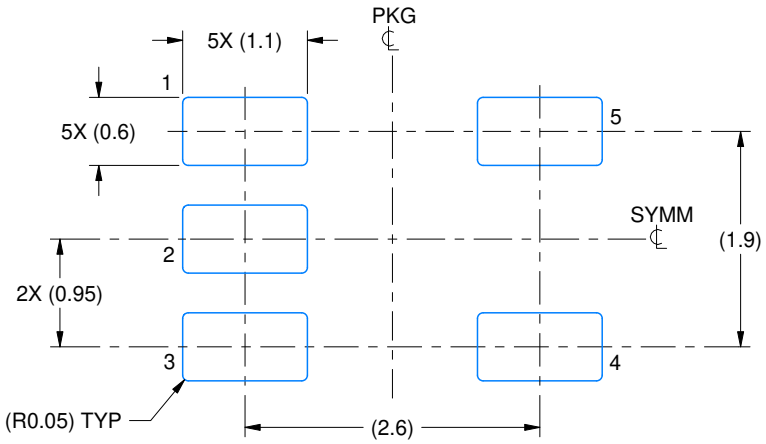
SMALL OUTLINE TRANSISTOR



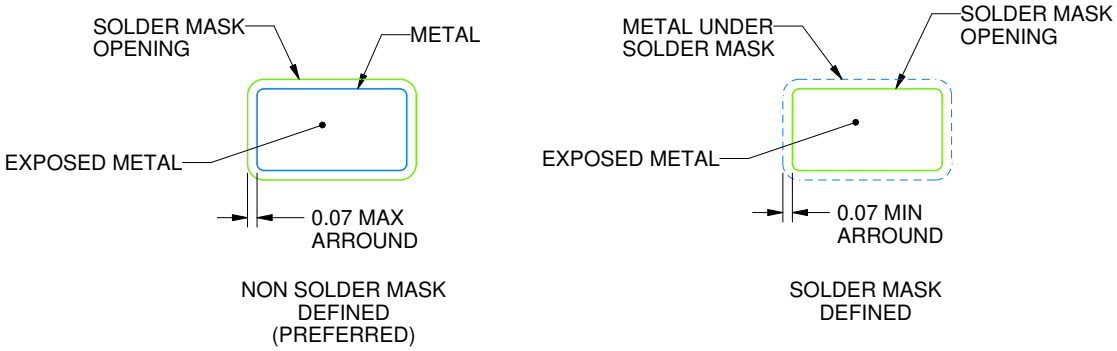

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

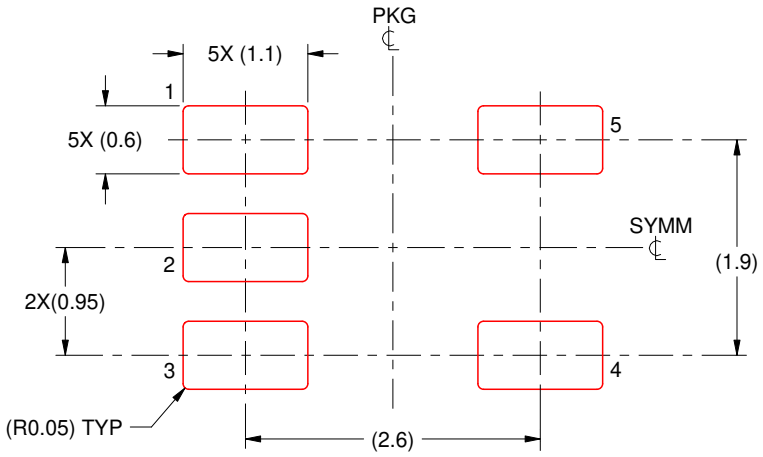



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



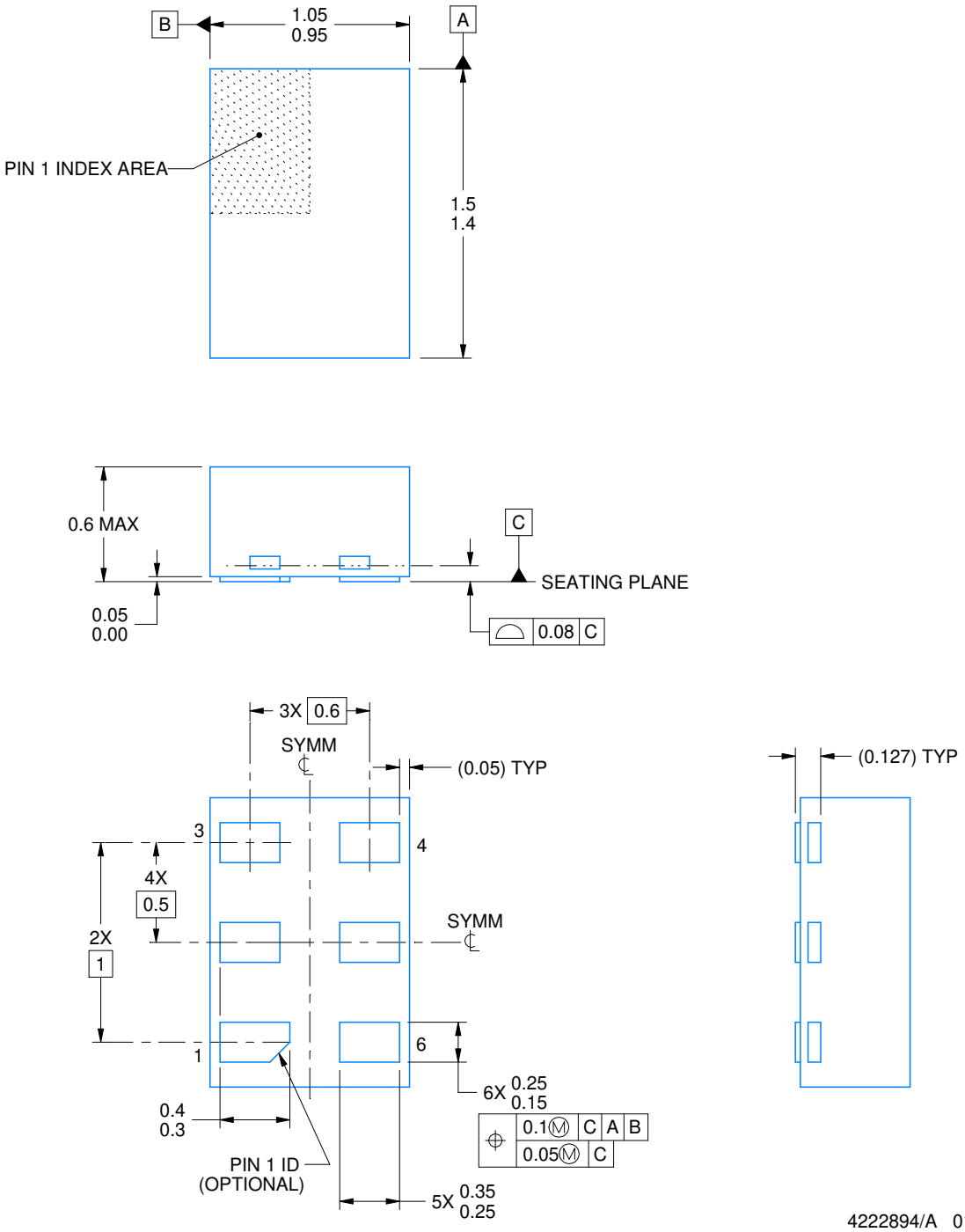

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DRY0006A

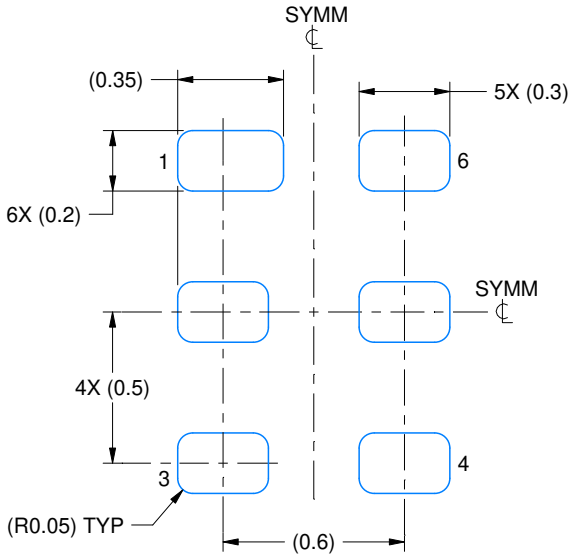
## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

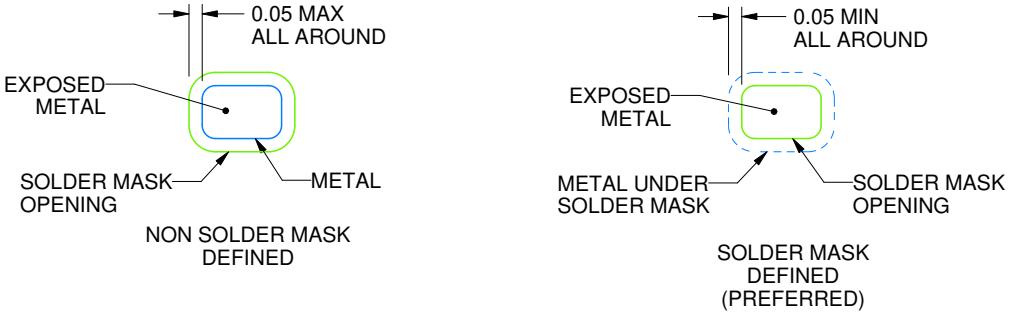



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

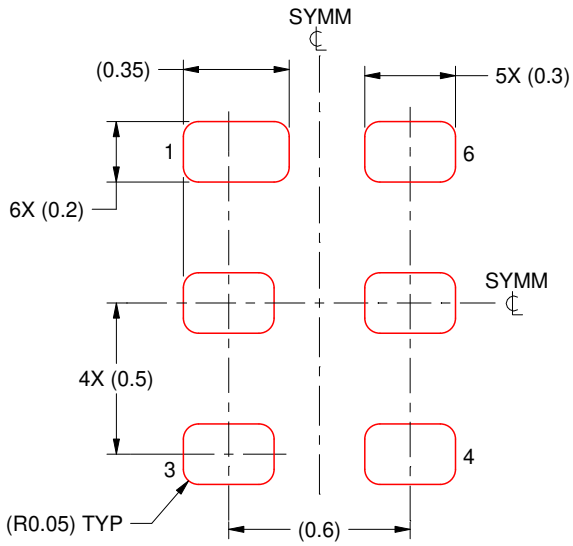
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

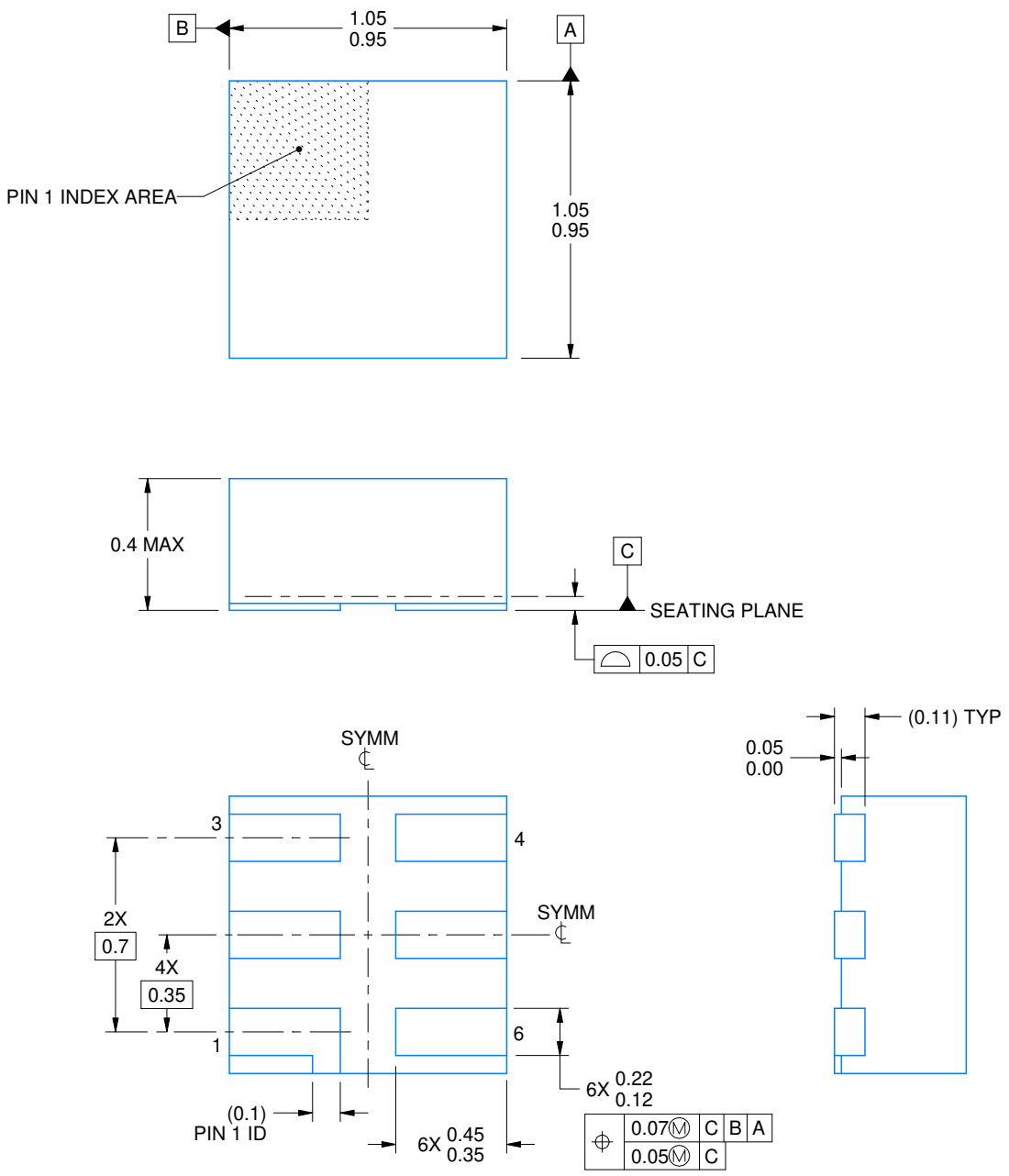
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

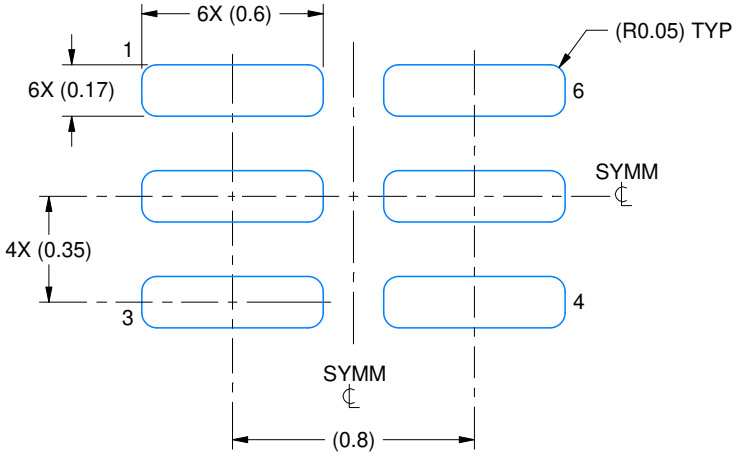
## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

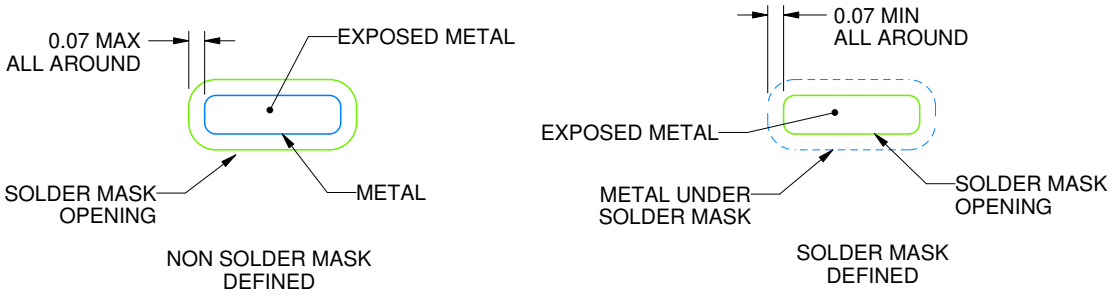



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

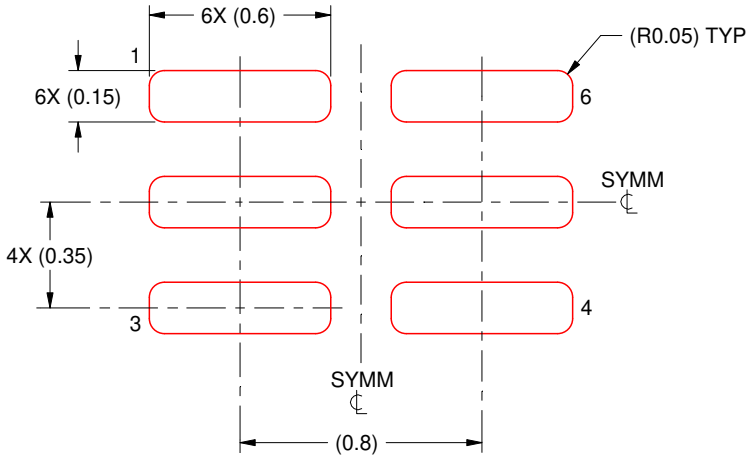
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

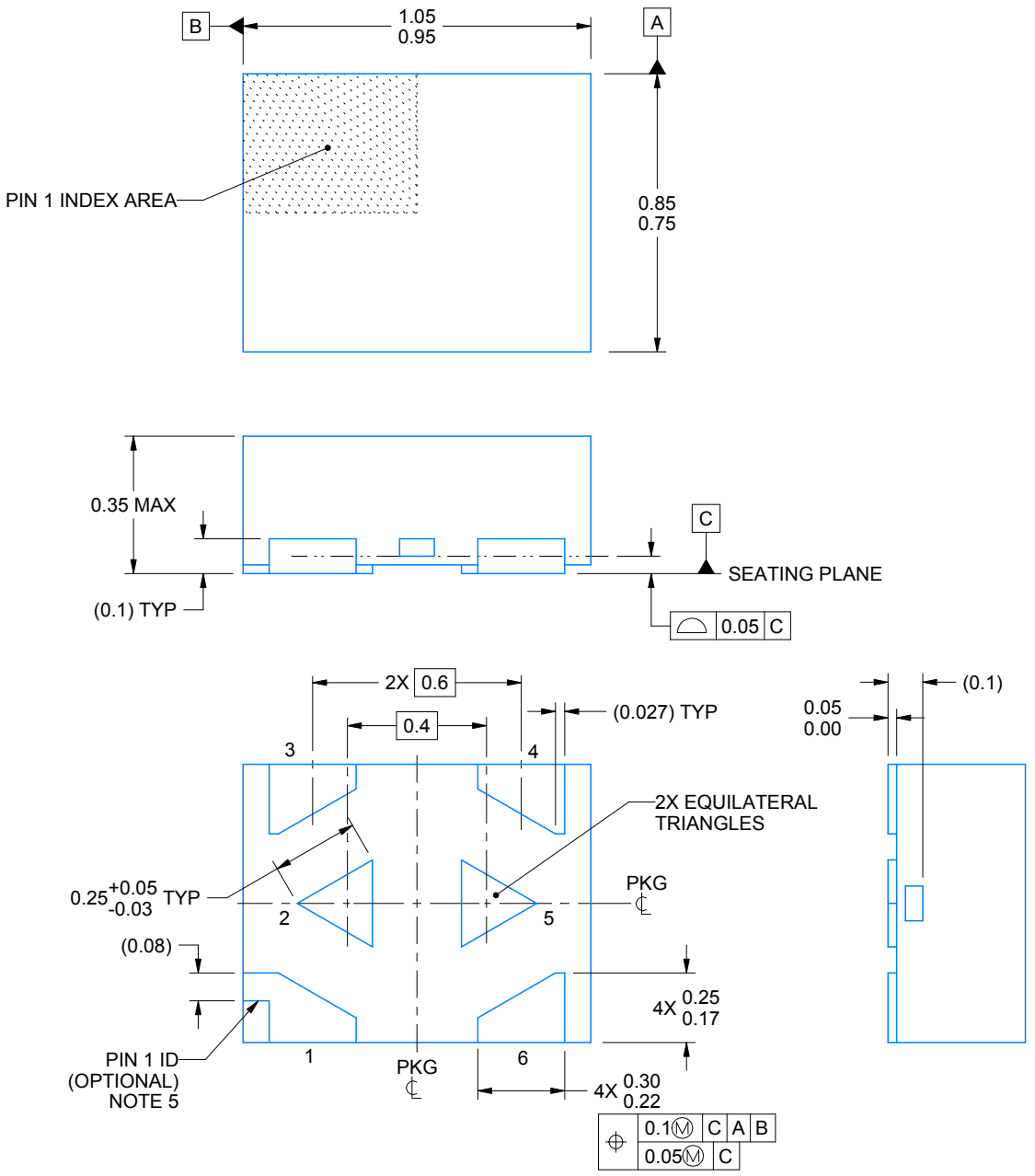
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DTB0006A

## X2SON - 0.35 mm max height

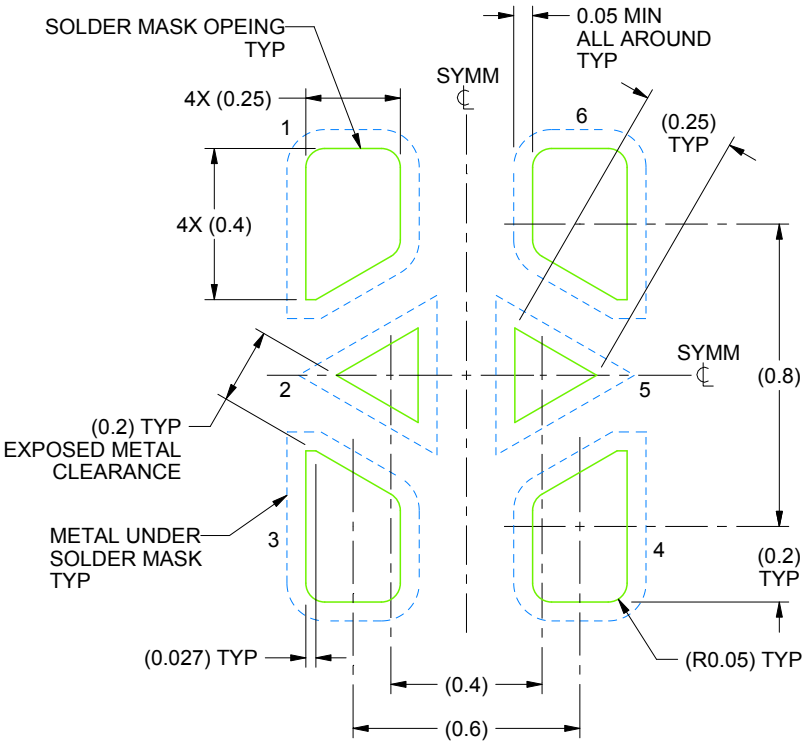
PLASTIC SMALL OUTLINE - NO LEAD




4223406/C 02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

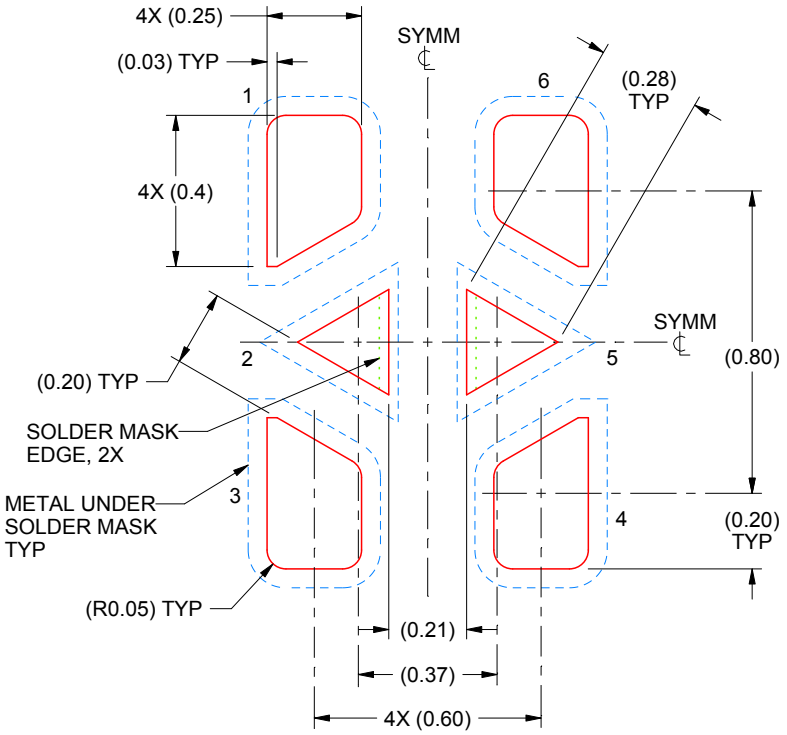



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

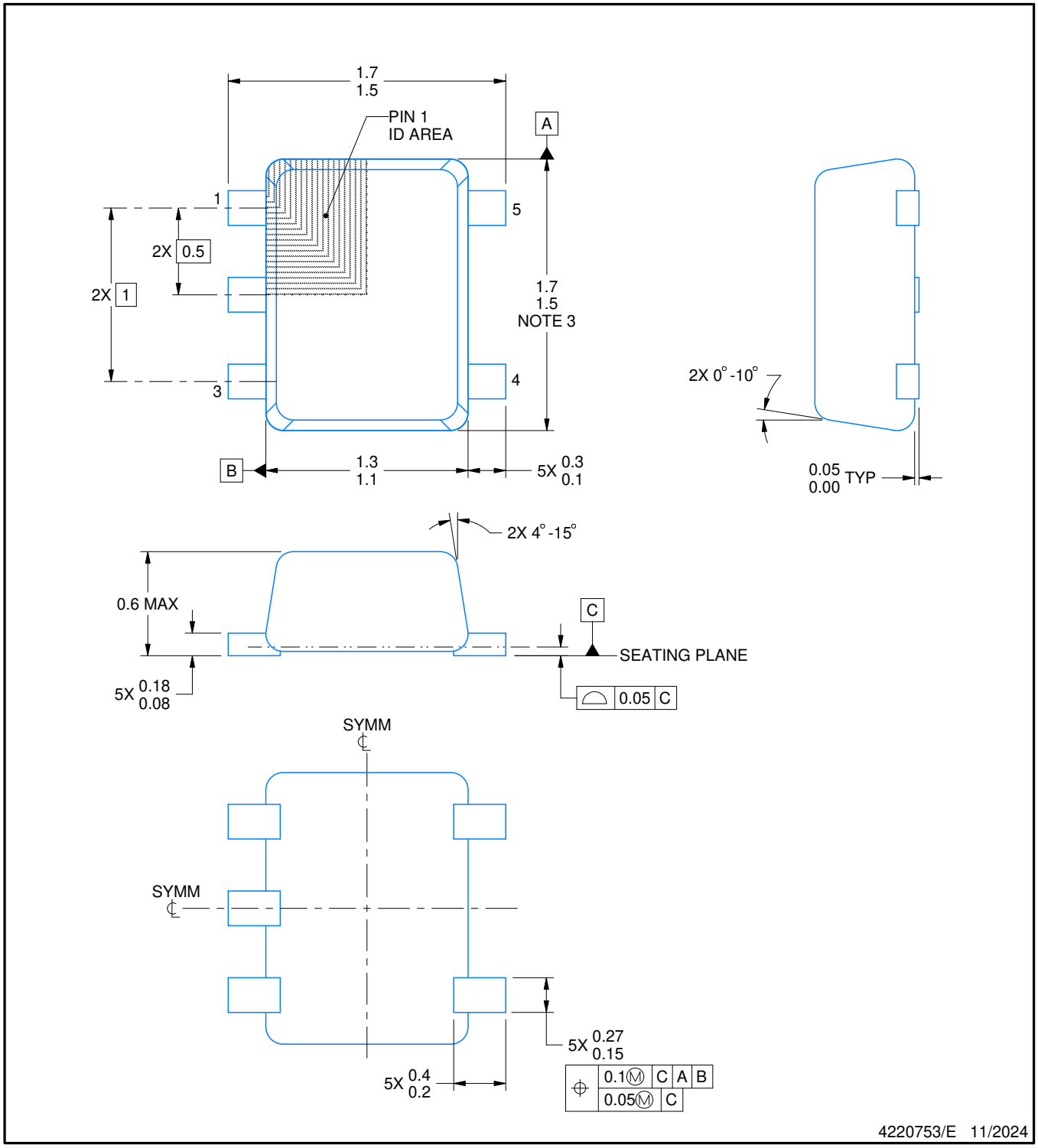
# DRL0005A



# PACKAGE OUTLINE

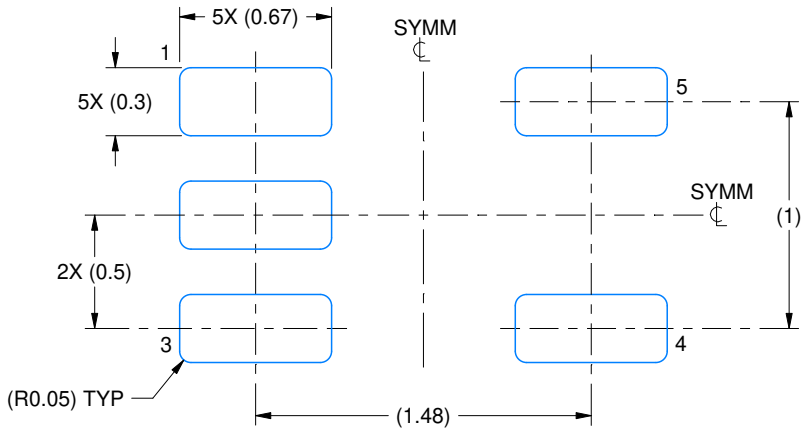
## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

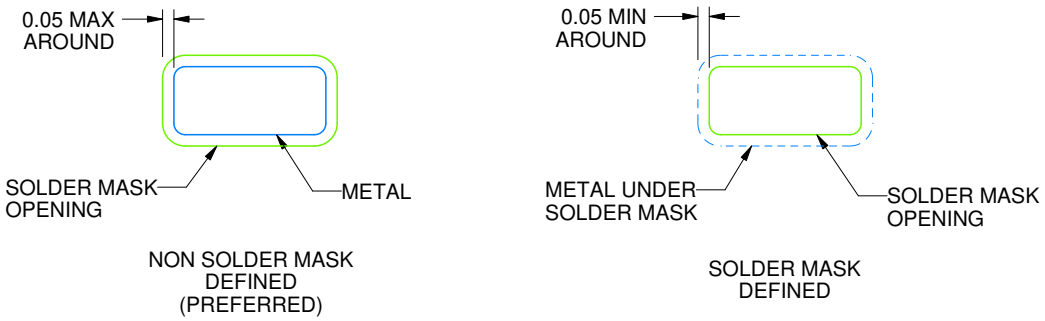



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




LAND PATTERN EXAMPLE
SCALE:30X

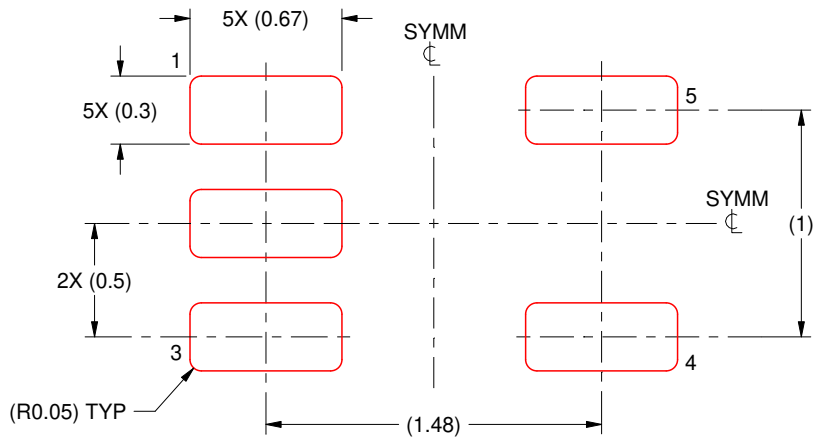



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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