16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: SN74AVCB164245-EP

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC}**
- **Control Inputs V_{IH} and V_{IL} Levels Are Referenced to V_{CCB} Voltage**
- **If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State**
- **Overvoltage-Tolerant Inputs and Outputs Allow Mixed-Voltage-Mode Data Communications**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.4-V to 3.6-V Power-Supply Range**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **750-V Charged-Device Model (C101)**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (-55°C to 125°C) Temperature Ranges** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

DESCRIPTION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCB164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCB164245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are supplied by V_{CCB}.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CCB} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, both ports are in the high-impedance state.

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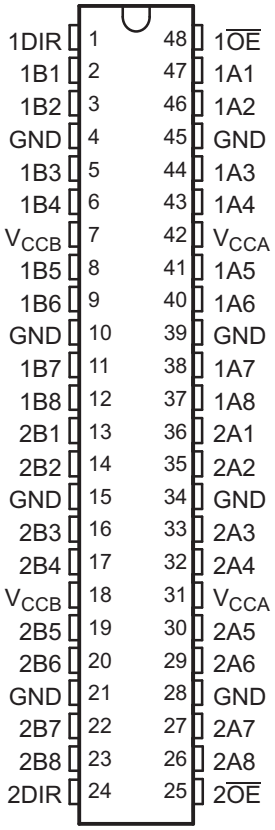
Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TSSOP-DGG	Reel of 2000	CAVCB164245MDGGREP	AVCB164245M	V62/13602-01XE
		Tube of 40	CAVCB164245MDGGEP		V62/13602-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

TERMINAL ASSIGNMENTS

DGG PACKAGE
(TOP VIEW)

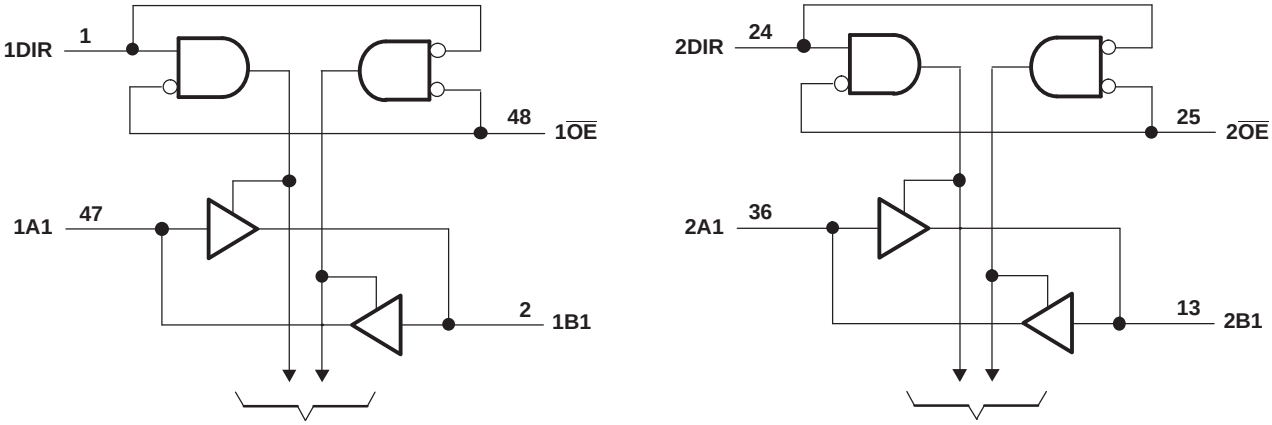


FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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Figure 1. LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DGV packages.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

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THERMAL INFORMATION

THERMAL METRIC(1)		SN74AVCB164245 DGG 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	59.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	13.9	
θ_{JB}	Junction-to-board thermal resistance(4)	27.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	26.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS(1)(2)(3)

T_A = −55°C to 125°C, over recommended input voltage range (unless otherwise noted)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.4	3.6	V
V_{CCB}	Supply voltage				1.4	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V		V_{CCB} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCB})	1.4 V to 1.95 V			V_{CCB} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.4 V to 1.6 V		–2	mA
				1.65 V to 1.95 V		–4	
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.4 V to 1.6 V		2	mA
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–55	125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the data output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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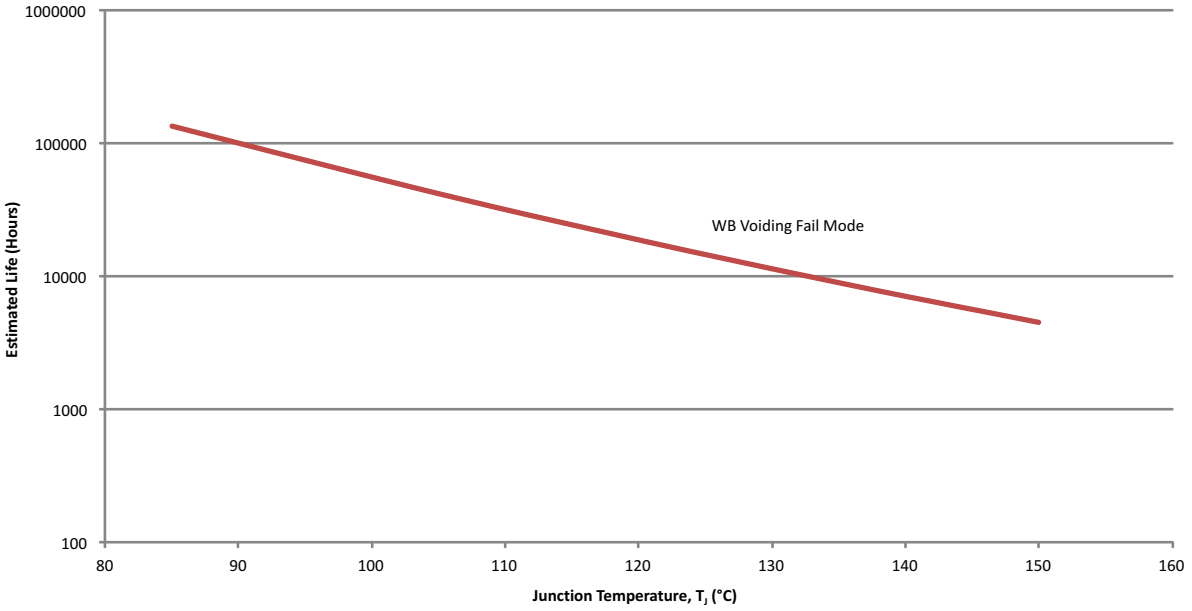
ELECTRICAL CHARACTERISTICS(1)(2)

T_A = −55°C to 125°C, over recommended input voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP(3)	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.4 V to 3.6 V	1.4 V to 3.6 V	V_{CCO} – 0.2			V
		I_{OH} = –2 mA	$V_I = V_{IH}$	1.4 V	1.4 V	1.05			
		I_{OH} = –4 mA	$V_I = V_{IH}$	1.65 V	1.65 V	1.2			
		I_{OH} = –8 mA	$V_I = V_{IH}$	2.3 V	2.3 V	1.7			
		I_{OH} = –12 mA	$V_I = V_{IH}$	3 V	3 V	2.2			
V_{OL}		I_{OH} = 100 µA	$V_I = V_{IL}$	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		I_{OH} = 2 mA	$V_I = V_{IL}$	1.4 V	1.4 V			0.35	
		I_{OH} = 4 mA	$V_I = V_{IL}$	1.65 V	1.65 V			0.45	
		I_{OH} = 8 mA	$V_I = V_{IL}$	2.3 V	2.3 V			0.6	
		I_{OH} = 12 mA	$V_I = V_{IL}$	3 V	3 V			0.75	
I_I	Control inputs	$V_I = V_{CCB}$ or GND		1.4 V to 3.6 V	3.6 V			±2.5	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V			±10	µA
	B port			0 to 3.6 V	0 V			±10	
I_{OZ} (4)	A or B ports	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V			±12.5	µA
	B port		$\overline{OE}$ = don't care	0 V	3.6 V			±12.5	
	A port			3.6 V	0 V			±12.5	
I_{CCA}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.6 V	1.6 V			35	µA
				1.95 V	1.95 V			35	
				2.7 V	2.7 V			45	
				0 V	3.6 V			-50	
				3.6 V	0 V			50	
				3.6 V	3.6 V			50	
I_{CCB}		$V_I = V_{CCI}$ or GND,	I_O = 0	1.6 V	1.6 V			35	µA
				1.95 V	1.95 V			35	
				2.7 V	2.7 V			45	
				0 V	3.6 V			50	
				3.6 V	0 V			-50	
				3.6 V	3.6 V			50	
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		4		pF
C_{io}	A or B ports	V_O = 3.3 V or GND		3.3 V	3.3 V		5		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) All typical values are at T_A = 25°C.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

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(1) See datasheet for absolute maximum and minimum recommended operating conditions.

Figure 2. SN74AVCB164245-EP Operating Life Derating Chart

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 1.5 V ± 0.1 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t_{en}	$\overline{OE}$	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
		B	2.1	9	2.9	9.8	3.2	10	3	9.8	
t_{dis}	$\overline{OE}$	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
		B	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 1.5 V ± 0.1 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12.7		12.3		11.5		11.8	ns
	B	A		12.8		13.4		13.6		13.3	
t_{en}	$\overline{OE}$	A		14.8		13.9		12.4		11.9	ns
		B		15		15.8		16		15.8	
t_{dis}	$\overline{OE}$	A		12.9		12.1		9.6		9	ns
		B		13.1		12.4		11.1		10.8	

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 1.8 V ± 0.15 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.7	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t_{en}	$\overline{OE}$	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t_{dis}	$\overline{OE}$	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
		B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 1.8 V ± 0.15 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12.7		12		10.7		10.3	ns
	B	A		11.5		12		11.8		11.5	
t_{en}	$\overline{OE}$	A		14.5		13.5		12.1		11.9	ns
		B		13.6		13.7		13.6		13.4	
t_{dis}	$\overline{OE}$	A		13		12.1		9.6		9	ns
		B		13		12.3		10.7		10.4	

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Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 2.5 V ± 0.2 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	$\overline{OE}$	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
t_{dis}	$\overline{OE}$	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
		B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 2.5 V ± 0.2 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		12		11.6		10		9.4	ns
	B	A		10.6		10.4		10		9.7	
t_{en}	$\overline{OE}$	A		14.5		13.5		11.3		10.2	ns
		B		11.7		11.5		11.3		11.1	
t_{dis}	$\overline{OE}$	A		13		12.1		9.6		9	ns
		B		11.8		11		9.6		9.3	

Switching Characteristics

T_A = −40°C to 85°C, V_{CCA} = 3.3 V ± 0.3 V (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	$\overline{OE}$	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
		B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t_{dis}	$\overline{OE}$	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
		B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

SWITCHING CHARACTERISTICS

T_A = −55°C to 125°C, V_{CCA} = 3.3 V ± 0.3 V (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		11.9		11.4		9.7		9.1	ns
	B	A		10.5		9.8		9.3		9.1	
t_{en}	$\overline{OE}$	A		14.3		13.4		11.2		10.1	ns
		B		11.3		10.5		10.3		10.1	
t_{dis}	$\overline{OE}$	A		13		12		9.5		9.5	ns
		B		12.9		11.5		9.8		9.5	

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OPERATING CHARACTERISTICS

V_{CCA} and V_{CCB} = 3.3 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
C_{pdB} (V_{CCB})	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	C_L = 0, f = 10 MHz	20	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		14	
		Outputs disabled		7	

OUTPUT DESCRIPTION

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

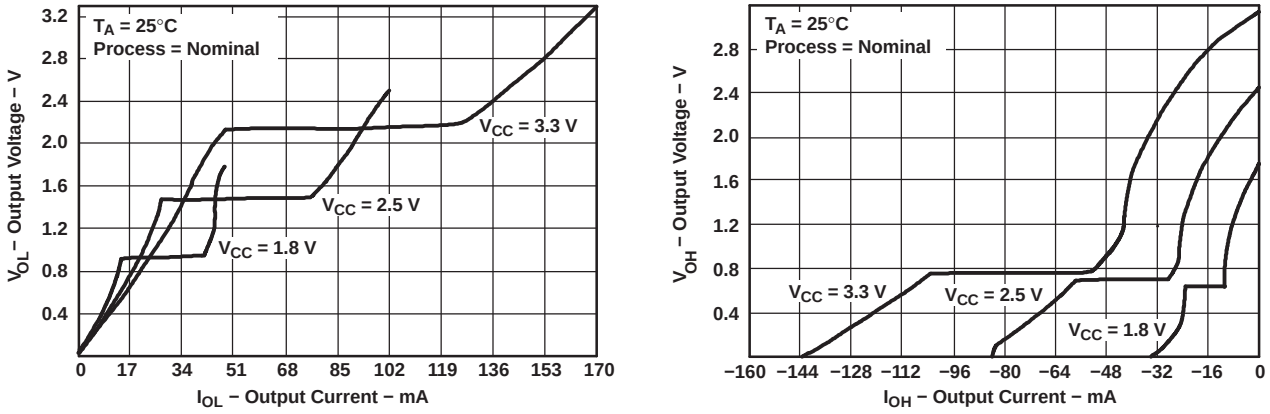
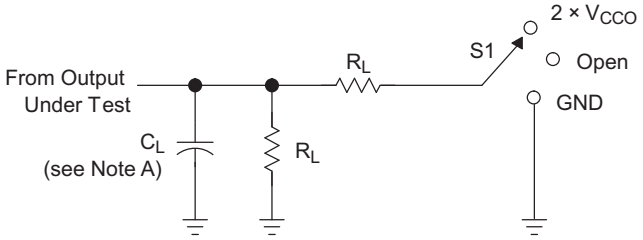


Figure 3. Typical Output Voltage vs Output Current

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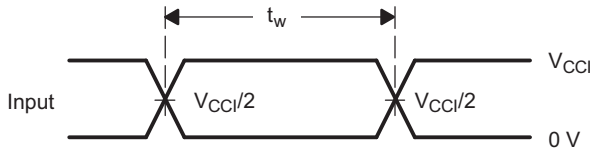
PARAMETER MEASUREMENT INFORMATION



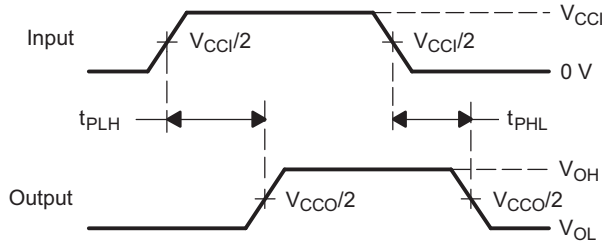
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

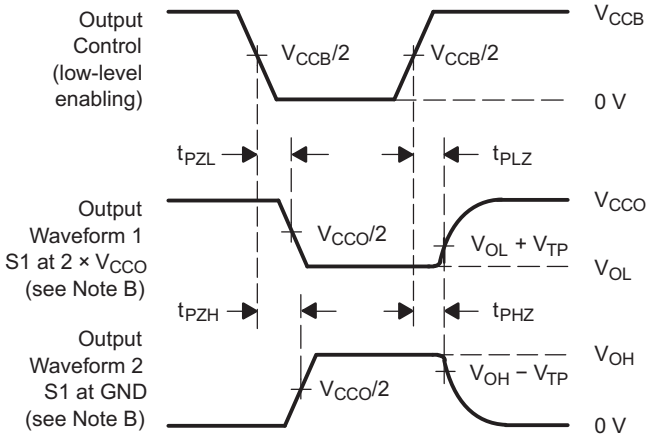
V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	500 Ω	0.1 V
1.8 V ± 0.15 V	30 pF	500 Ω	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	30 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 4. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CAVCB164245MDGGEP	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M
CAVCB164245MDGGREP	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M
V62/13602-01XE	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M
V62/13602-01XE-T	Active	Production	TSSOP (DGG) | 48	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AVCB164245M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AVCB164245-EP :

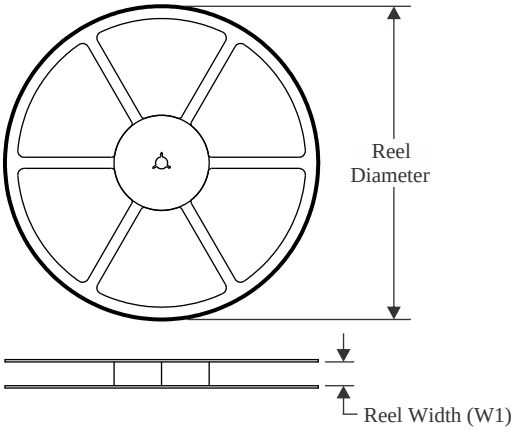
- Catalog : SN74AVCB164245
- Automotive : SN74AVCB164245-Q1

NOTE: Qualified Version Definitions:

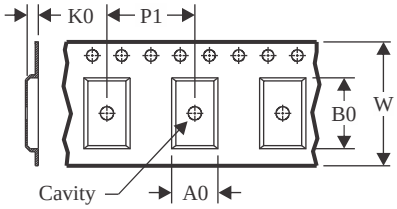
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

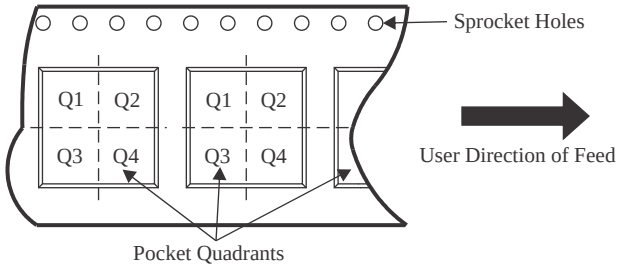


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

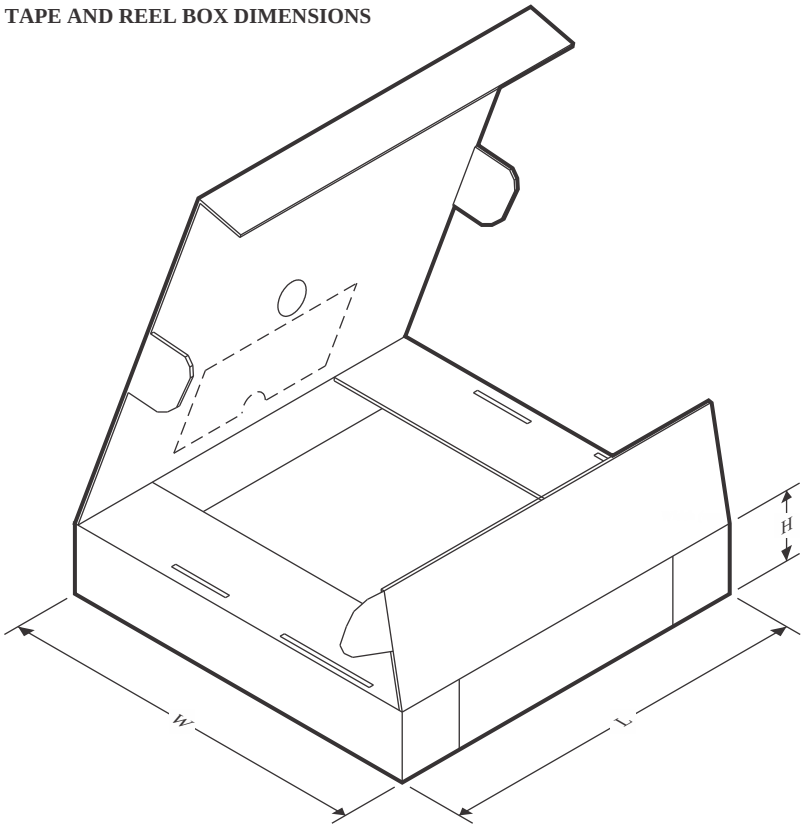
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVCB164245MDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

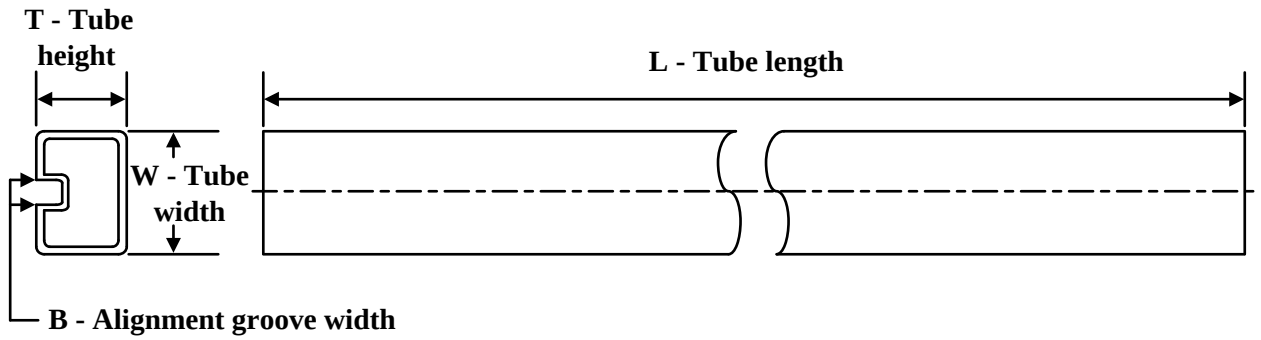
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVCB164245MDGGREP	TSSOP	DGG	48	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

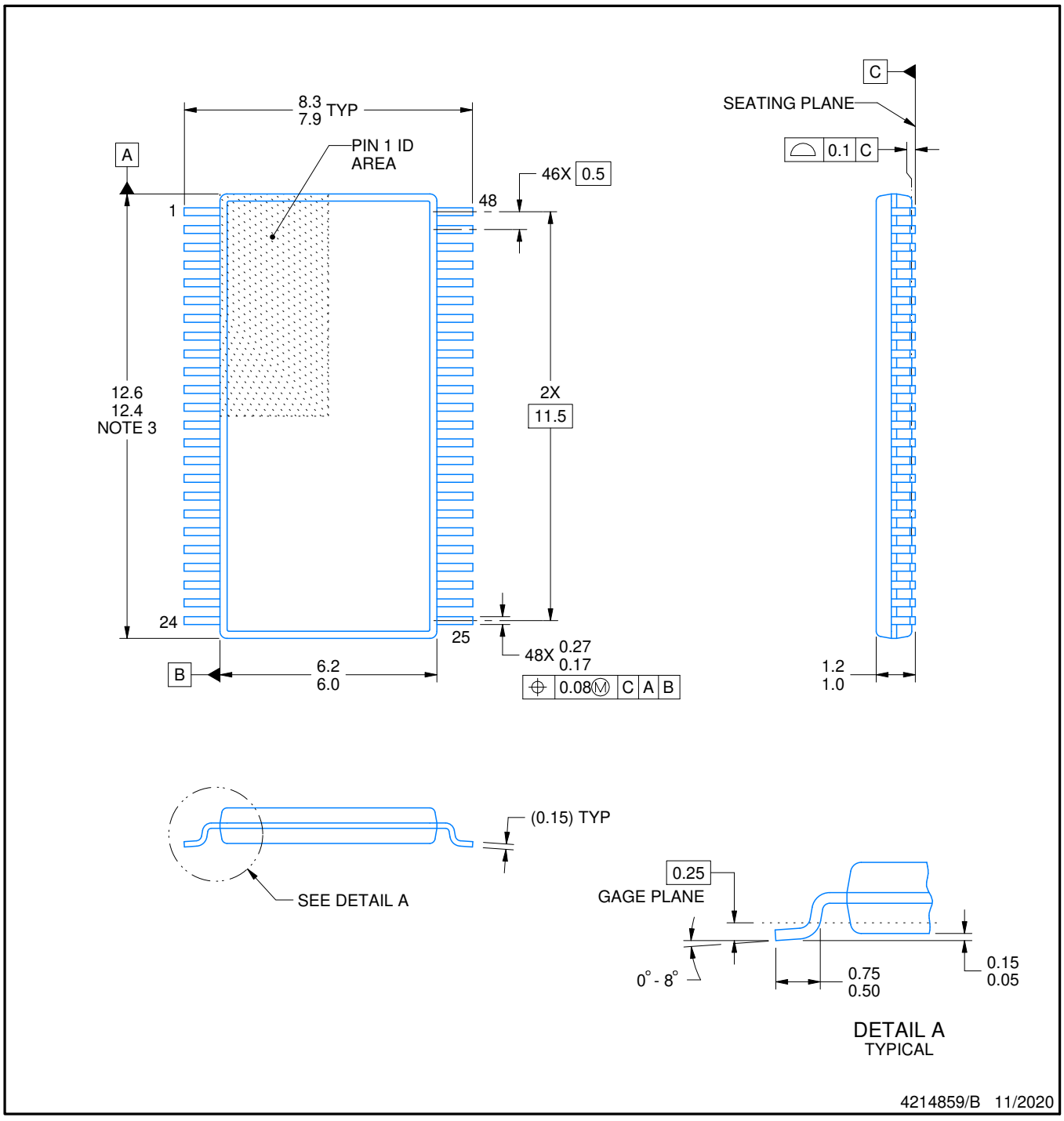
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CAVCB164245MDGGEP	DGG	TSSOP	48	40	530	11.89	3600	4.9
V62/13602-01XE-T	DGG	TSSOP	48	40	530	11.89	3600	4.9

PACKAGE OUTLINE

DGG0048A

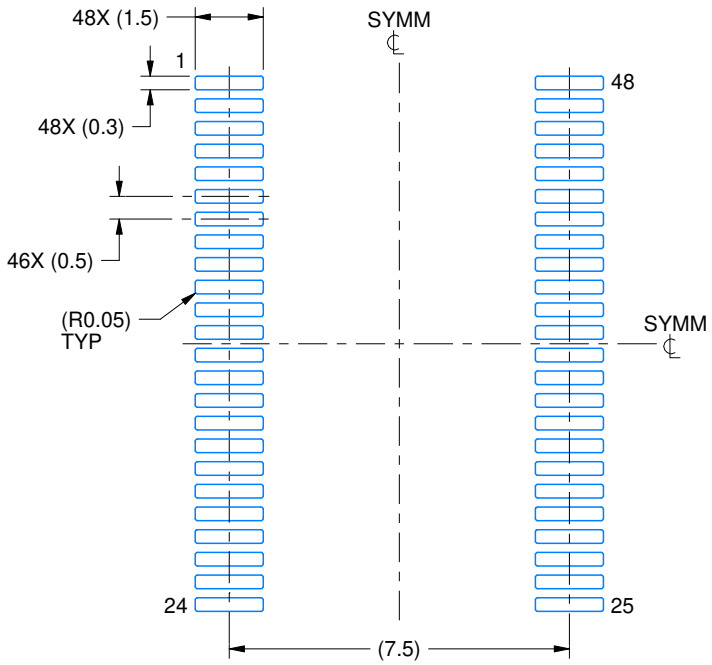
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

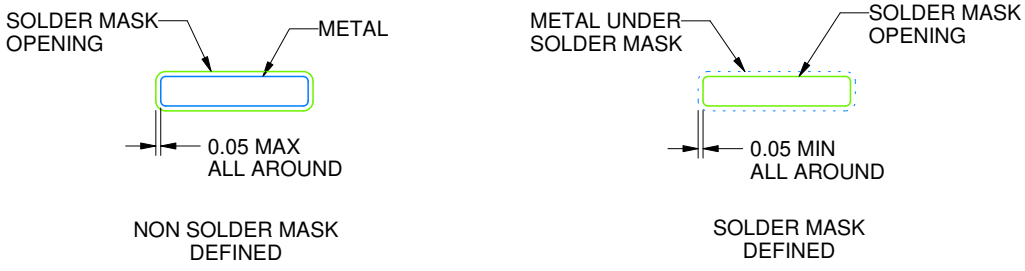


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

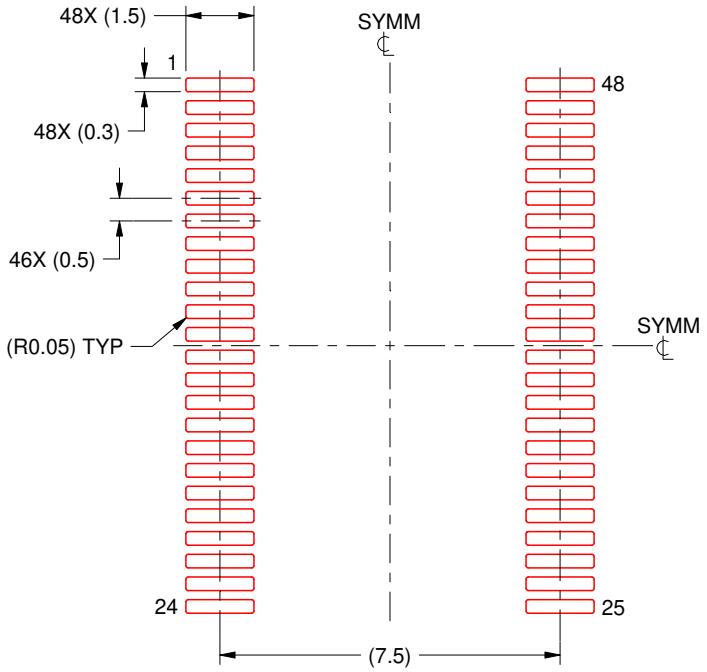


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

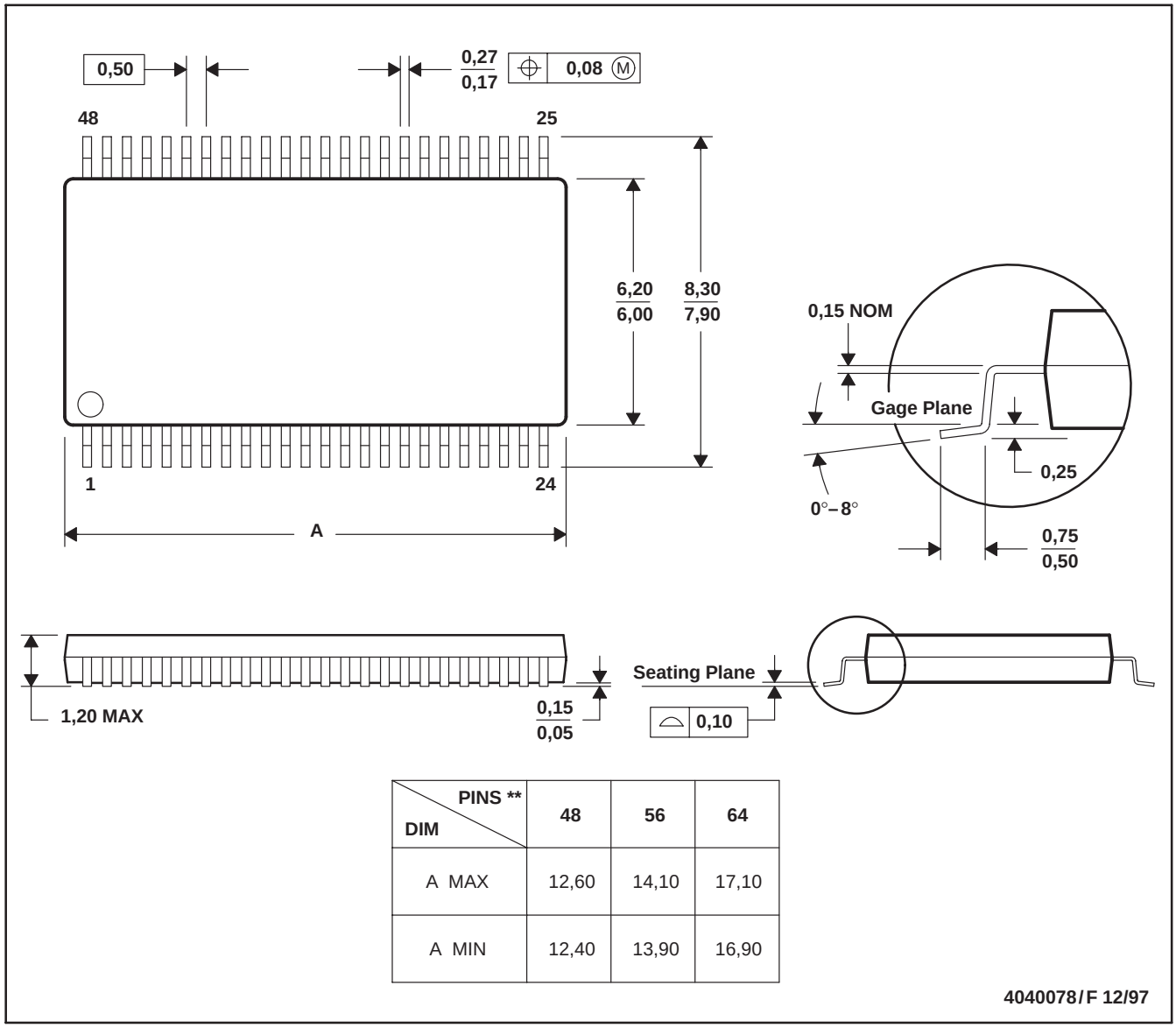
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Last updated 10/2025