SN74AXC2T245-Q1 Automotive 2-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and Tri-State Outputs

1 Features

- AEC-Q100 automotive qualified
- Fully configurable dual-rail design allows each port to operate with a power supply range rrom 0.65 V to 3.6 V
- Operating temperature from –40°C to +125°C
- DIR control input for each channel
- Glitch-free power supply sequencing
- Up to 380 Mbps support when translating from 1.8 V to 3.3 V
- V_{CC} isolation feature
  - If either V_{CC} input is below 100 mV, all I/O outputs are disabled and become high-impedance
- I_{off} supports partial-power-down mode operation
- Compatible with AVC-family level shifters
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JEDEC JS-001
  - 8000-V Human-body model
  - 1000-V Charged-device model

2 Applications

- HEV/EV
- Infotainment head unit
- ADAS fusion
- ADAS front camera
- Enterprise and communications

3 Description

The SN74AXC2T245-Q1 is a two-bit noninverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 0.65 V. The A port is designed to track V_{CCA}, which accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track V_{CCB}, which also accepts any supply voltage from 0.65 V to 3.6 V. Additionally the SN74AXC2T245-Q1 is compatible with a single-supply system.

The SN74AXC2T245-Q1 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (DIRx). The SN74AXC2T245-Q1 device is designed so the control pin (DIR) is referenced to V_{CCA}.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is less than 100 mV, both I/O ports enter a high-impedance state by disabling their outputs.

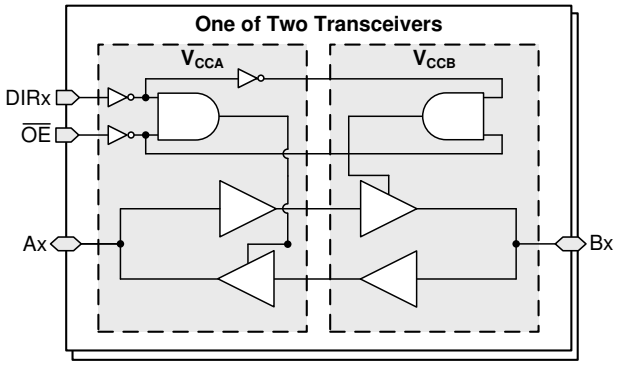
Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CAXC2T245QRSWRQ1	UQFN (10)	1.80 mm x 1.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

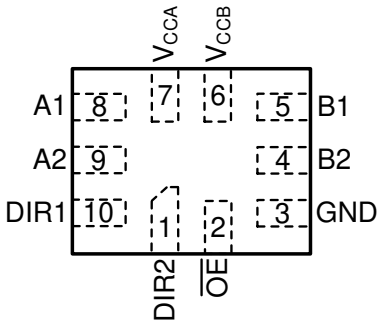
Changes from Original (February 2020) to Revision A **Page**

- Changed device status to Production Data ... 1

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5 Pin Configuration and Functions

RSW Package
10-Pin UQFN
Transparent Top View



Pin Functions

PIN	NO.	DESCRIPTION
NAME	RSW	
DIR2	1	Direction Pin for channel A2/B2, Connect to GND or to V_{CCA}
$\overline{OE}$	2	Tri-state output-mode enable. Pull OE high to place all outputs in tri-state mode. Referenced to V_{CCA}.
GND	3	Ground
B2	4	Output or input depending on state of DIR2. Output level depends on V_{CCB}.
B1	5	Output or input depending on state of DIR1. Output level depends on V_{CCB}.
V_{CCB}	6	Supply Voltage B
V_{CCA}	7	Supply Voltage A
A1	8	Output or input depending on state of DIR1. Output level depends on V_{CCA}.
A2	9	Output or input depending on state of DIR2. Output level depends on V_{CCA}.
DIR1	10	Direction Pin for channel A1/B1, Connect to GND or to VCCA

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2)(3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±8000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} x 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} x 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control Inputs(DIRx, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} x 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} x 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} x 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control Inputs(DIRx, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} x 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} x 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
$\Delta t/\Delta v$	Input transition rate				10	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AXC2T245-Q1 RSW (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	209.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	129.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	122.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	122.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						-40°C to 85°C			-40°C to 125°C			
						MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = -100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = -50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = -200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = -500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_I	Input leakage current	Control inputs (DIRx, $\overline{OE}$): $V_I = V_{CCA}$ or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–0.5		0.5	–1		1	µA
		Data Inputs (Ax, Bx) $V_I = V_{CCI}$ or GND		0.65 V- 3.6 V	0.65 V- 3.6 V	–4		4	–8		8	µA
I_{off}	Partial power down current	A or B Port V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	–4		4	–8		8	µA
				0 V - 3.6 V	0 V	–4		4	–8		8	
I_{OZ}	Tri-state output current (4)	A or B Port $V_I = V_{CCI}$ or GND, $V_O = V_{CCO}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	–4		4	–8		8	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			10			14	µA
				0 V	3.6 V	–2			–12			
				3.6 V	0 V			5			10	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			10			14	µA
				0 V	3.6 V			5			10	
				3.6 V	0 V	–2			–12			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65 V- 3.6 V	0.65 V- 3.6 V			16			23	µA
C_i	Control input capacitance	V_I = 3.3 V or GND		3.3 V	3.3 V		3.0			3.0		pF
C_{io}	Data I/O capacitance	$\overline{OE} = V_{CCA}$, V_O = 1.65V DC +1 MHz -16 dBm sine wave		3.3 V	3.3 V		5.1			5.1		pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All typical data is taken at 25°C.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

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6.6 Switching Characteristics, V_{CCA} = 0.7 ± 0.05 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	169	0.5	115	0.5	84	0.5	50	0.5	51	0.5	56	0.5	72	0.5	106	ns
				-40°C to 125°C	0.5	169	0.5	115	0.5	84	0.5	50	0.5	51	0.5	56	0.5	72	0.5	106	
		B	A	-40°C to 85°C	0.5	169	0.5	149	0.5	122	0.5	84	0.5	79	0.5	78	0.5	77	0.5	76	
				-40°C to 125°C	0.5	169	0.5	149	0.5	122	0.5	84	0.5	79	0.5	78	0.5	77	0.5	76	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	ns
				-40°C to 125°C	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	0.5	132	
		$\overline{OE}$	B	-40°C to 85°C	0.5	129	0.5	102	0.5	88	0.5	48	0.5	43	0.5	43	0.5	53	0.5	98	
				-40°C to 125°C	0.5	129	0.5	102	0.5	88	0.5	48	0.5	43	0.5	43	0.5	53	0.5	98	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	ns
				-40°C to 125°C	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	0.5	196	
		$\overline{OE}$	B	-40°C to 85°C	0.5	212	0.5	131	0.5	94	0.5	54	0.5	42	0.5	43	0.5	60	0.5	128	
				-40°C to 125°C	0.5	212	0.5	136	0.5	102	0.5	59	0.5	43	0.5	43	0.5	60	0.5	128	

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6.7 Switching Characteristics, V_{CCA} = 0.8 ± 0.04 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	149	0.5	94	0.5	63	0.5	34	0.5	28	0.5	27	0.5	28	0.5	34	ns
				-40°C to 125°C	0.5	149	0.5	94	0.5	63	0.5	34	0.5	28	0.5	27	0.5	28	0.5	34	
		B	A	-40°C to 85°C	0.5	115	0.5	94	0.5	76	0.5	50	0.5	41	0.5	40	0.5	39	0.5	38	
				-40°C to 125°C	0.5	115	0.5	94	0.5	76	0.5	50	0.5	41	0.5	40	0.5	39	0.5	38	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	ns
				-40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	0.5	91	
		$\overline{OE}$	B	-40°C to 85°C	0.5	121	0.5	94	0.5	79	0.5	38	0.5	32	0.5	31	0.5	30	0.5	35	
				-40°C to 125°C	0.5	121	0.5	94	0.5	79	0.5	38	0.5	32	0.5	31	0.5	30	0.5	35	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	ns
				-40°C to 125°C	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	0.5	109	
		$\overline{OE}$	B	-40°C to 85°C	0.5	198	0.5	121	0.5	84	0.5	46	0.5	33	0.5	28	0.5	28	0.5	35	
				-40°C to 125°C	0.5	198	0.5	128	0.5	95	0.5	52	0.5	35	0.5	30	0.5	28	0.5	35	

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6.8 Switching Characteristics, V_{CCA} = 0.9 ± 0.045 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	122	0.5	76	0.5	51	0.5	23	0.5	18	0.5	16	0.5	15	0.5	17	ns
				-40°C to 125°C	0.5	122	0.5	76	0.5	51	0.5	23	0.5	18	0.5	16	0.5	15	0.5	17	
		B	A	-40°C to 85°C	0.5	84	0.5	63	0.5	51	0.5	39	0.5	28	0.5	24	0.5	21	0.5	21	
				-40°C to 125°C	0.5	84	0.5	63	0.5	51	0.5	39	0.5	28	0.5	24	0.5	21	0.5	21	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	ns
				-40°C to 125°C	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	0.5	70	
		$\overline{OE}$	B	-40°C to 85°C	0.5	116	0.5	89	0.5	74	0.5	33	0.5	26	0.5	25	0.5	22	0.5	25	
				-40°C to 125°C	0.5	116	0.5	89	0.5	75	0.5	33	0.5	27	0.5	25	0.5	23	0.5	26	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	ns
				-40°C to 125°C	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	0.5	65	
		$\overline{OE}$	B	-40°C to 85°C	0.5	184	0.5	115	0.5	78	0.5	42	0.5	29	0.5	25	0.5	20	0.5	21	
				-40°C to 125°C	0.5	184	0.5	123	0.5	91	0.5	48	0.5	32	0.5	26	0.5	21	0.5	22	

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6.9 Switching Characteristics, V_{CCA} = 1.2 ± 0.1 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	84	0.5	50	0.5	39	0.5	15	0.5	10	0.5	9	0.5	7	0.5	8	ns
				-40°C to 125°C	0.5	84	0.5	50	0.5	39	0.5	15	0.5	11	0.5	9	0.5	8	0.5	8	
		B	A	-40°C to 85°C	0.5	50	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7	
				-40°C to 125°C	0.5	50	0.5	33	0.5	23	0.5	15	0.5	12	0.5	10	0.5	8	0.5	7	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	0.5	25	ns
				-40°C to 125°C	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	0.5	26	
		$\overline{OE}$	B	-40°C to 85°C	0.5	110	0.5	83	0.5	69	0.5	27	0.5	20	0.5	18	0.5	15	0.5	15	
				-40°C to 125°C	0.5	110	0.5	84	0.5	70	0.5	28	0.5	22	0.5	20	0.5	16	0.5	16	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	0.5	29	ns
				-40°C to 125°C	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	0.5	30	
		$\overline{OE}$	B	-40°C to 85°C	0.5	154	0.5	102	0.5	70	0.5	37	0.5	25	0.5	20	0.5	15	0.5	13	
				-40°C to 125°C	0.5	165	0.5	112	0.5	83	0.5	43	0.5	28	0.5	22	0.5	17	0.5	15	

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6.10 Switching Characteristics, V_{CCA} = 1.5 ± 0.1 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	79	0.5	41	0.5	28	0.5	12	0.5	9	0.5	7	0.5	6	0.5	6	ns
				-40°C to 125°C	0.5	79	0.5	41	0.5	28	0.5	12	0.5	9	0.5	8	0.5	6	0.5	6	
		B	A	-40°C to 85°C	0.5	50	0.5	28	0.5	18	0.5	10	0.5	9	0.5	8	0.5	6	0.5	5	
				-40°C to 125°C	0.5	50	0.5	28	0.5	18	0.5	11	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	0.5	17	ns
				-40°C to 125°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	
		$\overline{OE}$	B	-40°C to 85°C	0.5	108	0.5	82	0.5	67	0.5	25	0.5	18	0.5	16	0.5	13	0.5	13	
				-40°C to 125°C	0.5	108	0.5	82	0.5	68	0.5	26	0.5	20	0.5	18	0.5	14	0.5	14	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	0.5	18	ns
				-40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	0.5	19	
		$\overline{OE}$	B	-40°C to 85°C	0.5	148	0.5	92	0.5	65	0.5	34	0.5	22	0.5	18	0.5	13	0.5	11	
				-40°C to 125°C	0.5	157	0.5	106	0.5	78	0.5	40	0.5	25	0.5	20	0.5	15	0.5	13	

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6.11 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	78	0.5	40	0.5	24	0.5	10	0.5	8	0.5	7	0.5	6	0.5	5	ns
				-40°C to 125°C	0.5	78	0.5	40	0.5	24	0.5	10	0.5	8	0.5	7	0.5	6	0.5	5	
		B	A	-40°C to 85°C	0.5	56	0.5	27	0.5	16	0.5	9	0.5	7	0.5	7	0.5	5	0.5	4	
				-40°C to 125°C	0.5	56	0.5	27	0.5	16	0.5	9	0.5	8	0.5	7	0.5	6	0.5	5	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	ns
				-40°C to 125°C	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	0.5	16	
		$\overline{OE}$	B	-40°C to 85°C	0.5	108	0.5	81	0.5	67	0.5	24	0.5	18	0.5	16	0.5	12	0.5	12	
				-40°C to 125°C	0.5	108	0.5	82	0.5	67	0.5	26	0.5	19	0.5	17	0.5	13	0.5	13	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	0.5	14	ns
				-40°C to 125°C	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	0.5	15	
		$\overline{OE}$	B	-40°C to 85°C	0.5	147	0.5	88	0.5	62	0.5	32	0.5	21	0.5	17	0.5	13	0.5	11	
				-40°C to 125°C	0.5	155	0.5	103	0.5	74	0.5	38	0.5	24	0.5	19	0.5	14	0.5	12	

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6.12 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	77	0.5	39	0.5	22	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	ns
				-40°C to 125°C	0.5	77	0.5	39	0.5	22	0.5	8	0.5	6	0.5	5	0.5	5	0.5	5	
		B	A	-40°C to 85°C	0.5	71	0.5	28	0.5	15	0.5	7	0.5	6	0.5	5	0.5	5	0.5	4	
				-40°C to 125°C	0.5	71	0.5	28	0.5	15	0.5	8	0.5	6	0.5	6	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	ns
				-40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	0.5	12	
		$\overline{OE}$	B	-40°C to 85°C	0.5	108	0.5	81	0.5	66	0.5	24	0.5	17	0.5	15	0.5	11	0.5	11	
				-40°C to 125°C	0.5	108	0.5	81	0.5	67	0.5	25	0.5	18	0.5	16	0.5	12	0.5	12	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$	B	-40°C to 85°C	0.5	146	0.5	86	0.5	59	0.5	29	0.5	19	0.5	15	0.5	12	0.5	10	
				-40°C to 125°C	0.5	153	0.5	101	0.5	72	0.5	35	0.5	21	0.5	17	0.5	13	0.5	11	

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6.13 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

See Figure 1 and Table 1 for test circuit and loading. See Figure 2, Figure 3, and Figure 4 for measurement waveforms.

PARAMETER		FROM	TO	Test Conditions	B-Port Supply Voltage (V_{CCB})														UNIT
					0.7 ± 0.05 V		0.8 ± 0.04 V		0.9 ± 0.045 V		1.2 ± 0.1 V		1.5 ± 0.1 V		1.8 ± 0.15 V		2.5 ± 0.2 V		3.3 ± 0.3 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	A	B	-40°C to 85°C	0.5	76	0.5	38	0.5	21	0.5	7	0.5	5	0.5	4	0.5	4	0.5	4	ns
				-40°C to 125°C	0.5	76	0.5	38	0.5	21	0.5	8	0.5	5	0.5	5	0.5	4	0.5	4	
		B	A	-40°C to 85°C	0.5	106	0.5	34	0.5	17	0.5	8	0.5	6	0.5	5	0.5	4	0.5	4	
				-40°C to 125°C	0.5	106	0.5	34	0.5	17	0.5	8	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	$\overline{OE}$	A	-40°C to 85°C	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	ns
				-40°C to 125°C	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	0.5	11	
		$\overline{OE}$	B	-40°C to 85°C	0.5	108	0.5	81	0.5	66	0.5	24	0.5	17	0.5	15	0.5	11	0.5	11	
				-40°C to 125°C	0.5	108	0.5	81	0.5	67	0.5	25	0.5	18	0.5	16	0.5	12	0.5	11	
t_{en}	Enable time	$\overline{OE}$	A	-40°C to 85°C	0.5	8	0.5	8	0.5	8	0.5	8	0.5	8	0.5	8	0.5	8	0.5	8	ns
				-40°C to 125°C	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	0.5	9	
		$\overline{OE}$	B	-40°C to 85°C	0.5	146	0.5	85	0.5	58	0.5	28	0.5	18	0.5	14	0.5	11	0.5	9	
				-40°C to 125°C	0.5	153	0.5	101	0.5	72	0.5	34	0.5	21	0.5	16	0.5	12	0.5	10	

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6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.1		pF
			0.8 V	0.8 V		2.0		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.1		
			1.8 V	1.8 V		2.1		
			2.5 V	2.5 V		2.5		
			3.3 V	3.3 V		3.1		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.6		pF
			0.8 V	0.8 V		1.6		
			0.9 V	0.9 V		1.6		
			1.2 V	1.2 V		1.6		
			1.5 V	1.5 V		1.6		
			1.8 V	1.8 V		1.7		
			2.5 V	2.5 V		2.1		
			3.3 V	3.3 V		2.6		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		10.5		pF
			0.8 V	0.8 V		10.6		
			0.9 V	0.9 V		10.6		
			1.2 V	1.2 V		10.8		
			1.5 V	1.5 V		11.2		
			1.8 V	1.8 V		12.5		
			2.5 V	2.5 V		16.3		
			3.3 V	3.3 V		20.0		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.0		pF
			0.8 V	0.8 V		0.9		
			0.9 V	0.9 V		0.9		
			1.2 V	1.2 V		0.9		
			1.5 V	1.5 V		0.9		
			1.8 V	1.8 V		0.9		
			2.5 V	2.5 V		0.9		
			3.3 V	3.3 V		0.9		

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Operating Characteristics: T_A = 25°C (continued)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		10.9		pF
			0.8 V	0.8 V		10.9		
			0.9 V	0.9 V		10.9		
			1.2 V	1.2 V		11.1		
			1.5 V	1.5 V		11.4		
			1.8 V	1.8 V		12.6		
			2.5 V	2.5 V		16.3		
			3.3 V	3.3 V		20.0		
	Power Dissipation Capacitance per transceiver (A to B: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.3		pF
			0.8 V	0.8 V		1.2		
			0.9 V	0.9 V		1.2		
			1.2 V	1.2 V		1.1		
			1.5 V	1.5 V		1.1		
			1.8 V	1.8 V		1.1		
			2.5 V	2.5 V		1.1		
			3.3 V	3.3 V		1.2		
	Power Dissipation Capacitance per transceiver (B to A: outputs enabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		2.1		pF
			0.8 V	0.8 V		2.1		
			0.9 V	0.9 V		2.0		
			1.2 V	1.2 V		2.0		
			1.5 V	1.5 V		2.1		
			1.8 V	1.8 V		2.2		
			2.5 V	2.5 V		2.5		
			3.3 V	3.3 V		3.1		
	Power Dissipation Capacitance per transceiver (B to A: outputs disabled)	CL = 0, RL = Open f = 1 MHz, tr = tf = 1 ns	0.7 V	0.7 V		1.6		pF
			0.8 V	0.8 V		1.6		
			0.9 V	0.9 V		1.6		
			1.2 V	1.2 V		1.6		
			1.5 V	1.5 V		1.6		
			1.8 V	1.8 V		1.7		
			2.5 V	2.5 V		2.1		
			3.3 V	3.3 V		2.6		

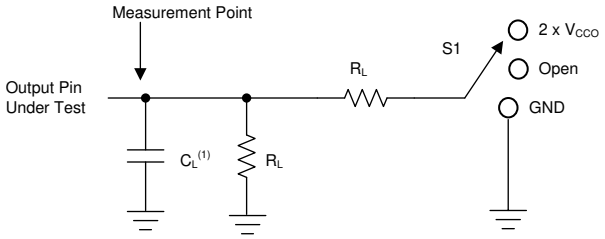
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7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- Z_O = 50 Ω
- dv/dt ≤ 1 ns/V

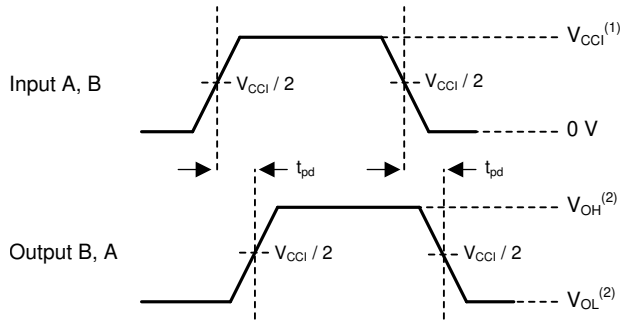


(1) C_L includes probe and jig capacitance.

Figure 1. Load Circuit

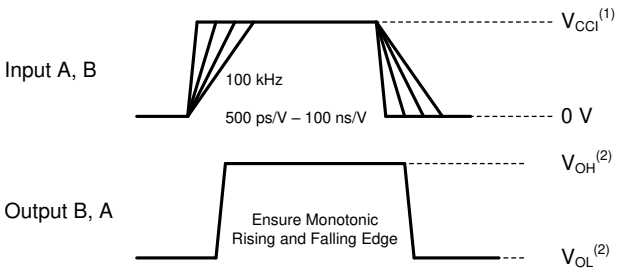
Table 1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv	Input transition rise or fall rate	0.65 V – 3.6 V	1 MΩ	15 pF	Open	N/A
t_{pd}	Propagation (delay) time	1.1 V – 3.6 V	2 kΩ	15 pF	Open	N/A
		0.65 V – 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	2 × V_{CCO}	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	2 × V_{CCO}	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	2 × V_{CCO}	0.1 V
t_{en}, t_{dis}	Enable time, disable time	3 V – 3.6 V	2 kΩ	15 pF	GND	0.3 V
		1.65 V – 2.7 V	2 kΩ	15 pF	GND	0.15 V
		1.1 V – 1.6 V	2 kΩ	15 pF	GND	0.1 V
		0.65 V – 0.95 V	20 kΩ	15 pF	GND	0.1 V



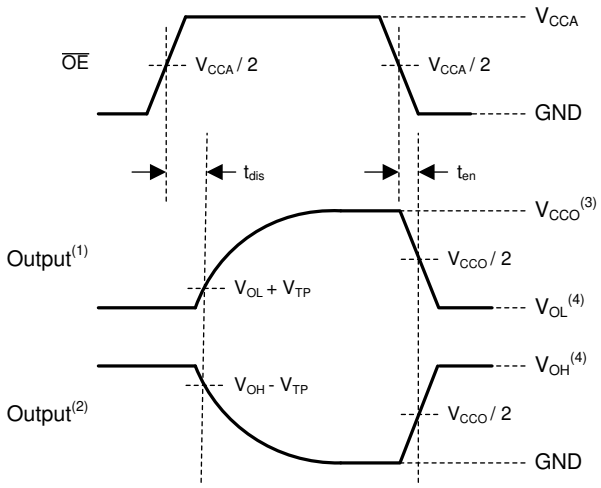
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 3. Input Transition Rise or Fall Rate



(1) Output waveform on the condition that input is driven to a valid Logic Low.

(2) Output waveform on the condition that input is driven to a valid Logic High.

(3) V_{CCO} is the supply pin associated with the output port.

(4) V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

Figure 4. Enable Time And Disable Time

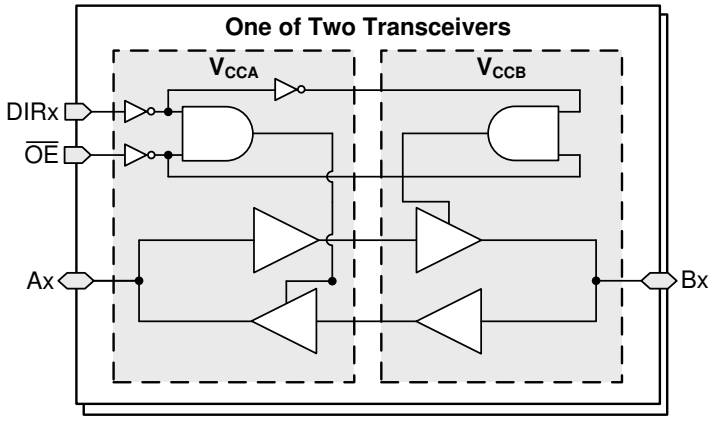
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8 Detailed Description

8.1 Overview

The SN74AXC2T245-Q1 is a 2-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (DIRx and $\overline{OE}$) are reference to V_{CCA} logic levels, and Bx pins are referenced to V_{CCB} logic levels. The A port is able to accept I/O voltages ranging from 0.65 V to 3.6 V, while the B port can accept I/O voltages from 0.65 V to 3.6 V. A high on DIR enables data transmission from A to B and a low on DIR enables data transmission from B to A. See *Device Functional Modes* for a summary of the operation of the control logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

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Feature Description (continued)

8.3.6 Glitch-free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

8.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 5.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

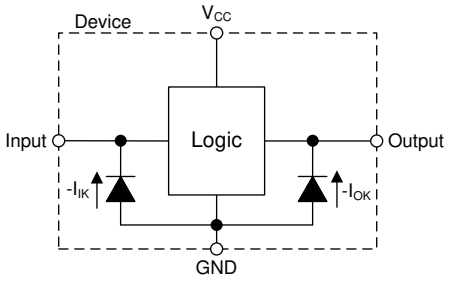


Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.8 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

8.3.9 Supports High-Speed Translation

The SN74AXC2T245-Q1 device can support high data-rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.4 Device Functional Modes

Table 2. Function Table (Each Transceiver)(1)(2)

CONTROL INPUTS		Port Status		OPERATION
$\overline{OE}$	DIRx	A PORT	B PORT	
L	L	Output (Enabled)	Input (Hi-Z)	B data to A bus
L	H	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	X	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AXC2T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC2T245-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380 Mbps when device translates a signal from 1.8 V to 3.3 V.

One example application is shown in Figure 6, where the SN74AXC2T245-Q1 device is used to translate low voltage UART signals from a CPU to a higher voltage signal to properly drive the inputs of a bluetooth module.

9.2 Typical Application

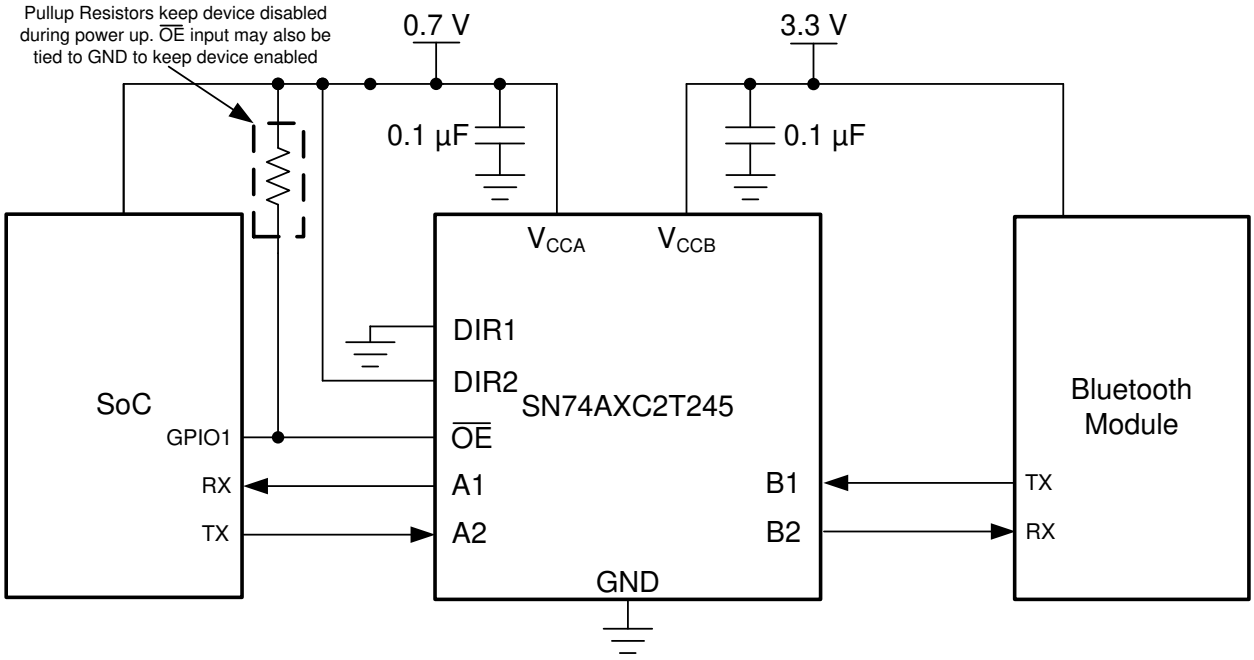


Figure 6. 2-Pin UART Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in *Table 3*.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC2T245-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device being driven by the SN74AXC2T245-Q1 determine the output voltage range of the SN74AXC2T245-Q1.

9.2.3 Application Curve

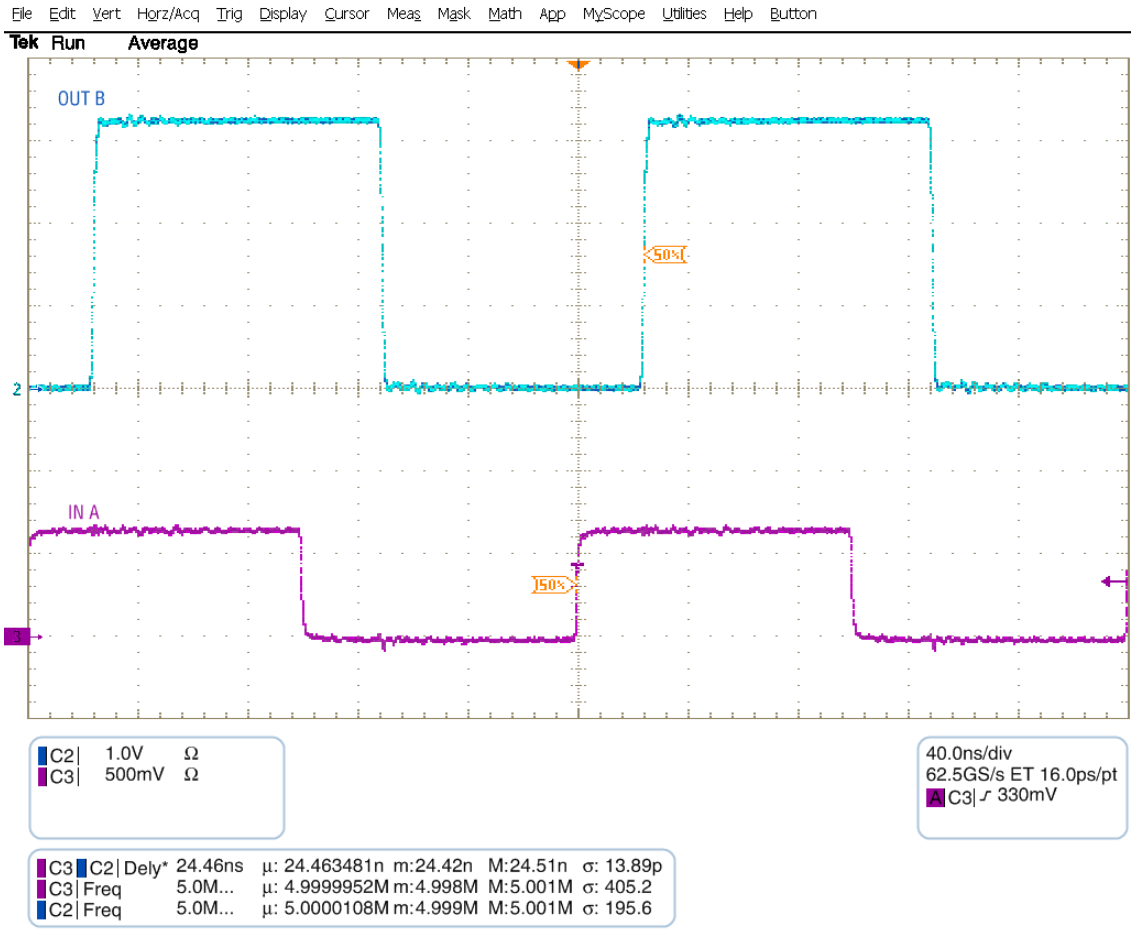


Figure 7. Up Translation at 2.5 MHz (0.7 V to 3.3 V)

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10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch-free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device is designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power-up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

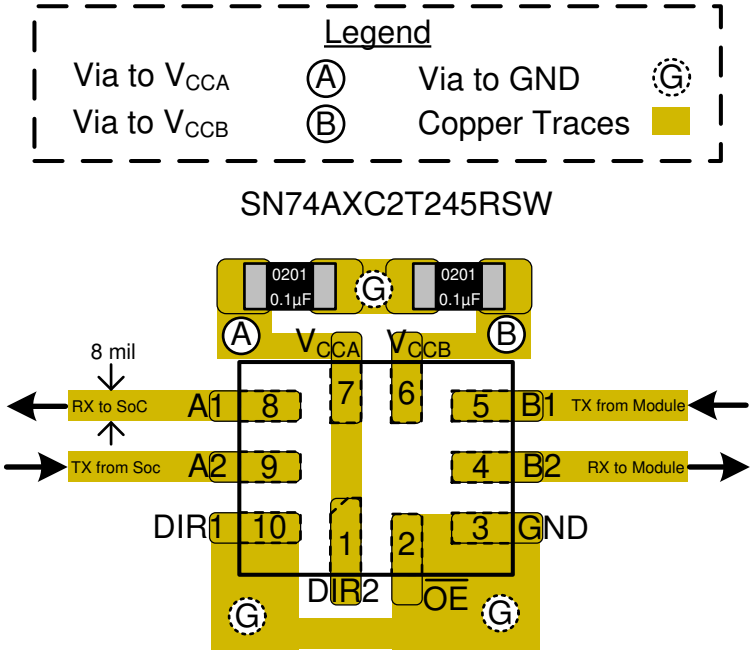
11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1 µF capacitor is recommended, but transient performance can be improved by having both 1 µF and 0.1 µF capacitors in parallel as bypass capacitors.
- Use short trace lengths to avoid excessive loading.

11.2 Layout Example



12 Device and Documentation Support

12.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

Texas Instruments, *Power Sequencing for AXC Family of Devices* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CAXC2T245QRSWRQ1	Active	Production	UQFN (RSW) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HM
CAXC2T245QRSWRQ1.A	Active	Production	UQFN (RSW) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AXC2T245-Q1 :

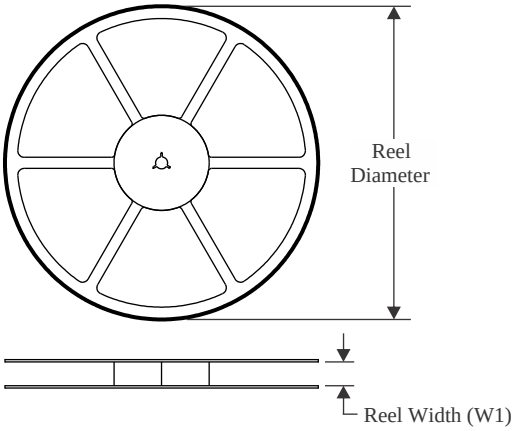
- Catalog : SN74AXC2T245

NOTE: Qualified Version Definitions:

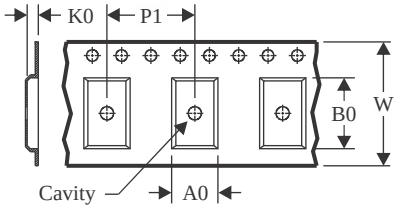
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

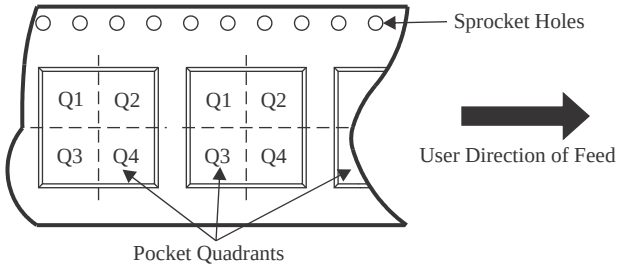


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

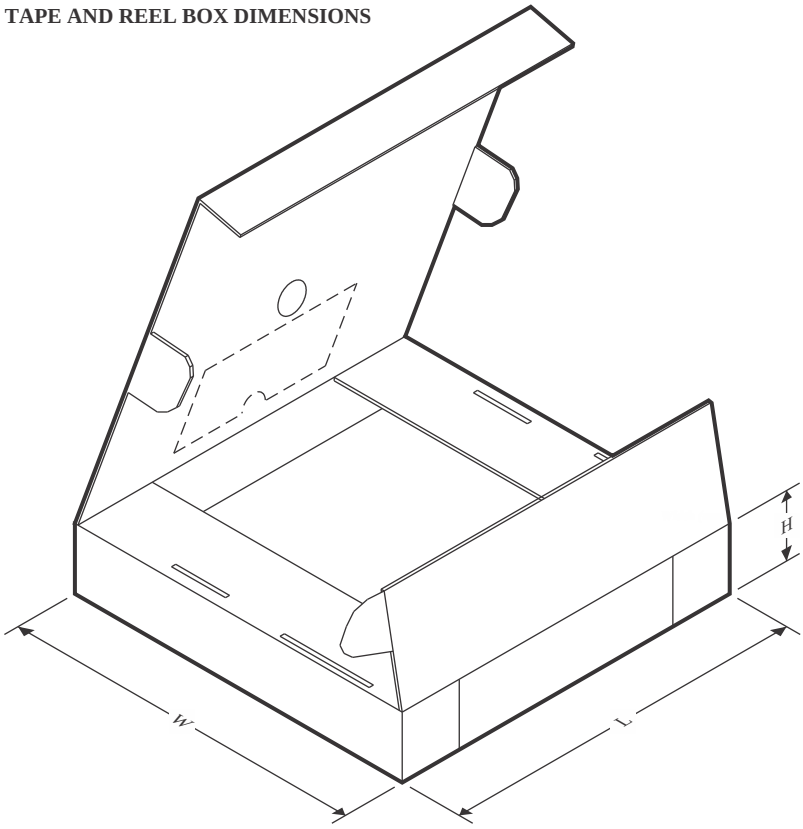
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAXC2T245QRSWRQ1	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

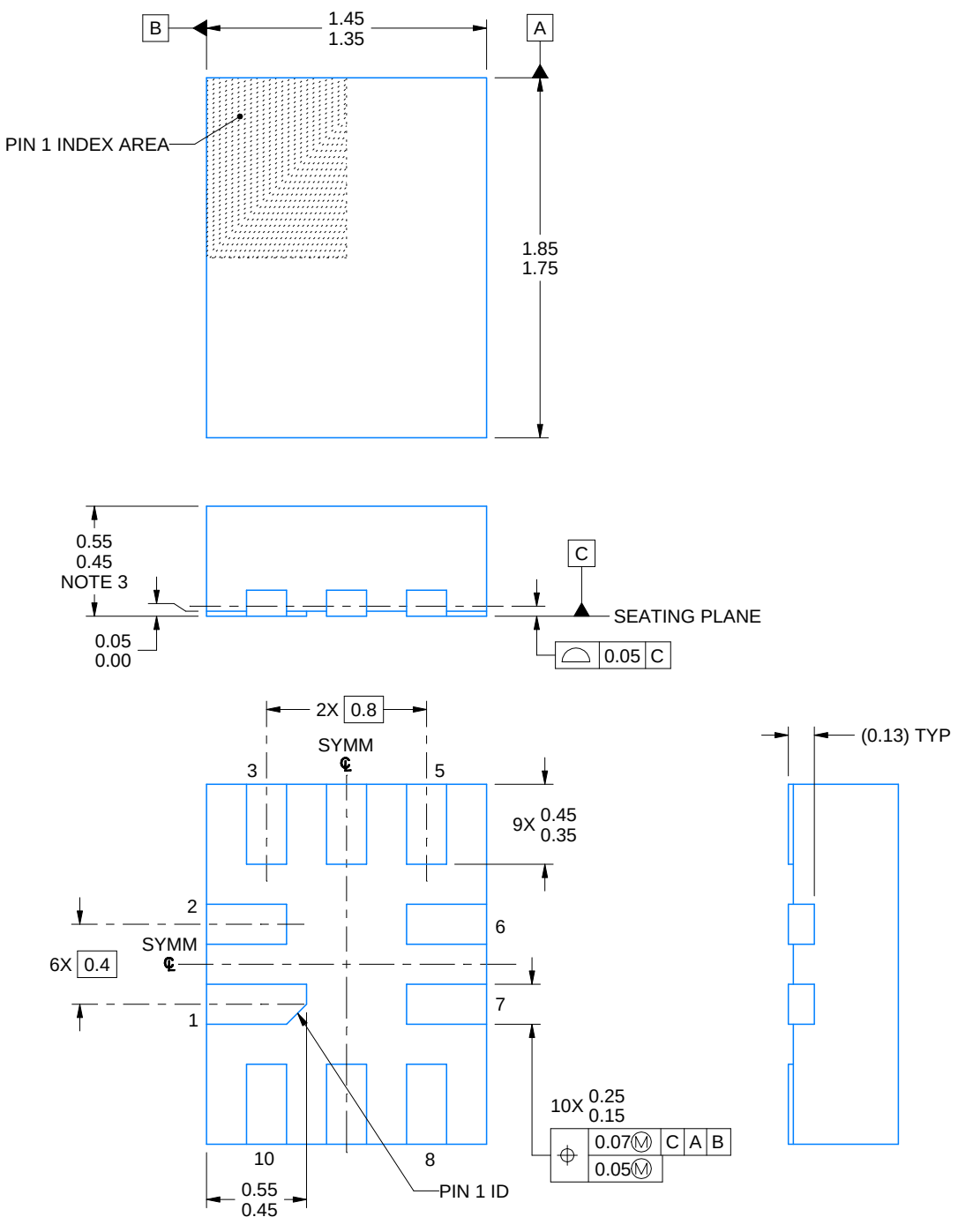
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAXC2T245QRSWRQ1	UQFN	RSW	10	3000	189.0	185.0	36.0

PACKAGE OUTLINE

RSW0010A

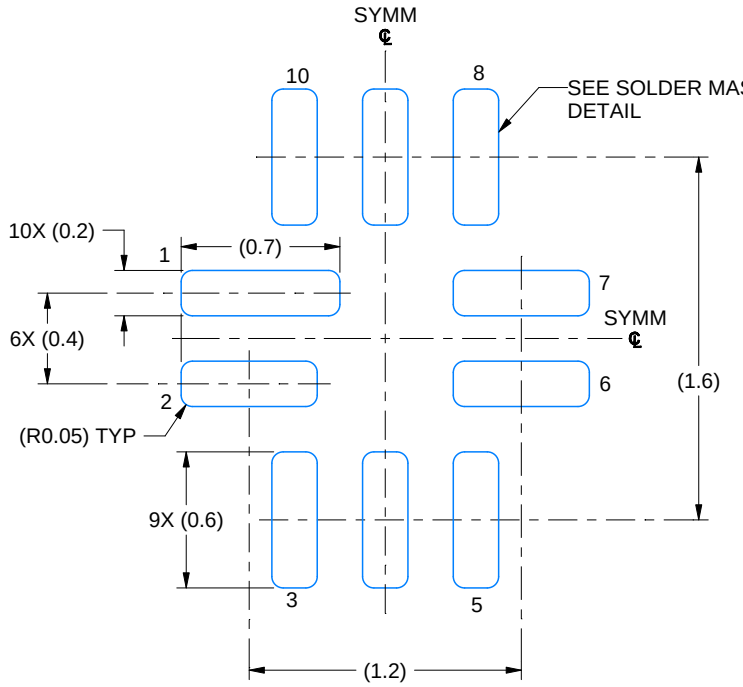
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

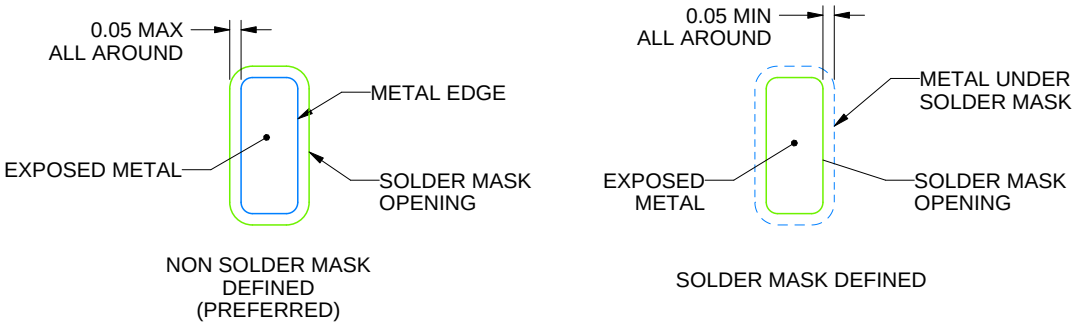


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

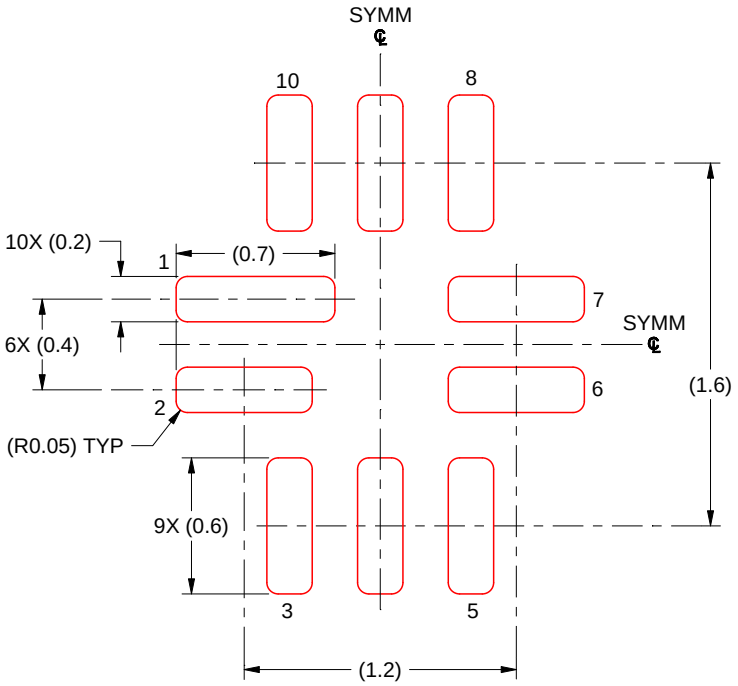


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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