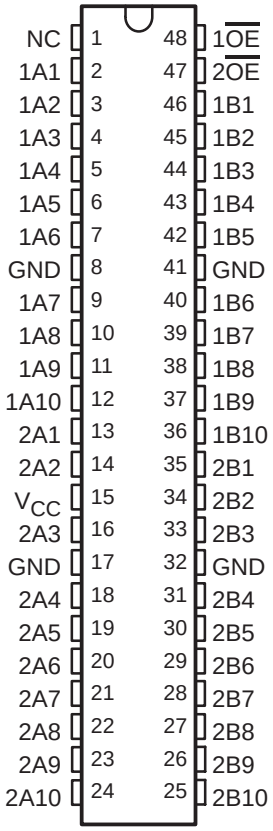
- **Member of the Texas Instruments Widebus™ Family**
- **Undershoot Protection for Off-Isolation on A and B Ports Up To −2 V**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 3 Ω Typical)**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 5.5 pF Typical)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **V_{CC} Operating Range From 4 V to 5.5 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP − DL	Tube	SN74CBT16210CDL	CBT16210C
		Tape and reel	SN74CBT16210CDLR	
	TSSOP − DGG	Tube	SN74CBT16210CDGG	CBT16210C
		Tape and reel	SN74CBT16210CDGGR	
	TVSOP − DGV	Tape and reel	SN74CBT16210CDGVR	CY210C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The SN74CBT16210C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16210C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16210C is organized as two 10-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When $\overline{OE}$ is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 10-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

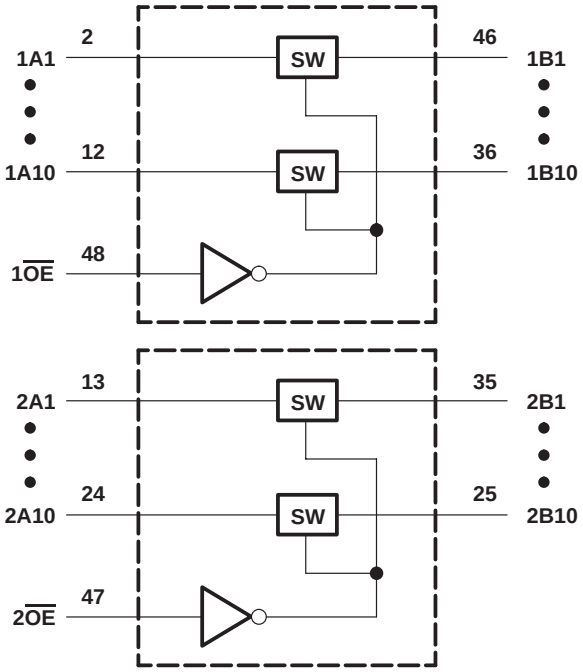
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

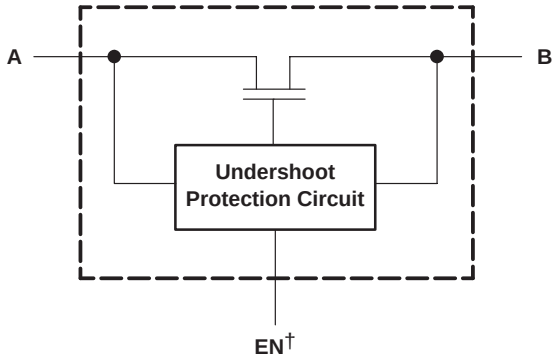
FUNCTION TABLE
(each 10-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
DL package . . . . . 63°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	V_{CC} = 4.5 V,	I_{IN} = −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC} = 5 V,	0 mA > I_I ≥ −50 mA, V_{IN} = V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC} = 5.5 V,	V_{IN} = V_{CC} or GND				±1	μA
I_{OZ}‡		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±10	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			10	μA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0, V_{IN} = V_{CC} or GND,	Switch ON or OFF			3	μA
ΔI_{CC}§	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN} = 3 V or 0				4.5		pF
$C_{io(OFF)}$		$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		5.5		pF
$C_{io(ON)}$		$V_{I/O}$ = 3 V or 0,	Switch ON,	V_{IN} = V_{CC} or GND		14.5		pF
r_{on}¶		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_O = −15 mA		8	12	Ω
		V_{CC} = 4.5 V	V_I = 0	I_O = 64 mA		3	6	Ω
				I_O = 30 mA		3	6	Ω
			V_I = 2.4 V,	I_O = −15 mA		5	10	Ω

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}#	A or B	B or A		0.24		0.15	ns
t_{en}	$\overline{OE}$	A or B		6.5	1.5	6	ns
t_{dis}	$\overline{OE}$	A or B		6.5	1.5	6	ns

The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	V_{IN} = V_{CC} or GND	2	V_{OH}–0.3		V

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

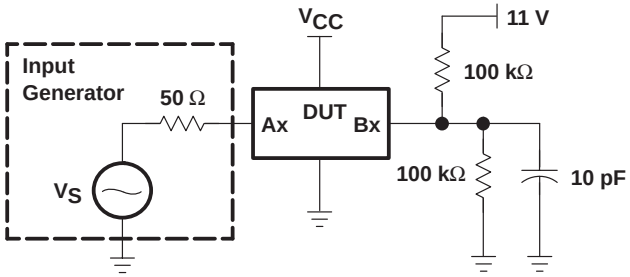


Figure 1. Device Test Setup

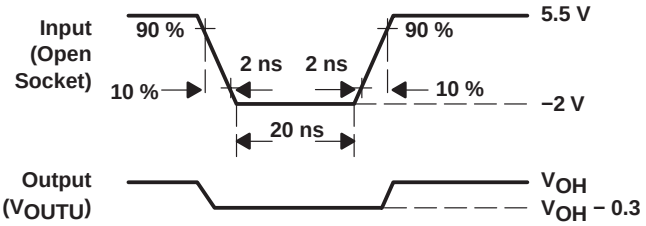
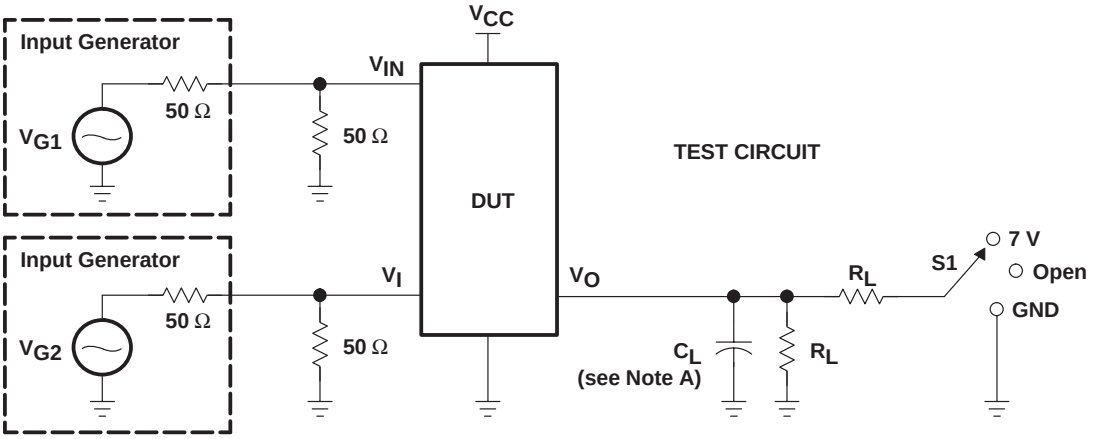
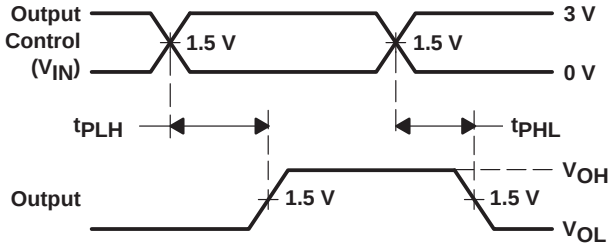


Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

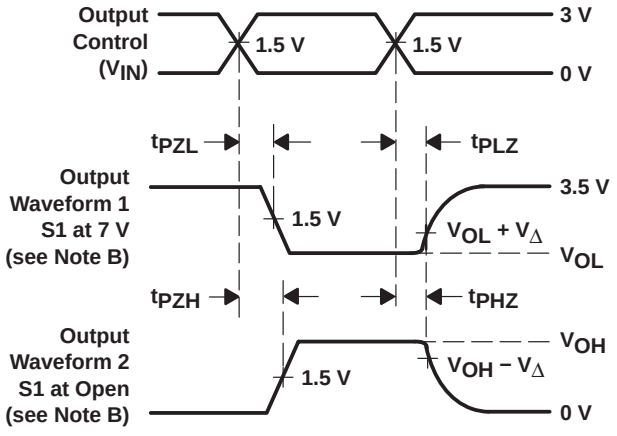
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT16210CDGGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16210C
SN74CBT16210CDGGR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16210C
SN74CBT16210CDGVR	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY210C
SN74CBT16210CDGVR.B	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY210C
SN74CBT16210CDLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16210C
SN74CBT16210CDLR.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16210C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

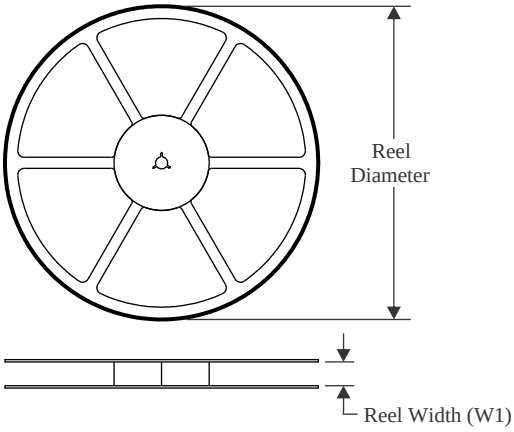
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

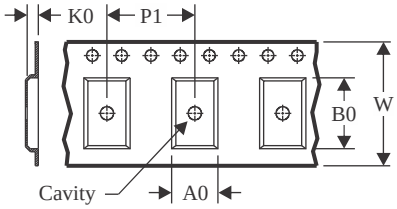
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

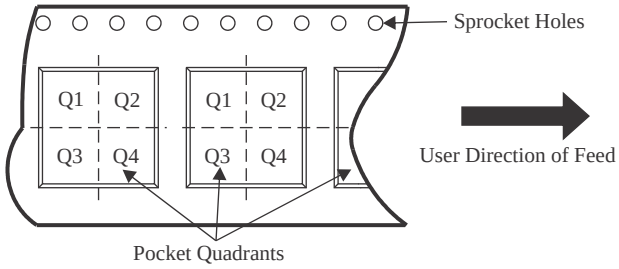


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

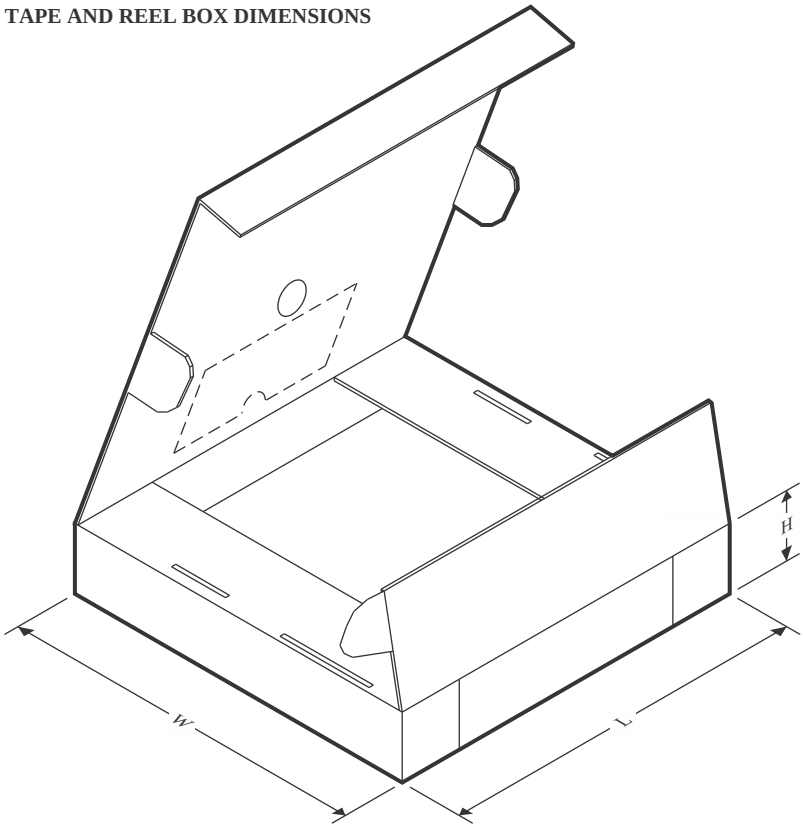
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16210CDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74CBT16210CDGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CBT16210CDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

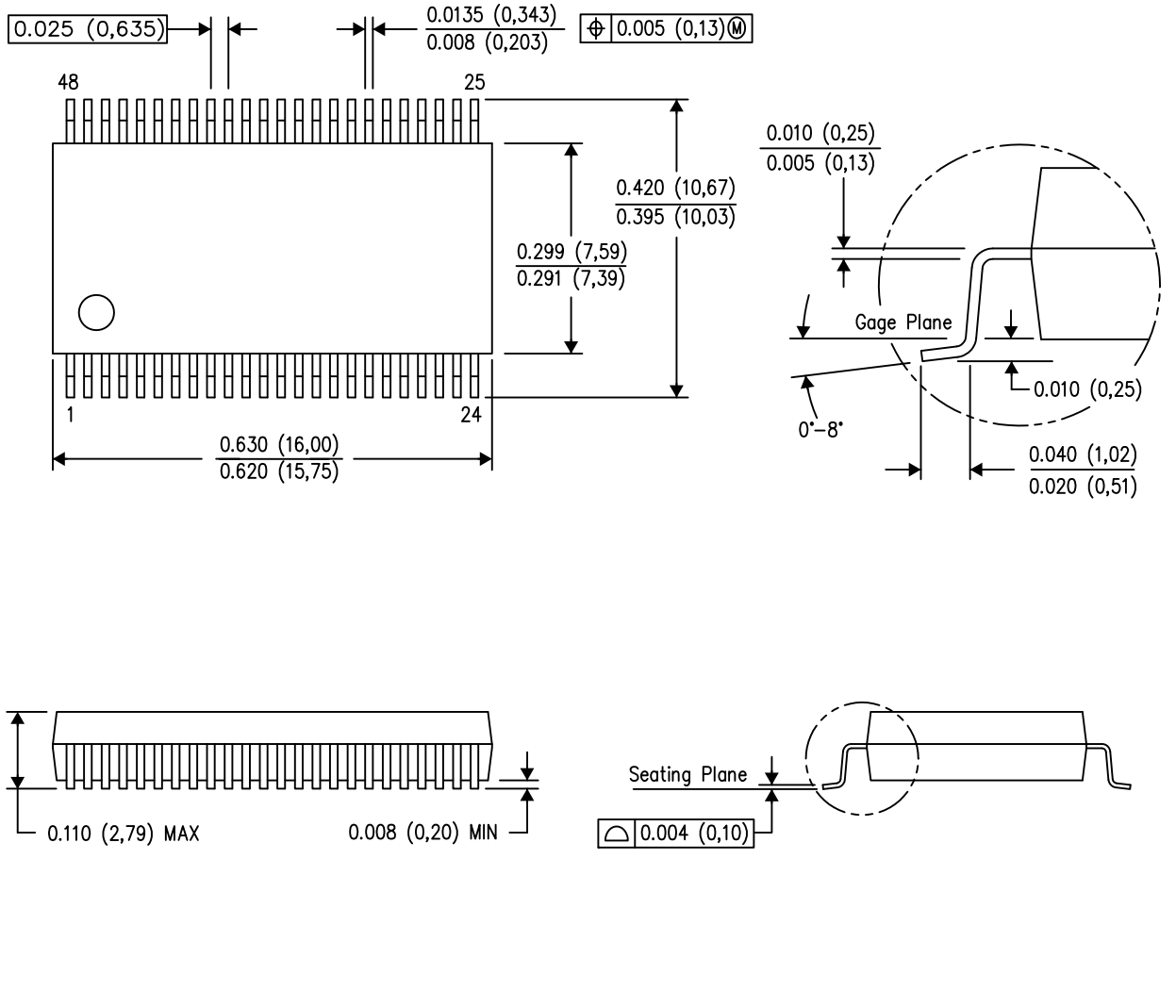
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16210CDGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74CBT16210CDGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74CBT16210CDLR	SSOP	DL	48	1000	356.0	356.0	53.0

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE

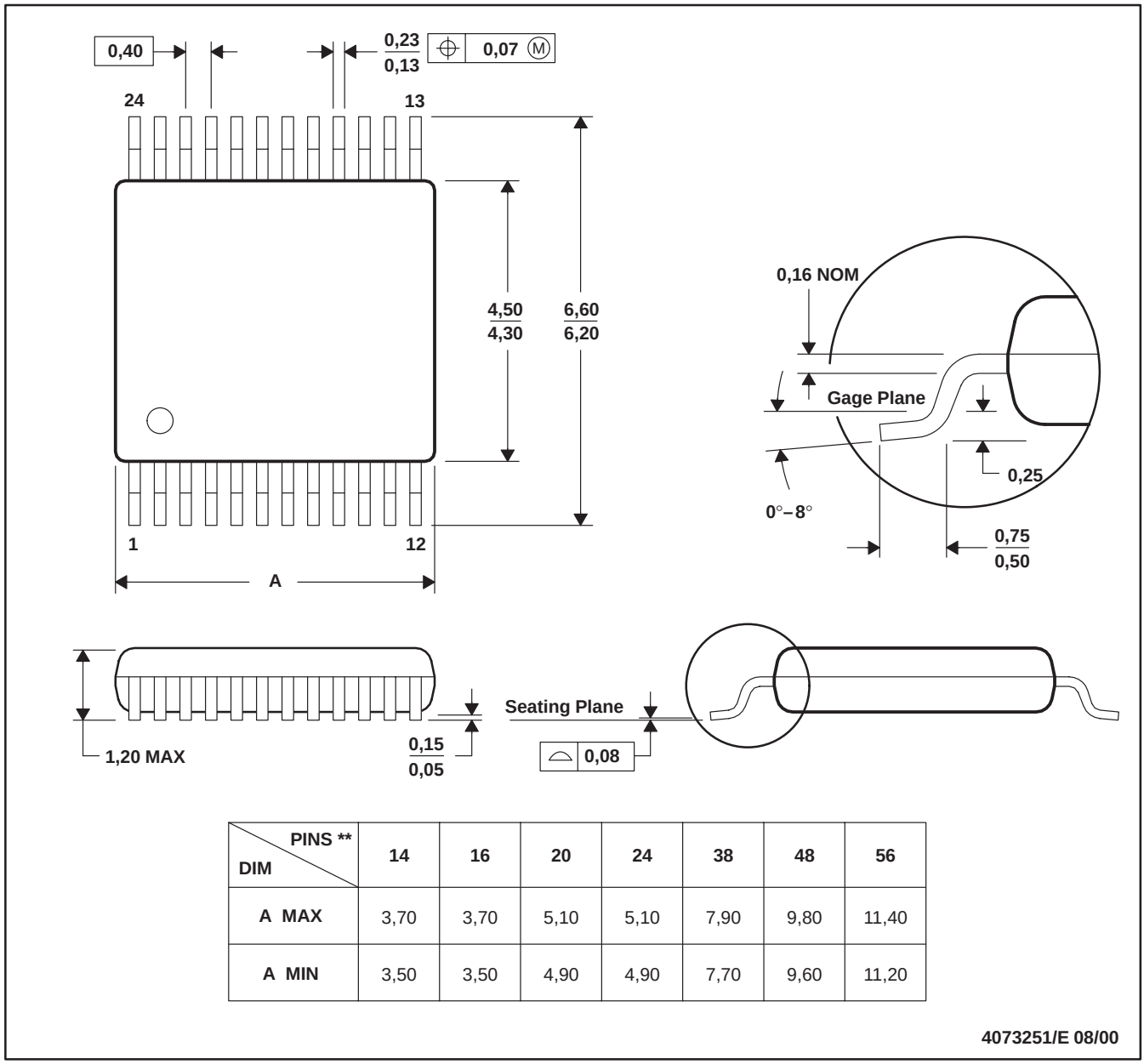


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

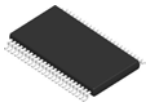
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

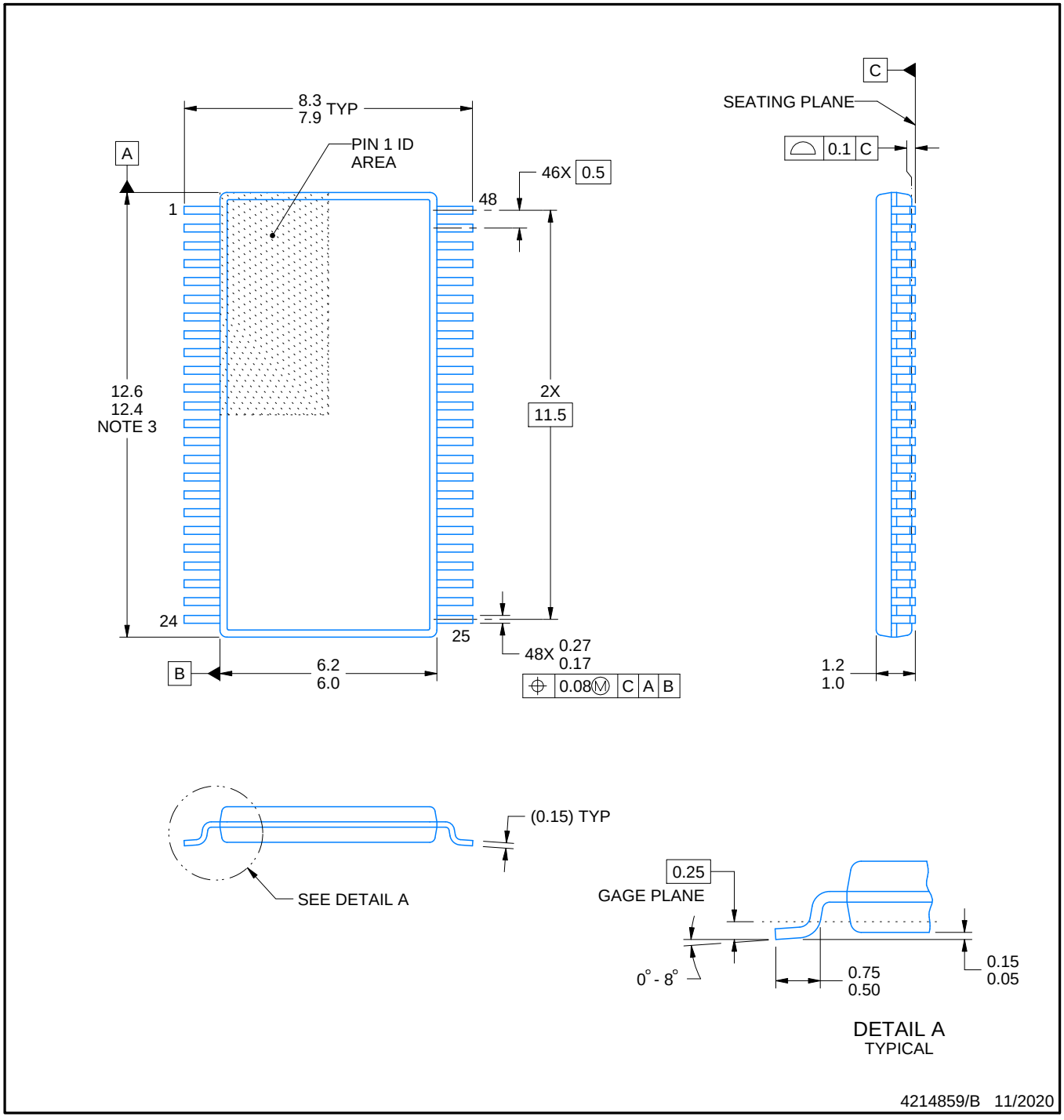


PACKAGE OUTLINE

DGG0048A

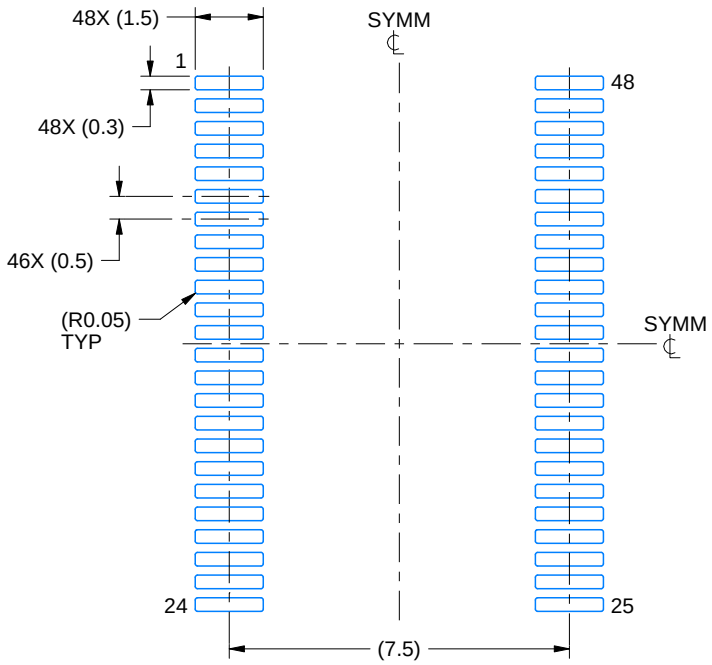
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

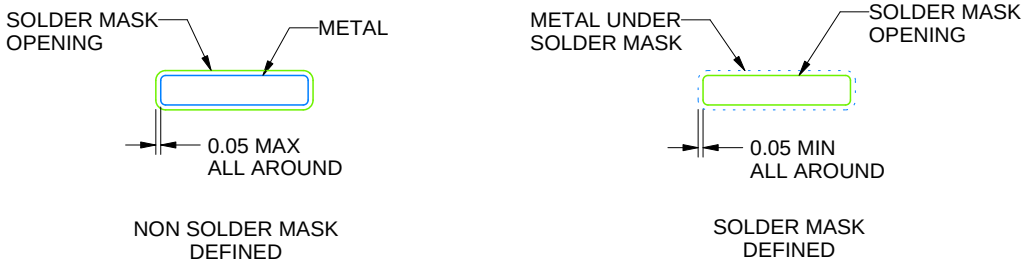


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

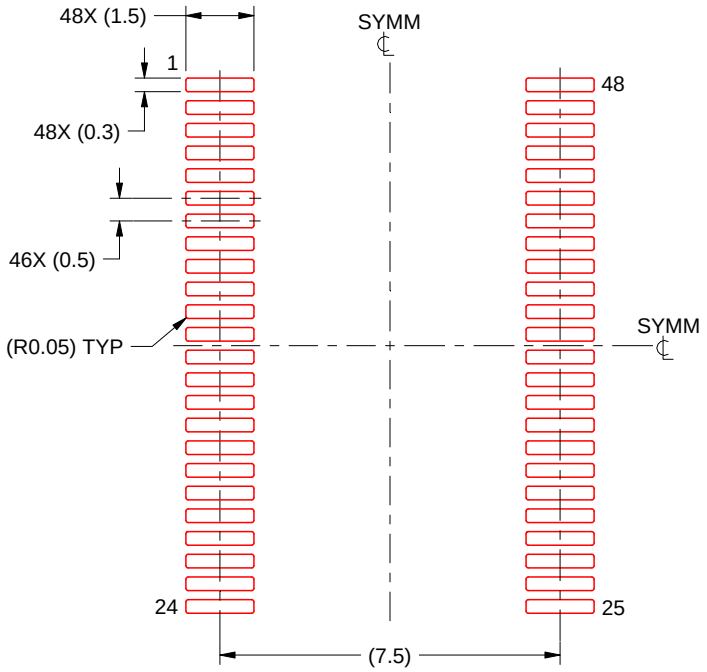


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

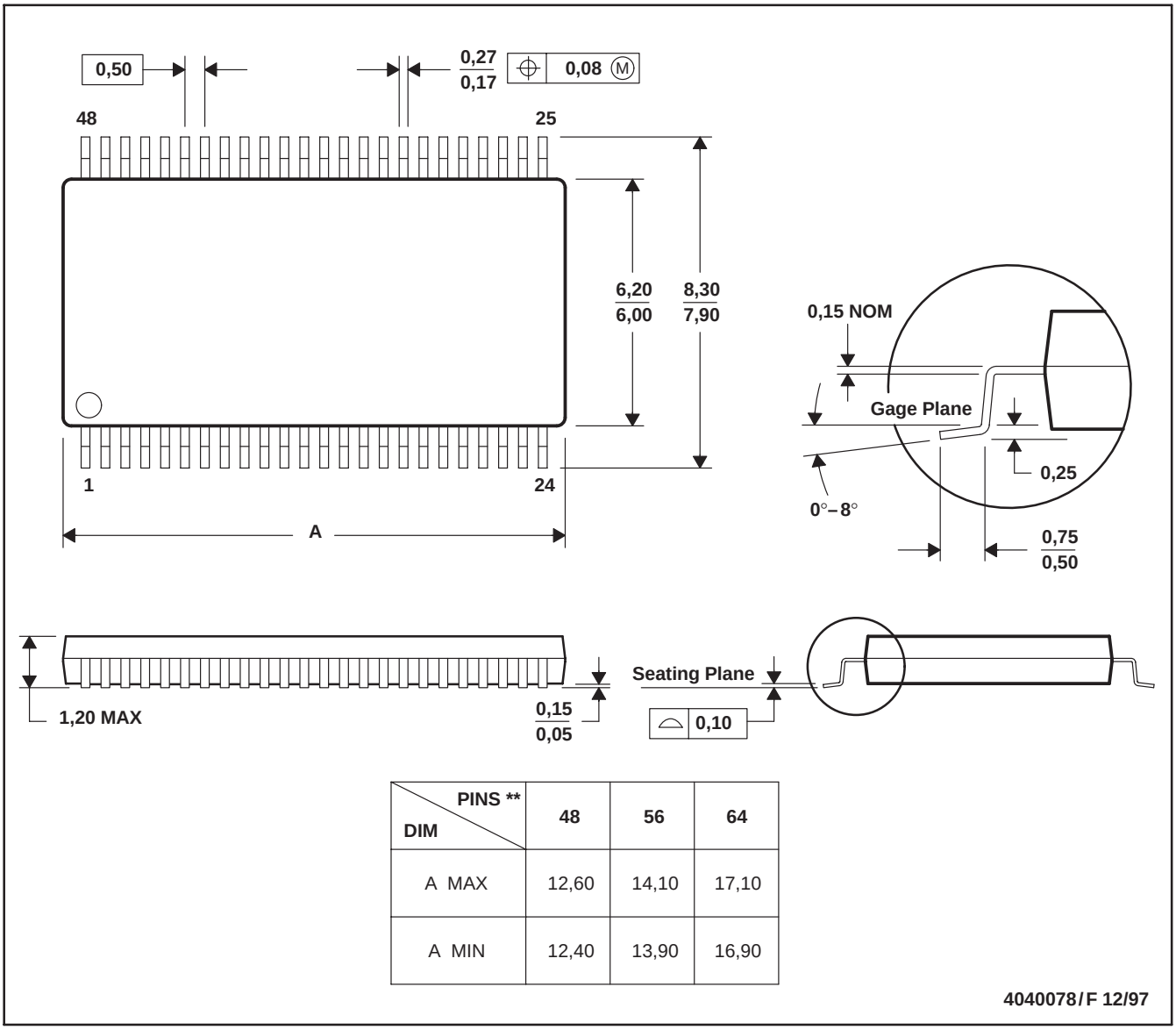
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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