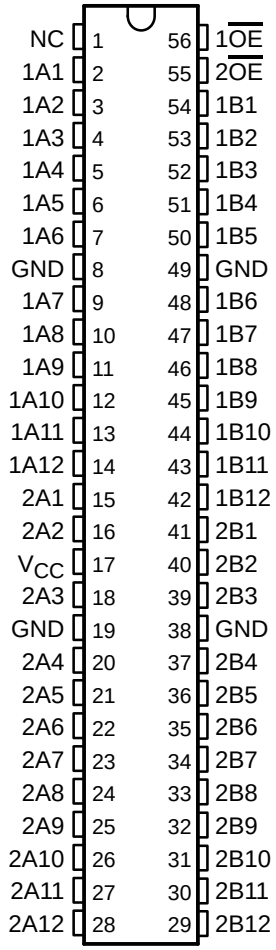
- **Member of Texas Instruments Widebus™ Family**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The SN74CBTD16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated in the circuit to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as a dual 12-bit bus switch with separate output-enable ($\overline{OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When $\overline{OE}$ is low, the associated 12-bit bus switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBTD16211DL	CBTD16211
		Tape and reel	SN74CBTD16211DLR	
	TSSOP – DGG	Tape and reel	SN74CBTD16211DGGR	CBTD16211
	TVSOP – DGV	Tape and reel	SN74CBTD16211DGVR	CYD211

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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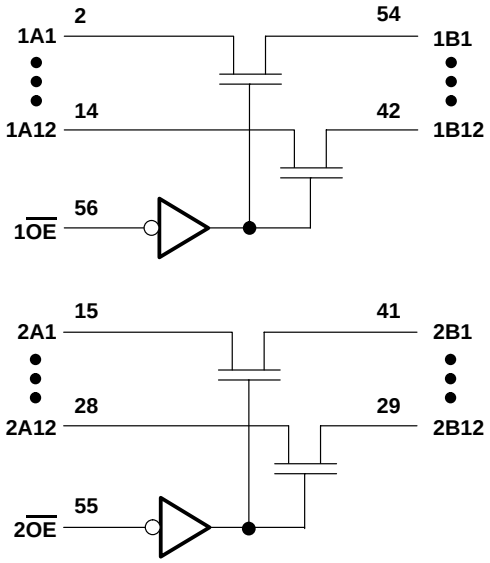
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FUNCTION TABLE
(each 12-bit bus switch)

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package . . . . . 64°C/W
DGV package . . . . . 48°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}		See Figure 2						
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±1	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			1.5	mA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			5.5		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		35	50	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

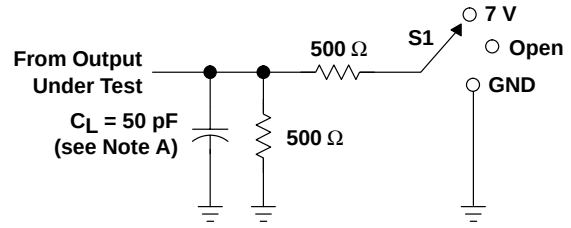
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}¶	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.5	9.8	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8.9	ns

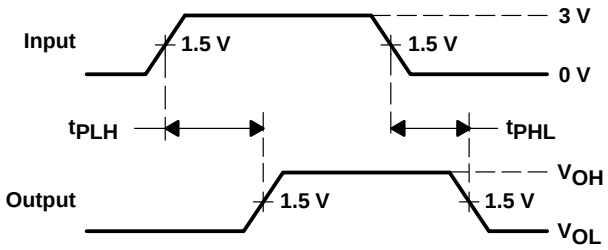
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

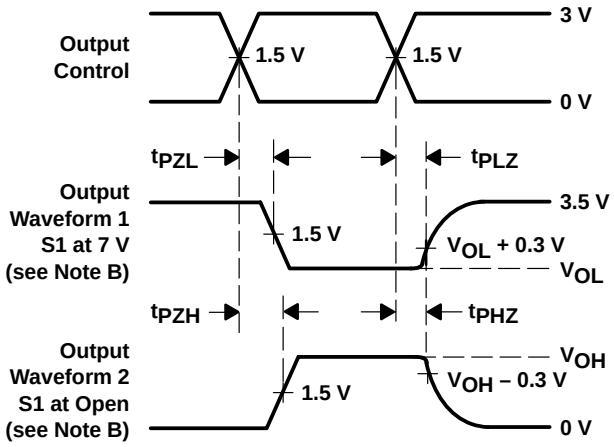


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

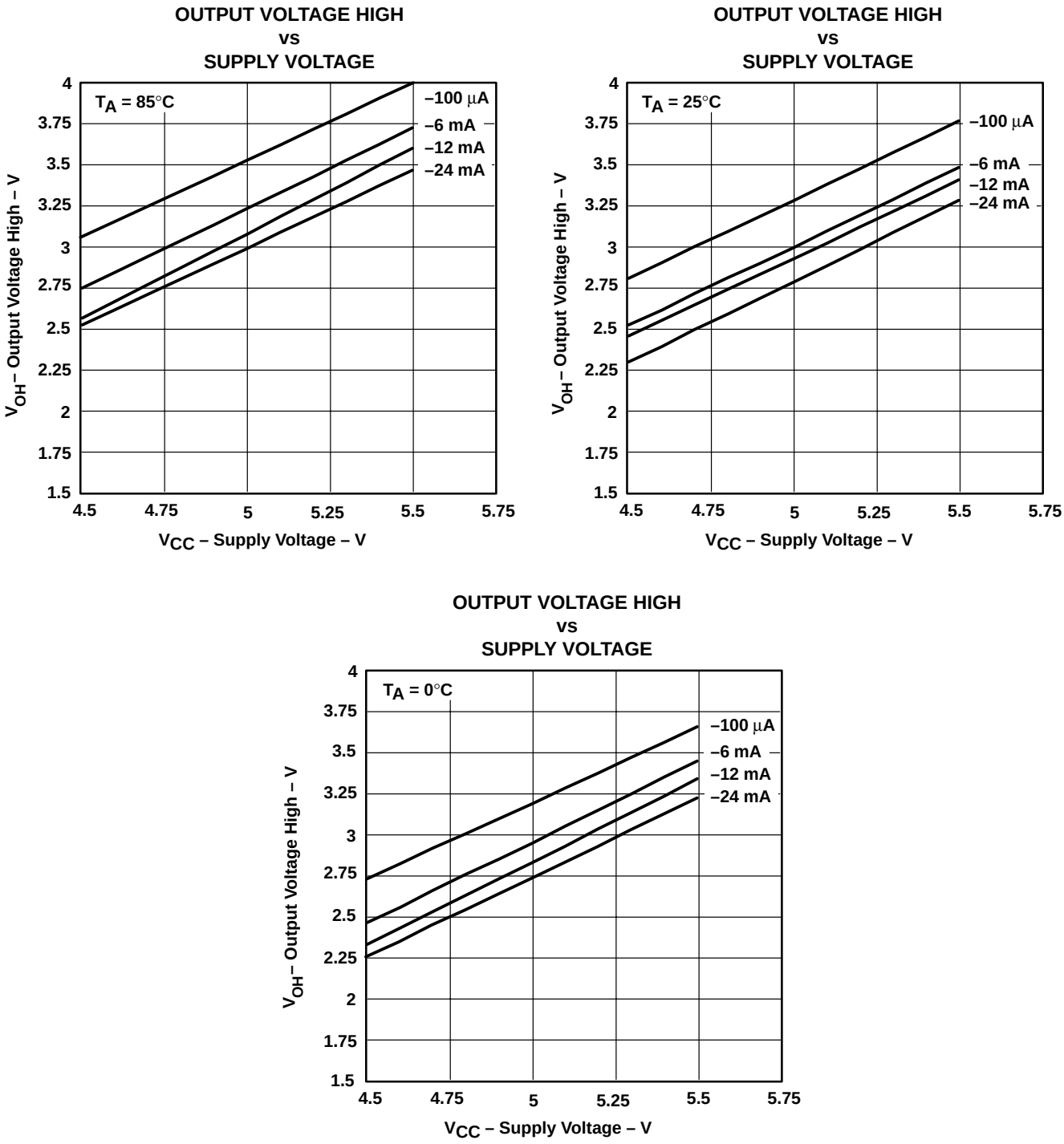


Figure 2. V_{OH} Values

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