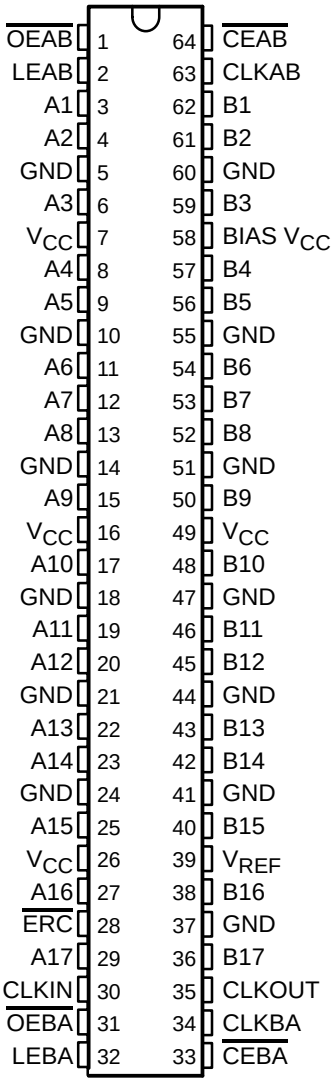
17-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE UNIVERSAL BUS TRANSCEIVER WITH BUFFERED CLOCK OUTPUTS

SCES346C– JANUARY 2001 – REVISED AUGUST 2001

- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Modes**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP Buffered CLKAB Signal (CLKOUT)**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



description

The SN74GTLPH1616 is a high-drive, 17-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer. Additionally, it provides for a copy of CLKAB at GTLP signal levels (CLKOUT) and conversion of a GTLP clock to LVTTL logic levels (CLKIN). The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11 Ω.

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description (continued)

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH1616 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the reference input voltage for the B port.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry is provided to hold unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1616DGGR	GTLPH1616

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH1616 is a high-drive (100 mA), 17-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, clocked, or clock-enabled modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1616 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH1616 UBT transceiver replaces all above functions					

Additionally, the device allows for transparent conversion of CLKAB-to-GTLP signal levels (CLKOUT) and CLKOUT-to-LVTTL logic levels (CLKIN).

Data flow in each direction is controlled by clock enables ($\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$). $\overline{\text{CEAB}}$ and $\overline{\text{CEBA}}$ enable all 17 bits, and $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$ control the 17 bits of data and the CLKOUT/CLKIN buffered clock path for the A-to-B and B-to-A directions, respectively.

For A-to-B data flow, when $\overline{\text{CEAB}}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{\text{CEAB}}$ and LEAB are low, the A data is latched regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{\text{OEAB}}$ is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except $\overline{\text{CEBA}}$, $\overline{\text{OEBA}}$, LEBA, and CLKBA are used.

Function Tables

OUTPUT ENABLE†

INPUTS					OUTPUT B	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown: B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

BUFFERED CLOCK

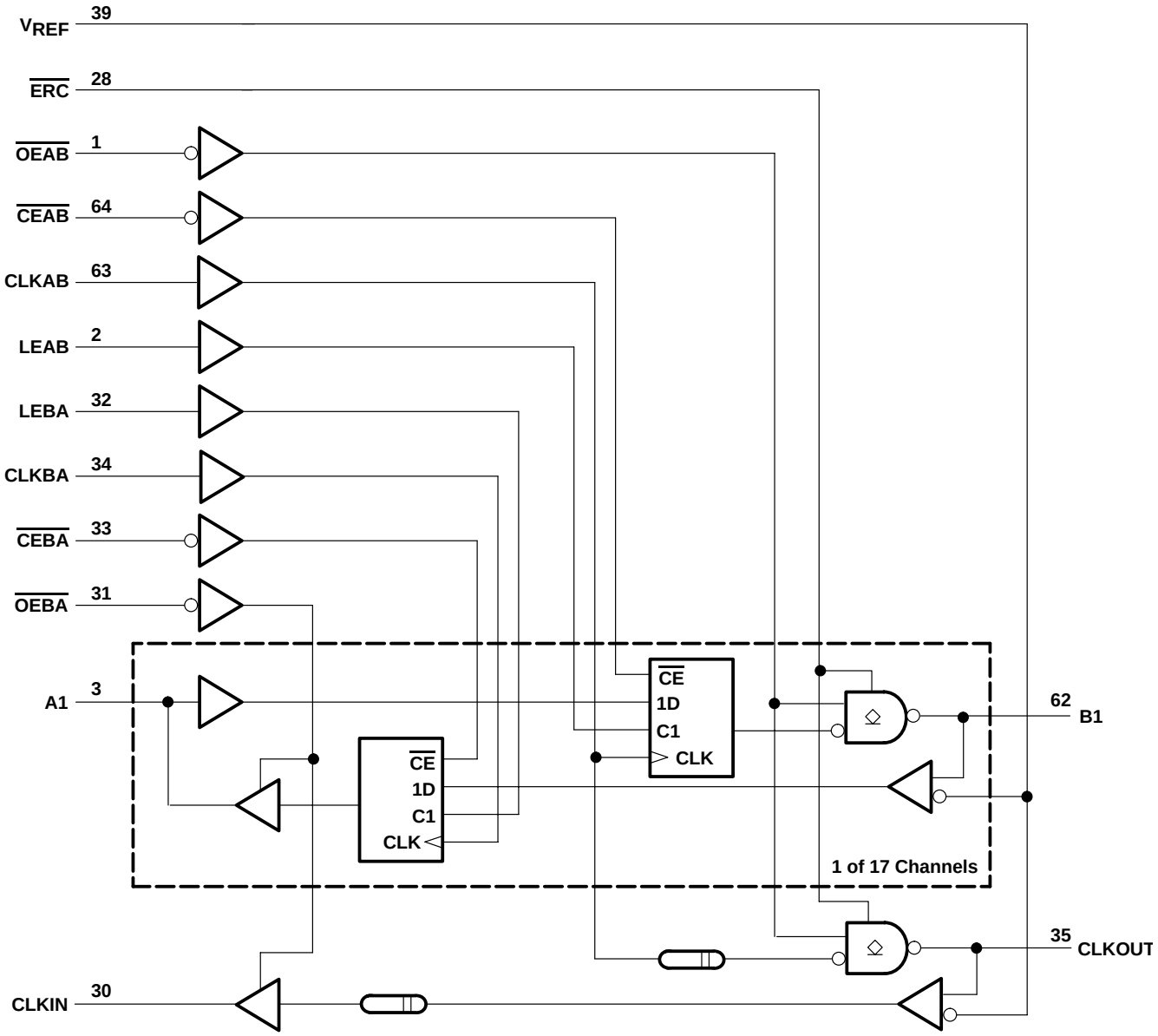
INPUTS				OPERATION OR FUNCTION	MODE
$\overline{CE}$	LE	$\overline{OEAB}$	$\overline{OEBA}$		
X	X	H	H	Z	Isolation
X	X	L	H	CLKAB to CLKOUT	True delayed clock signal
X	X	H	L	CLKOUT to CLKIN	
X	X	L	L	CLKAB to CLKOUT, CLKOUT to CLKIN	True delayed clock signal with feedback path¶

¶ This condition is not recommended.

B-PORT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A-port, $\overline{ERC}$, and control inputs . . . . . –0.5 V to 7 V
B port and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): A port . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . . 48 mA
B port . . . . . 200 mA
Current into any A port output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 55°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}	5.5	
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			μs/V
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.

7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 μA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	Control inputs	V_{CC} = 3.45 V,	V_I = 0 or 5.5 V			±10	μA
I_{OZH}‡	A port	V_{CC} = 3.45 V	V_O = V_{CC}			10	μA
	B port		V_O = 1.5 V			10	
I_{OZL}‡	A and B ports	V_{CC} = 3.45 V,	V_O = GND			–10	μA
I_{BHL}§	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			μA
I_{BHH}¶	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			μA
I_{BHLO}#	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			μA
I_{BHHO}‖	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			μA
I_{CC}	A or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			45	mA
			Outputs low			45	
			Outputs disabled			45	
ΔI_{CC}☆		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	Control inputs	V_I = 3.15 V or 0			4	5.5	pF
C_{io}	A port	V_O = 3.15 V or 0			6.5	8	pF
	B port or CLKOUT	V_O = 1.5 V or 0			9.5	11.5	
C_o	CLKIN	V_O = 3.15 V or 0			4.5	5.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
§ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL}max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL}max.
¶ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH}min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH}min.
# An external driver must source at least I_{BHLO} to switch this node from low to high.
‖ An external driver must sink at least I_{BHHO} to switch this node from high to low.
☆ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

hot-insertion specifications for A port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	μA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	μA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		μA

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (unless otherwise noted)

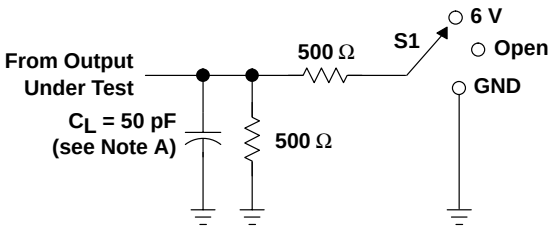
			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	LEAB or LEBA high	3		ns
		CLKAB or CLKBA high or low	3		
t_{su}	Setup time	A before CLKAB↑	2.2		ns
		B before CLKBA↑	2.4		
		A before LEAB↓, CLK = Don't care	1.8		
		B before LEBA↓, CLK = Don't care	2.1		
		$\overline{CEAB}$ before CLKAB↑	1.5		
		$\overline{CEBA}$ before CLKBA↑	1.5		
t_h	Hold time	A after CLKAB↑	0.7		ns
		B after CLKBA↑	0.5		
		A after LEAB↓, CLK = Don't care	1.2		
		B after LEBA↓, CLK = Don't care	0.9		
		$\overline{CEAB}$ after CLKAB↑	1.5		
		$\overline{CEBA}$ after CLKBA↑	1.5		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (normal mode) (see Figure 1)

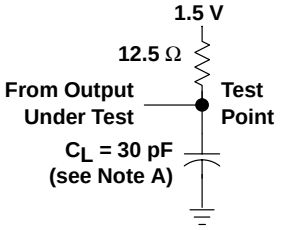
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f_{max}				175			MHz
t_{PLH}	A	B	Slow	4.3	5.6	7.1	ns
t_{PHL}				3.2	4.6	6.4	
t_{PLH}	A	B	Fast	3.2	4.3	5.6	ns
t_{PHL}				2.7	3.9	5.3	
t_{PLH}	LEAB	B	Slow	4.8	6.2	7.8	ns
t_{PHL}				3.5	4.9	6.7	
t_{PLH}	LEAB	B	Fast	3.5	4.8	6.2	ns
t_{PHL}				3.1	4.3	5.8	
t_{PLH}	CLKAB	B	Slow	4.8	6.1	7.6	ns
t_{PHL}				3.5	4.8	6.6	
t_{PLH}	CLKAB	B	Fast	3.6	4.9	6.2	ns
t_{PHL}				3.1	4.3	5.7	
t_{PLH}	CLKAB	CLKOUT	Slow	5.5	6.9	8.5	ns
t_{PHL}				5.5	7	9.3	
t_{PLH}	CLKAB	CLKOUT	Fast	4	5.3	6.7	ns
t_{PHL}				4.4	5.8	7.6	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Slow	4.8	6.2	7.8	ns
t_{dis}				3.4	5.2	7.8	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Fast	3.6	4.8	6.2	ns
t_{dis}				3	4.4	6.1	
t_r	Rise time, B outputs (20% to 80%)		Slow		2.5		ns
			Fast		1.4		
t_f	Fall time, B outputs (80% to 20%)		Slow		3.3		ns
			Fast		2.4		
t_{PLH}	B	A	—	1.1	2.8	4.3	ns
t_{PHL}				1.9	3.1	4.1	
t_{PLH}	LEBA	A	—	1.3	3.1	4.6	ns
t_{PHL}				1.4	2.6	3.8	
t_{PLH}	CLKBA	A	—	1.3	3.3	4.8	ns
t_{PHL}				1.8	2.9	4.1	
t_{PLH}	CLKOUT	CLKIN	—	2.2	3.7	5.3	ns
t_{PHL}				2.7	3.9	5.1	
t_{en}	$\overline{OEBA}$	A or CLKIN	—	1.2	2.9	4.8	ns
t_{dis}				2.3	4	5.5	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

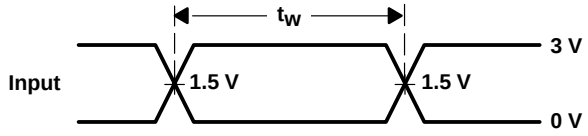


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

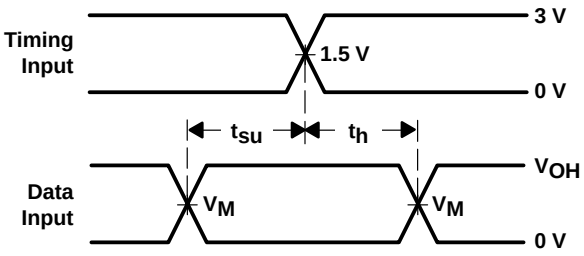


LOAD CIRCUIT FOR A OUTPUTS

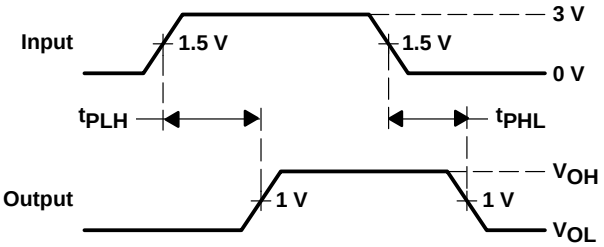
LOAD CIRCUIT FOR B OUTPUTS



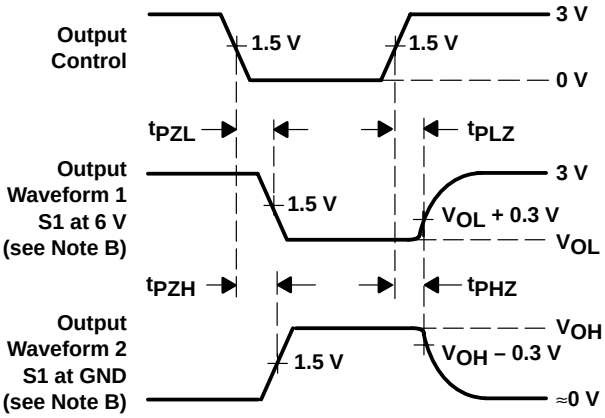
VOLTAGE WAVEFORMS
PULSE DURATION



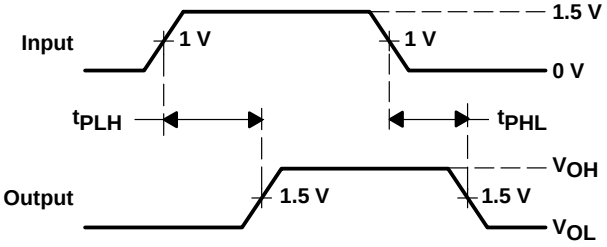
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≈ 10 MHz, Z_O = 50 Ω, t_r ≈ 2 ns, t_f ≈ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (see Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

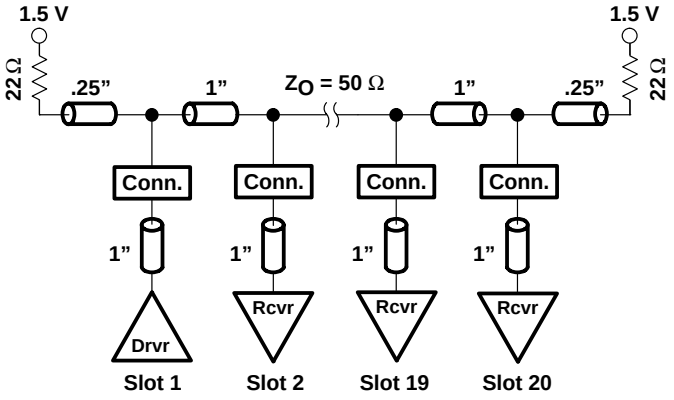


Figure 2. High-Drive Test Backplane

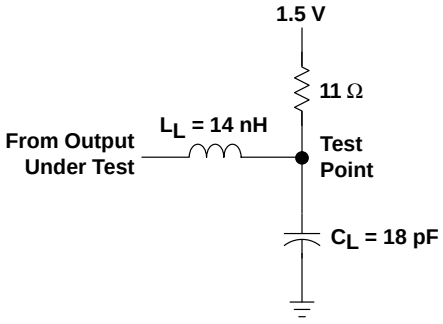


Figure 3. High-Drive RLC Network

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

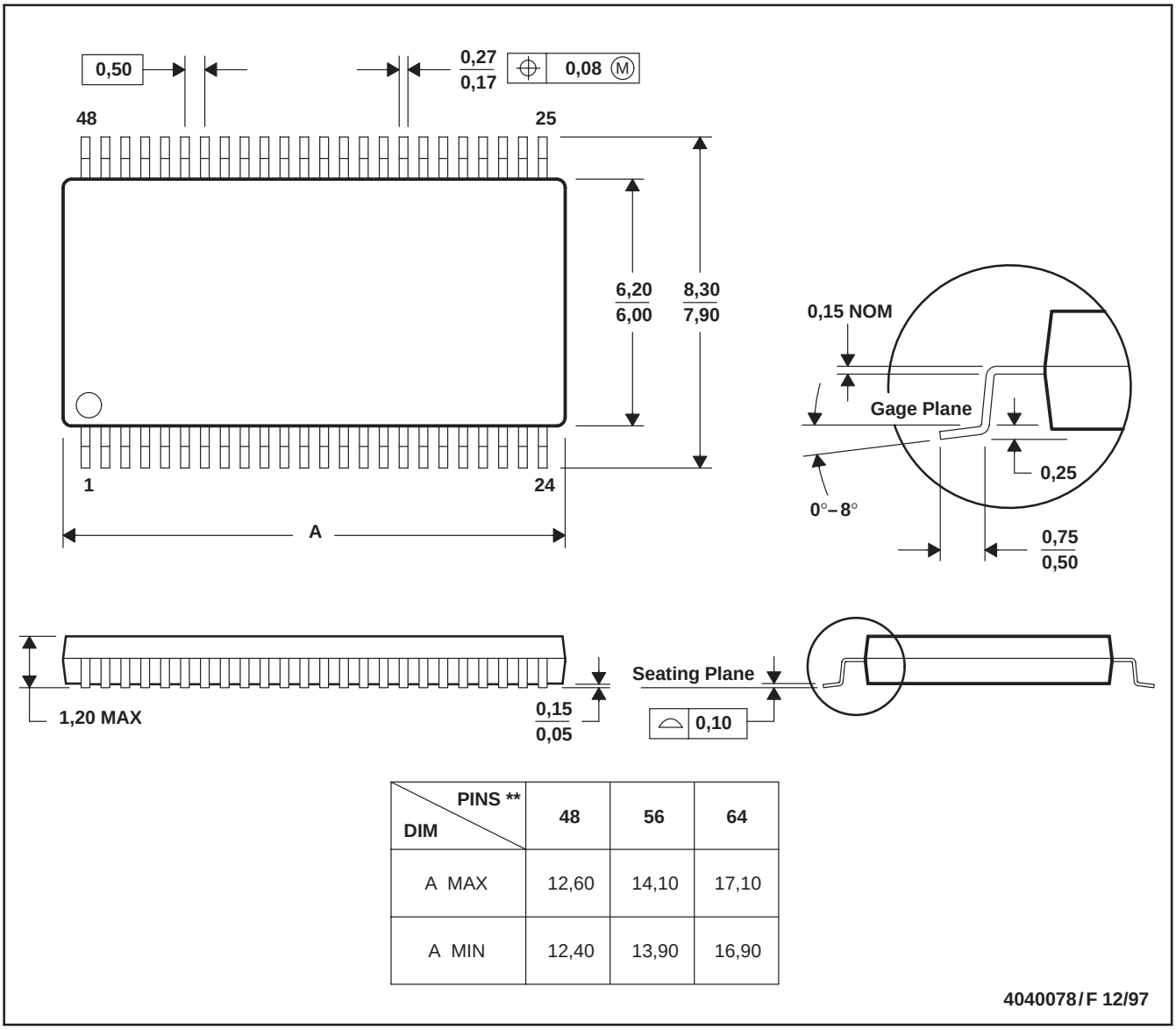
PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
t_{PLH}	A	B	Slow	5.3	ns
t_{PHL}				5.3	
t_{PLH}	A	B	Fast	4	ns
t_{PHL}				4	
t_{PLH}	LEAB	B	Slow	5.2	ns
t_{PHL}				5.2	
t_{PLH}	LEAB	B	Fast	3.9	ns
t_{PHL}				3.9	
t_{PLH}	CLK	B	Slow	5.5	ns
t_{PHL}				5.5	
t_{PLH}	CLK	B	Fast	4.3	ns
t_{PHL}				4.3	
t_{PLH}	CLKAB	CLKOUT	Slow	5.9	ns
t_{PHL}				5.9	
t_{PLH}	CLKAB	CLKOUT	Fast	4.8	ns
t_{PHL}				4.8	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Slow	5.7	ns
t_{dis}				4.3	
t_{en}	$\overline{OEAB}$	B or CLKOUT	Fast	4.3	ns
t_{dis}				3.8	
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI-SPICE models.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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