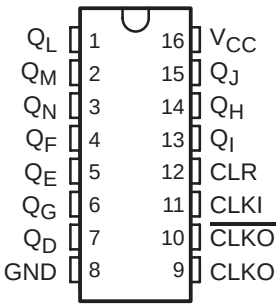
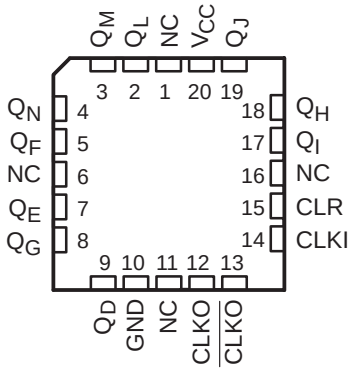
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 14 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Allow Design of Either RC- or Crystal-Oscillator Circuits**

SN54HC4060 . . . J OR W PACKAGE
SN74HC4060 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC4060 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The ’HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock (CLKI) input increments the counter. A high level at the clear (CLR) input disables the oscillator ($\overline{\text{CLKO}}$ goes high and CLKO goes low) and resets the counter to zero (all Q outputs low).

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 25	SN74HC4060N	SN74HC4060N
	SOIC − D	Tube of 40	SN74HC4060D	HC4060
		Reel of 2500	SN74HC4060DR	
		Reel of 250	SN74HC4060DT	
	SOP − NS	Reel of 2000	SN74HC4060NSR	HC4060
	SSOP − DB	Reel of 2000	SN74HC4060DBR	HC4060
	TSSOP − PW	Tube of 90	SN74HC4060PW	HC4060
		Reel of 2000	SN74HC4060PWR	
		Reel of 250	SN74HC4060PWT	
−55°C to 125°C	CDIP − J	Tube of 25	SNJ54HC4060J	SNJ54HC4060J
	CFP − W	Tube of 150	SNJ54HC4060W	SNJ54HC4060W
	LCCC − FK	Tube of 55	SNJ54HC4060FK	SNJ54HC4060FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

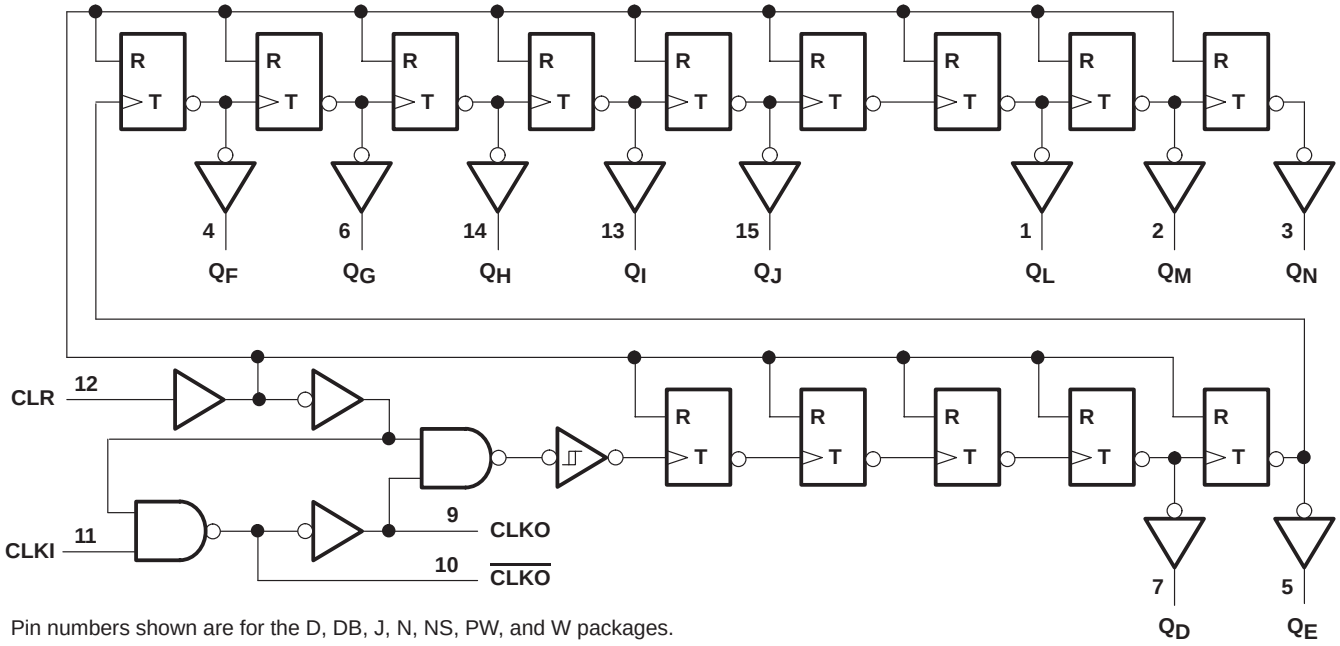
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 73°C/W
DB package . . . . . 82°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC4060			SN74HC4060			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC4060		SN74HC4060		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	All outputs	V_I = V_{IH} or V_{IL},	I_{OH} = −20 µA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
	Q outputs	V_I = V_{IH} or V_{IL}	I_{OH} = −4 mA	4.5 V	3.98	4.3		3.7		3.84		
			I_{OH} = −5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	All outputs	V_I = V_{IH} or V_{IL},	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
	Q outputs	V_I = V_{IH} or V_{IL}	I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
			I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I		V_I = V_{CC} or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	µA
C_i				2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC4060		SN74HC4060		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		5.5		3.7		4.3	MHz
			4.5 V		28		19		22	
			6 V		33		22		25	
t_w	Pulse duration	CLKI high or low	2 V	90		135		115		ns
			4.5 V	18		27		23		
			6 V	15		23		20		
		CLR high	2 V	90		135		115		
			4.5 V	18		27		23		
			6 V	15		23		20		
t_{su}	Setup time, CLR inactive before CLKI↓		2 V	160		240		200		ns
			4.5 V	32		48		40		
			6 V	27		41		34		

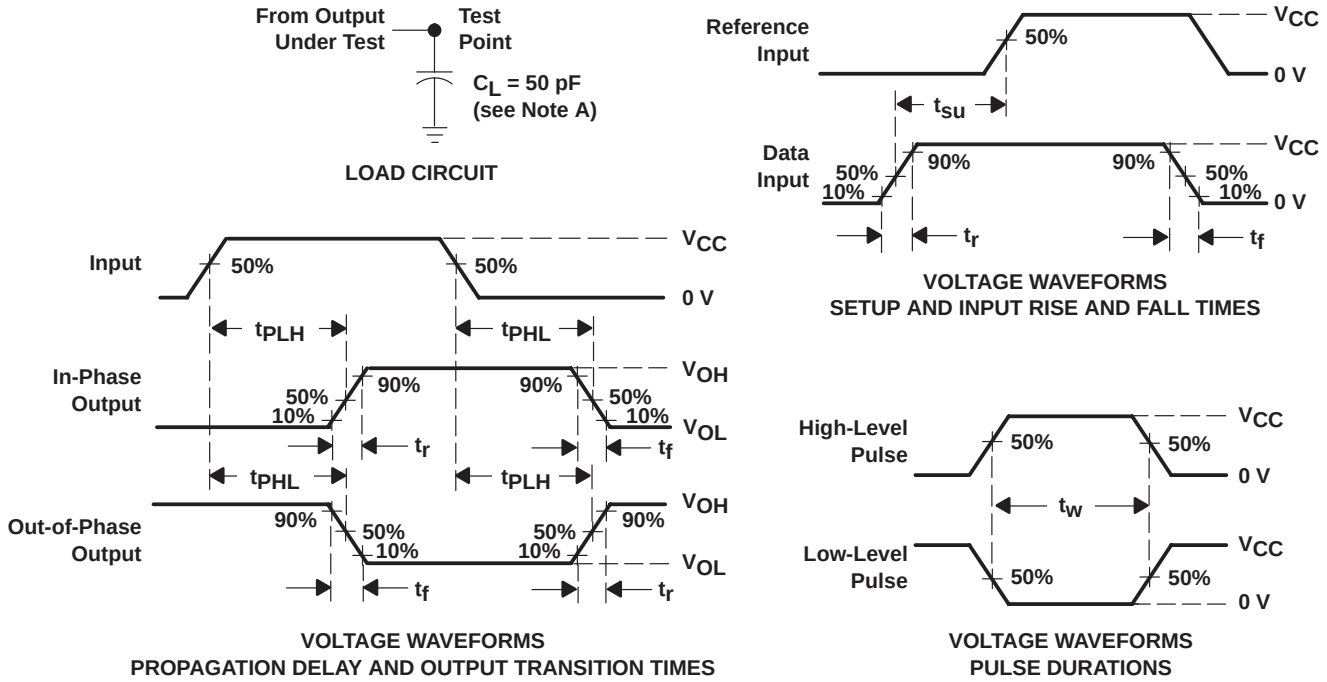
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC4060		SN74HC4060		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLKI	Q_D	2 V		240	490		735		615	ns
			4.5 V		58	98		147		123	
			6 V		42	83		125		105	
t_{PHL}	CLR	Any Q	2 V		66	140		210		175	ns
			4.5 V		18	28		42		35	
			6 V		14	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	30		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

PARAMETER MEASUREMENT INFORMATION



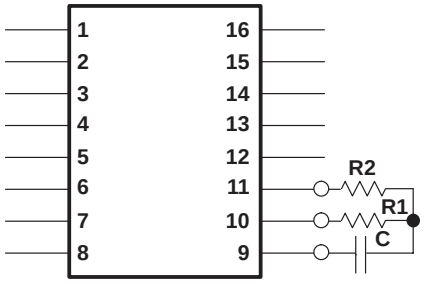
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE ’HC4060 DEVICES

The ’HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:



To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405\ R2}{R1 + R2} + 0.693\right)}$$

If R2 > > R1 (i.e., R2 = 10R1), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54HC4060FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC 4060FK
SN54HC4060FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC 4060FK
SN74HC4060D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	HC4060
SN74HC4060DBR	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060DBR.A	NRND	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060DT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	HC4060
SN74HC4060N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4060N
SN74HC4060N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC4060N
SN74HC4060NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060NSRE4	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	HC4060
SN74HC4060PWR	NRND	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060PWR.A	NRND	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060
SN74HC4060PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	HC4060

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC4060, SN74HC4060 :

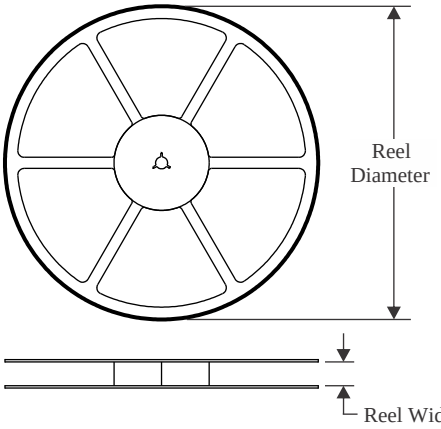
- Catalog : SN74HC4060
- Automotive : SN74HC4060-Q1, SN74HC4060-Q1
- Military : SN54HC4060

NOTE: Qualified Version Definitions:

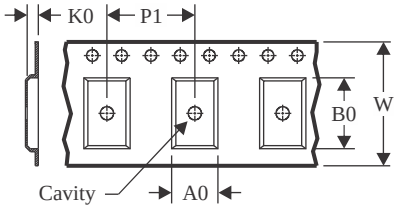
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

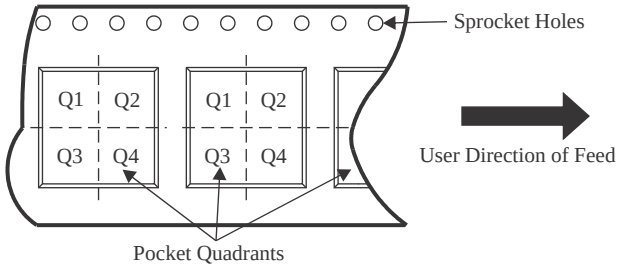


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

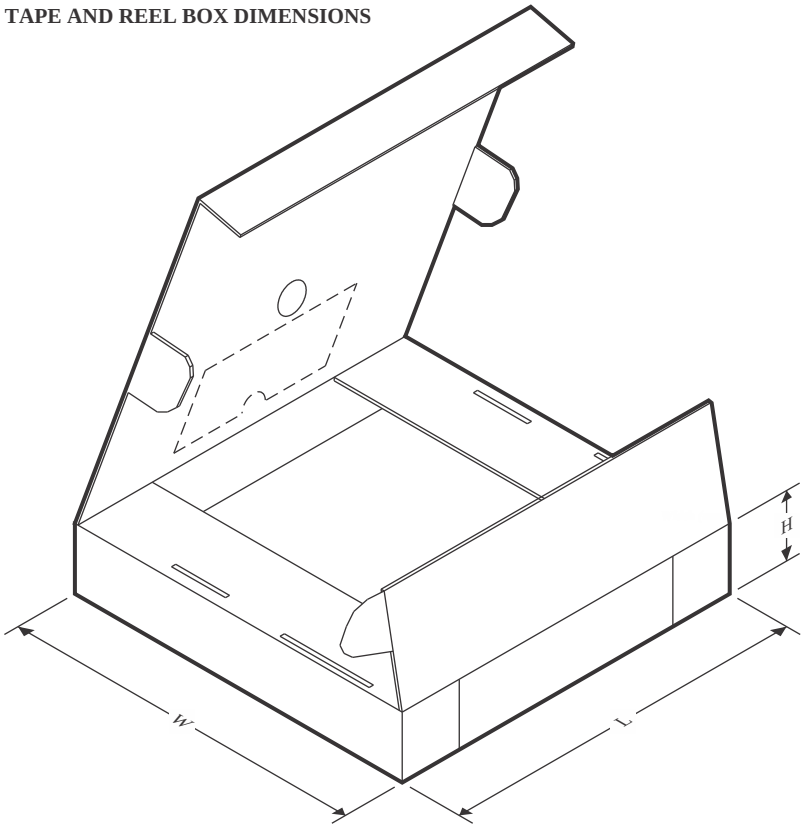
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4060DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC4060DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4060NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC4060PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

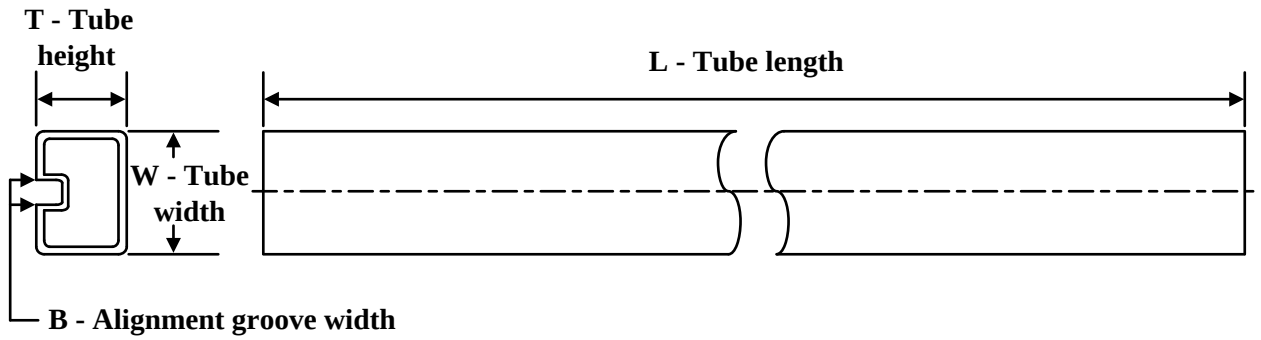
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4060DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74HC4060DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC4060NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC4060PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74HC4060PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN54HC4060FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SN54HC4060FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC4060N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4060N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4060N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4060N.A	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

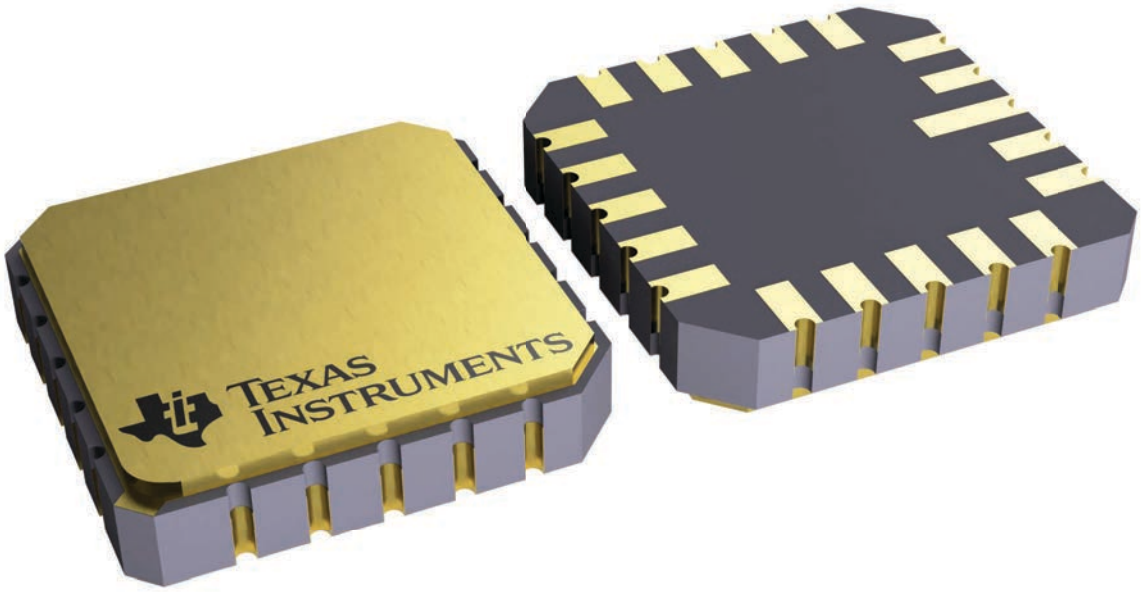
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



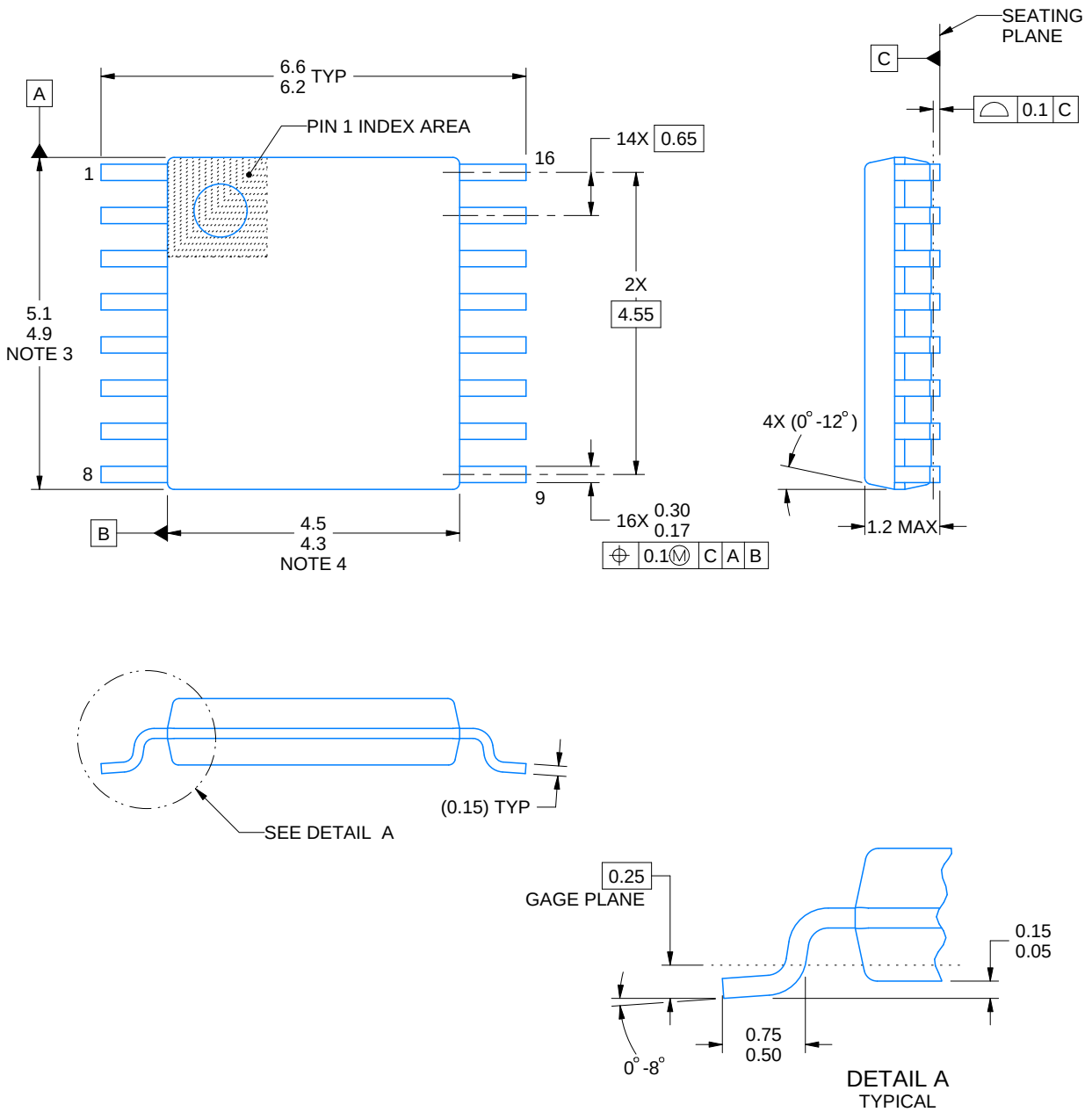
4229370VA\

PACKAGE OUTLINE

PW0016A

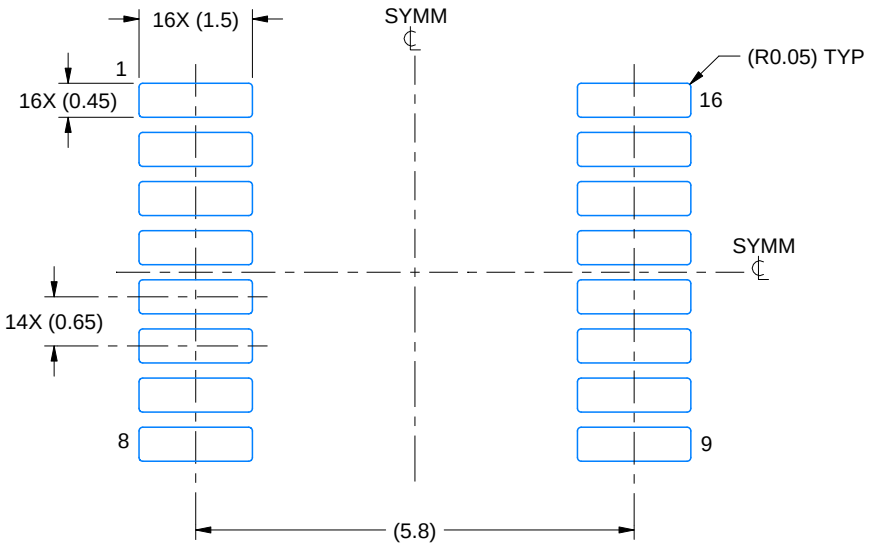
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

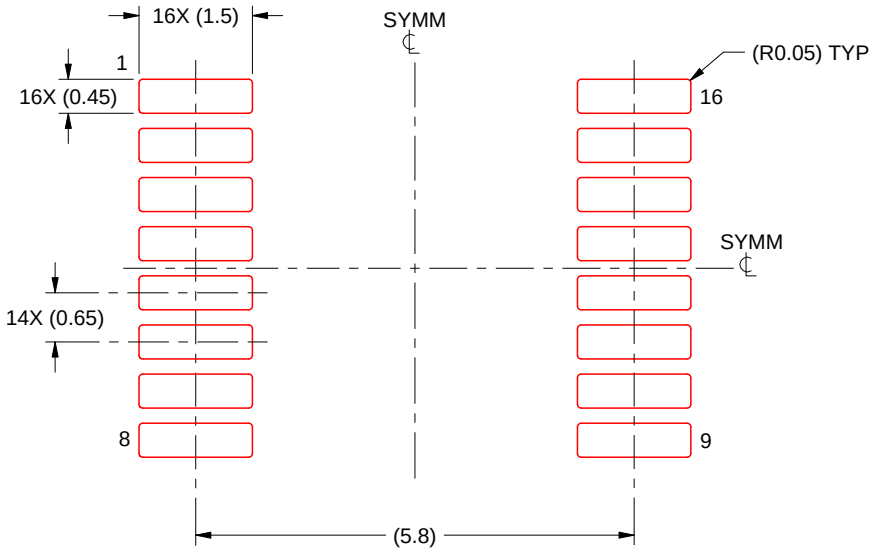


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

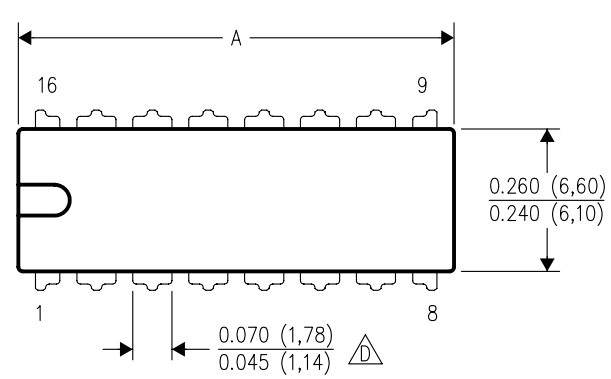
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

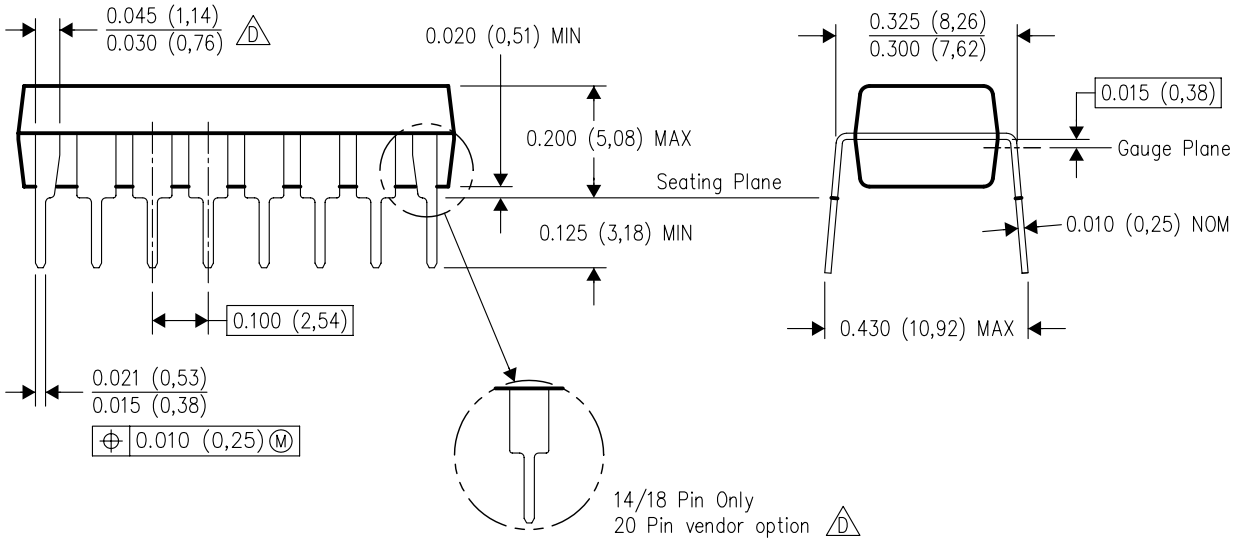
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

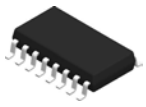


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

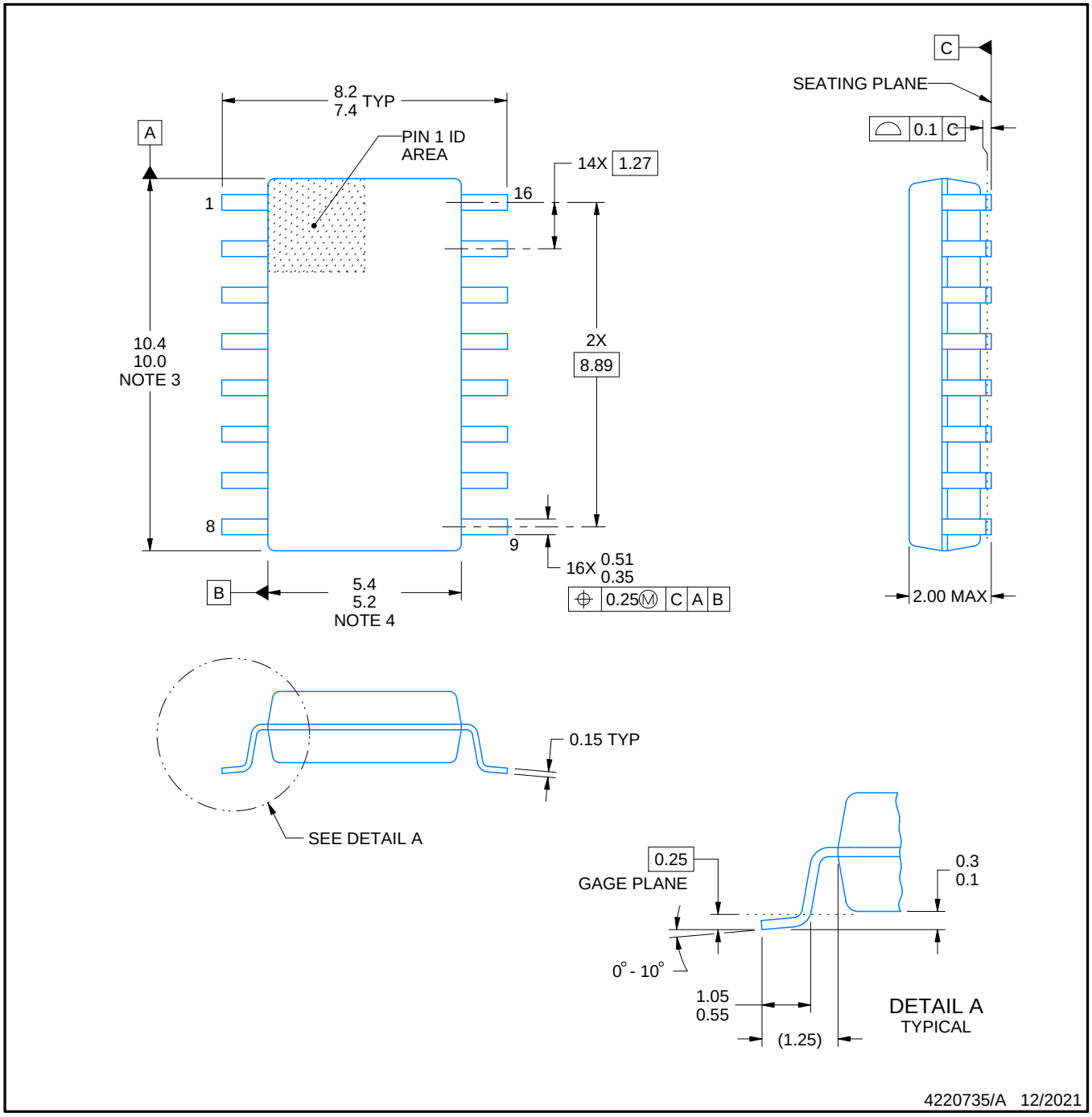


PACKAGE OUTLINE

NS0016A

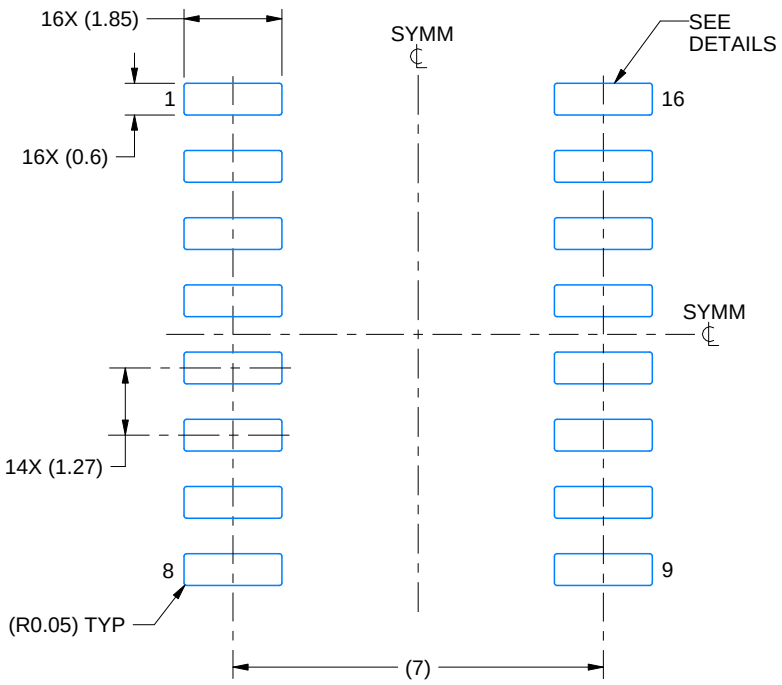
SOP - 2.00 mm max height

SOP

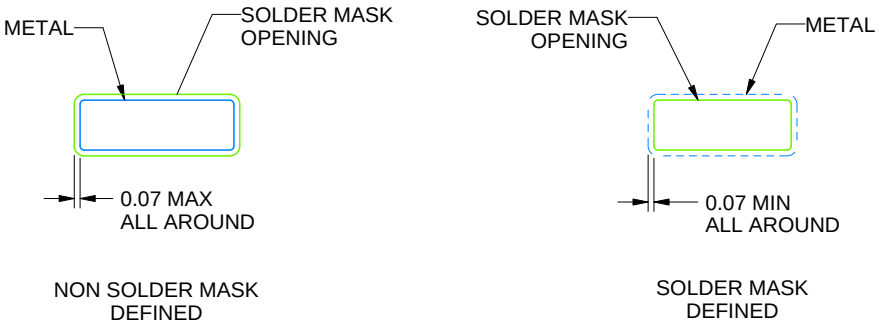


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

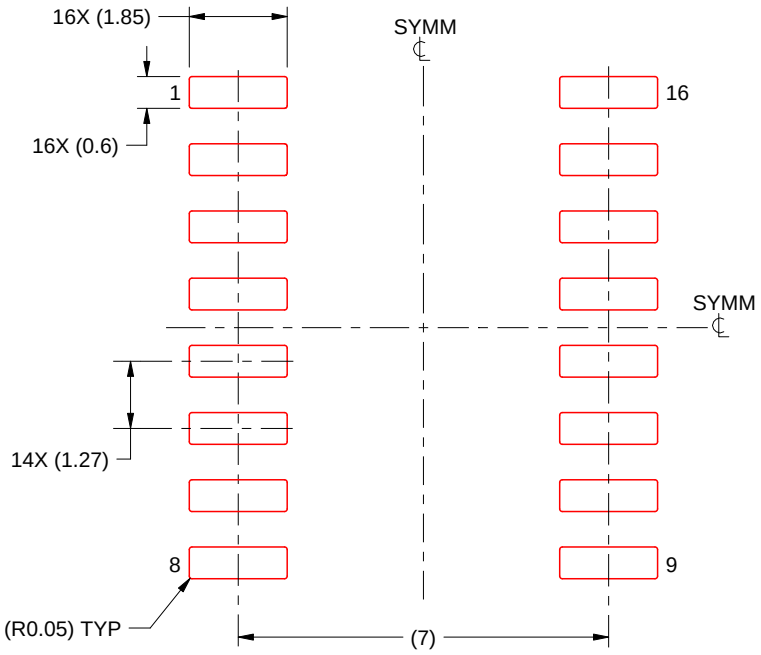
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



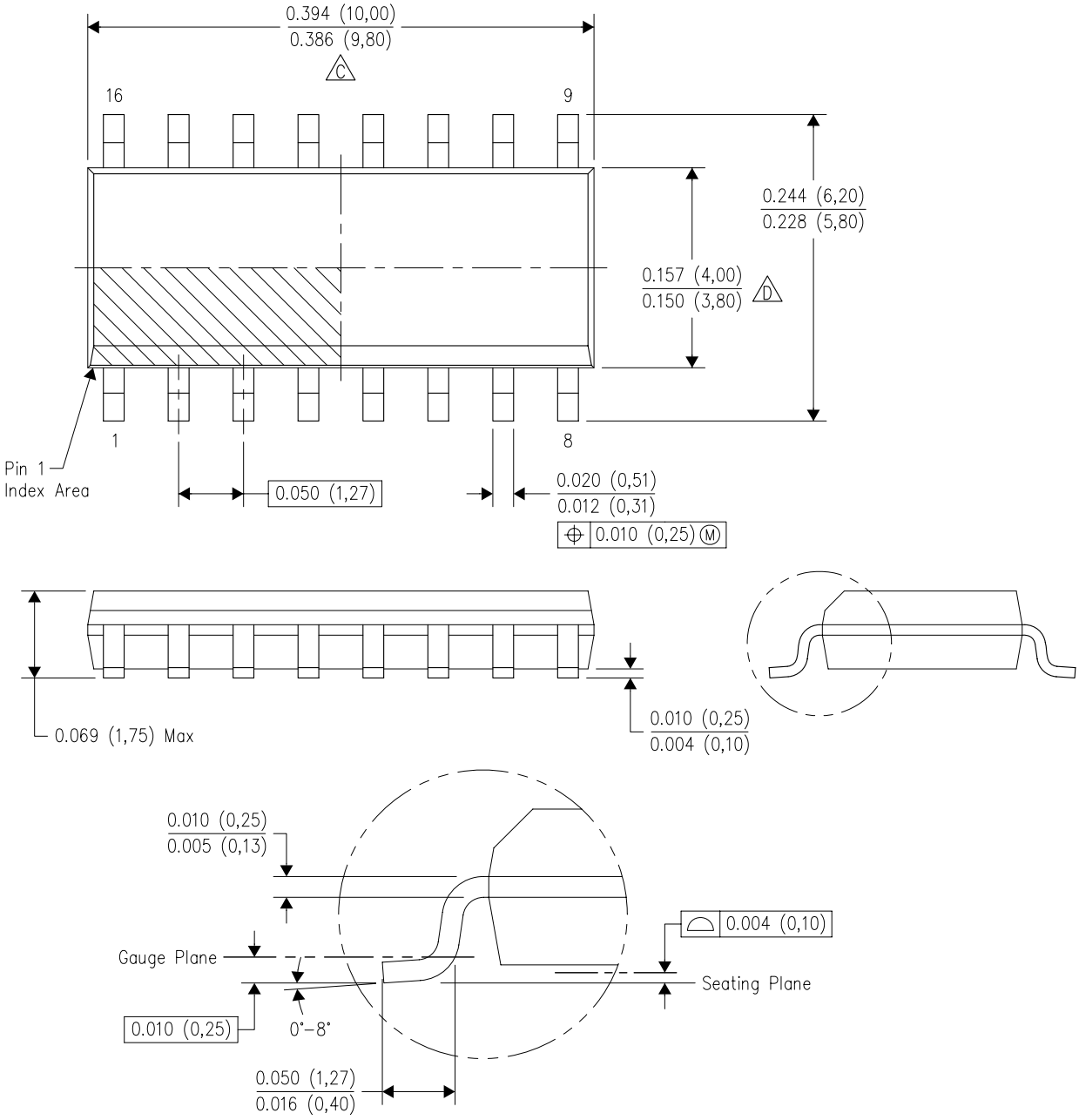
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



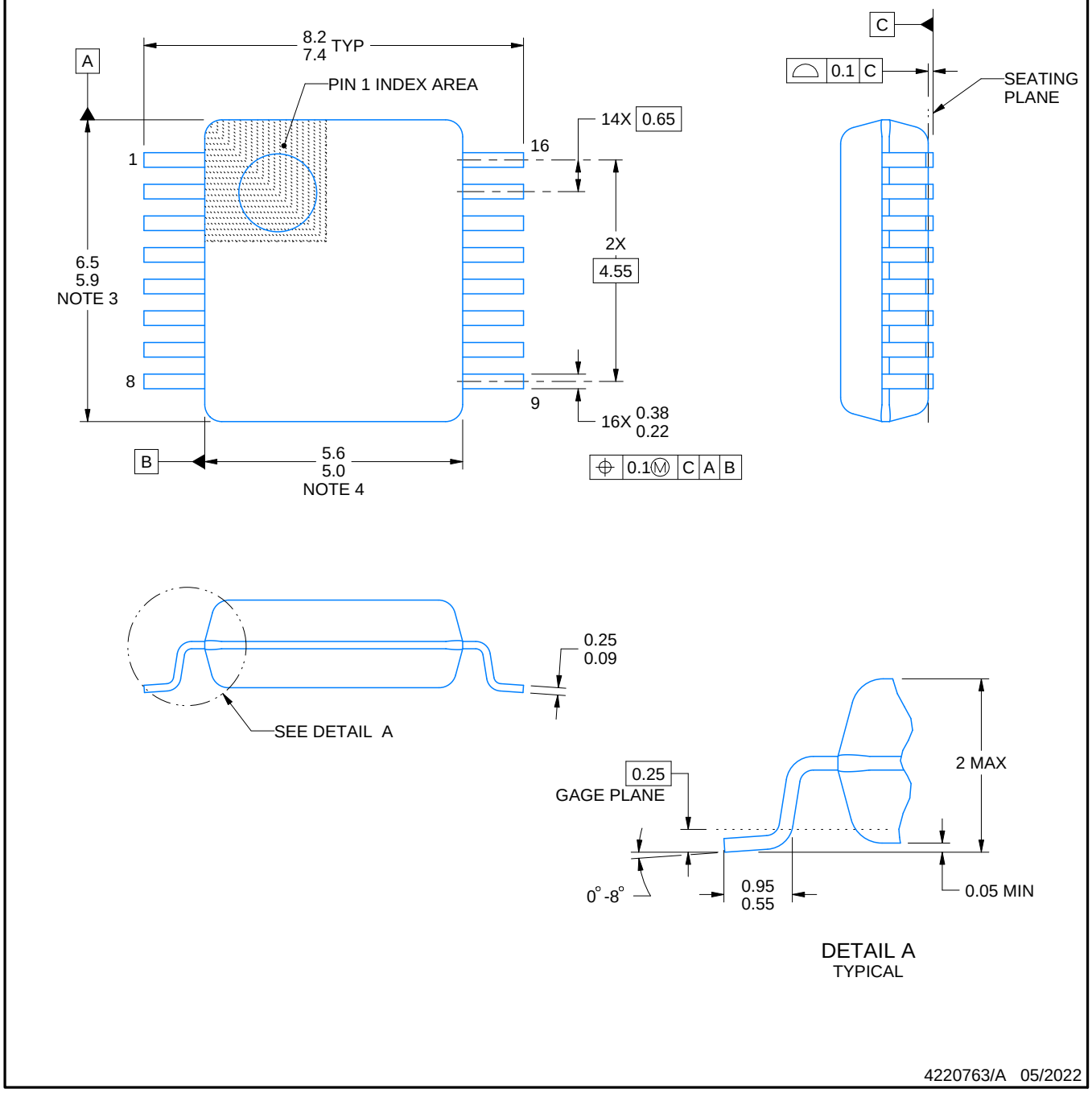
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

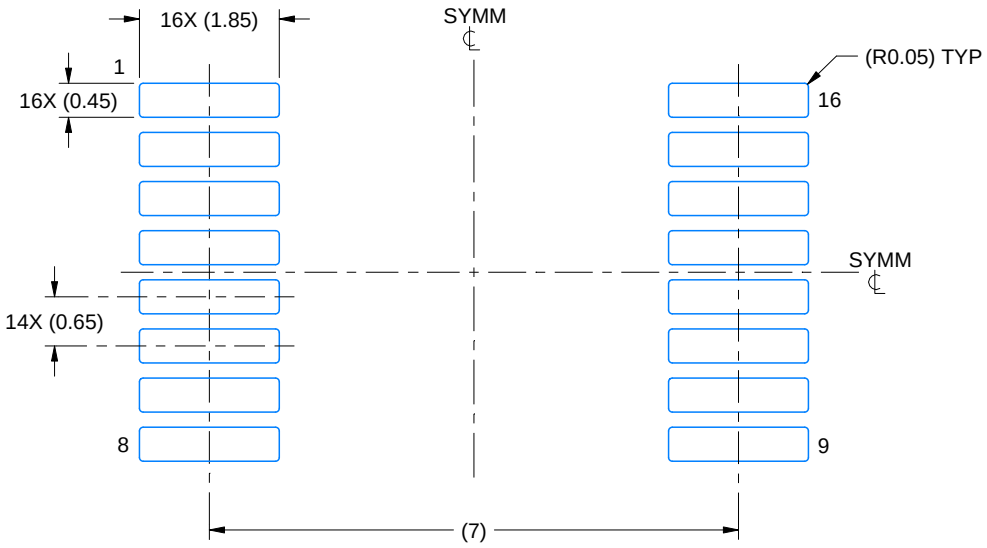
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

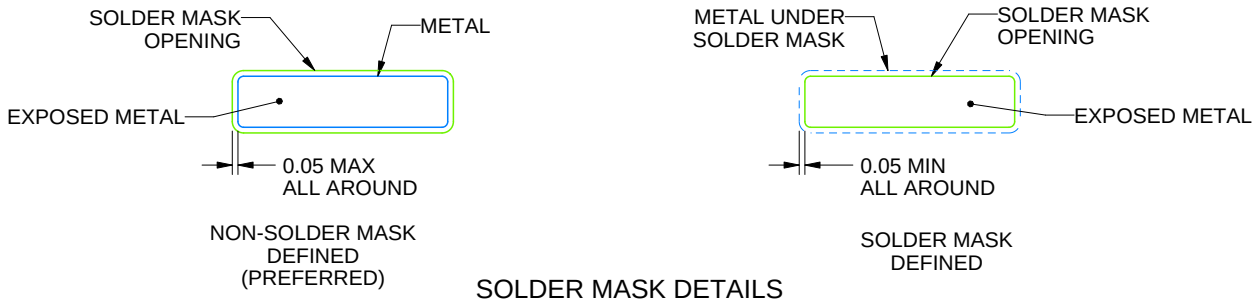


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

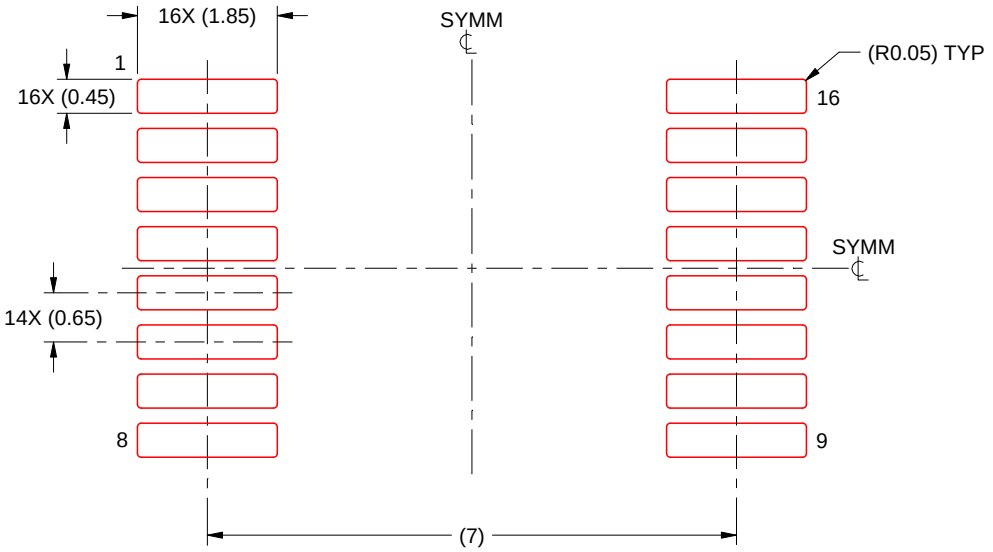


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025