# SN74HCS86-Q1 Automotive Quadruple 2-Input XOR Gates with Schmitt-Trigger Inputs

## 1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, $T_A$
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classifcation Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical $I_{CC}$ of 100 nA
  - Typical input leakage current of ±100 nA
- ±7.8-mA output drive at 6 V

## 2 Applications

- Detect phase differences in input signals
- Create a selectable inverter / buffer

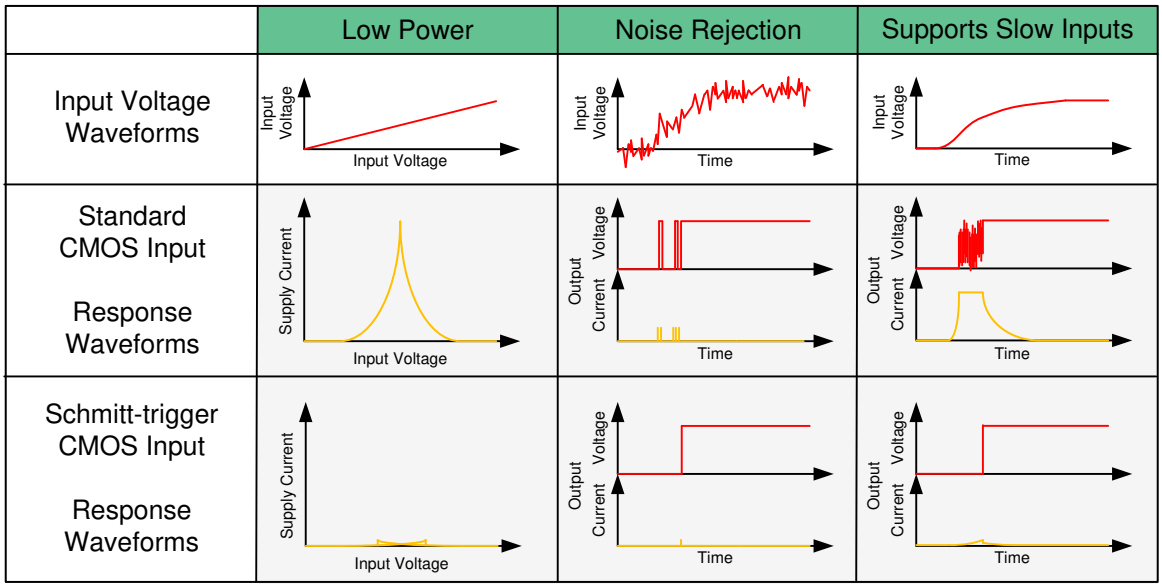
## 3 Description

This device contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ⊕ B in positive logic.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| SN74HCS86PW-Q1 | TSSOP (14) | 5.00 mm × 4.40 mm |
| SN74HCS86D-Q1 | SOIC (14) | 9.90 mm × 3.90 mm |
| SN74HCS86BQA-Q1 | WQFN (14) | 3.00 mm × 2.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Benefits of Schmitt-trigger inputs**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Revision History**....2
**5 Pin Configuration and Functions**....3
Pin Functions....3
**6 Specifications**....4
6.1 Absolute Maximum Ratings....4
6.2 ESD Ratings....4
6.3 Recommended Operating Conditions....4
6.4 Thermal Information....5
6.5 Electrical Characteristics....5
6.6 Switching Characteristics....6
6.7 Typical Characteristics....6
**7 Parameter Measurement Information**....7
**8 Detailed Description**....8
8.1 Overview....8
8.2 Functional Block Diagram....8
8.3 Feature Description....8
8.4 Device Functional Modes....9
**9 Application and Implementation**....10
9.1 Application Information....10
9.2 Typical Application....10
**10 Power Supply Recommendations**....13
**11 Layout**....13
11.1 Layout Guidelines....13
11.2 Layout Example....13
**12 Device and Documentation Support**....14
12.1 Documentation Support....14
12.2 Receiving Notification of Documentation Updates....14
12.3 Support Resources....14
12.5 Electrostatic Discharge Caution....14
12.6 Glossary....14
**13 Mechanical, Packaging, and Orderable Information**....15

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (September 2019) to Revision C (March 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added BQA package information to the *Device Information* table | 1 |
| • Added BQA package information to *Pin Configuration and Functions* | 3 |
| • Added BQA package information to *Thermal Information* table | 5 |

| Changes from Revision A (August 2019) to Revision B (September 2019) | Page |
|---|---|
| • Added D package to *Device Information* table | 1 |
| • Added D package information to *Pin Configuration and Functions* | 3 |
| • Added D package column to *Thermal Information* table | 5 |

| Changes from Revision * (July 2019) to Revision A (August 2019) | Page |
|---|---|
| • Deleted "$I_{CC}$" and "output" from "Continuous current through $V_{CC}$ or GND" row for clarity | 4 |


Copyright © 2021 Texas Instruments Incorporated

## 5 Pin Configuration and Functions

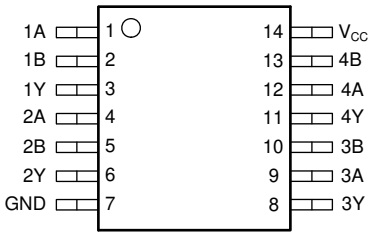



**Figure 5-1. D or PW Package**
**14-Pin SOIC or TSSOP**
**Top View**

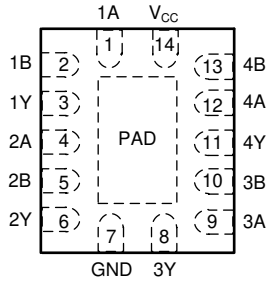



**Figure 5-2. BQA Package**
**14-Pin WQFN**
**Top View**

### Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | Input | Channel 1, Input A |
| 1B | 2 | Input | Channel 1, Input B |
| 1Y | 3 | Output | Channel 1, Output Y |
| 2A | 4 | Input | Channel 2, Input A |
| 2B | 5 | Input | Channel 2, Input B |
| 2Y | 6 | Output | Channel 2, Output Y |
| GND | 7 | — | Ground |
| 3Y | 8 | Output | Channel 3, Output Y |
| 3A | 9 | Input | Channel 3, Input A |
| 3B | 10 | Input | Channel 3, Input B |
| 4Y | 11 | Output | Channel 4, Output Y |
| 4A | 12 | Input | Channel 4, Input A |
| 4B | 13 | Input | Channel 4, Input B |
| $V_{CC}$ | 14 | — | Positive Supply |

1. BQA Package only.

Copyright © 2021 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_J$ | Junction temperature(3) | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2 | ±4000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6 | ±1500 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | | $V_{CC}$ | V |
| Δt/Δv | Input transition rise and fall rate | | | Unlimited | ns/V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |


Copyright © 2021 Texas Instruments Incorporated

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74HCS86-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | PW (TSSOP) | D (SOIC) | BQA (WQFN) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 151.7 | 133.6 | 109.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 79.4 | 89.0 | 111.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 94.7 | 89.5 | 77.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 25.2 | 45.5 | 20.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 94.1 | 89.1 | 77.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 56.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.7 | | 3.15 | |
| | | | | 6 V | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | | 1.0 | V |
| | | | | 4.5 V | 0.9 | | 2.2 | |
| | | | | 6 V | 1.2 | | 3.0 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$) | | | 2 V | 0.2 | | 1.0 | V |
| | | | | 4.5 V | 0.4 | | 1.4 | |
| | | | | 6 V | 0.6 | | 1.6 | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V to 6 V | $V_{CC}$ – 0.1 | $V_{CC}$ – 0.002 | | V |
| | | | $I_{OH}$ = -6 mA | 4.5 V | 4.0 | 4.3 | | |
| | | | $I_{OH}$ = -7.8 mA | 6 V | 5.4 | 5.75 | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V to 6 V | | 0.002 | 0.1 | V |
| | | | $I_{OL}$ = 6 mA | 4.5 V | | 0.18 | 0.30 | |
| | | | $I_{OL}$ = 7.8 mA | 6 V | | 0.22 | 0.33 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±100 | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 6 V | | 0.1 | 2 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | | 5 | pF |
| $C_{pd}$ | Power dissipation capacitance per gate | No load | | 2 V to 6 V | | 10 | | pF |

Copyright © 2021 Texas Instruments Incorporated

## 6.6 Switching Characteristics

$C_L$ = 50 pF; over operating free-air temperature range; typical ratings measured at $T_A$ = 25°C (unless otherwise noted). See Parameter Measurement Information.

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay | A or B | Y | 2 V | | 15 | 36 | ns |
| | | | | 4.5 V | | 7 | 13 | |
| | | | | 6 V | | 6 | 12 | |
| $t_t$ | Transition-time | | Y | 2 V | | 9 | 16 | ns |
| | | | | 4.5 V | | 5 | 9 | |
| | | | | 6 V | | 4 | 8 | |

## 6.7 Typical Characteristics

$T_A$ = 25°C

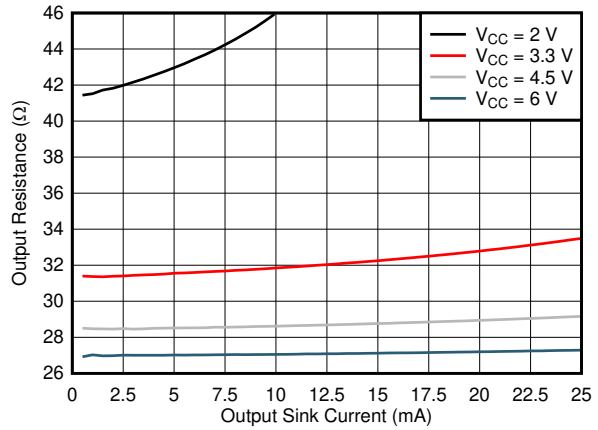



**Figure 6-1. Output driver resistance in LOW state.**

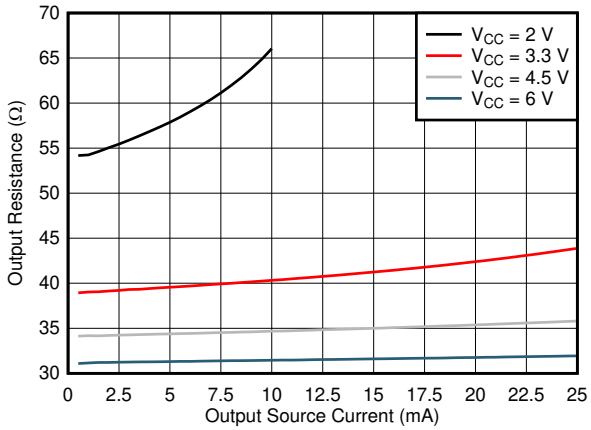



**Figure 6-2. Output driver resistance in HIGH state.**

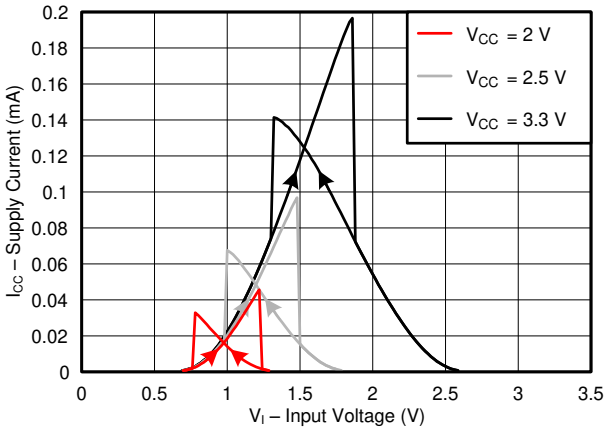



**Figure 6-3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply**

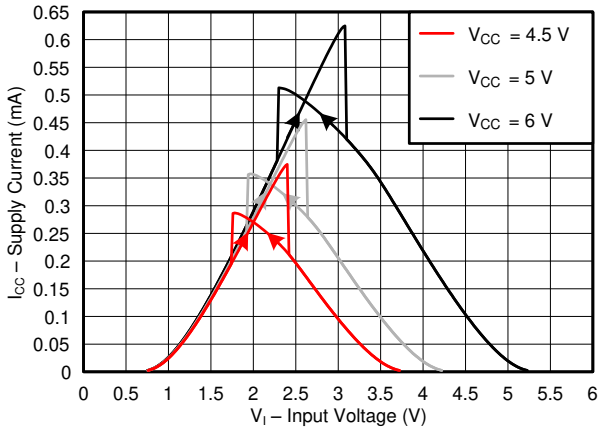



**Figure 6-4. Supply current across input voltage, 4.5-, 5-, and 6-V supply**

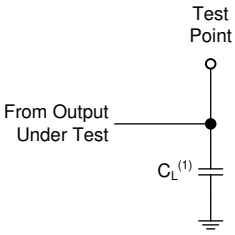

Copyright © 2021 Texas Instruments Incorporated

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 2.5 ns.

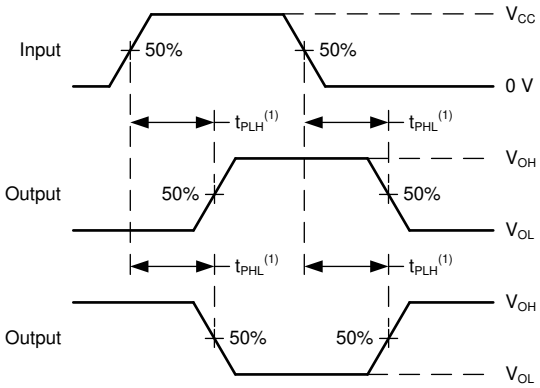
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



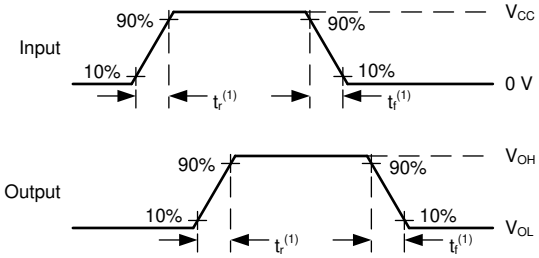

(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 7-1. Load Circuit for Push-Pull Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 7-2. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

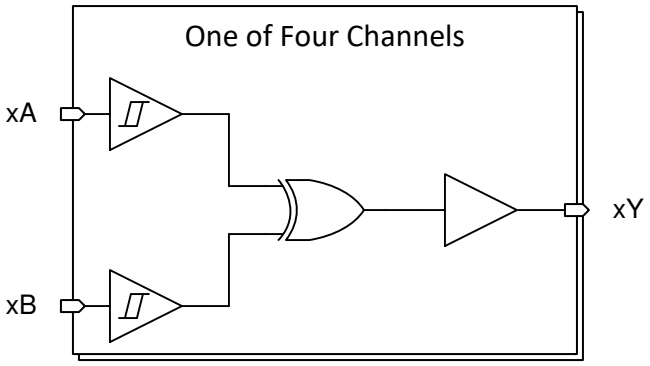
**Figure 7-3. Voltage Waveforms, Input and Output Transition Times**

# 8 Detailed Description

## 8.1 Overview

This device contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A ⊕ B in positive logic.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.


Copyright © 2021 Texas Instruments Incorporated

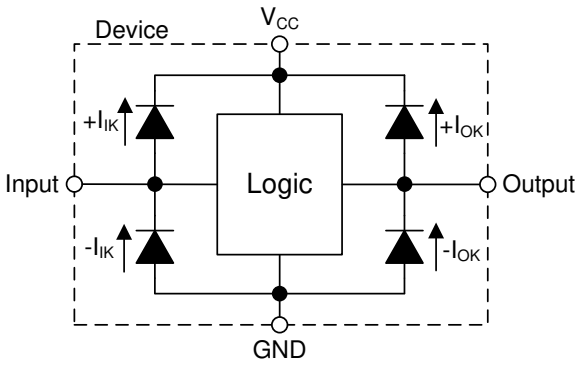



**Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

Function Table lists the functional modes of the SN74HCS86-Q1.

**Table 8-1. Function Table**

| INPUTS(1) | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

(1) H = High Voltage Level, L = Low Voltage Level

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in Typical application block diagram. The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The SN74HCS86-Q1 is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

Typically, clock signals have fast transition rates, but additional filtering can be added to the clock signals which can lead to slower transitions rates. This makes the SN74HCS86-Q1 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

## 9.2 Typical Application

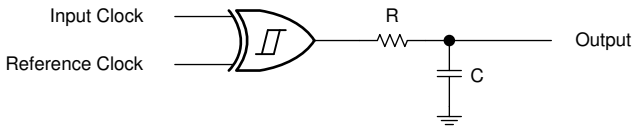



**Figure 9-1. Typical application block diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS86-Q1 plus the maximum static supply current, $I_{CC}$, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS86-Q1 plus the maximum supply current, $I_{CC}$, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS86-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS86-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.


Copyright © 2021 Texas Instruments Incorporated

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS86-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS86-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS86-Q1 to the receiving device(s).
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

Copyright © 2021 Texas Instruments Incorporated

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

### 9.2.3 Application Curves

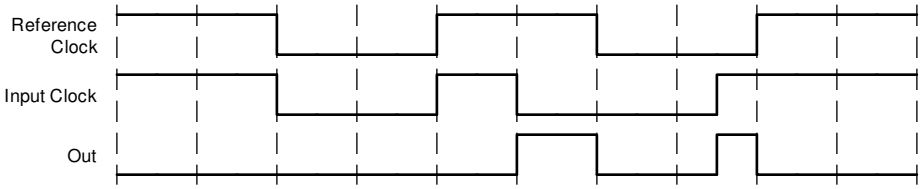



**Figure 9-2. Application timing diagram**


Copyright © 2021 Texas Instruments Incorporated

# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

## 11.2 Layout Example

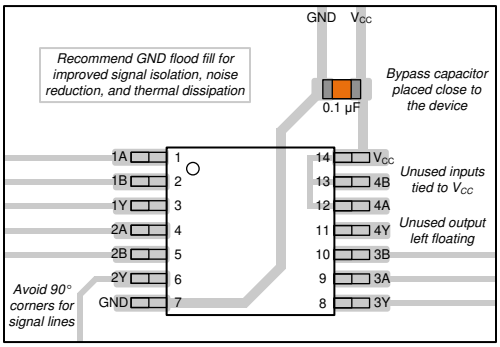



**Figure 11-1. Example layout for the SN74HCS86-Q1**

Copyright © 2021 Texas Instruments Incorporated

# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.


Copyright © 2021 Texas Instruments Incorporated

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2021 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HCS86QBQARQ1 | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS86Q |
| SN74HCS86QBQARQ1.A | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS86Q |
| SN74HCS86QDRQ1 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS86Q1 |
| SN74HCS86QDRQ1.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS86Q1 |
| SN74HCS86QPWRQ1 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | HCS86Q |
| SN74HCS86QPWRQ1.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS86Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74HCS86-Q1 :**

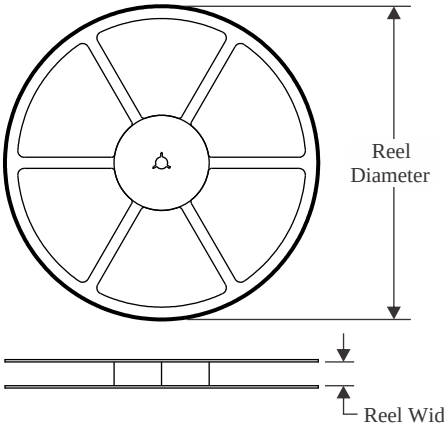
- Catalog : SN74HCS86

NOTE: Qualified Version Definitions:

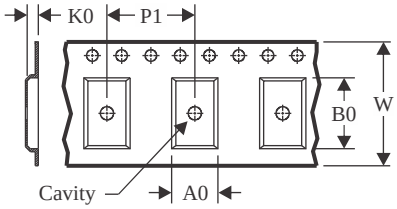
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

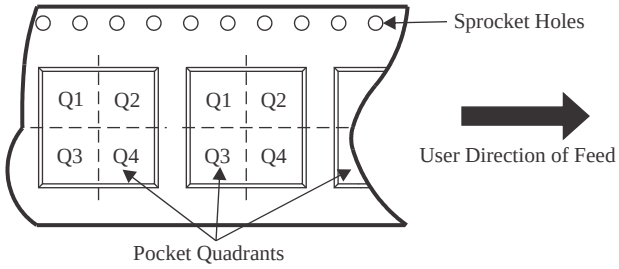



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

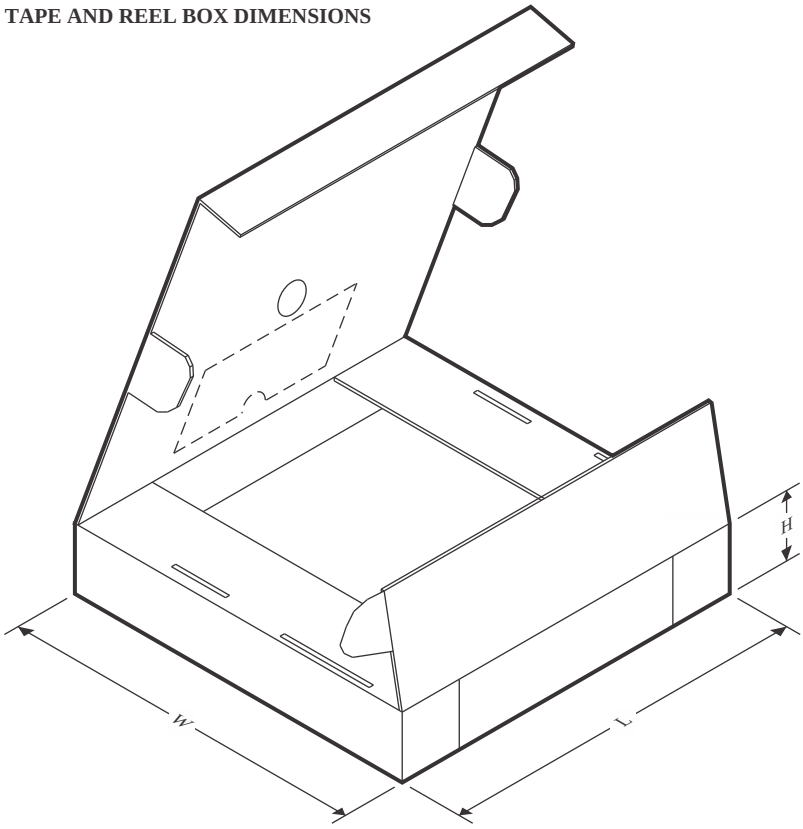
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HCS86QBQARQ1 | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74HCS86QDRQ1 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HCS86QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HCS86QBQARQ1 | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74HCS86QDRQ1 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HCS86QPWRQ1 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

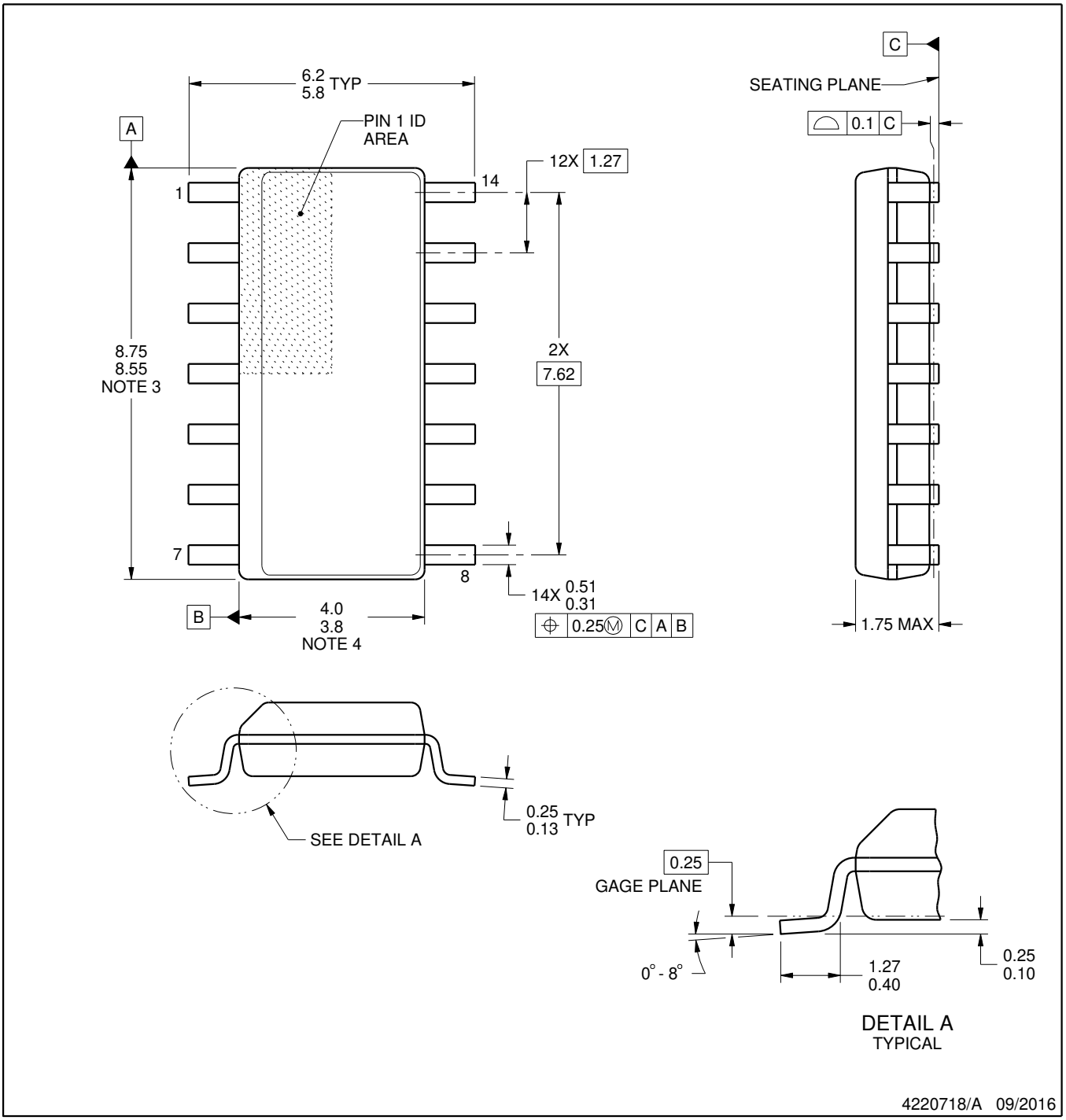


# PACKAGE OUTLINE

## D0014A

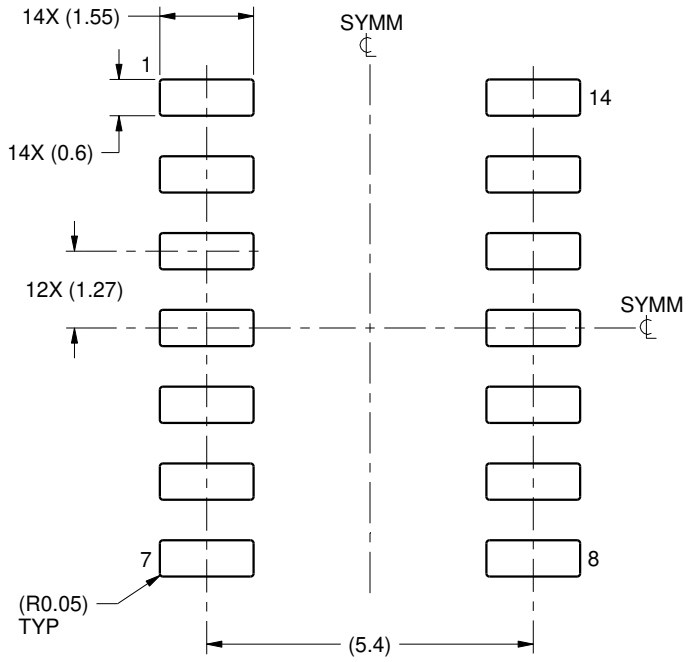
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

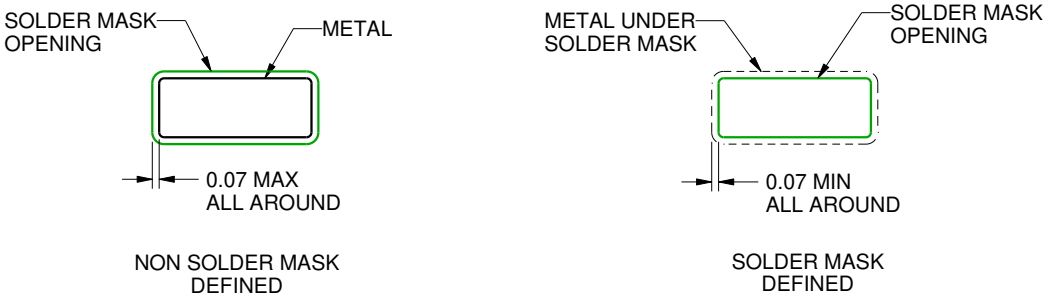



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

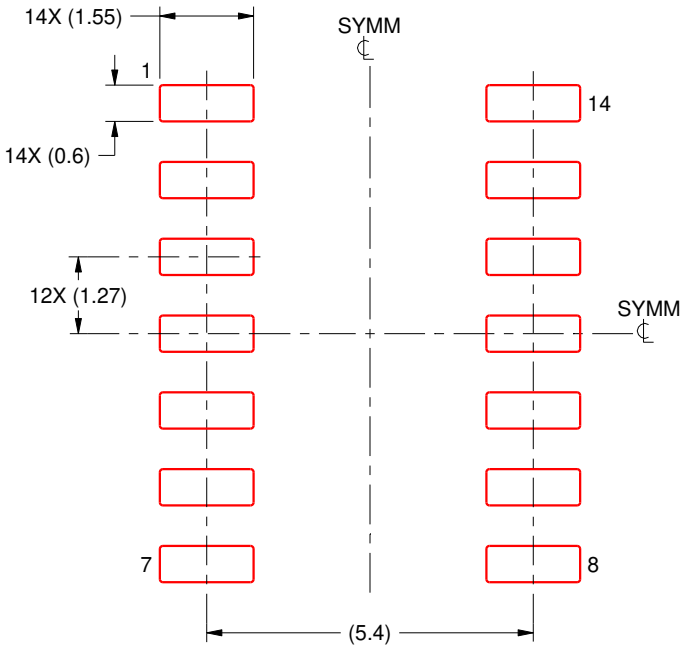
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

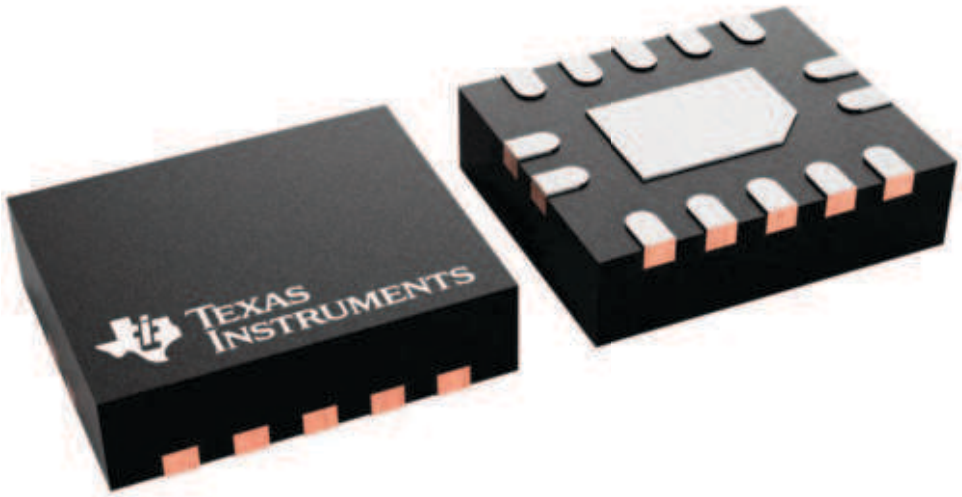
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



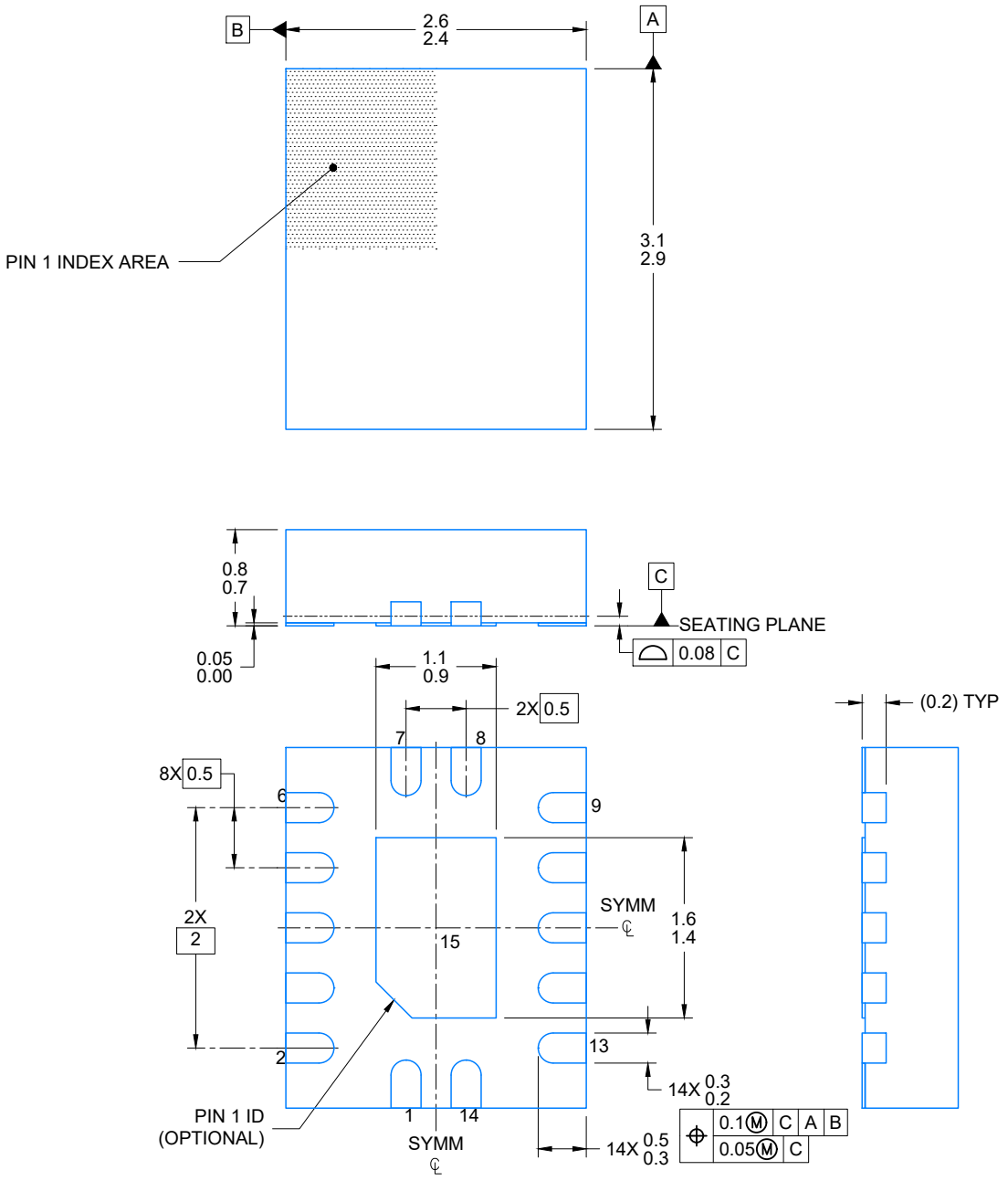

4227145/A

# PACKAGE OUTLINE

## BQA0014A

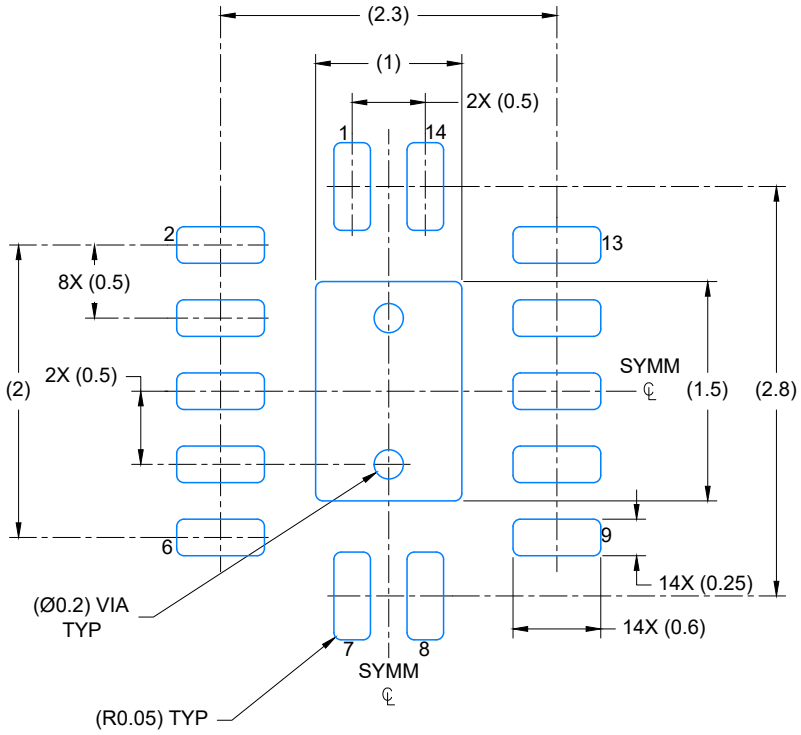
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

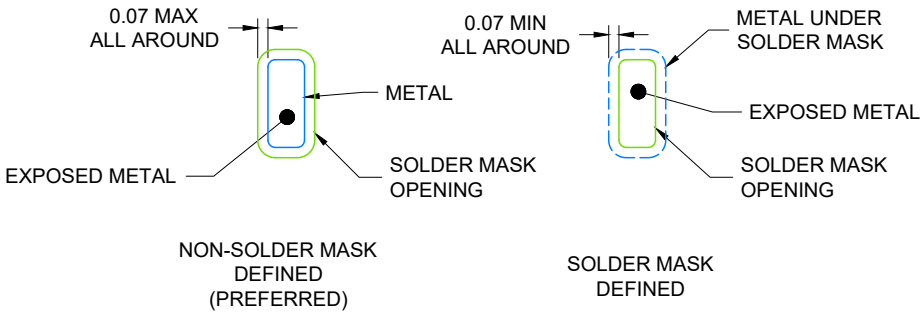



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



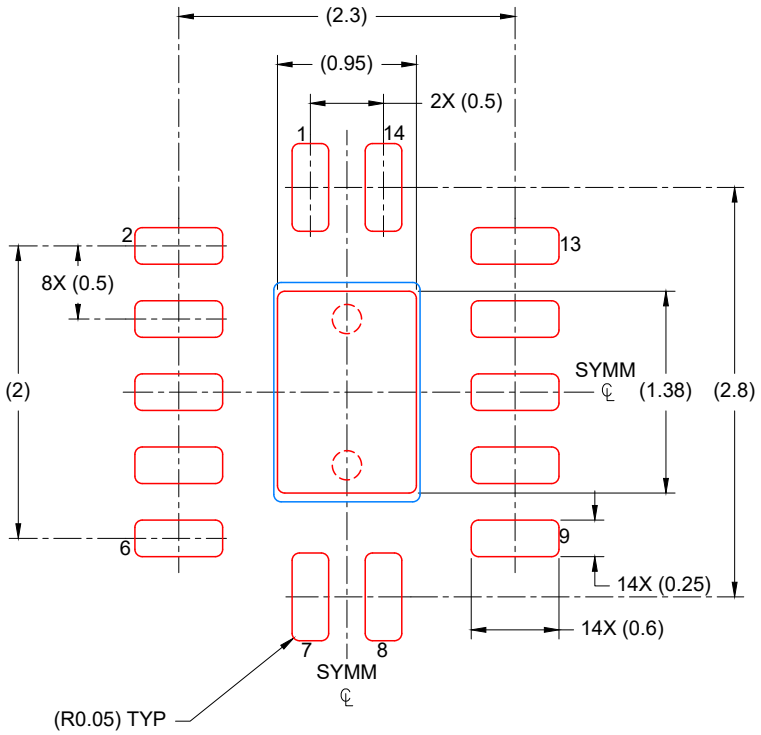

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

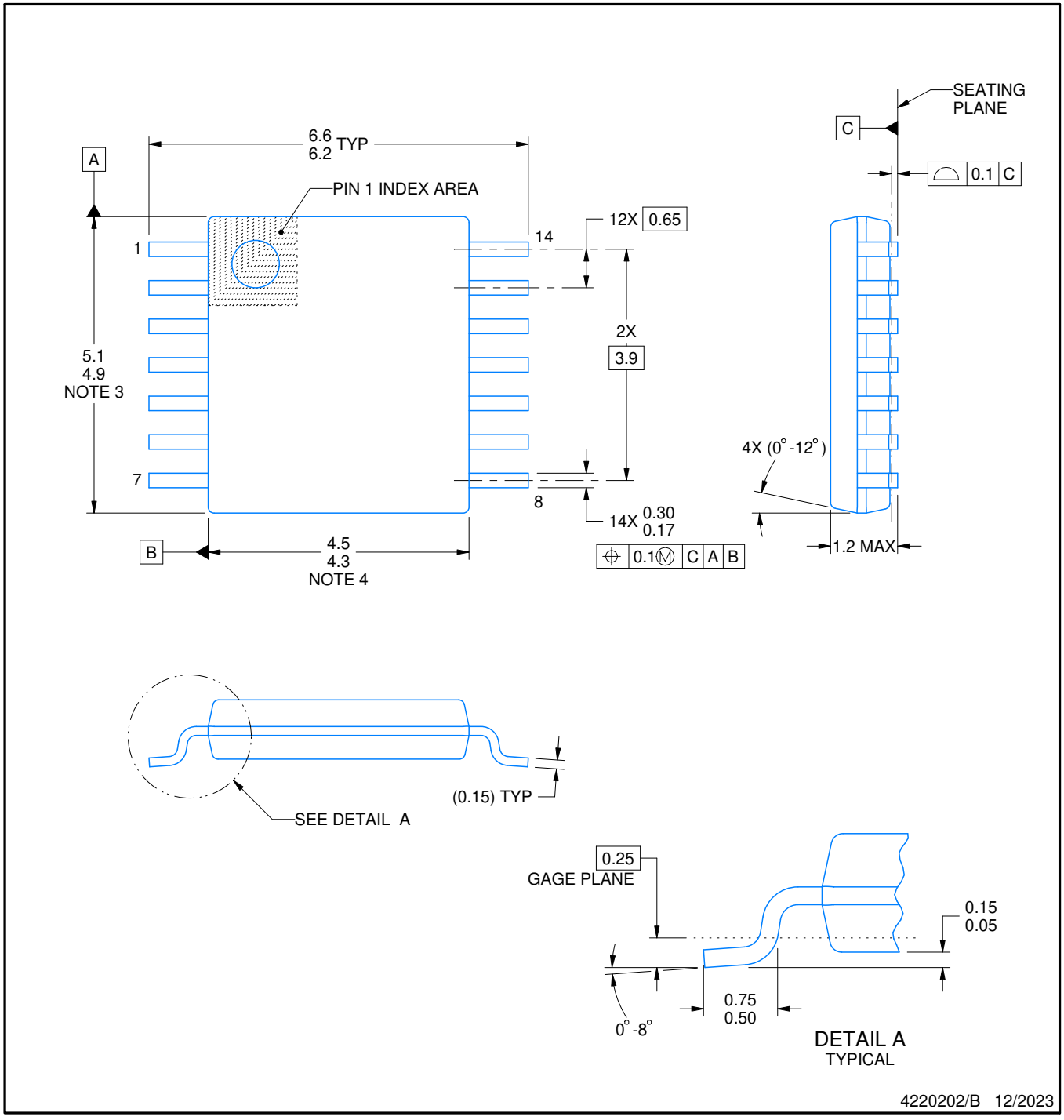
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0014A

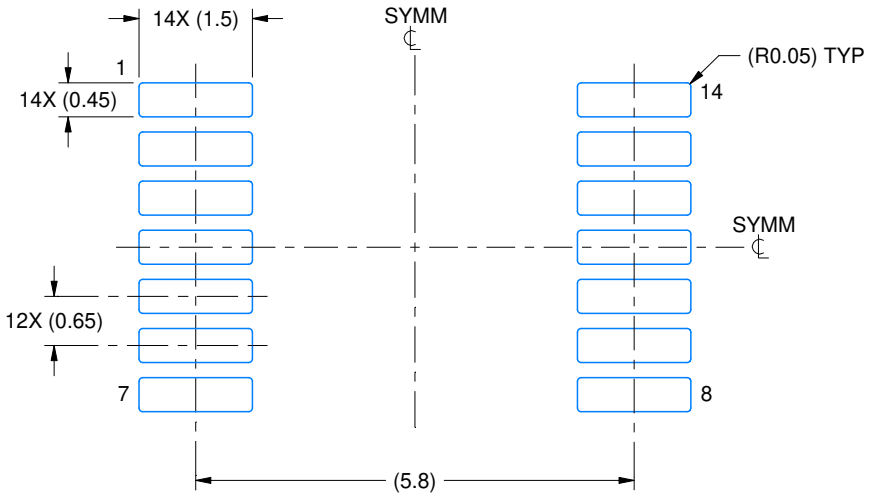
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

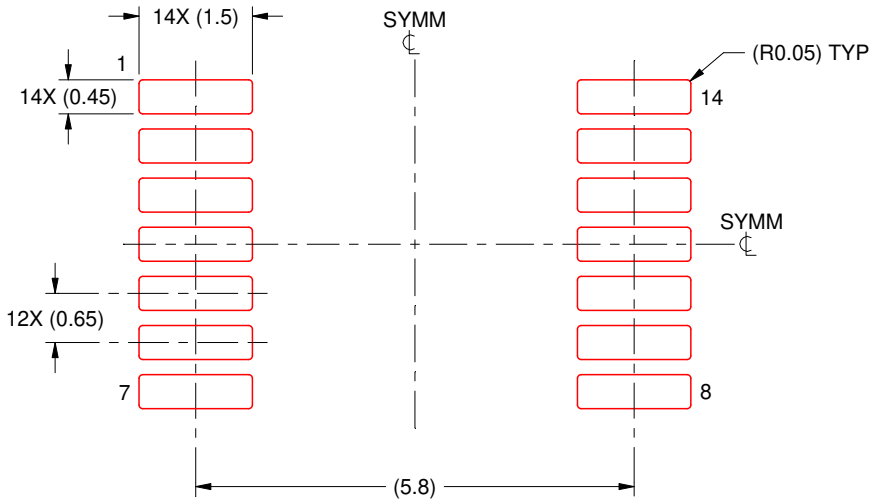
SOLDER MASK DETAILS

SOLDER MASK DEFINED

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025