SN74LVC1G00 Single 2-Input Positive-NAND Gate

1 Features

- Available in the ultra small 0.64mm^2 package (DPW) with 0.5mm pitch
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Provides down translation to V_{CC}
- Max t_{pd} of 3.8ns at 3.3V
- Low power consumption, 10µA max I_{CC}
- ±24mA output drive at 3.3V
- I_{off} Supports live insertion, partial-power-down mode, and back drive protection
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- Embedded PC
- MP3 player/recorder (portable audio)
- Personal Digital Assistant (PDA)
- Power: telecom/Server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

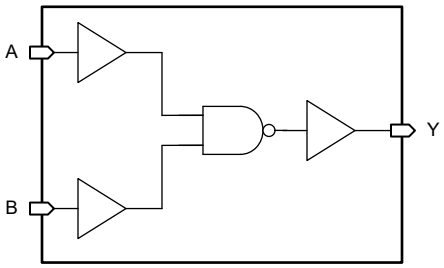
3 Description

The SN74LVC1G00 device is a single 2-input positive NAND gate. This device performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \bar{A} + \bar{B}$ in positive logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC1G00	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 5)	2mm × 2.1mm	2mm × 1.25mm
	DRY (SON, 6)	1.45mm × 1mm	1.45mm × 1mm
	YZP (DSBGA, 5)	1.39mm × 0.89mm	1.39mm × 0.89mm
	DSF (SON, 6)	1mm × 1mm	1mm × 1mm
	DPW (X2SON, 5)	0.8mm × 0.8mm	0.8mm × 0.8mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

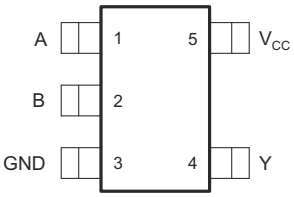
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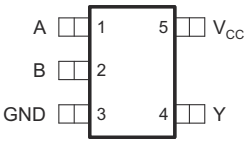
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4 Pin Configuration and Functions

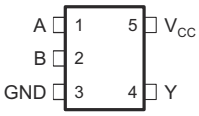
DBV PACKAGE (TOP VIEW)



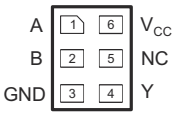
DCK PACKAGE (TOP VIEW)



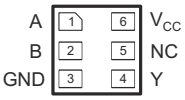
DRL PACKAGE (TOP VIEW)



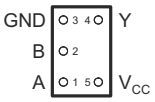
DRY PACKAGE (TOP VIEW)



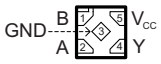
DSF PACKAGE (TOP VIEW)



YZP PACKAGE (BOTTOM VIEW)



DPW PACKAGE (TOP VIEW)



NC – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN				DESCRIPTION
NAME	DBV, DCK, DRL, YZP	DRY, DSF	DPW	
A	1	1	2	Input
B	2	2	1	Input
GND	3	3	3	Ground
NC		5		Not connected
V_{CC}	5	6	5	Power pin
Y	4	4	4	Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	0	2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	0	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC} (1)	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65V to 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W
DCK (SOT-SC70)	5	371	297.5	258.6	195.6	256.2	-	°C/W
DRY (SON)	6	439	277	271	84	271	–	°C/W
YZP (DSBGA)	5	130	54	51	1	50	–	°C/W
DPW (X2SON)	5	340	215	294	41	294	250	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–40°C to 85°C			RECOMMENDED –40°C to 125°C			UNIT
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{OH}		I_{OH} = –100µA	1.65V to 5.5V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –4mA	1.65V	1.2			1.2			
		I_{OH} = –8mA	2.3V	1.9			1.9			
		I_{OH} = –16mA	3V	2.4			2.4			
		I_{OH} = –24mA		2.3			2.3			
		I_{OH} = –32mA	4.5V	3.8			3.8			
V_{OL}		I_{OL} = 100µA	1.65V to 5.5V			0.1			0.1	V
		I_{OL} = 4mA	1.65V			0.45			0.45	
		I_{OL} = 8mA	2.3V			0.3			0.3	
		I_{OL} = 16mA	3V			0.4			0.4	
		I_{OL} = 24mA				0.55			0.55	
		I_{OL} = 32mA	4.5V			0.55			0.55	
I_I	A or B inputs	V_I = 5.5V or GND	0 to 5.5V			±5			±5	µA
I_{off}		V_I or V_O = 5.5V	0			±10			±10	µA
I_{CC}		V_I = 5.5V or GND I_O = 0	1.65V to 5.5V			10			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6V, Other inputs at V_{CC} or GND	3V to 5.5V			500			500	µA
C_i		V_I = V_{CC} or GND	3.3V		4			4		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics, C_L = 15pF

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2.2	7.2	0.9	4.4	0.8	3.8	0.8	3.4	ns

5.7 Switching Characteristics, –40°C to 85°C

over recommended operating free-air temperature range, C_L = 30pF or 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C to 85°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	3.1	9	1.3	5.5	1	4.7	1	4	ns

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5.8 Switching Characteristics, –40°C to 125°C

over recommended operating free-air temperature range, C_L = 30pF or 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	RECOMMENDED –40°C to 125°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	3.1	9.7	1.3	5.8	1	5	1	4.3	ns

5.9 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10MHz	22	22	23	25	pF

5.10 Typical Characteristics

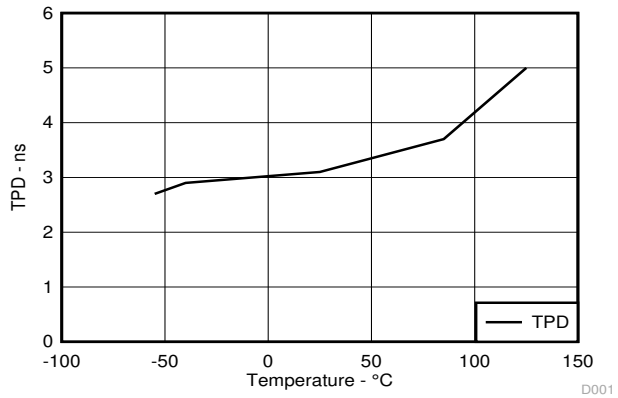


Figure 5-1. TPD Across Temperature at 3.3V Vcc

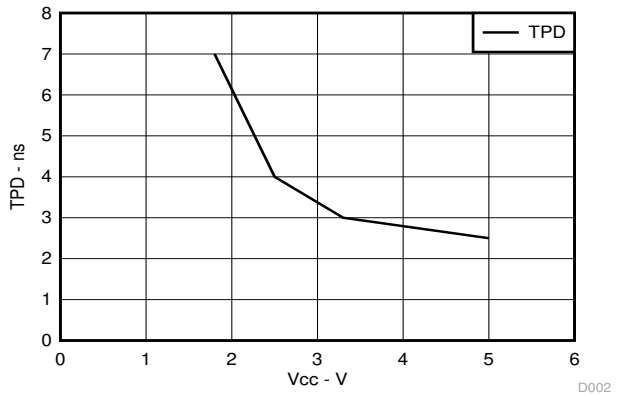
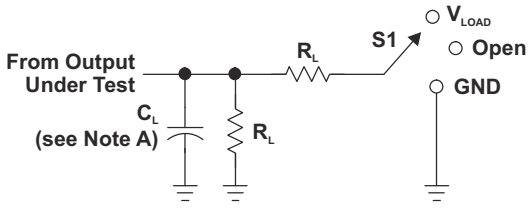


Figure 5-2. TPD Across Vcc at 25°C

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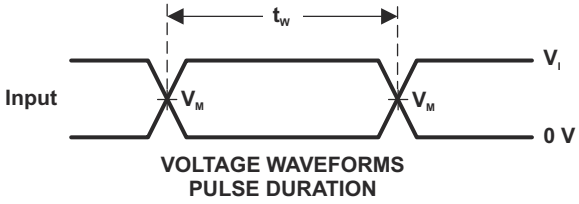
6 Parameter Measurement Information



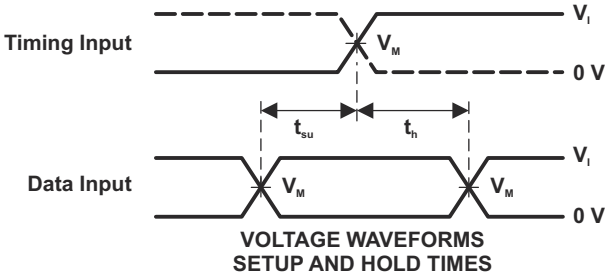
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

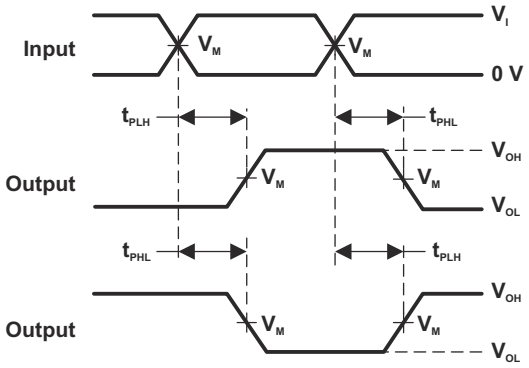
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



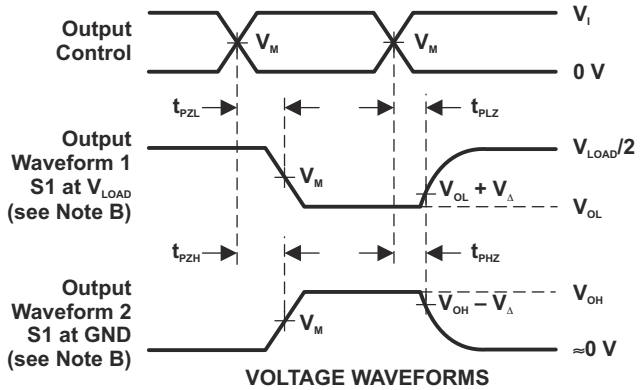
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

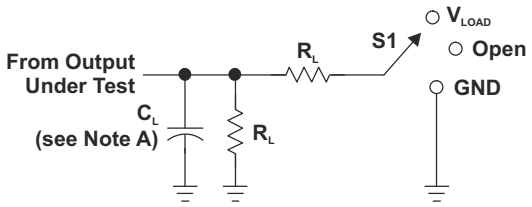


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

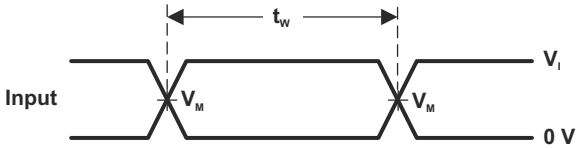
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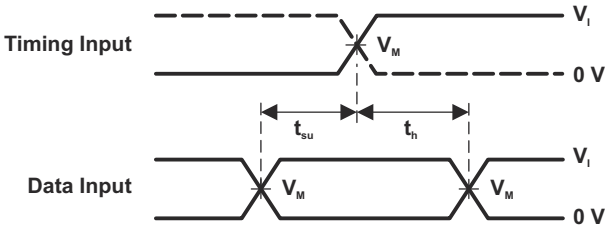
LOAD CIRCUIT

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t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

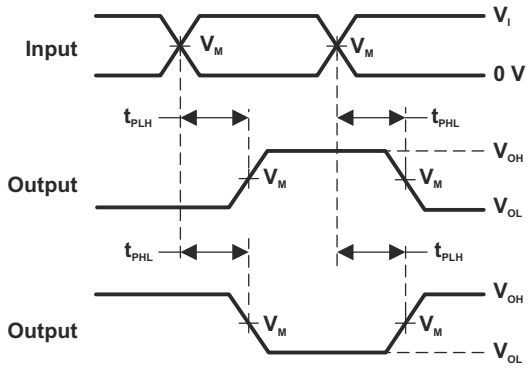
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



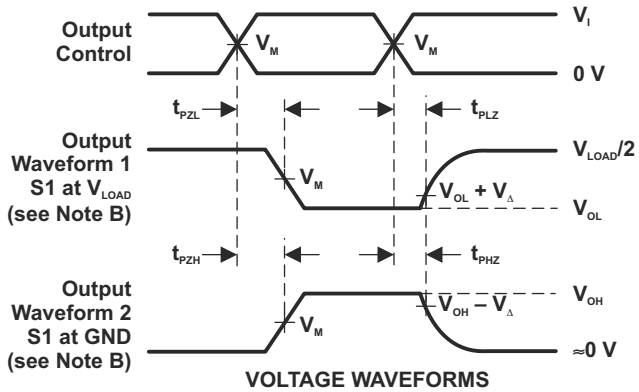
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
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C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
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F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

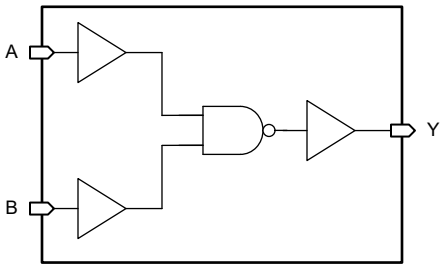
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7 Detailed Description

7.1 Overview

This device is a 2-input NAND Gate which performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

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CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

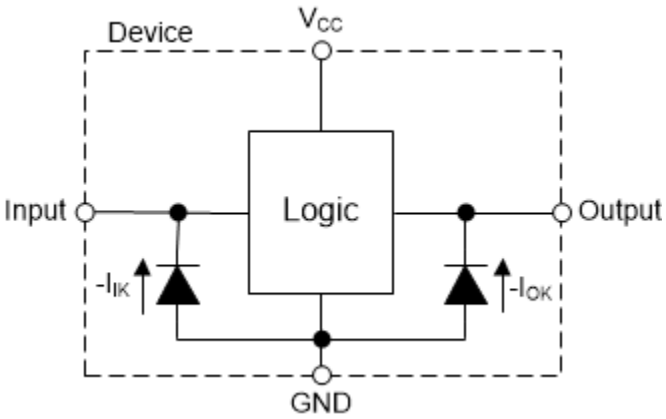


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.5 Over-Voltage Tolerant Inputs

The SN74LVC1G00 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
A	**B**	**Y**
H	H	L
L	X	H
X	L	H

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in *Figure 8-1*. The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74LVC1G00 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

8.2 Typical Application

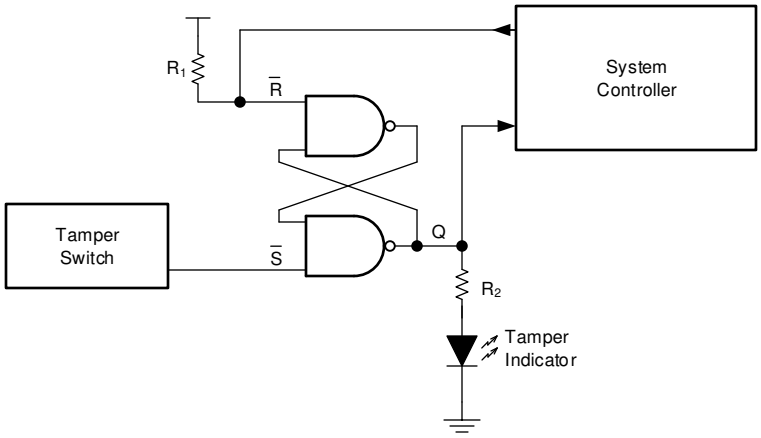


Figure 8-1. Typical application block diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC1G00 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G00 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

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The SN74LVC1G00 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74LVC1G00 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G00 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G00 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74LVC1G00 to the receiving device.

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3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

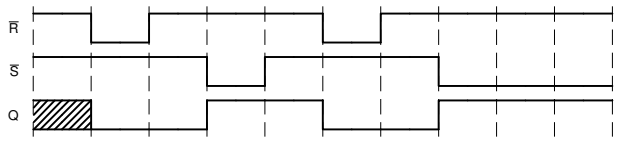


Figure 8-2. Application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC1G00, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

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8.4.2 Layout Example

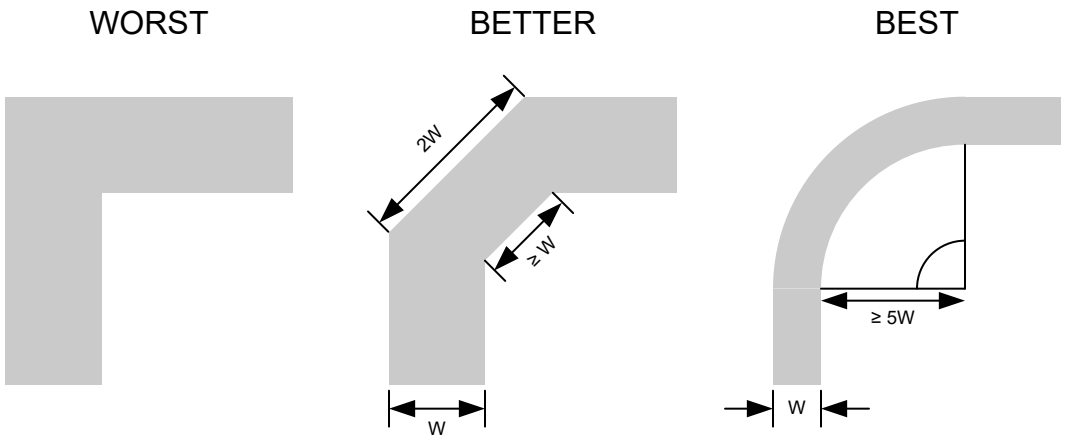


Figure 8-3. Example Trace Corners for Improved Signal Integrity

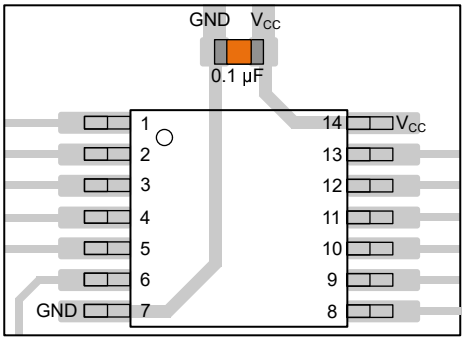


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

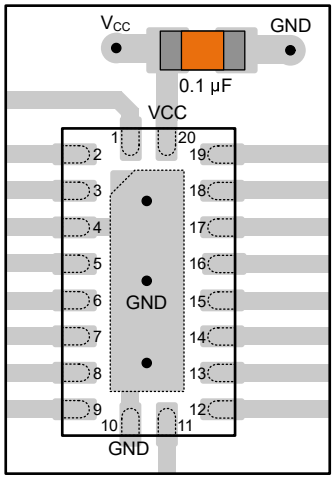


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

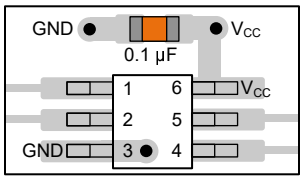


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

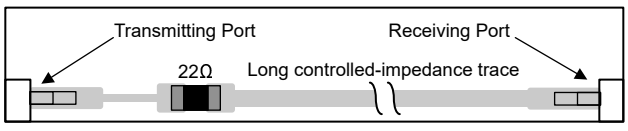


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 1, 2014 to August 12, 2026 (from Revision AB (April 2014) to Revision AC (August 2026)) **Page**

- Updated *Device Information* table to include body and package dimensions..... 1
- Changed *Handling Ratings* to *ESD Ratings* 4
- Moved *Storage temperature range* from *Handling Ratings* to *Absolute Maximum Ratings* 4
- Updated format for *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 264.4°C/W..... 5
- Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W..... 5

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- Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371°C/W.....5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W.....5
- Changed Junction-to-board characterization value for DCK package from: 65°C/W to: 258.6°C/W.....5
- Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W.....5
- Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W.....5
- Removed redundant t_{pd} specification from *Switching Characteristics, –40°C to 125°C* 7
- Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....14
- Updated *Overview*, *Application and Implementation*, *Device and Documentation Support* sections to extend detailed feature descriptions and more detailed information. 16

Changes from Revision AA (March 2014) to Revision AB (April 2014) **Page**

- Updated Handling Ratings table. 4
- Added Thermal Information table. 5
- Added Typical Characteristics. 7
- Added Application and Implementation section. 16
- Added Power Supply Recommendations section. 16
- Added Layout section. 16

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G00DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C005, C00F, C00J, C00K, C00R) (C00H, C00P, C00S)
SN74LVC1G00DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C005, C00F, C00J, C00K, C00R) (C00H, C00P, C00S)
SN74LVC1G00DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C005, C00F, C00J, C00K, C00R) (C00H, C00P, C00S)
SN74LVC1G00DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C00F
SN74LVC1G00DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C00F
SN74LVC1G00DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C00F
SN74LVC1G00DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C005, C00F, C00J, C00K, C00R) (C00H, C00P, C00S)
SN74LVC1G00DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C005, C00F, C00J, C00K, C00R) (C00H, C00P, C00S)
SN74LVC1G00DBVTE4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C00F
SN74LVC1G00DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C00F
SN74LVC1G00DBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C00F
SN74LVC1G00DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CA5, CAF, CAJ, CAK, CAR) (CAH, CAP, CAS)
SN74LVC1G00DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CA5, CAF, CAJ, CAK, CAR) (CAH, CAP, CAS)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G00DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CA5, CAF, CAJ, CAK, CAR) (CAH, CAP, CAS)
SN74LVC1G00DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA5 CAS
SN74LVC1G00DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA5 CAS
SN74LVC1G00DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA5 CAS
SN74LVC1G00DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA5 CAS
SN74LVC1G00DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CA5, CAF, CAJ, CAK, CAR) (CAH, CAP, CAS)
SN74LVC1G00DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA5, CAF, CAJ, CAK, CAR) (CAH, CAP, CAS)
SN74LVC1G00DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA5 CAS
SN74LVC1G00DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA5 CAS
SN74LVC1G00DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H4
SN74LVC1G00DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H4
SN74LVC1G00DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CA7, CAR)
SN74LVC1G00DRLR.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CA7, CAR)
SN74LVC1G00DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CA7, CAR)
SN74LVC1G00DRY2	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DRY2.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DSF2	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DSF2.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G00DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA
SN74LVC1G00YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CA7, CAN)
SN74LVC1G00YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CA7, CAN)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G00 :

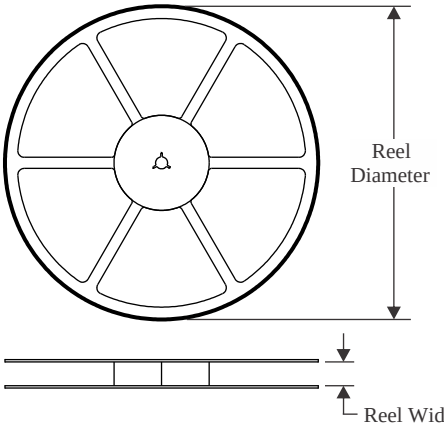
- Enhanced Product : SN74LVC1G00-EP

NOTE: Qualified Version Definitions:

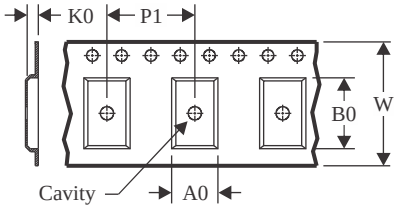
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

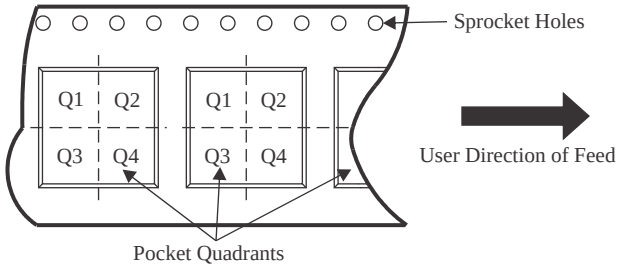


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

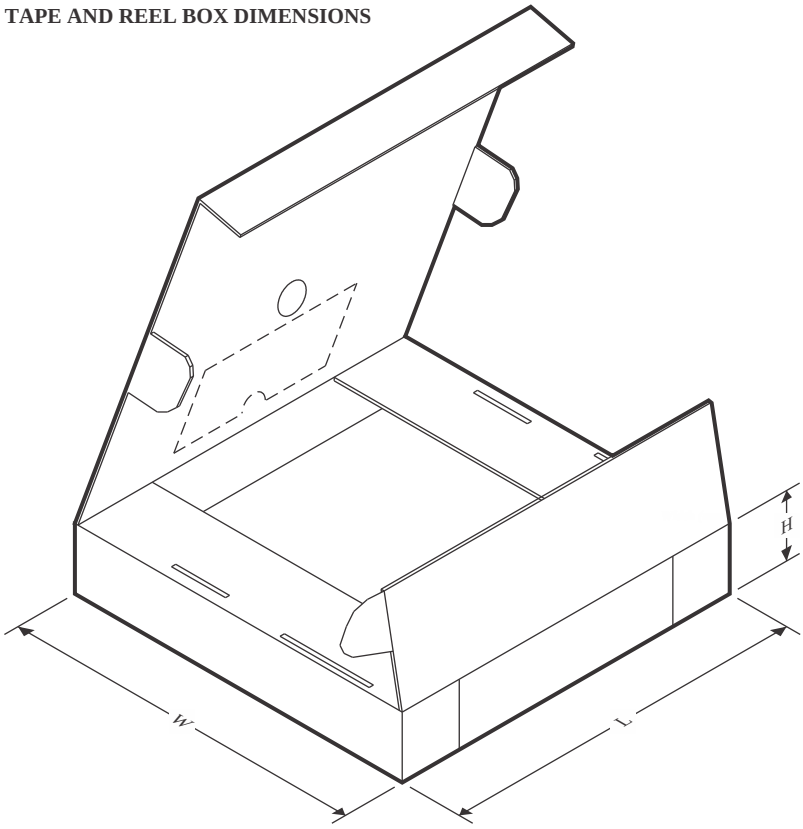


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G00DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G00DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G00DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G00DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G00DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G00DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G00DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G00DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G00DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G00DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G00DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G00DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G00DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G00DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G00DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G00DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G00DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G00DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G00DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G00DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74LVC1G00DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G00DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
SN74LVC1G00DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74LVC1G00DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G00DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74LVC1G00DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G00YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G00DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G00DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G00DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G00DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G00DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G00DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G00DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G00DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G00DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G00DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G00DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G00DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G00DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G00DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G00DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G00DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G00DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G00DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G00DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G00DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G00DSF2	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G00DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G00DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G00DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74LVC1G00DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G00YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

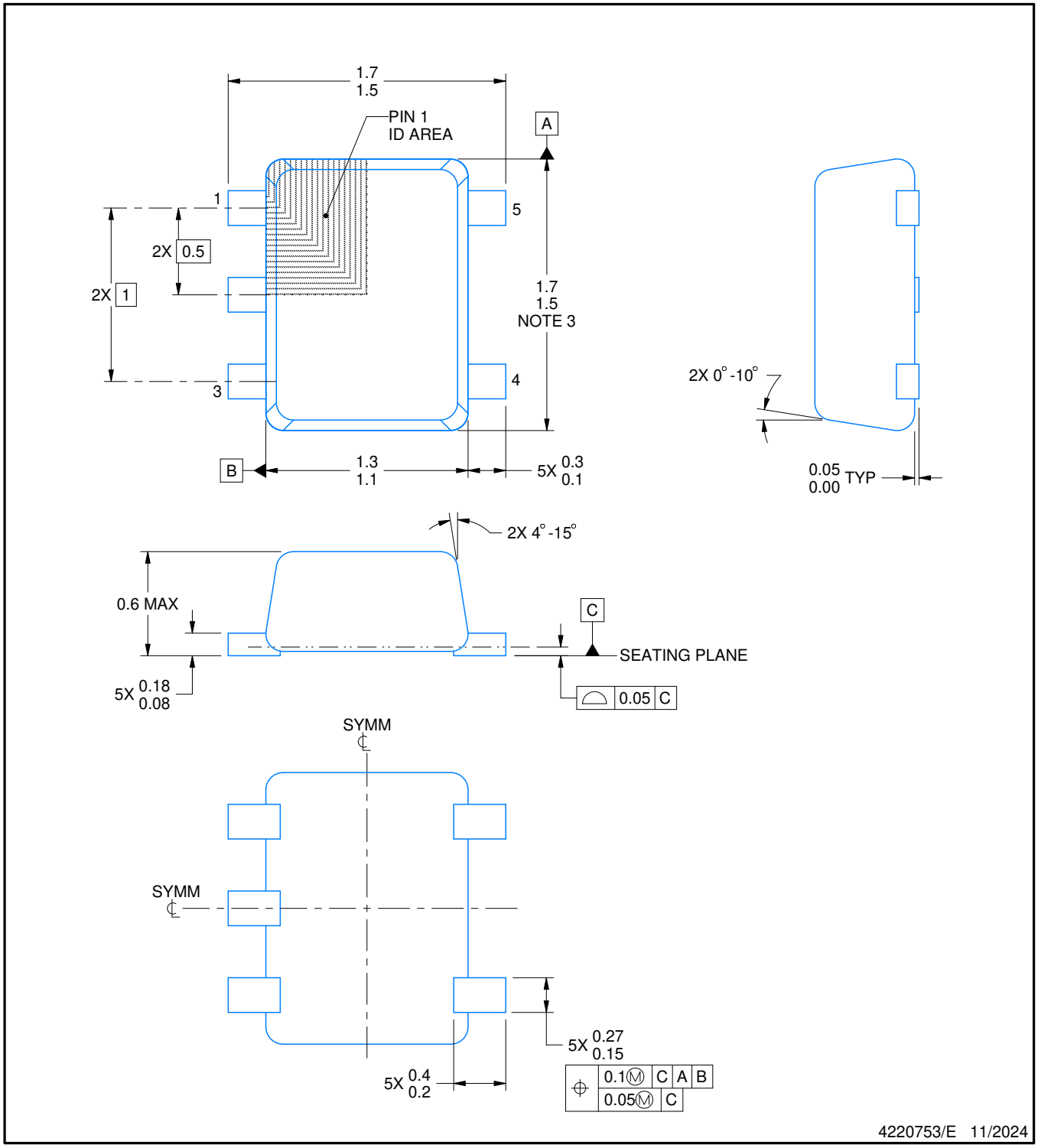
DRL0005A



PACKAGE OUTLINE

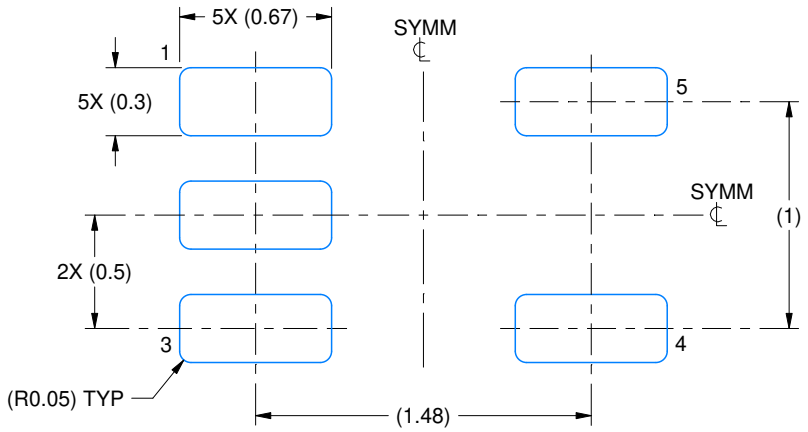
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

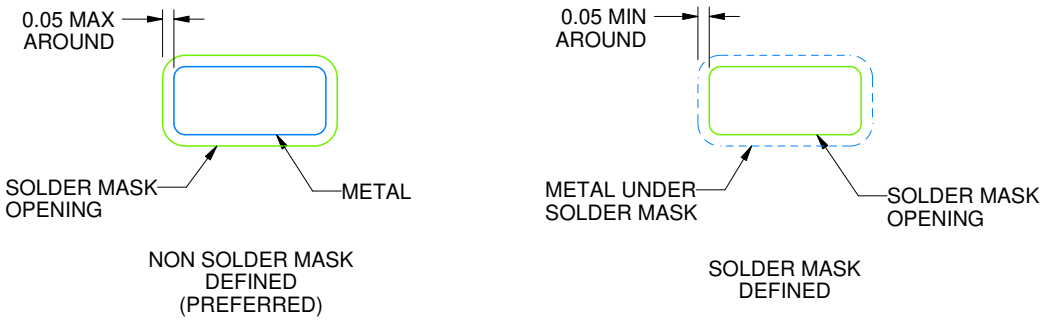


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

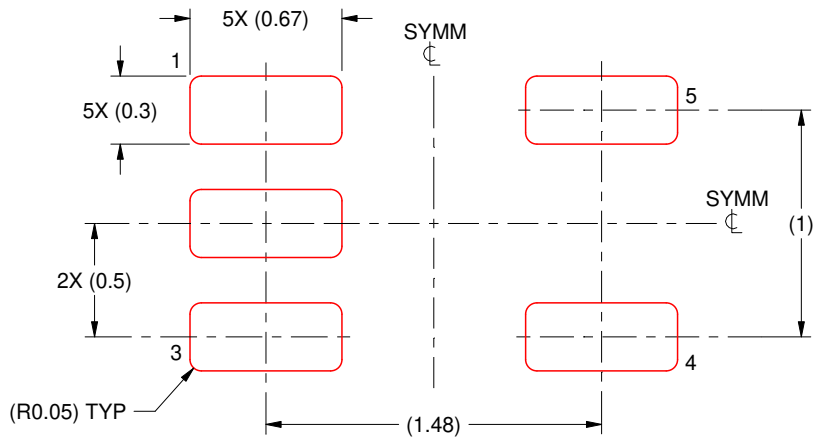


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



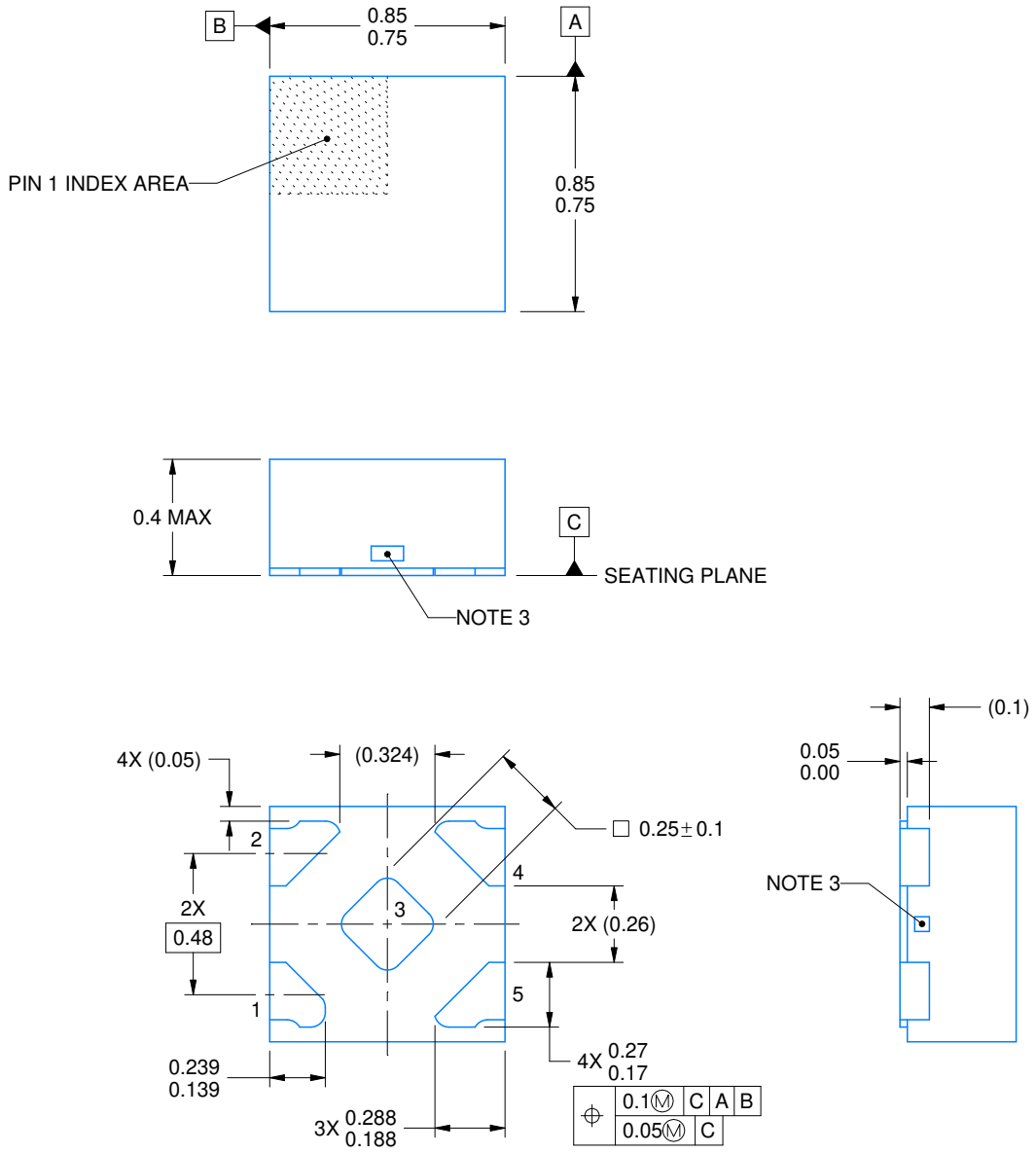
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

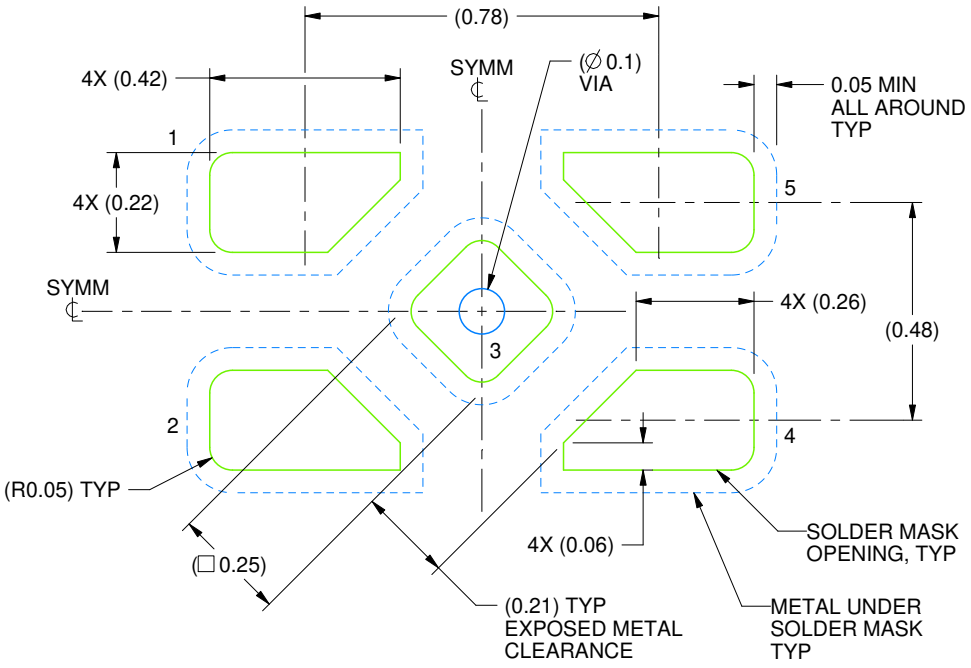
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

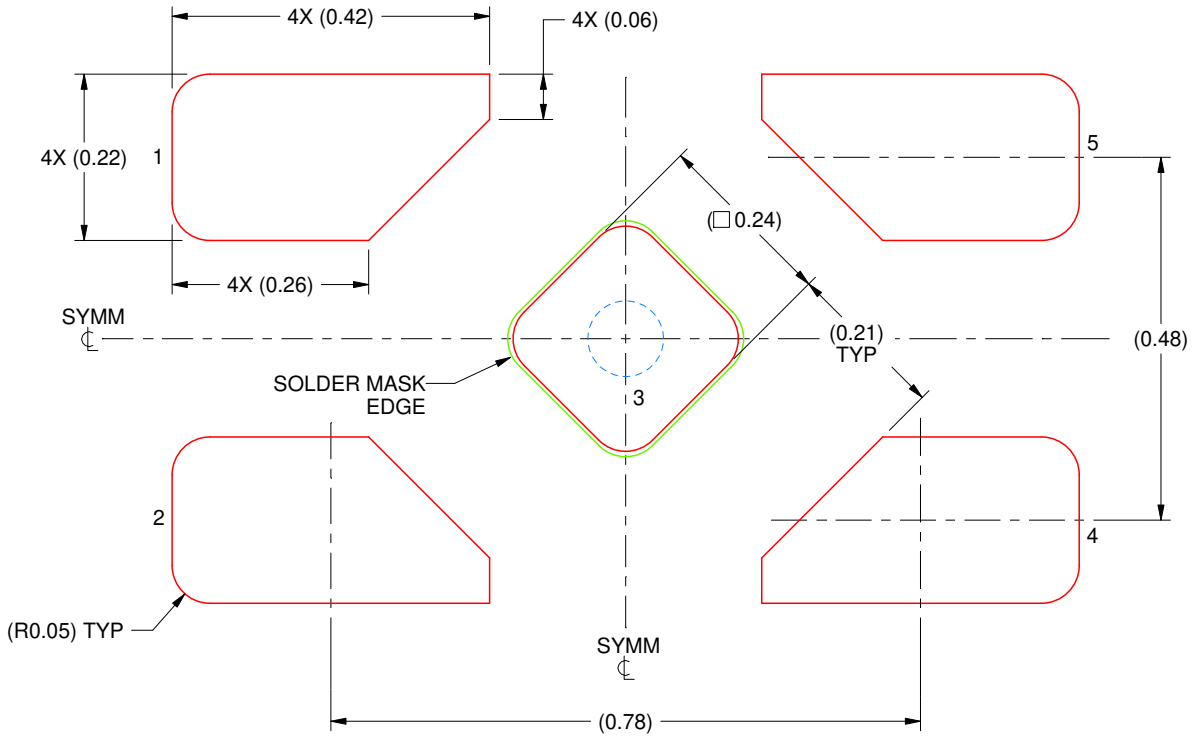


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

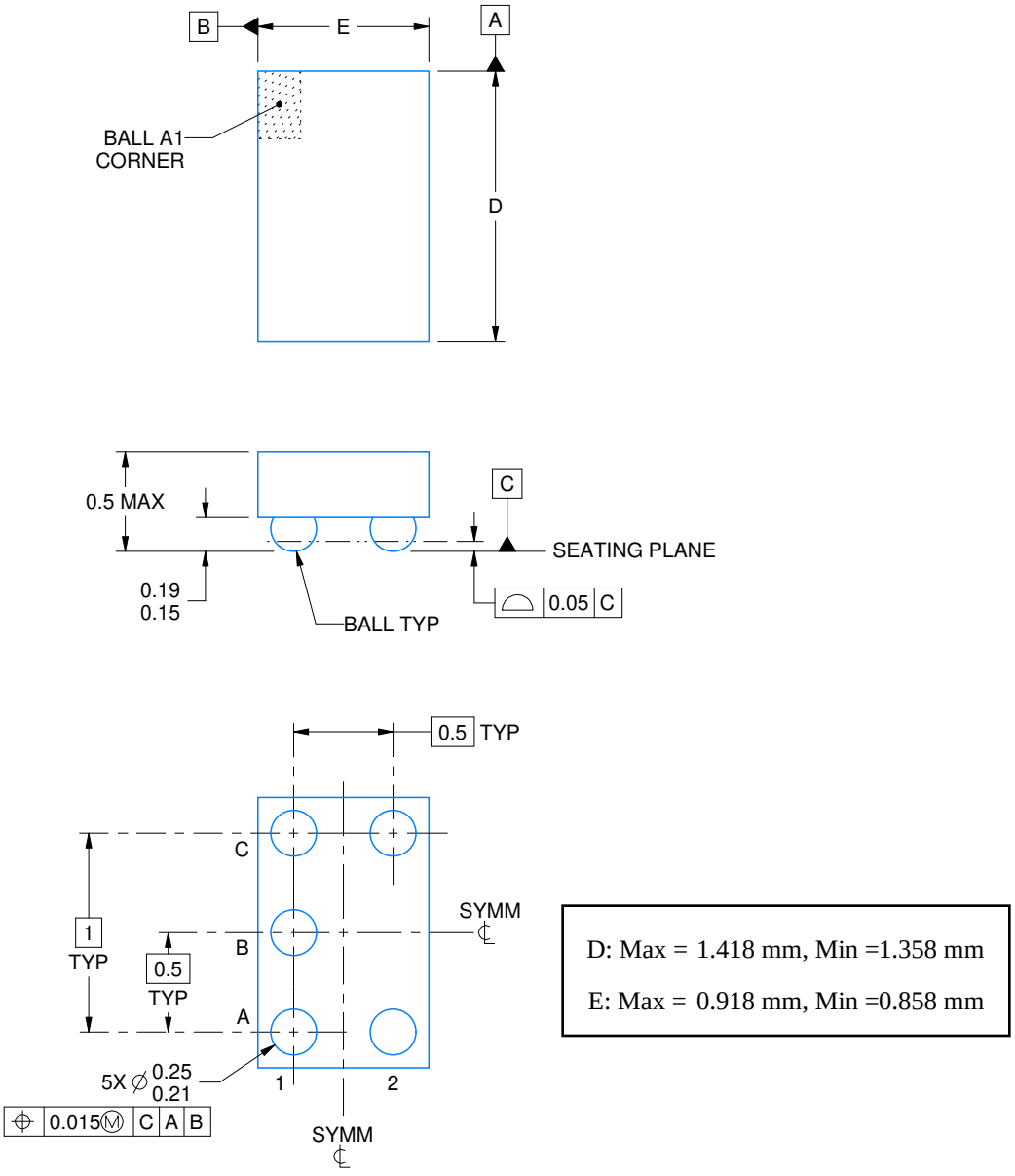
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



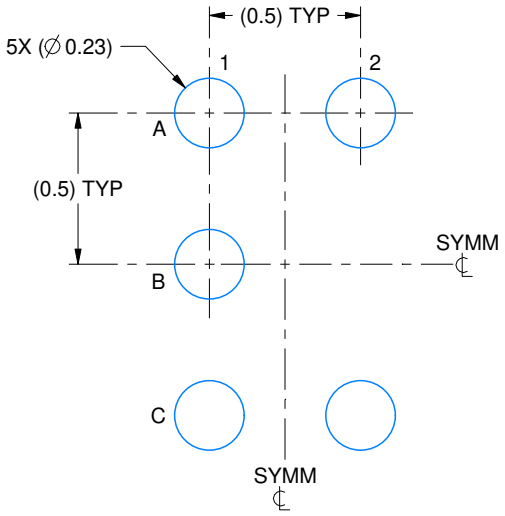
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

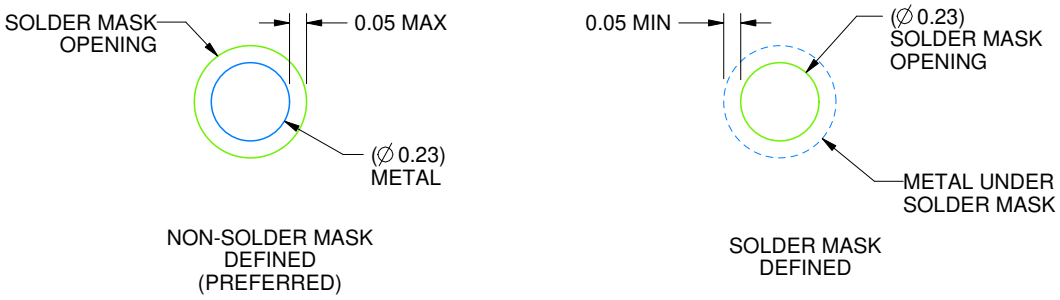
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

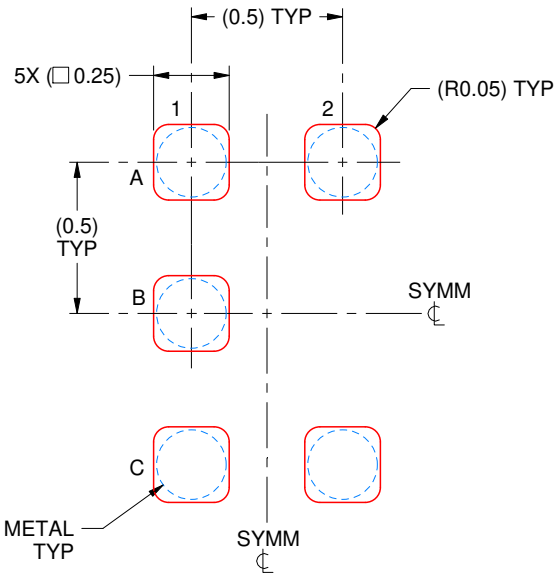


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

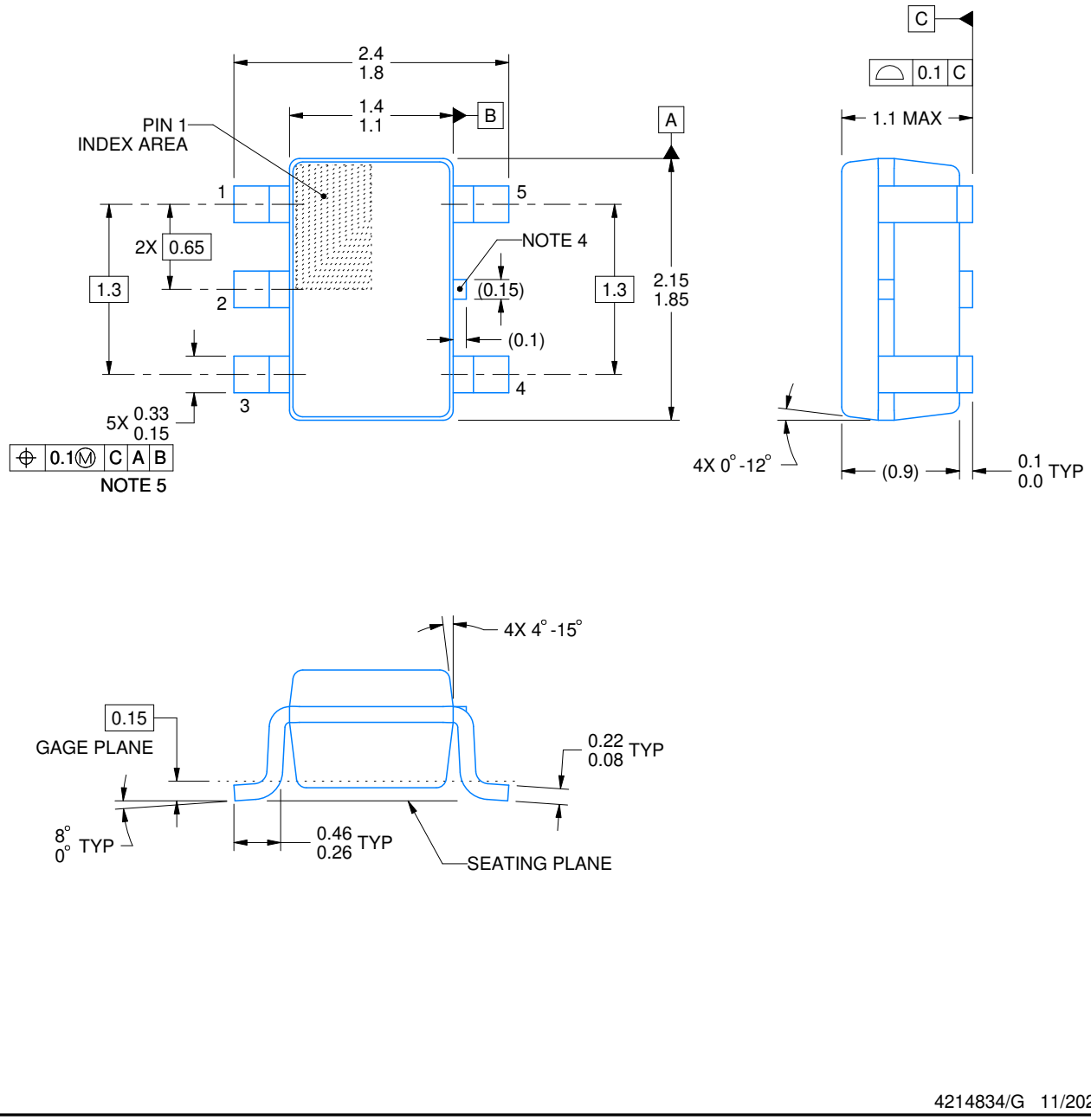
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

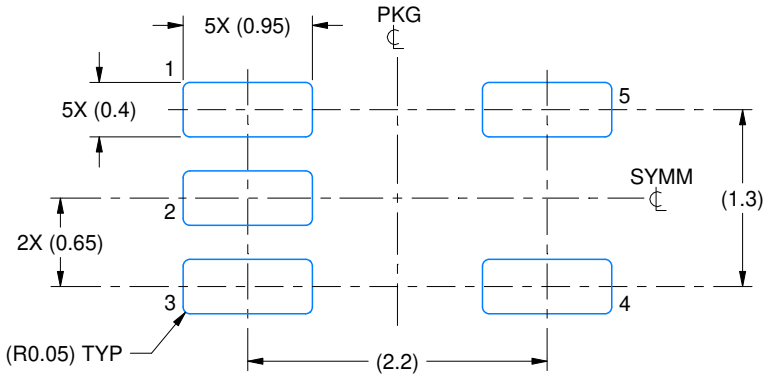
SMALL OUTLINE TRANSISTOR



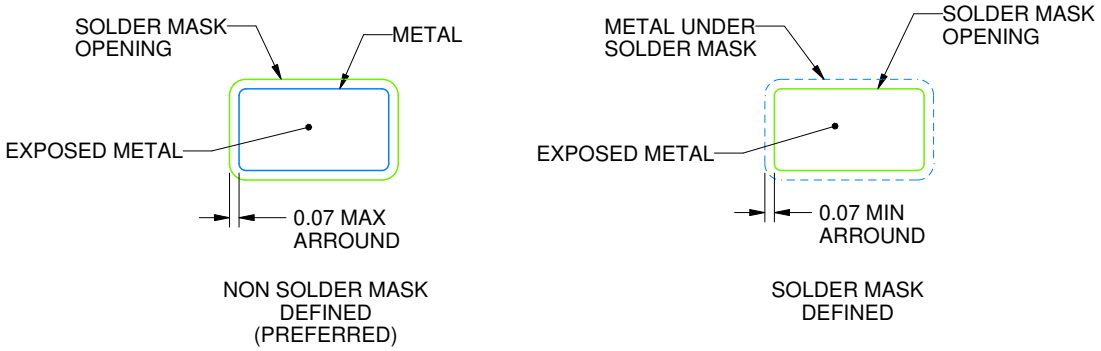
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

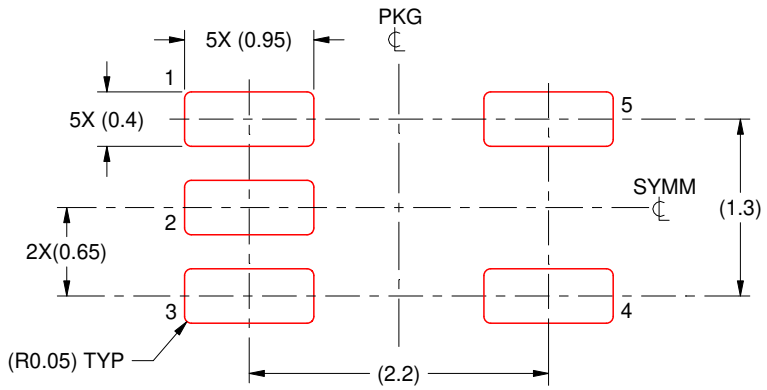


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

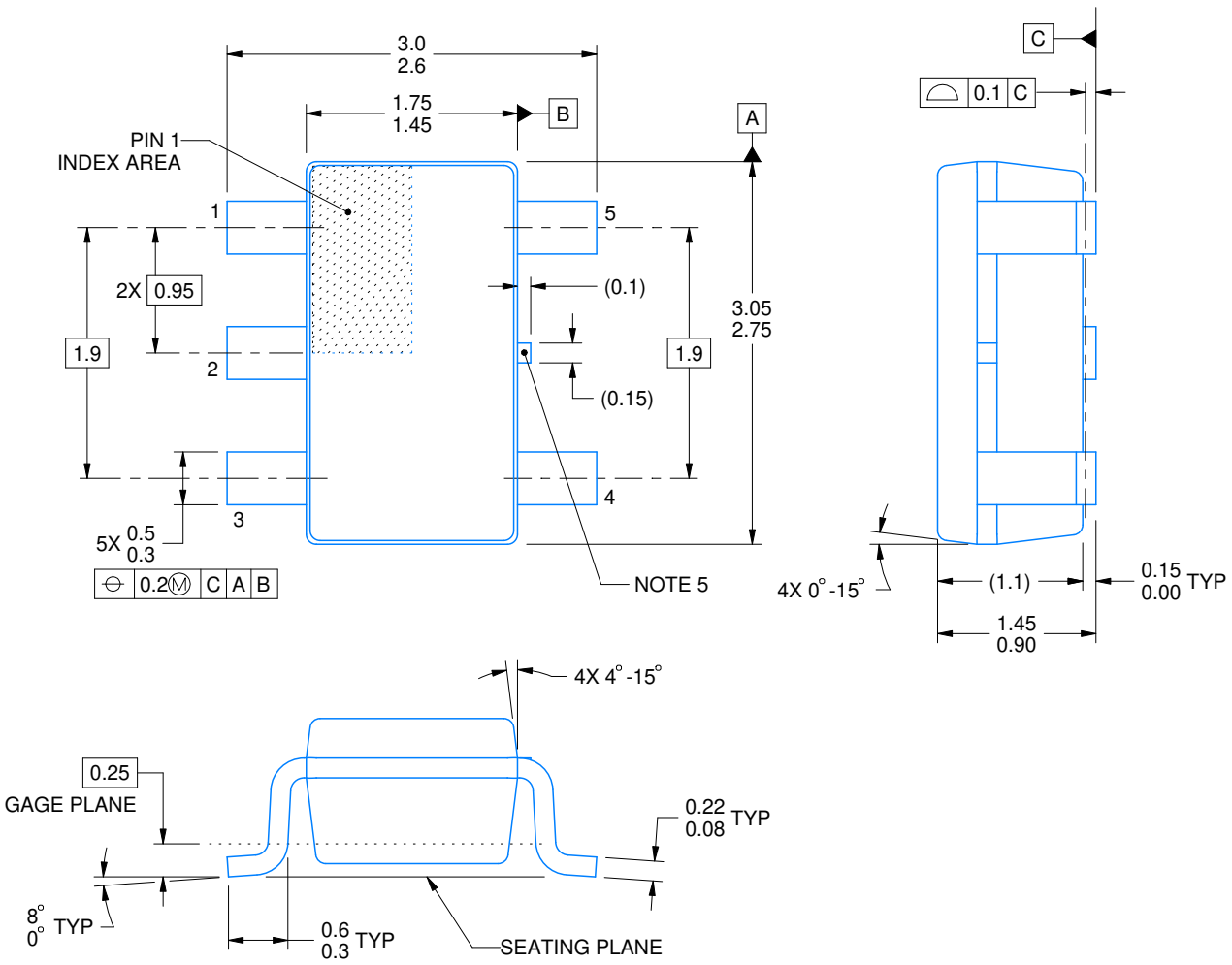
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

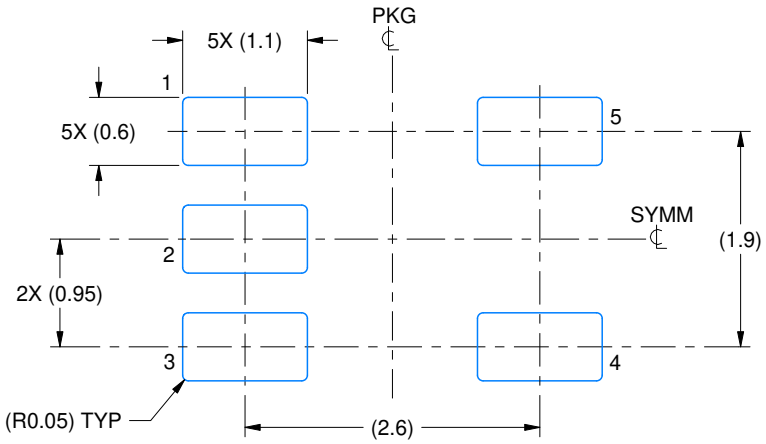
SMALL OUTLINE TRANSISTOR



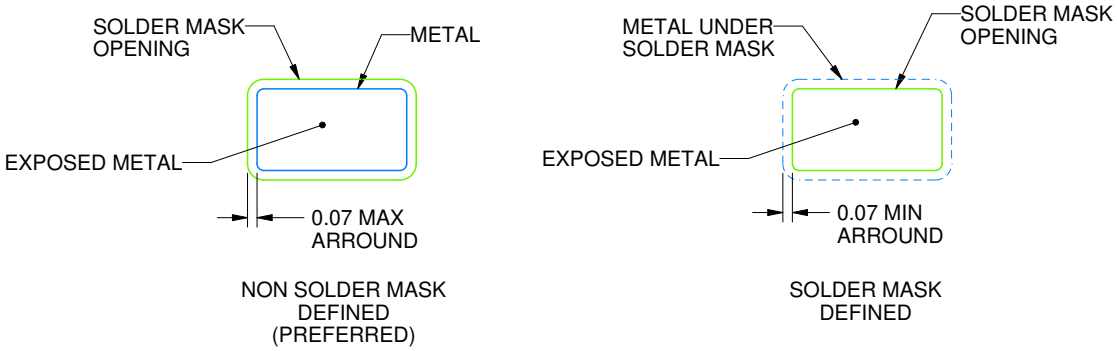
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

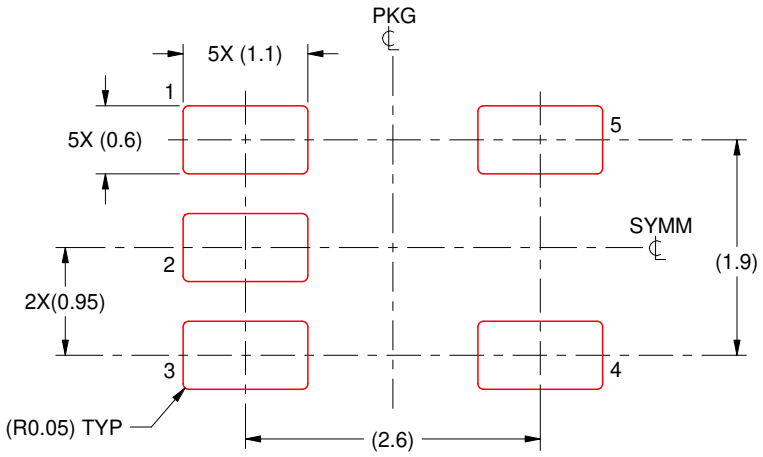


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



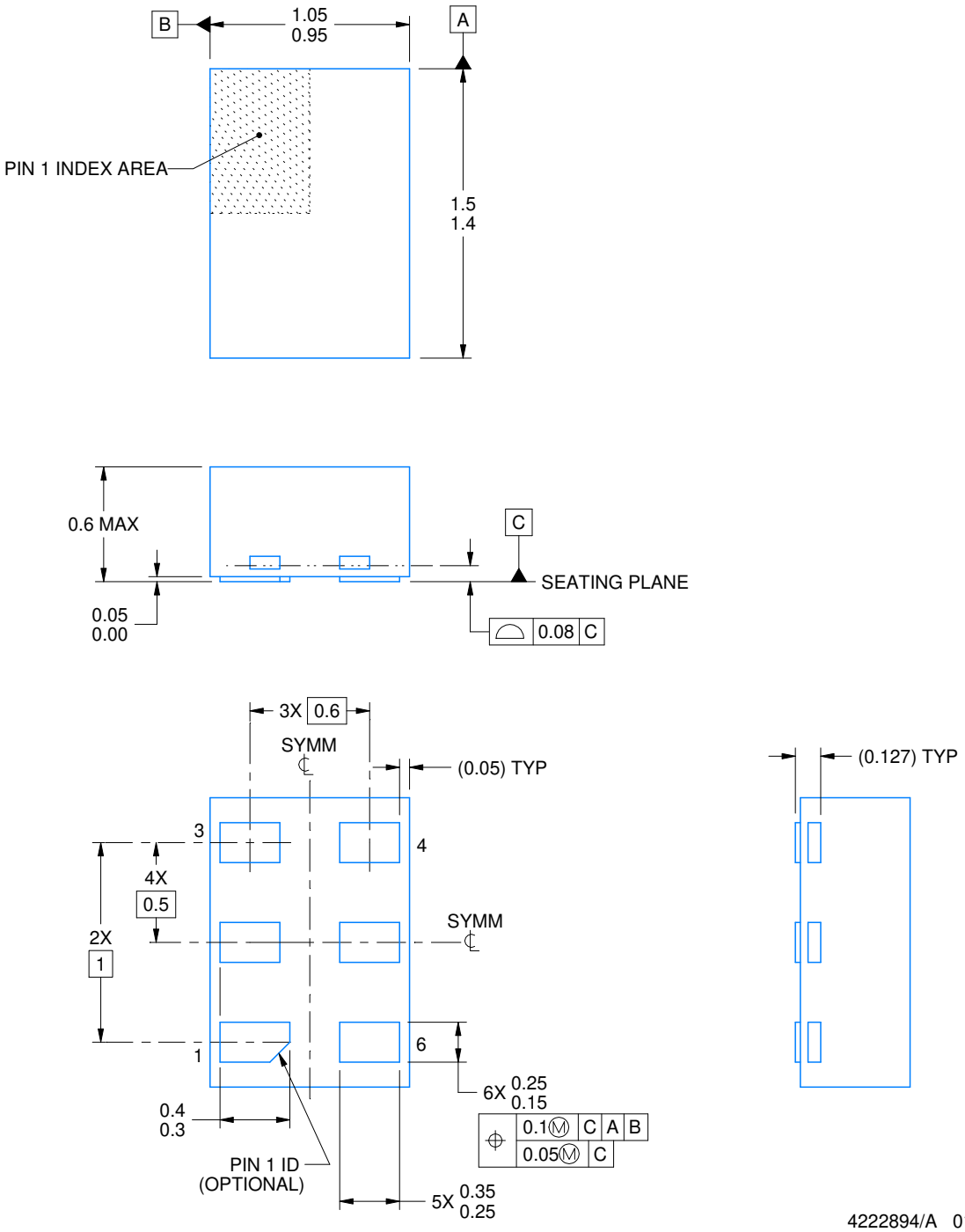
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006A

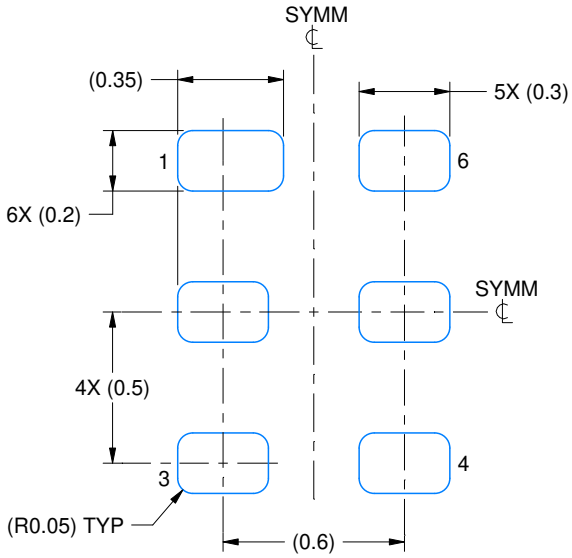
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

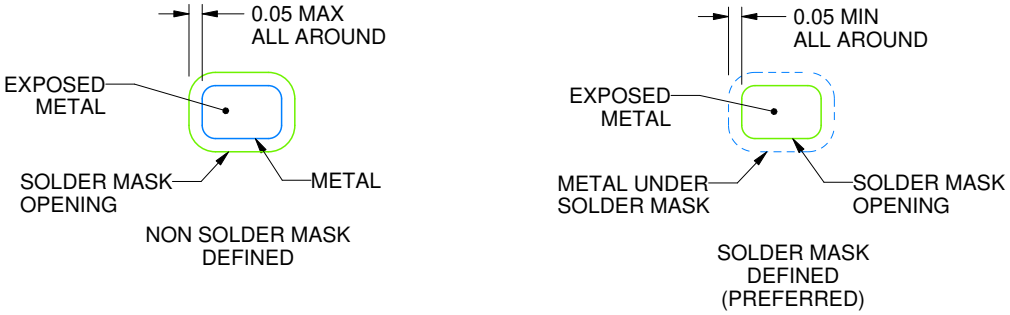


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

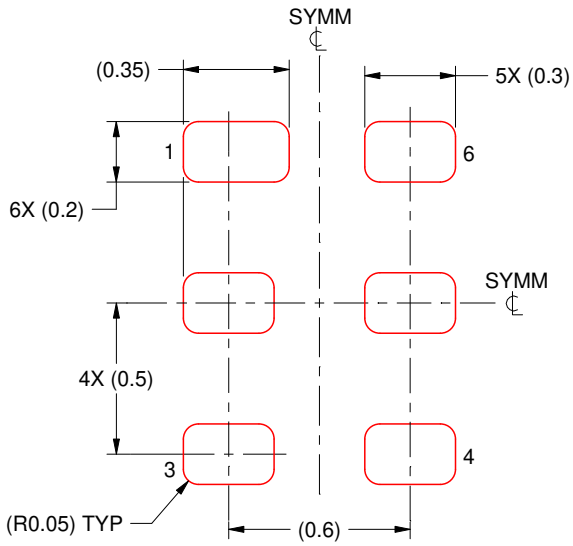
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

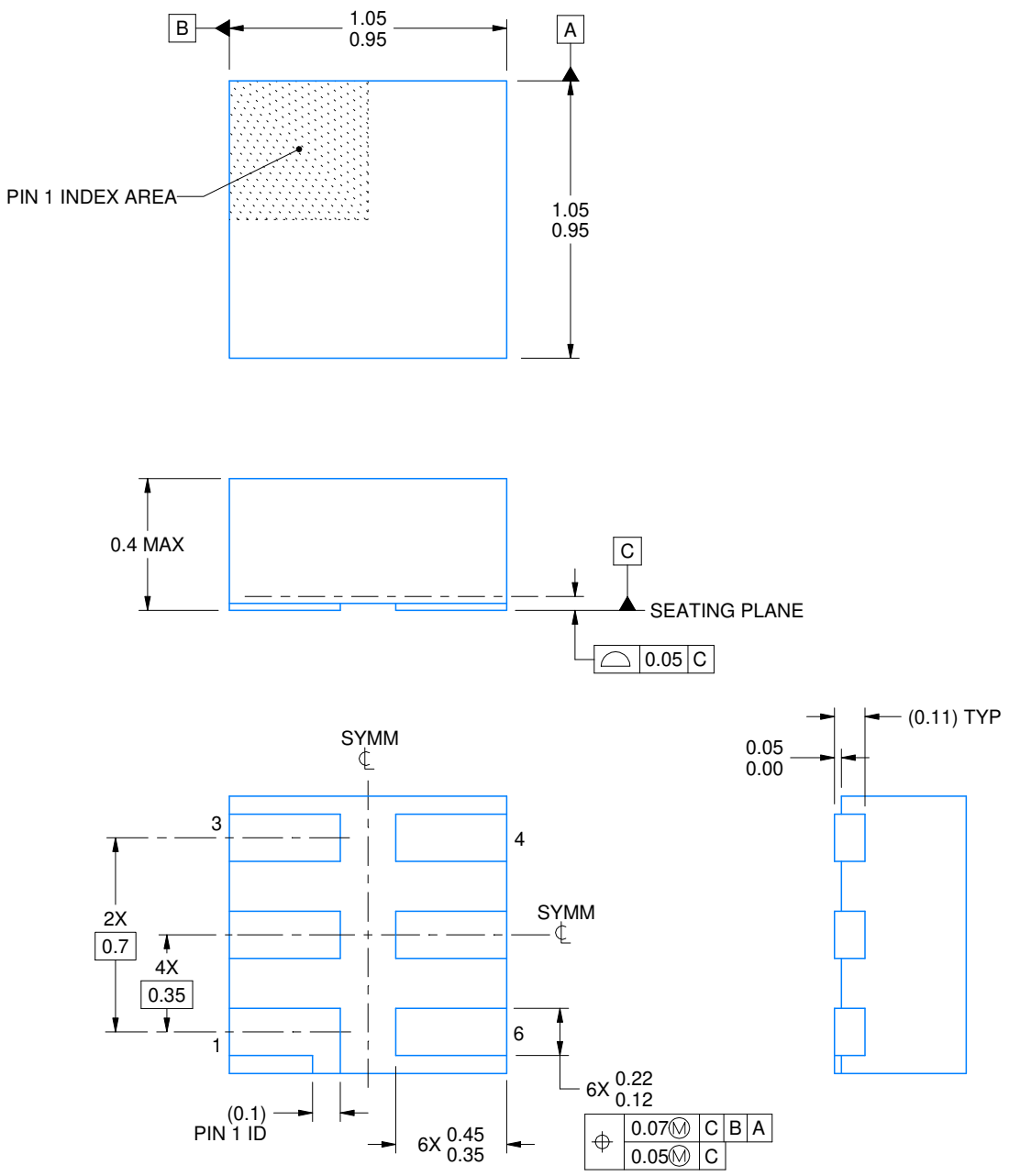
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

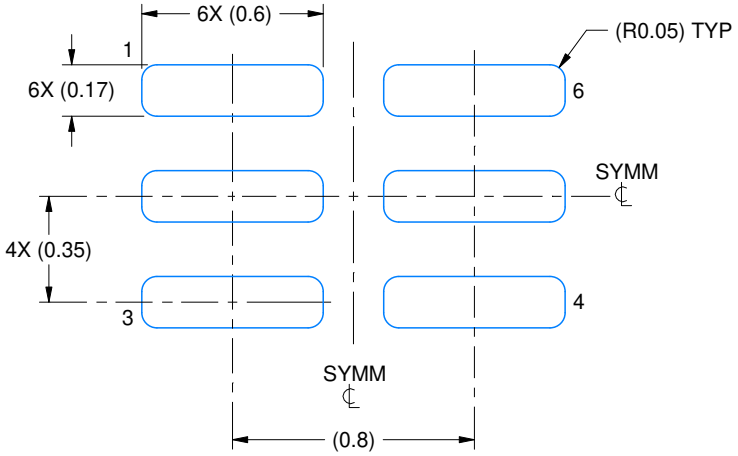
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

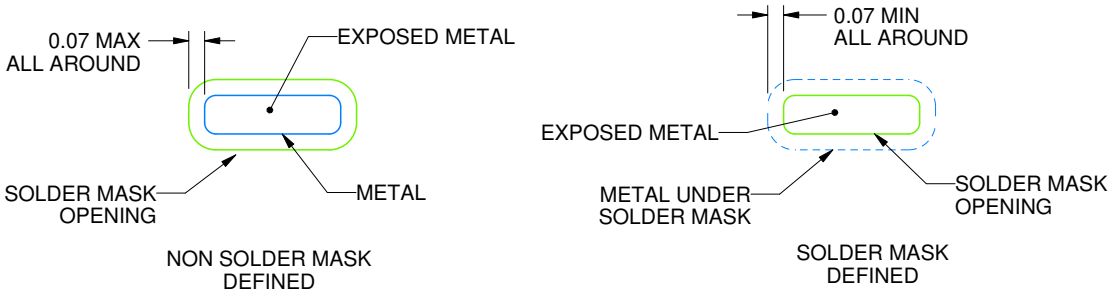


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

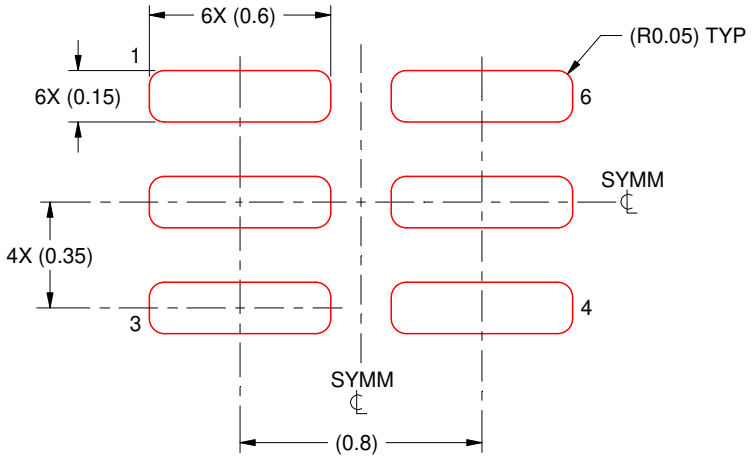
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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