SN74LVC1G123 Single Retriggerable Monostable Multivibrator With Schmitt-Trigger Inputs

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5V V_{CC} Operation
- Inputs Accept Voltages to 5.5V
- Max t_{pd} of 8ns at 3.3V
- Supports Mixed-Mode Voltage Operation on All Ports
- Supports Down Translation to V_{CC}
- Schmitt-Trigger Circuitry on $\overline{A}$ and B Inputs for Slow Input Transition Rates
- Edge Triggered From Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Glitch-Free Power-Up Reset on Outputs
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000V Human-Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop PCs or Notebook PCs
- Digital Radio and Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Attached Storage (NAS)
- Personal Digital Assistant (PDA)
- Server PSU
- Solid-State Drive (SSD): Client and Enterprise
- Video Analytics Servers
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC1G123 device is a single retriggerable monostable multivibrator designed for 1.65V to 5.5V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

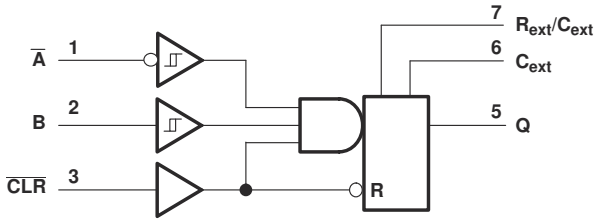
The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$ and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
SN74LVC1G123	SSOP (8)	2.95mm × 2.80mm
	VSSOP (8)	2.30mm × 2.00mm
	DSBGA (8)	1.91mm × 0.91mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

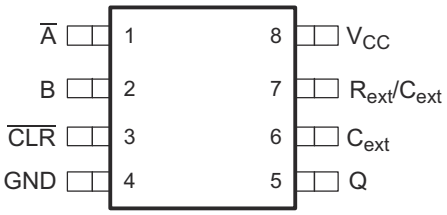
An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions



See mechanical drawings for dimensions.

Figure 4-1. DCT Package 8-Pin SSOP Top View

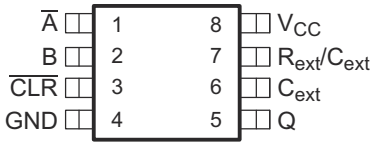


Figure 4-2. DCU Package 8-Pin VSSOP Top View

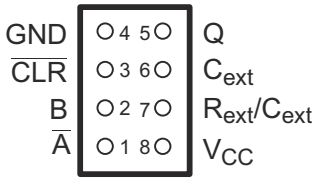


Figure 4-3. YZP Package 8-Pin DSBGA Bottom View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{A}$	1	I	Falling edge sensitive input; requires B and $\overline{CLR}$ to be held high.
B	2	I	Rising edge sensitive input; requires $\overline{A}$ to be held low and $\overline{CLR}$ to be held high.
$\overline{CLR}$	3	I	Clear, Active Low; also can operate as rising edge sensitive input if $\overline{A}$ is held low and B is held high.
GND	4	—	Ground
Q	5	O	Output
C_{ext}	6	—	Connects only to the external capacitor
R_{ext}/C_{ext}	7	—	Connects to the external capacitor and resistor
V_{CC}	8	—	Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
R_{ext} (2)	External timing resistance	V_{CC} = 2 V	5		kΩ
		V_{CC} ≥ 3 V	1		
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) R_{ext}/C_{ext} is an I/O and must not be connected directly to GND or V_{CC}.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G123			UNIT
		DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	–40°C TO 85°C			–40°C TO 125°C			UNIT
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{OH}		I_{OH} = –100 µA		1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
		I_{OH} = –4 mA		1.65 V	1.2			1.2			
		I_{OH} = –8 mA		2.3 V	1.9			1.9			
		I_{OH} = –16 mA		3 V	2.4			2.4			
		I_{OH} = –24 mA			2.3			2.3			
		I_{OH} = –32 mA		4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 100 µA		1.65 V to 5.5 V			0.1			0.1	V
		I_{OL} = 4 mA		1.65 V			0.45			0.45	
		I_{OL} = 8 mA		2.3 V			0.3			0.3	
		I_{OL} = 16 mA		3 V			0.4			0.4	
		I_{OL} = 24 mA					0.55			0.55	
		I_{OL} = 32 mA		4.5 V			0.55			0.55	
I_I	R_{ext}/C_{ext} (2)	B = GND,	$\overline{A}$ = $\overline{CLR}$ = V_{CC}	1.65 V to 5.5 V			±0.25			±0.25	µA
	$\overline{A}$, B, $\overline{CLR}$	V_I = 5.5 V or GND					±1			±1	
I_{off}	$\overline{A}$, B, Q, $\overline{CLR}$	V_I or V_O = 5.5 V		0			±10			±10	µA
I_{CC}	Quiescent	V_I = V_{CC} or GND,	I_O = 0	5.5 V			20			20	µA
I_{CC}	Active state	V_I = V_{CC} or GND,	R_{ext}/C_{ext} = 0.5 V_{CC}	1.65 V			165			165	µA
				2.3 V			220			220	
				3 V			280			280	
				4.5 V			650			650	
				5.5 V			975			975	

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5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	–40°C TO 85°C			–40°C TO 125°C			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
C_I	V_I = V_{CC} or GND	3.3 V		3					pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This test is performed with the terminal in the OFF-state condition.

5.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER			TEST CONDITIONS		–40°C TO 125°C						UNIT
					V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V	V_{CC} = 5 V ± 0.5 V	
					MIN	TYP	MIN	TYP	MIN TYP	MIN TYP	
t_wIN	Pulse duration	$\overline{CLR}$			8		4		3	2.5	ns
		$\overline{A}$ or B trigger			8		4		3	2.5	ns
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF					5.5	4.5	ns
				C_{ext} = 100 µF					1.4	1.1	µs
			R_{ext} = 5 kΩ	C_{ext} = 100 pF		75		45			ns
				C_{ext} = 100 µF		1.8		1.4			µs

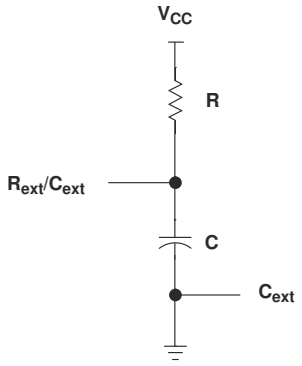


Figure 5-1. Required Timing Circuit

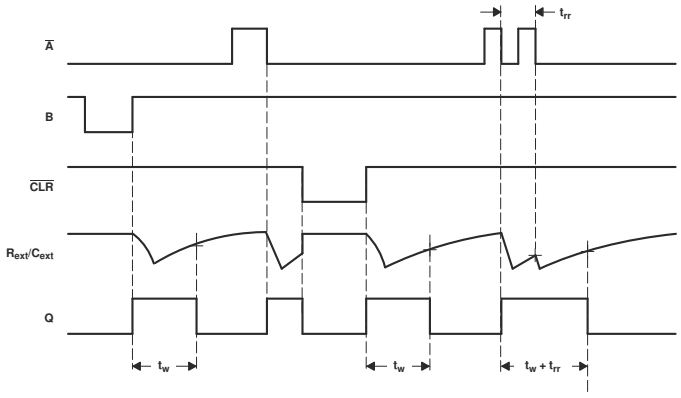


Figure 5-2. Input/Output Timing Diagram

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5.7 Switching Characteristics, C_L = 15 pF, –40°C to 85°C

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C									UNIT
			V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q	7	18.5	52	4	17	3	11.5	2	7.6	ns
	$\overline{CLR}$		5	12.4	34	3	11.5	2	8	1.5	5.5	
	$\overline{CLR}$ trigger		7	17.4	54	4	15.5	3	10.5	2	7	

5.8 Switching Characteristics, C_L = 50 pF, –40°C to 85°C

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	–40°C TO 85°C									UNIT
				V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
				MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q		6	18.6	57	3	18.5	2	12.5	1.5	8.2	ns
	$\overline{CLR}$			4	11.6	36.5	2	12.5	1.5	8.6	1.5	6	
	$\overline{CLR}$ trigger			5	17.3	59	2.5	17	2	11.5	1.5	7.5	
t_wOUT(2)		Q	C_{ext} = 28 pF, R_{ext} = 2 kΩ		225	600	190	220	170	200	150	180	ns
			C_{ext} = 0.01 µF, R_{ext} = 10 kΩ		100	110	100	110	100	110	100	110	µs
			C_{ext} = 0.1 µF, R_{ext} = 10 kΩ		1	1.1	1	1.1	1	1.1	1	1.1	ms

(1) T_A = 25°C
(2) t_w = Duration of pulse at Q output

5.9 Switching Characteristics, C_L = 50 pF, –40°C to 125°C

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	–40°C TO 125°C									UNIT
				V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		
				MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q		6		58	3	19.5	2	13.2	1.5	8.7	ns
	$\overline{CLR}$			4		37	2	13.5	1.5	9.2	1.5	6.5	
	$\overline{CLR}$ trigger			5		60	2.5	18	2	12	1.5	8	
t_wOUT(2)		Q	C_{ext} = 28 pF, R_{ext} = 2 kΩ		225	600	190	220	170	200	150	180	ns
			C_{ext} = 0.01 µF, R_{ext} = 10 kΩ		100	110	100	110	100	110	100	110	µs
			C_{ext} = 0.1 µF, R_{ext} = 10 kΩ		1	1.1	1	1.1	1	1.1	1	1.1	ms

(1) T_A = 25°C
(2) t_w = Duration of pulse at Q output

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5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
				TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$\overline{A}$ = low, B = high, $\overline{CLR}$ = 10 MHz	R_{ext} = 1 kΩ, No C_{ext}			35	37	pF
			R_{ext} = 5 kΩ, No C_{ext}	41	40			

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5.11 Typical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

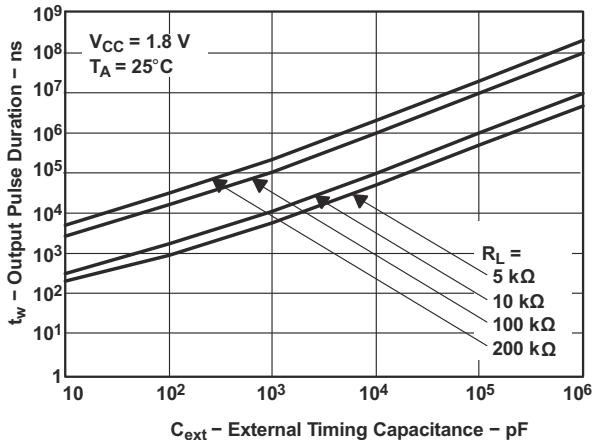


Figure 5-3. Output Pulse Duration vs External Timing Capacitance

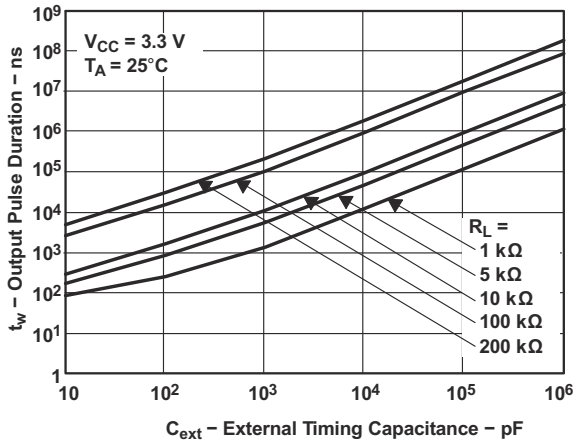


Figure 5-4. Output Pulse Duration vs External Timing Capacitance

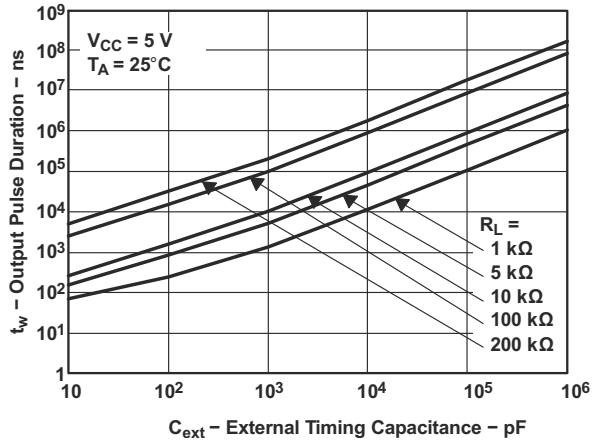


Figure 5-5. Output Pulse Duration vs External Timing Capacitance

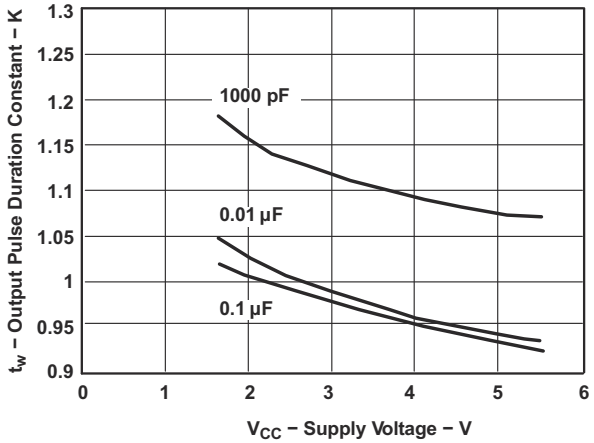


Figure 5-6. Output Pulse Duration Constant vs Supply Voltage

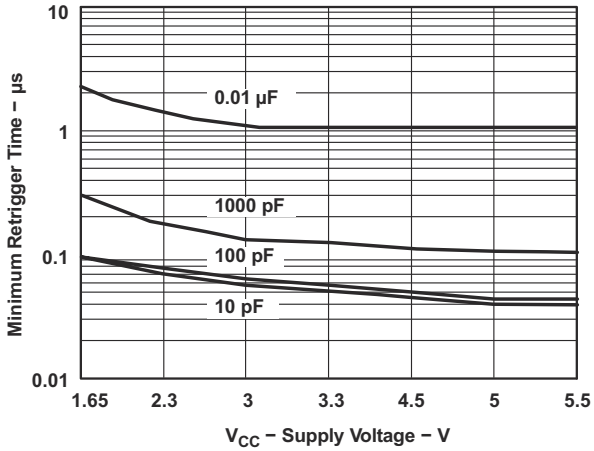
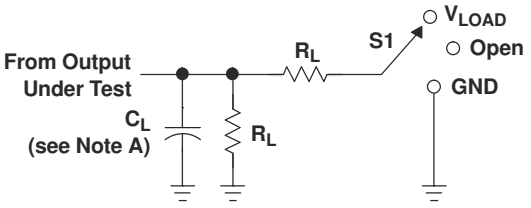


Figure 5-7. Minimum Retrigger Time vs Supply Voltage

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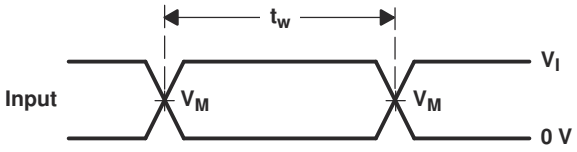
6 Parameter Measurement Information



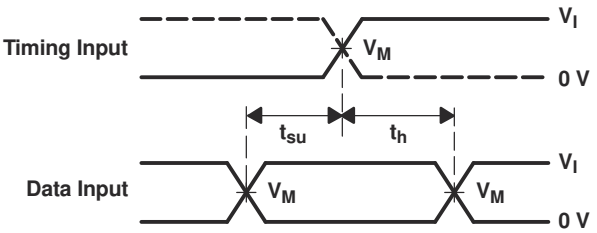
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

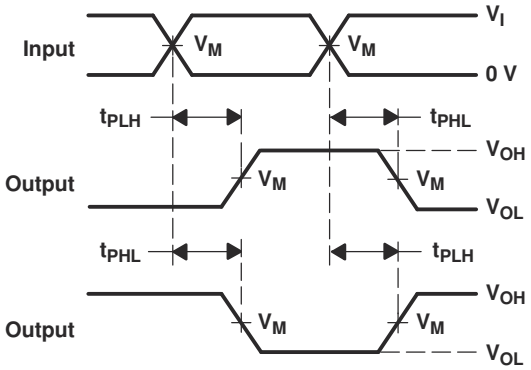
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V



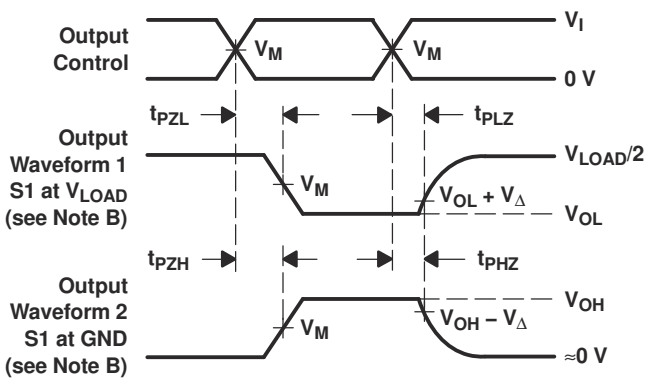
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

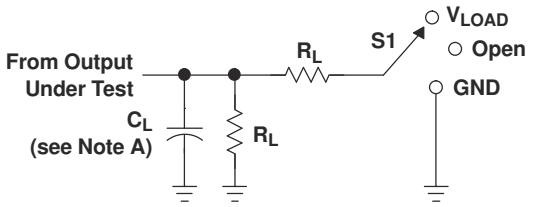


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

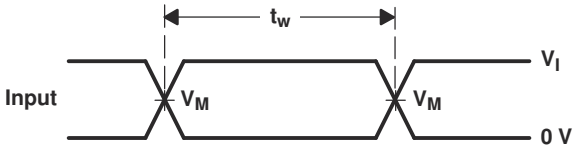
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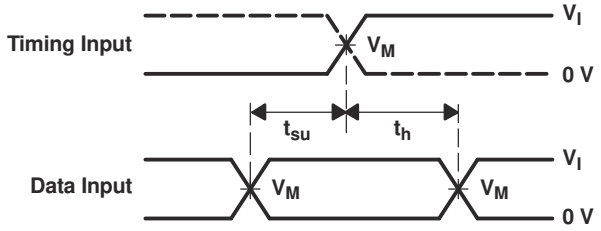
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

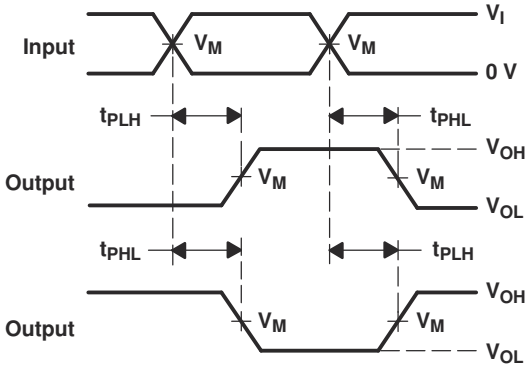
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



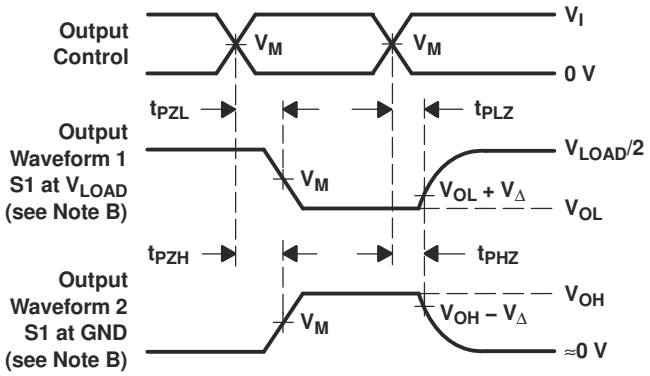
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74LVC1G123 device is a single retriggerable monostable multivibrator designed for 1.65-V to 5.5-V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

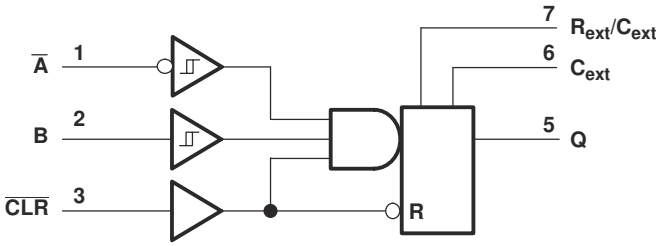
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$ and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. $\overline{CLR}$ can be used to override $\overline{A}$ or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The SN74LVC1G123 device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

7.2 Functional Block Diagram



7.3 Feature Description

This part is available in the Texas Instruments NanoFree™ package. It supports 5-V V_{CC} operation and accepts inputs up to 5.5 V. The max t_{pd} is 8 ns at 3.3 V. It supports mixed-mode voltage operation on all ports.

Down translation can be achieved to V_{CC} from up to 5.5 V.

Schmitt-trigger circuitry on $\overline{A}$ and B inputs allows for slow input transition rates. The device can be edge triggered from active-high or active-low gated logic inputs. It can support up to 100% duty cycle from retriggering.

Clear can be used to terminate the output pulse early.

Glitch-free power-up reset is on all outputs.

I_{off} supports live insertion, partial-power-down mode, and back-drive protection.

Latch-up performance exceeds 100 mA per JESD 78, Class II.

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7.4 Device Functional Modes

Table 7-1 lists the functional modes for the SN74LVC1G123.

Table 7-1. Function Table

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L[1]
X	X	L	L[1]
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G123 can be used for many applications. The application shown here is a switch debounce circuit. Many switches produce multiple triggers when pressed, and the debounce circuit turns the many triggers into one. This circuit takes advantage of the retrigger capability of the SN74LVC1G123 in that the output pulse length only has to be longer than the longest individual bounce (typically less than 1 ms).

8.2 Typical Application

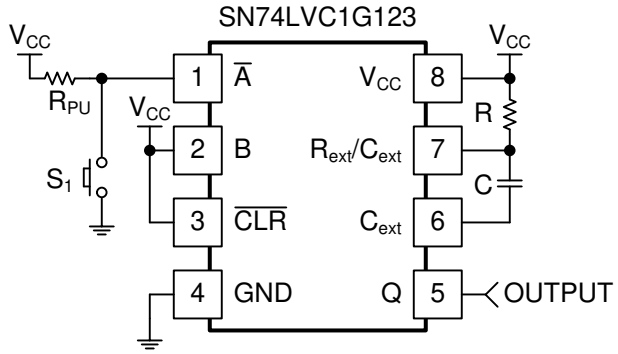


Figure 8-1. Typical Application of the SN74LVC1G123

8.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Section 5.3*.
   - Inputs and outputs are overvoltage tolerant, allowing them to go as high as 4.6 V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load current should not exceed values listed in *Section 5.3*.

8.2.2 Detailed Design Procedure

The values for V_{CC}, R_{PU}, R, and C must be selected for proper operation.

V_{CC} is selected at 1.8 V. This value is usually driven by the logic voltage of the system, but is arbitrary in this case.

R_{PU} is selected at 10 kΩ.

R and C are selected via the plots in *Section 8.2.3* and are based on the time desired for the output pulse. In this case, the output pulse will be 1 ms. Since the supply voltage has been selected at 1.8 V, Figure 8-2 is used to determine the R and C values required. First convert the desired pulse width (t_w), 1 ms, to ns. This yields 10^6 ns. Next follow that line across to see which R and C values intersect it.

R is selected at 10 kΩ because that line intersects nicely with 10^6 ns and 10^5 pF, making the selection of C at 0.1 µF easy.

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Table 8-1. Application Specific Values

PARAMETER	VALUE
V_{CC}	1.8 V
R_{PU}	10 kΩ
t_w	1 ms
R (R_{ext})	10 kΩ
C (C_{ext})	0.1 µF

In addition to the shown components, a 0.1-µF decoupling capacitor from V_{CC} to ground should be placed as close as possible to the device.

8.2.3 Application Curves

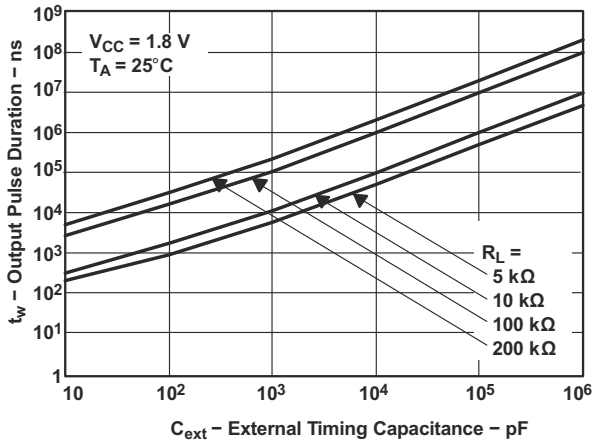


Figure 8-2. Output Pulse Duration vs External Timing Capacitance

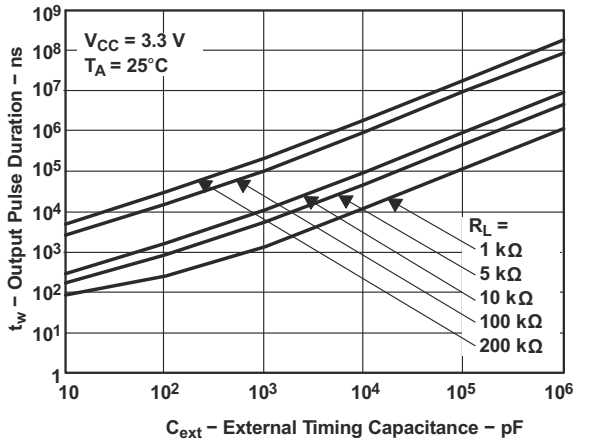


Figure 8-3. Output Pulse Duration vs External Timing Capacitance

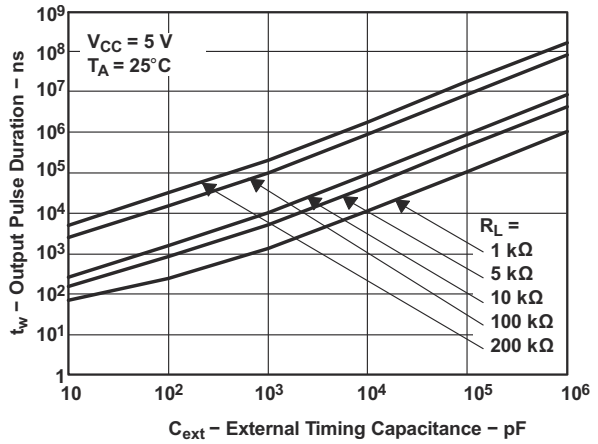


Figure 8-4. Output Pulse Duration vs External Timing Capacitance

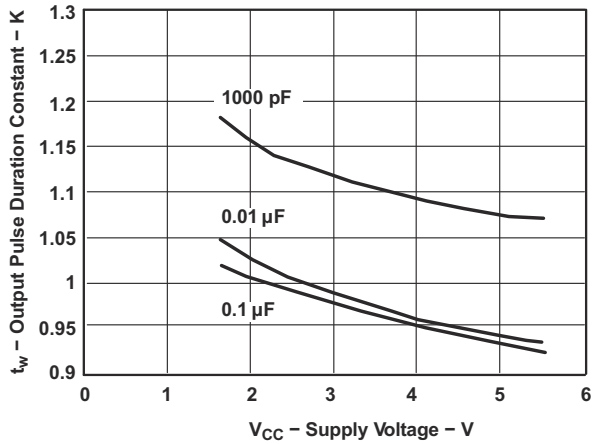


Figure 8-5. Output Pulse Duration Constant vs Supply Voltage

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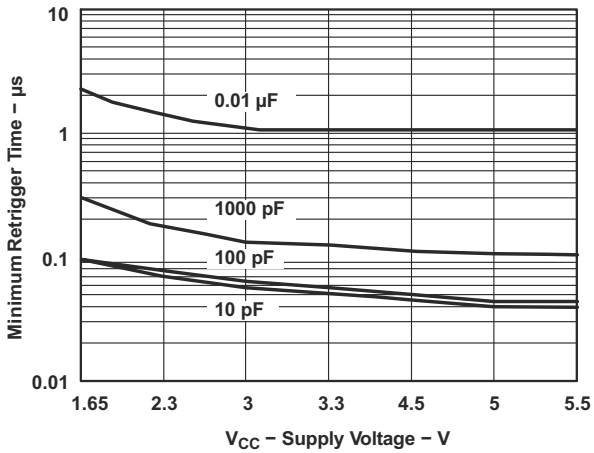


Figure 8-6. Minimum Retrigger Time vs Supply Voltage

9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Section 5.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

10 Layout

10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

10.2 Layout Example

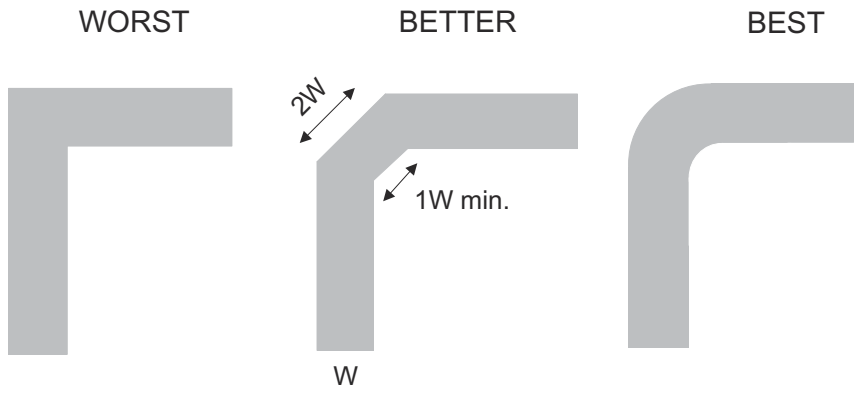


Figure 10-1. Trace Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2015) to Revision E (March 2024)	Page
• Updated format to match new TI layout and flow. Tables, figures and cross-references use a new numbering sequence throughout the document	1

Changes from Revision C (October 2013) to Revision D (June 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed duplicate *Timing Requirements* table	6

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Changes from Revision B (January 2007) to Revision C (October 2013)	Page
• Updated document to new TI data sheet format	1
• Updated *Features*	1
• Updated operating temperature range	4
• Added *Thermal Information* table	5

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1G123DCTRE4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTRE4.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTRG4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTRG4.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTTE4	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTTE4.B	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTTG4	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCTTG4.B	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23 (R, Z)
74LVC1G123DCURE4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R
74LVC1G123DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R
74LVC1G123DCURG4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R
74LVC1G123DCUTG4	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R
74LVC1G123DCUTG4.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C23R
SN74LVC1G123DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)
SN74LVC1G123DCTR.B	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)
SN74LVC1G123DCTT	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)
SN74LVC1G123DCTT.B	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2W95, C23) (R, Z)
SN74LVC1G123DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C23J, C23Q, C23R)
SN74LVC1G123DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C23J, C23Q, C23R)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G123DCUT	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C23J, C23Q, C23R)
SN74LVC1G123DCUT.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C23J, C23Q, C23R)
SN74LVC1G123YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(D87, D8N)
SN74LVC1G123YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(D87, D8N)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

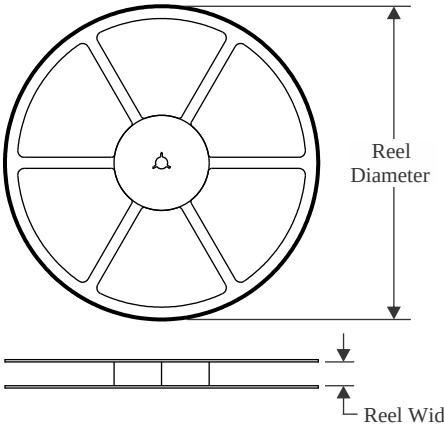
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

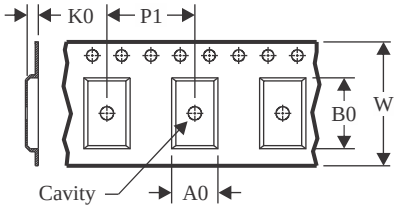
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

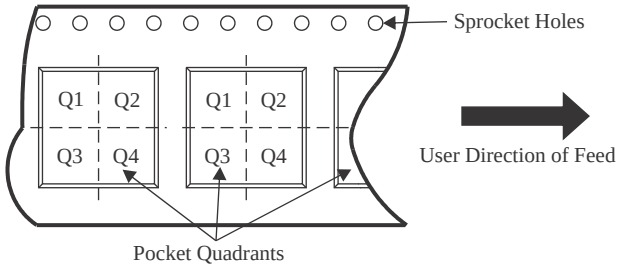


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

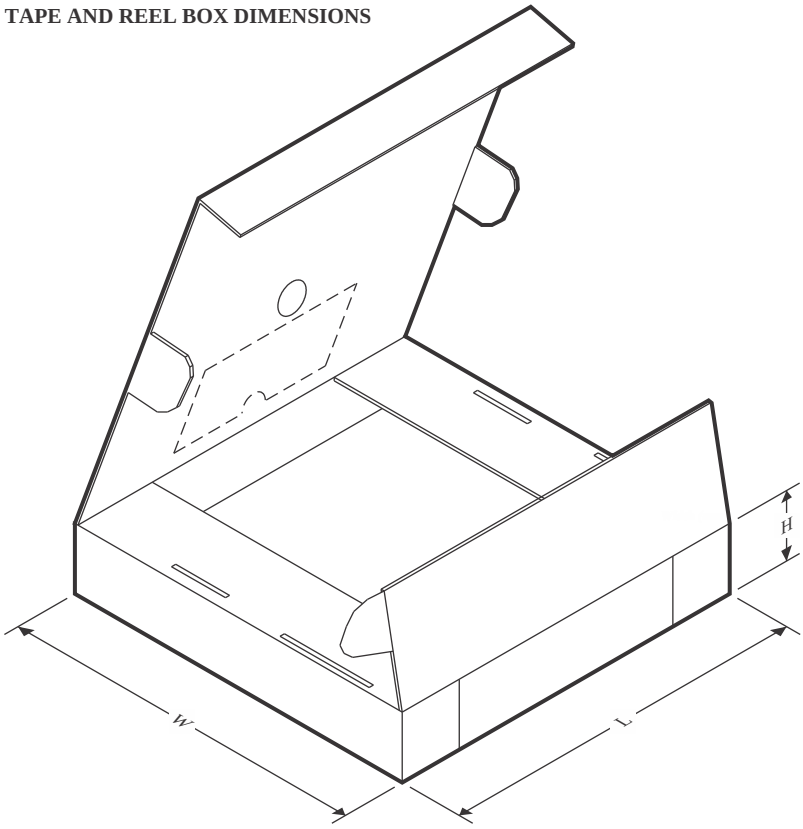
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G123DCTRE4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
74LVC1G123DCTRG4	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
74LVC1G123DCTTE4	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
74LVC1G123DCTTG4	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
74LVC1G123DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
74LVC1G123DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123DCTR	SSOP	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC1G123DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G123DCTT	SSOP	DCT	8	250	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74LVC1G123DCTT	SSOP	DCT	8	250	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

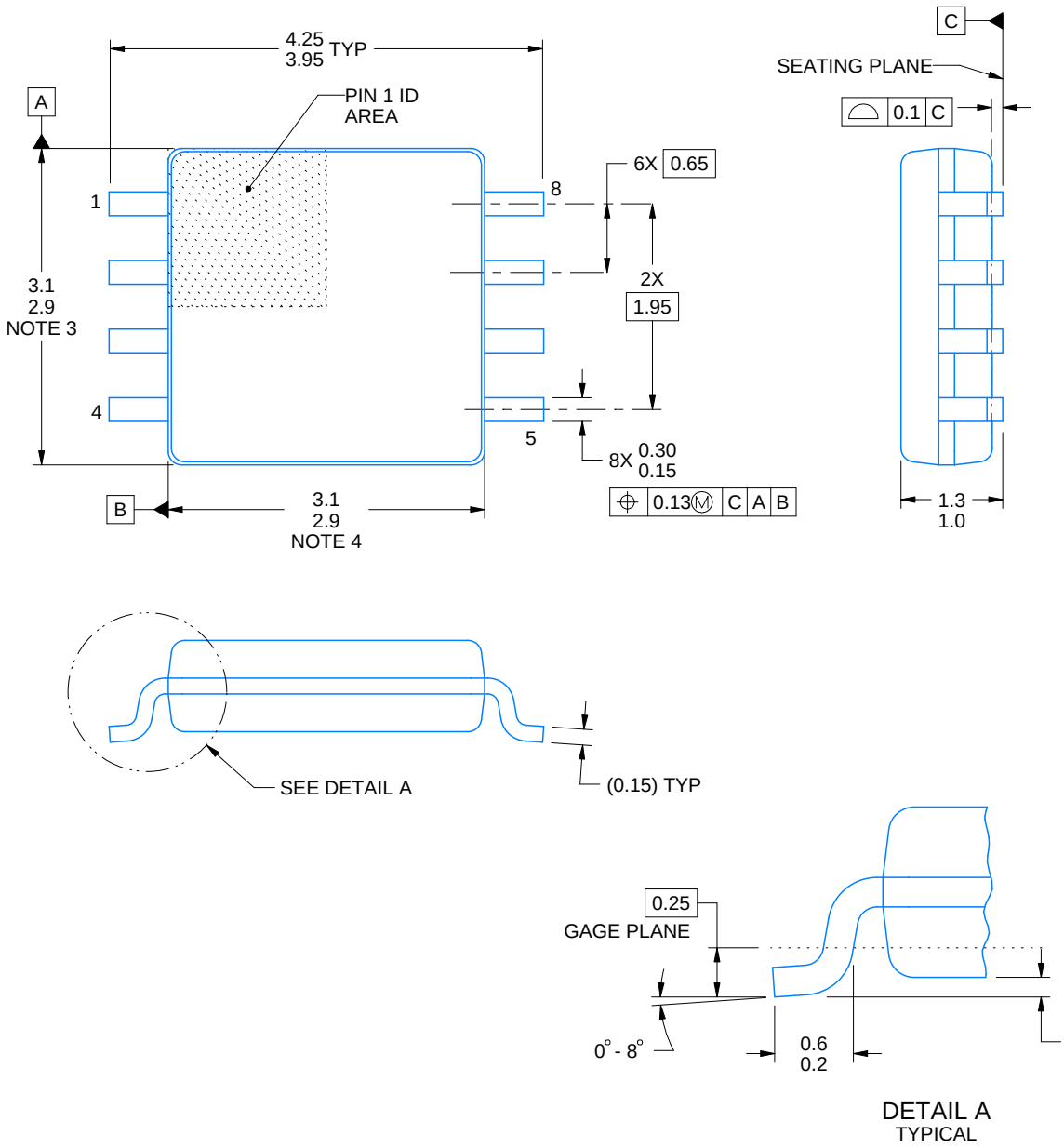
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G123DCTRE4	SSOP	DCT	8	3000	183.0	183.0	20.0
74LVC1G123DCTRG4	SSOP	DCT	8	3000	183.0	183.0	20.0
74LVC1G123DCTTE4	SSOP	DCT	8	250	183.0	183.0	20.0
74LVC1G123DCTTG4	SSOP	DCT	8	250	183.0	183.0	20.0
74LVC1G123DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
74LVC1G123DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G123DCTR	SSOP	DCT	8	3000	183.0	183.0	20.0
SN74LVC1G123DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC1G123DCTT	SSOP	DCT	8	250	183.0	183.0	20.0
SN74LVC1G123DCTT	SSOP	DCT	8	250	190.0	190.0	30.0
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G123DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1G123DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC1G123DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G123YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCT0008A

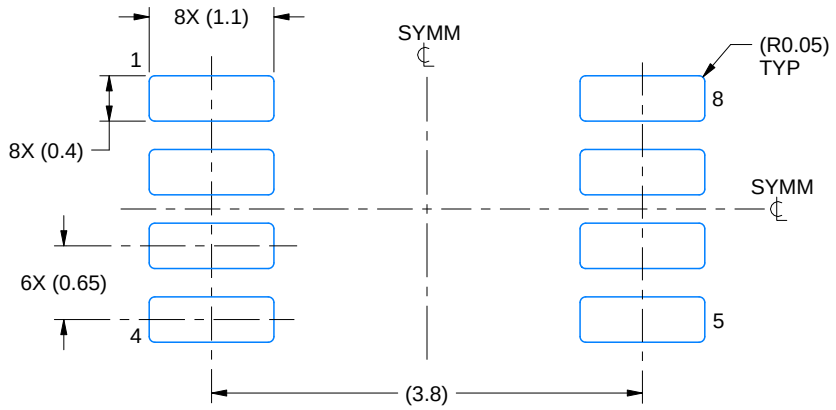
SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE

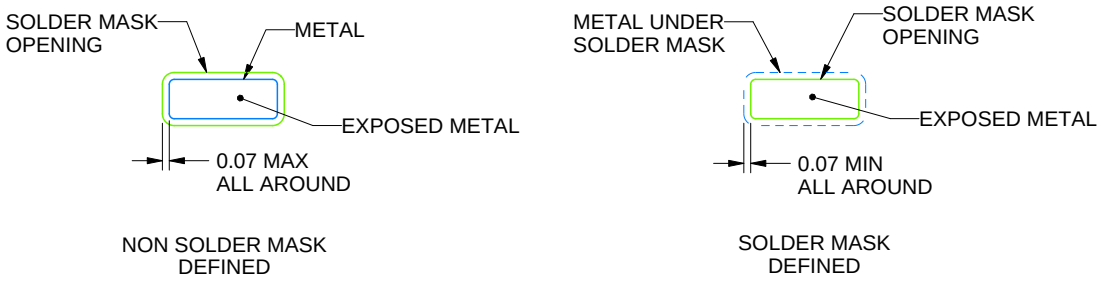


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

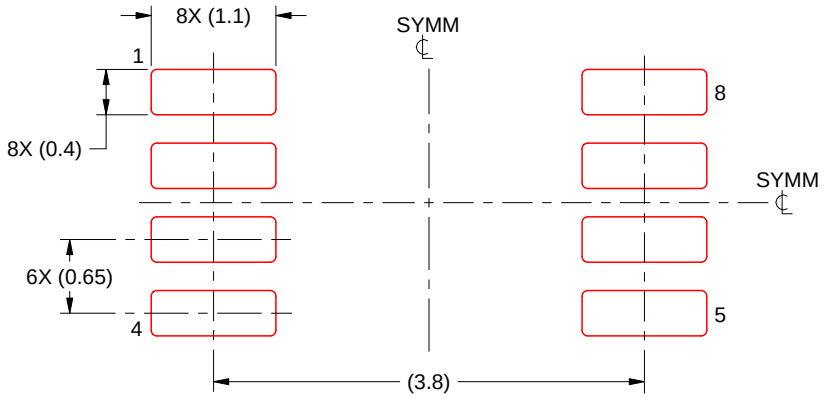


SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

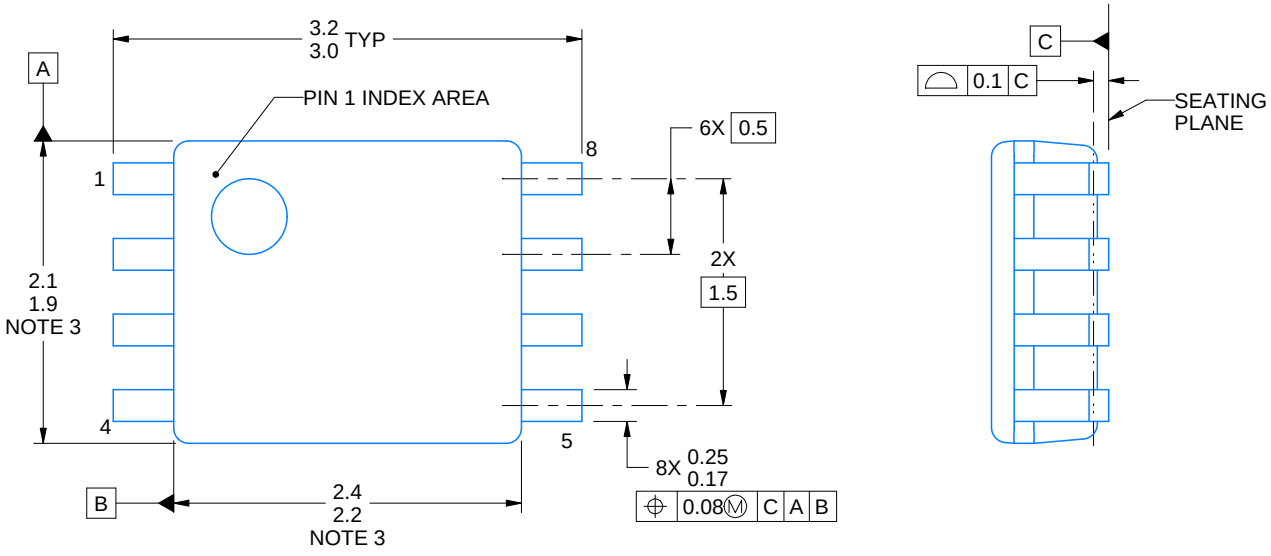
DCU0008A

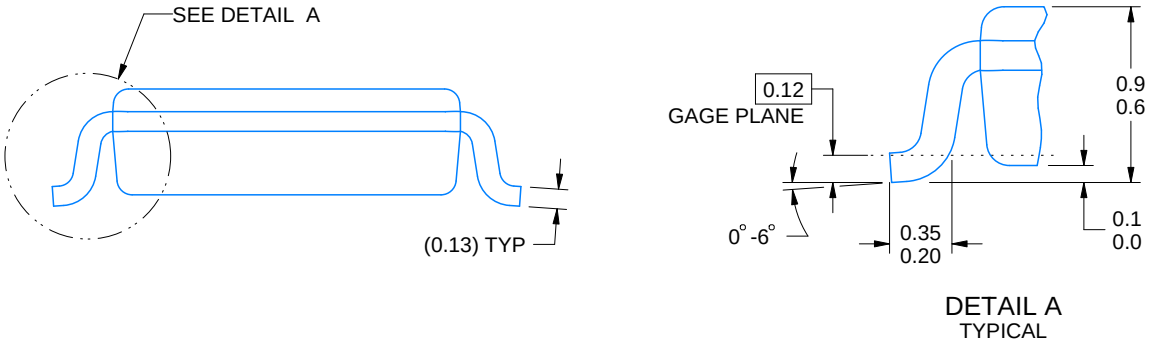


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

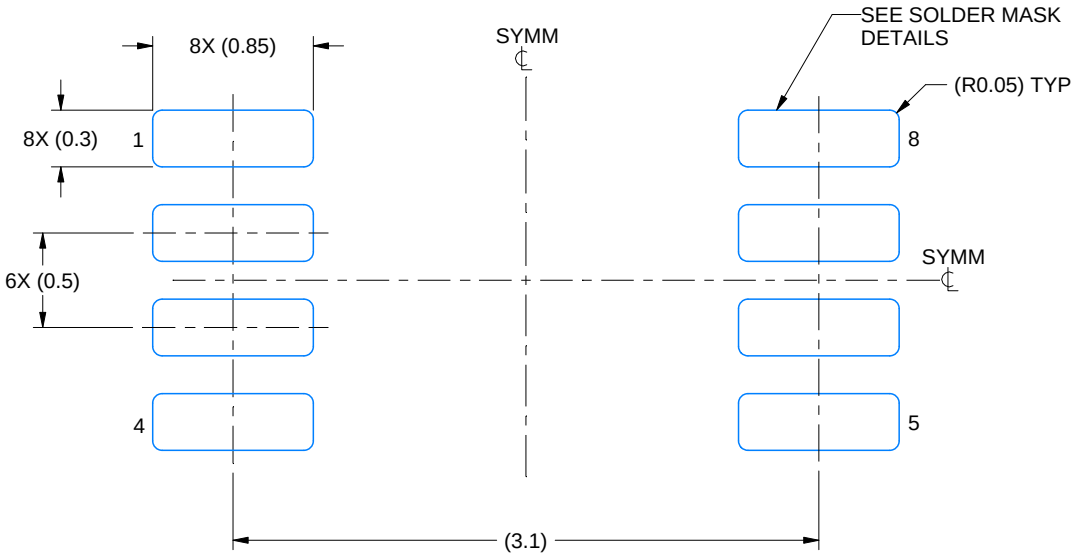




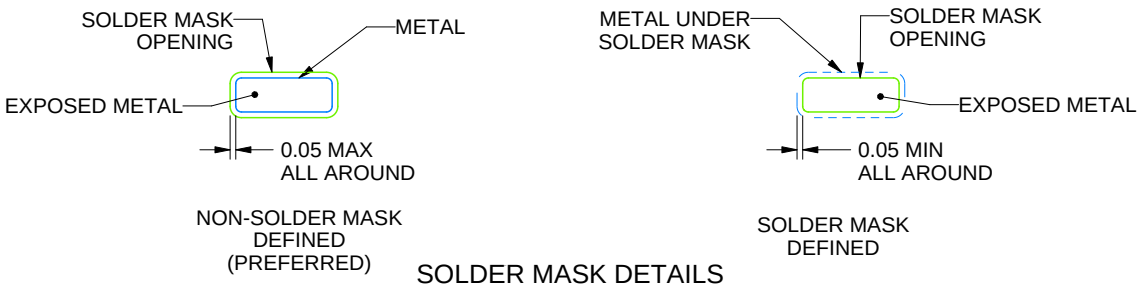
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

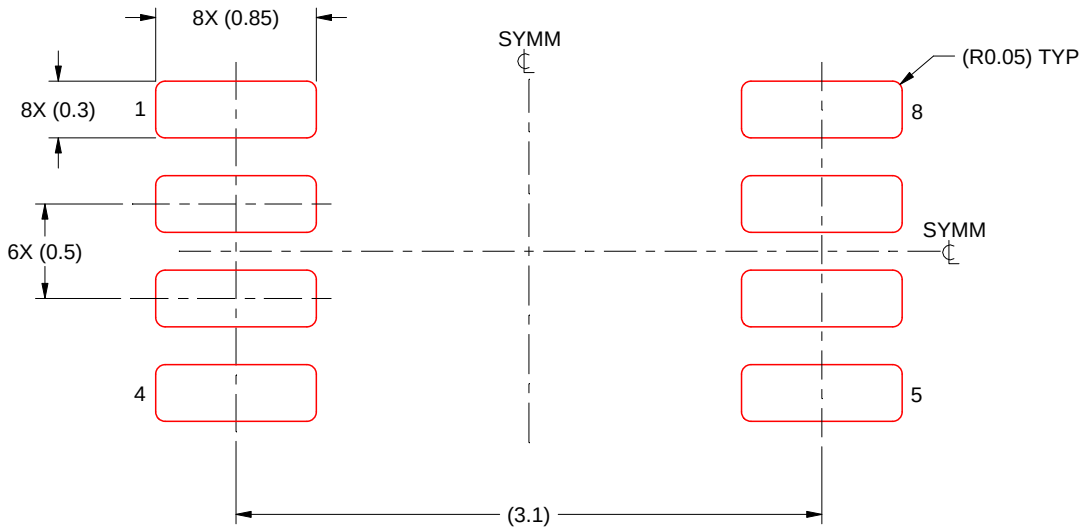


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

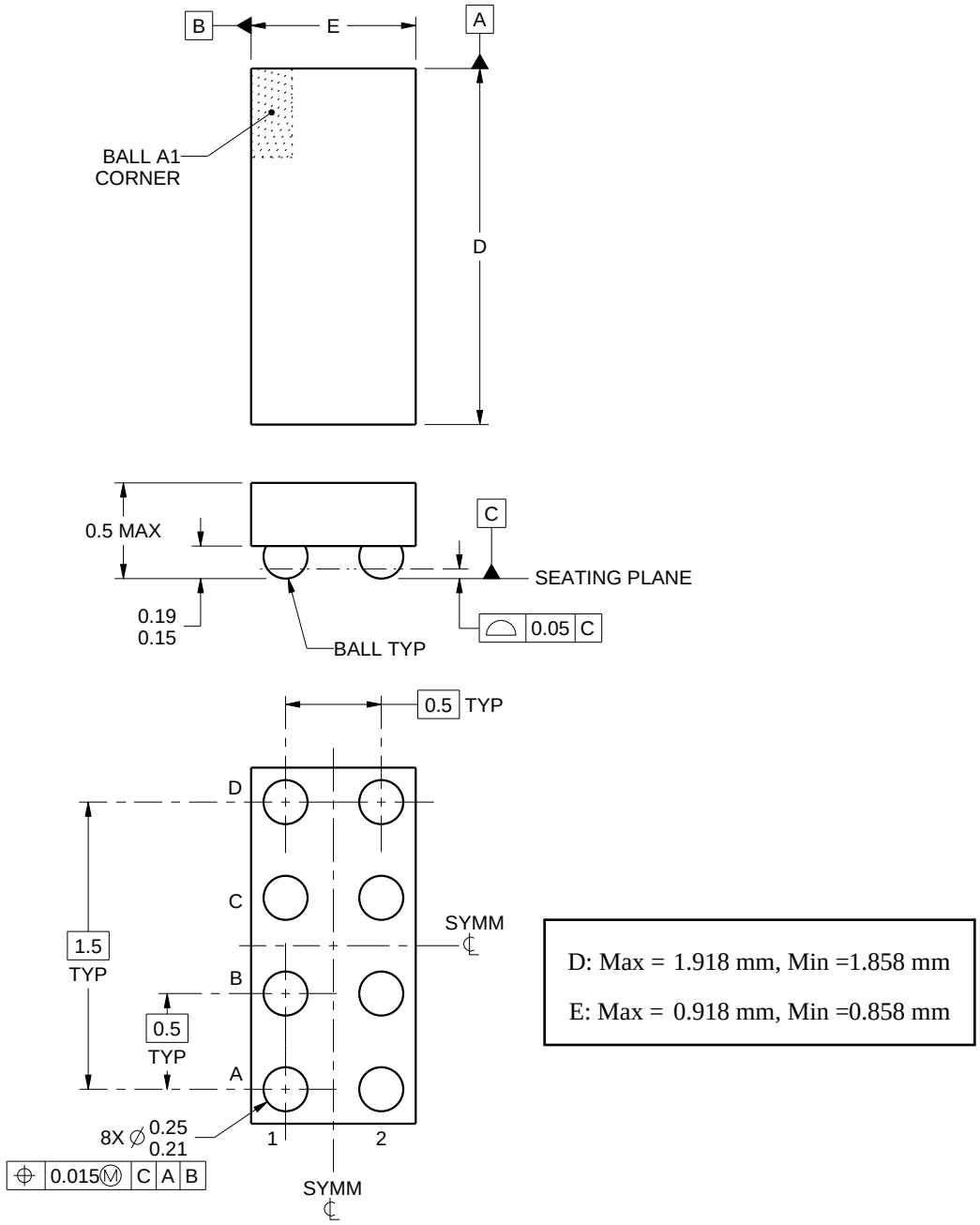
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

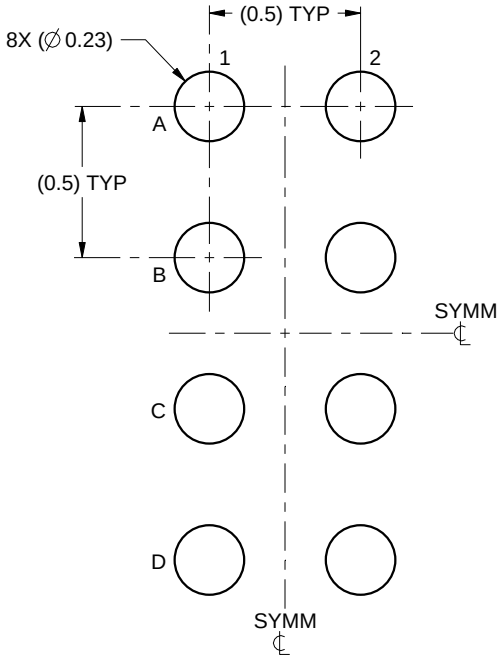
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

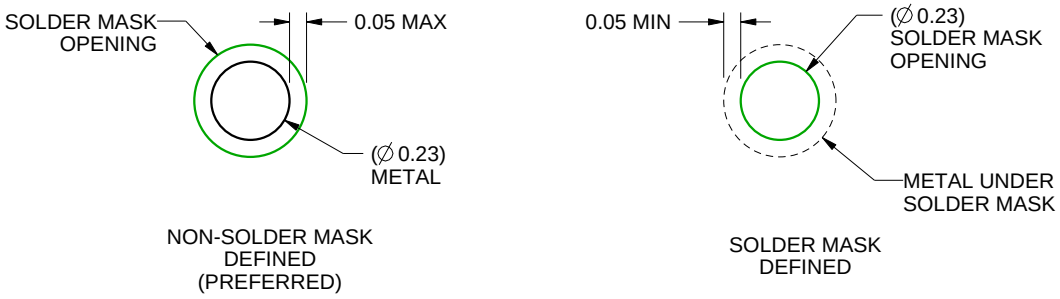


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

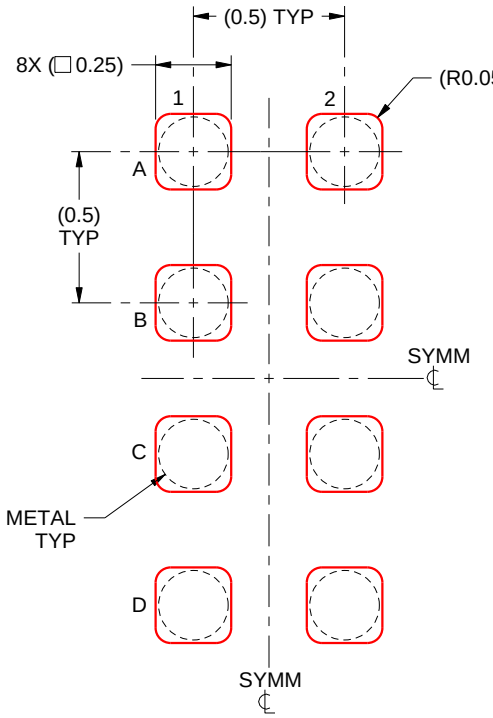


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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