

SN74LVC1G79 Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Available in the Texas Instruments NanoFree™ package
- Latch-up performance exceeds 100mA per JESD 78, Class II
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 6ns at 3.3V and 50pF load
- Low power consumption, 10μA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports partial-power-down mode and back-drive protection

2 Applications

- Test and measurement
- Enterprise switching
- Telecom infrastructure
- Personal electronics
- White goods

3 Description

The SN74LVC1G79 device is a single positive-edge-triggered D-type flip-flop that is designed for 1.65V to 5.5V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

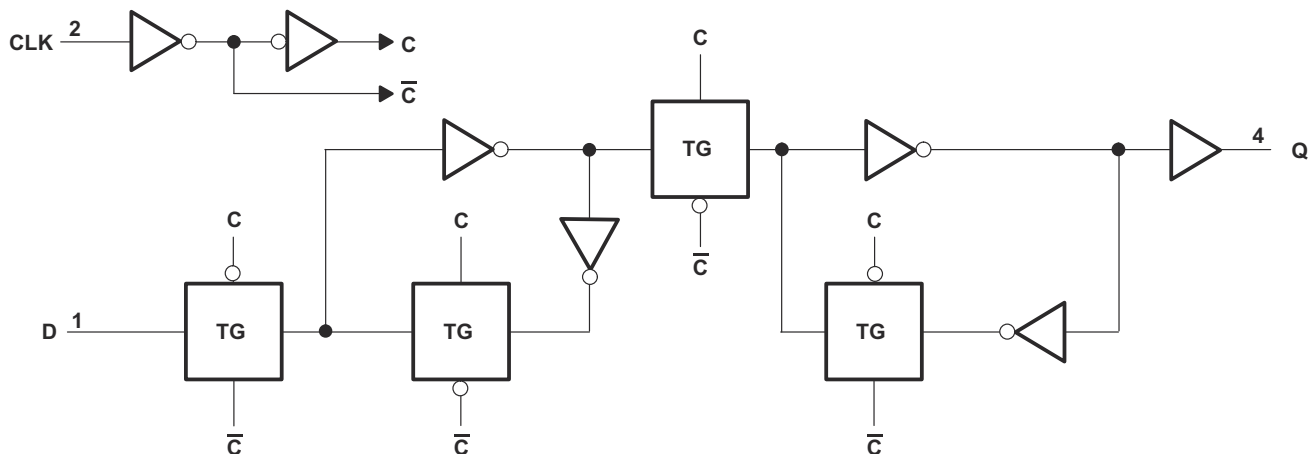
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74LVC1G79DBV	DBV (SOT-23, 5)	2.90mm × 2.80mm
SN74LVC1G79DCK	DCK (SC70, 5)	2.00mm × 2.10mm
SN74LVC1G79DRL	DRL (SOT, 5)	1.60mm × 1.60mm
SN74LVC1G79YZP	YZP (DSBGA, 5)	1.14mm × 0.91mm

- (1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



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Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	6 Parameter Measurement Information	9
2 Applications	1	7 Detailed Description	11
3 Description	1	7.1 Overview.....	11
4 Pin Configuration and Functions	3	7.2 Functional Block Diagram.....	11
5 Specifications	4	7.3 Feature Description.....	11
5.1 Absolute Maximum Ratings.....	4	7.4 Device Functional Modes.....	12
5.2 ESD Ratings.....	4	8 Application and Implementation	13
5.3 Recommended Operating Conditions.....	5	8.1 Application Information.....	13
5.4 Thermal Information.....	5	8.2 Typical Application.....	13
5.5 Electrical Characteristics.....	6	8.3 Power Supply Recommendations.....	14
5.6 Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	6	8.4 Layout.....	14
5.7 Timing Requirements: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	6	9 Device and Documentation Support	15
5.8 Switching Characteristics: $C_L = 15\text{pF}$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	7	9.1 Documentation Support.....	15
5.9 Switching Characteristics: $C_L = 30$ or 50pF , $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	7	9.2 Receiving Notification of Documentation Updates....	15
5.10 Switching Characteristics: $C_L = 30\text{pF}$ or 50pF , $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	7	9.3 Community Resources.....	15
5.11 Operating Characteristics.....	7	9.4 Trademarks.....	15
5.12 Typical Characteristics.....	7	10 Revision History	15
		11 Mechanical, Packaging, and Orderable Information	16

4 Pin Configuration and Functions

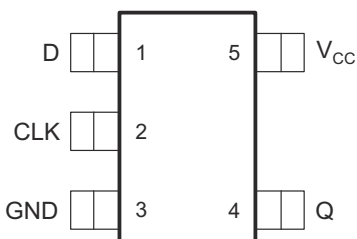
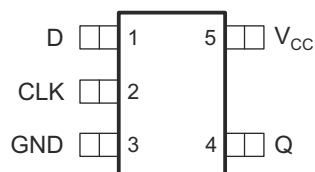


Figure 4-1. DBV Package 5-Pin SOT-23 Top View



See mechanical drawings for dimensions.

Figure 4-2. DCK Package 5-Pin SC70 Top View

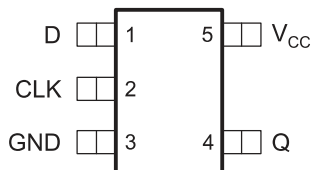


Figure 4-3. DRL Package 5-Pin SOT Top View

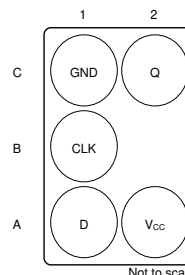


Figure 4-4. YZP Package 5-Pin DSBGA Bottom View

Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	DBV, DCK, DRL	YZP		
CLK	2	B1	I	Positive-Edge-Triggered Clock input
D	1	A1	I	Data input
GND	3	C1	—	Ground
Q	4	C2	O	Non-inverted output
V _{CC}	5	A2	—	Positive Supply

(1) I = Input; O=Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage		−0.5	6.5	V
V _I	Input voltage ⁽²⁾		−0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾ ⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−50	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
T _{stg}	Storage temperature		−65	150	°C
T _J	Junction temperature			150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	
		Machine Model (MM), A115A	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC} Supply voltage	Operating	1.65	5.5	V
	Data retention only	1.5		
V _{IH} High-level input voltage	V _{CC} = 1.65V to 1.95V	0.65 × V _{CC}		V
	V _{CC} = 2.3V to 2.7V	1.7		
	V _{CC} = 3V to 3.6V	2		
	V _{CC} = 4.5V to 5.5V	0.7 × V _{CC}		
V _{IL} Low-level input voltage	V _{CC} = 1.65V to 1.95V		0.35 × V _{CC}	V
	V _{CC} = 2.3V to 2.7V		0.7	
	V _{CC} = 3V to 3.6V		0.8	
	V _{CC} = 4.5V to 5.5V		0.3 × V _{CC}	
V _I Input voltage		0	5.5	V
V _O Output voltage		0	V _{CC}	V
I _{OH} High-level output current	V _{CC} = 1.65V		–4	mA
	V _{CC} = 2.3V		–8	
	V _{CC} = 3V		–16	
			–24	
	V _{CC} = 4.5V		–32	
I _{OL} Low-level output current	V _{CC} = 1.65V		4	mA
	V _{CC} = 2.3V		8	
	V _{CC} = 3V		16	
			24	
	V _{CC} = 4.5V		32	
Δt/Δv Input transition rise or fall rate	V _{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
	V _{CC} = 3.3V ± 0.3V		10	
	V _{CC} = 5V ± 0.5V		5	
T _A Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, [Implications of Slow or Floating CMOS Inputs](#).

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
DBV (SOT-23)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W
DCK (SOT-SC70)	5	371	297.5	258.6	195.6	256.2	-	°C/W
DRL (SOT-5X3)	5	364.1	280.6	261.5	195.6	259.2	-	°C/W
YZP (DSBGA)	5	144.4	1.3	39.9	0.5	39.7	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = –40°C to +85°C			T _A = –40°C to +125°C			UNIT
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OH}		I _{OH} = –100 μA	1.65V to 5.5V	V _{CC} – 0.1			V _{CC} – 0.1			V
		I _{OH} = –4mA	1.65V	1.2			1.2			
		I _{OH} = –8mA	2.3V	1.9			1.9			
		I _{OH} = –16mA	3V	2.4			2.4			
		I _{OH} = –24mA		2.3			2.3			
		I _{OH} = –32mA	4.5V	3.8			3.8			
V _{OL}		I _{OL} = 100 μA	1.65V to 5.5V	0.1			0.1			V
		I _{OL} = 4mA	1.65V	0.45			0.45			
		I _{OL} = 8mA	2.3V	0.3			0.3			
		I _{OL} = 16mA	3V	0.4			0.4			
		I _{OL} = 24mA		0.55			0.55			
		I _{OL} = 32mA	4.5V	0.55			0.55			
I _I	All inputs	V _I = 5.5V or GND	0 to 5.5V	±10			±5			μA
I _{off}		V _I or V _O = 5.5V	0	±10			±10			μA
I _{CC}		V _I = 5.5V or GND, I _O = 0	1.65V to 5.5V	10			10			μA
ΔI _{CC}		One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	500			500			μA
C _i		V _I = V _{CC} or GND	3.3V	4			4			pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Timing Requirements: T_A = –40°C to +85°C

over operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER			T _A = –40°C to +85°C								UNIT
			V _{CC} = 1.8 ± 0.15V		V _{CC} = 2.5 ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
t _{su}	Setup time before CLK↑	Data high	2.2		1.4		1.3		1.2		ns
		Data low	2.6		1.4		1.3		1.2		
t _h	Hold time, data after CLK↑		0.3		0.4		1		0.5		ns

5.7 Timing Requirements: T_A = –40°C to +125°C

over operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER			T _A = −40°C to +125°C								UNIT
			V _{CC} = 1.8 ± 0.15V		V _{CC} = 2.5 ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
t _{su}	Setup time before CLK↑	Data high	2.2		1.4		1.3		1.2		ns
		Data low	2.6		1.4		1.3		1.2		

over operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER		T _A = −40°C to +125°C								UNIT
		V _{CC} = 1.8 ± 0.15V		V _{CC} = 2.5 ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _h	Hold time, data after CLK↑	0.3		0.4		1		0.5		ns

5.8 Switching Characteristics: $C_L = 15\text{pF}$, $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$

over recommended operating free-air temperature range, $C_L = 15\text{pF}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = −40°C to +85°C								UNIT
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	Q	2.5	9.1	1.2	6	1	4	0.8	3.8	ns

5.9 Switching Characteristics: $C_L = 30$ or 50pF , $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$

over recommended operating free-air temperature range, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = −40°C to +85°C								UNIT
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	Q	3.9	9.9	2	7	1.7	5	1	4.5	ns

5.10 Switching Characteristics: $C_L = 30\text{pF}$ or 50pF , $T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$

over recommended operating free-air temperature range, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T _A = −40°C to +125°C								UNIT
			V _{CC} = 1.8V ± 0.15V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 3.3V ± 0.3V		V _{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			160		160		160		160		MHz
t _{pd}	CLK	Q	3.9	12	2	8.5	1.7	6	1	5	ns

5.11 Operating Characteristics

$T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 5\text{V} \pm 0.5\text{V}$		UNIT
		TYP		TYP		TYP		TYP		
C_{pd} Power dissipation capacitance	$f = 10\text{MHz}$	26		26		27		30		pF

5.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0V to 6.5V.

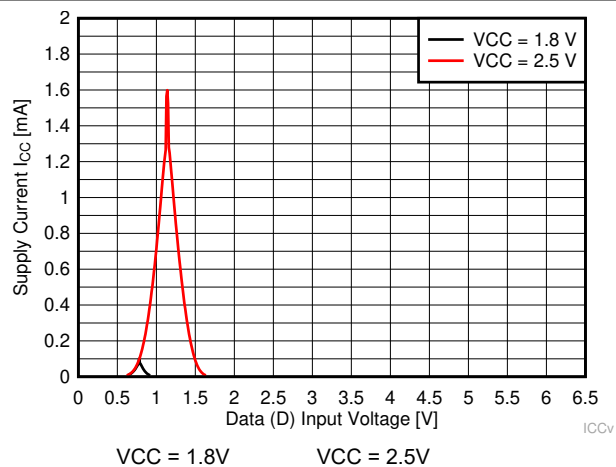


Figure 5-1. Supply Current (I_{CC}) vs Data (D) Input Voltage

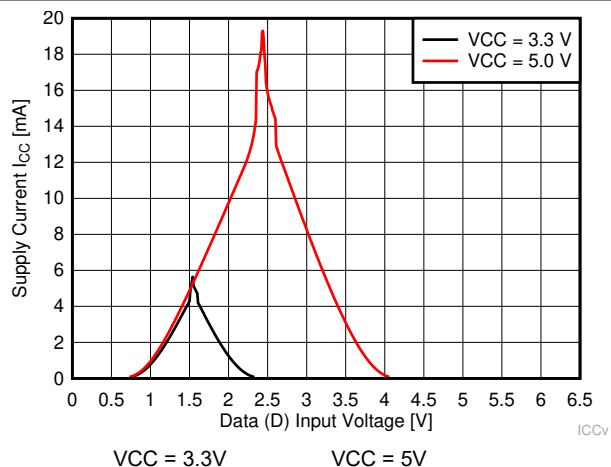
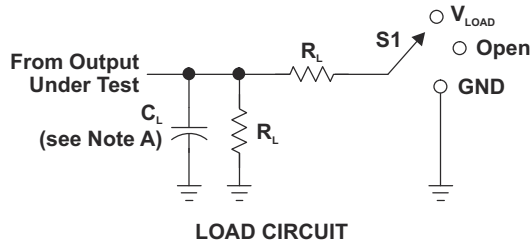


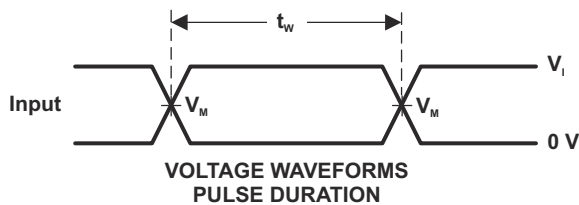
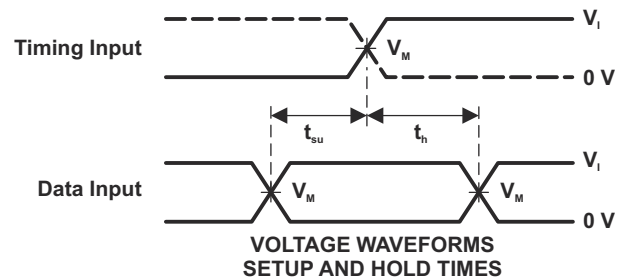
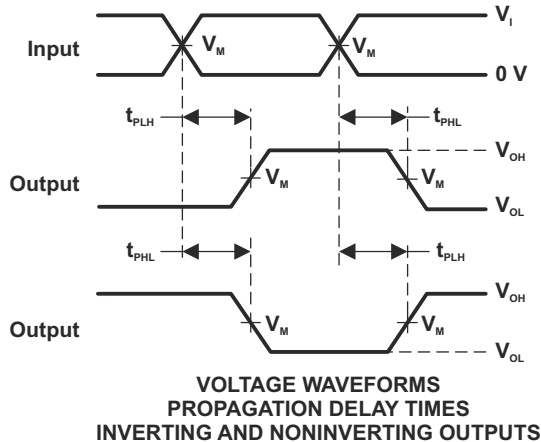
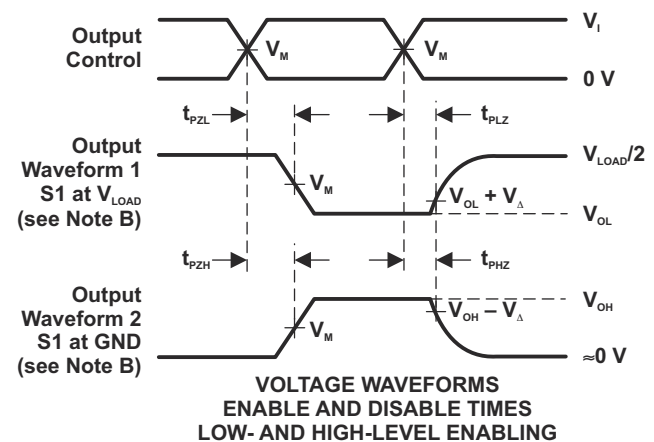
Figure 5-2. Supply Current (I_{CC}) vs Data (D) Input Voltage

6 Parameter Measurement Information



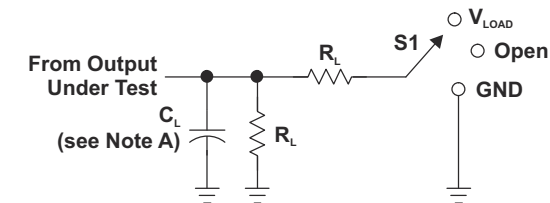
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{on} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

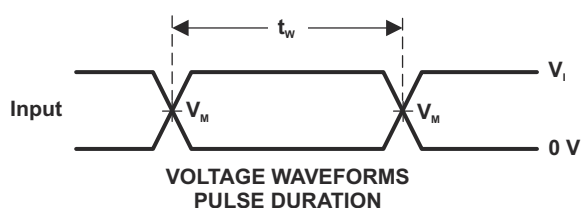
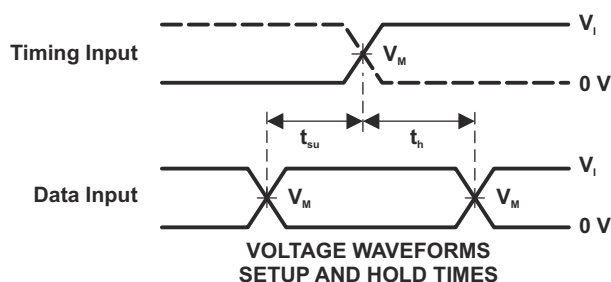
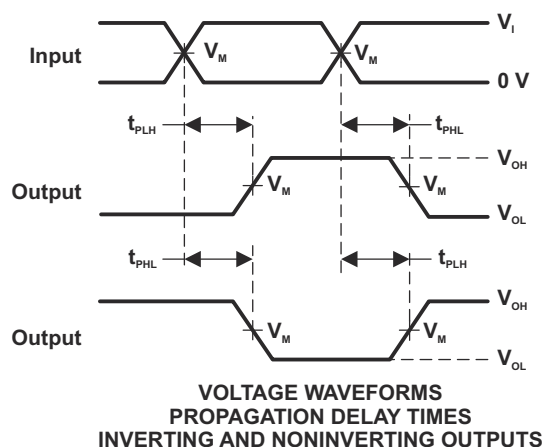
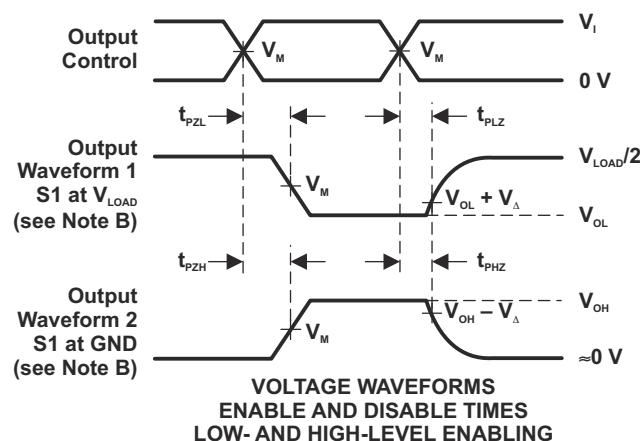
Figure 6-1. Load Circuit and Voltage Waveforms



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_o = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

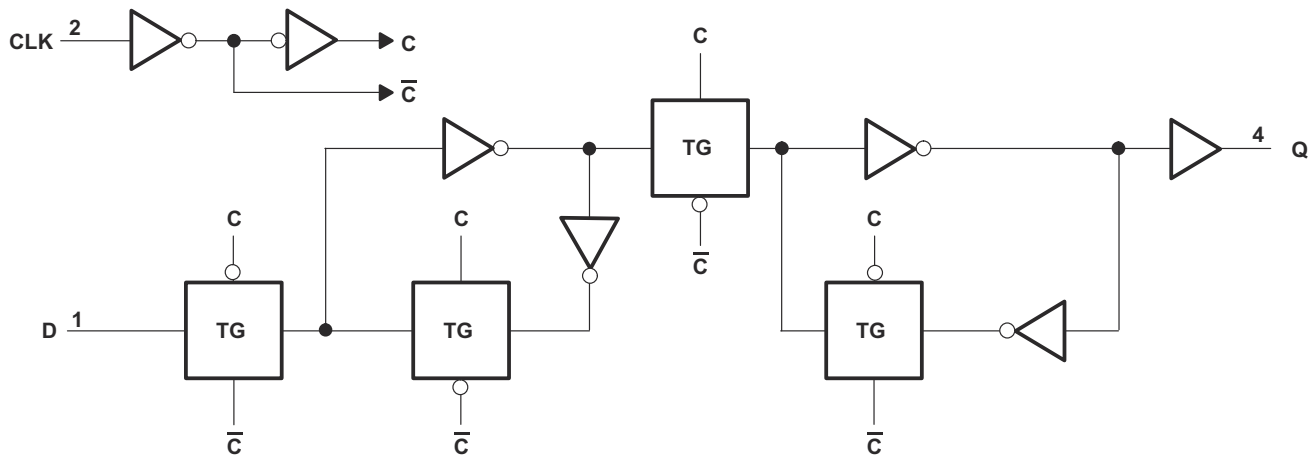
Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1G79 is a single positive-edge-triggered D-type flip-flop. Data at the input (D) is transferred to the output (Q) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Section 5.1](#) must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Section 5.5](#). The worst case resistance is calculated with the maximum input voltage, given in the [Section 5.3](#), and the maximum input leakage current, given in the [Section 5.5](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in [Section 5.3](#) to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input must be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Section 5.1](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

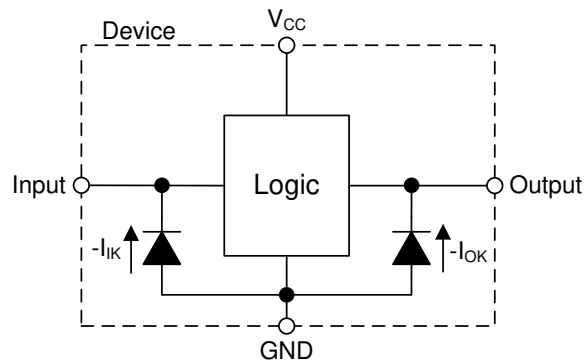


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Section 5.5](#).

7.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Section 5.1](#).

7.4 Device Functional Modes

[Table 7-1](#) lists the functional modes of SN74LVC1G79.

Table 7-1. Function Table

INPUTS		OUTPUT Y
CLK	D	
↑	H	H
↑	L	L
L	X	Q_0

8 Application and Implementation

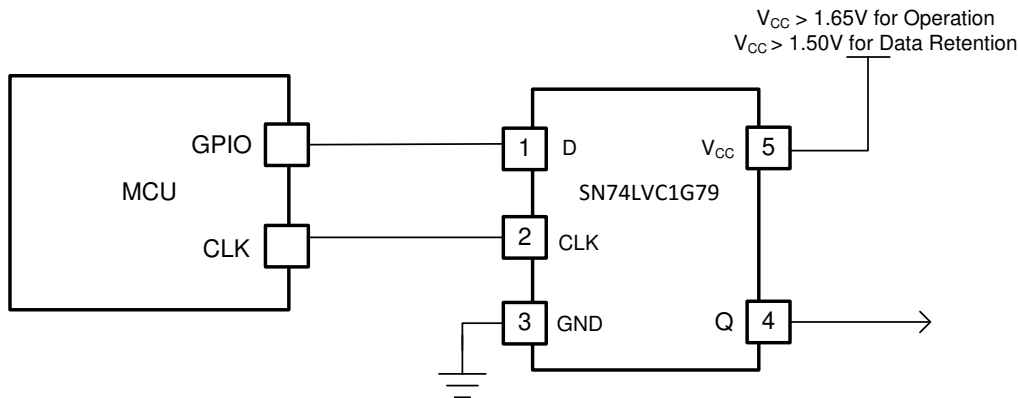
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A useful application for the SN74LVC1G79 is using it as a data latch with low-voltage data retention. This application implements the use of a microcontroller GPIO pin to act as a clock to set the output state and a second GPIO to provide the input data. If the SN74LVC1G79 is being powered from 1.8V and there is concern that a power glitch could exist as low as 1.5V, the device will retain the state of the Q output. An example of this data retention is shown in [Figure 8-2](#) where the V_{CC} drops to 1.5V and the Q output maintains the HIGH output state when V_{CC} returns to 1.8V. If the V_{CC} voltage drops below 1.5V, data retention is not guaranteed.

8.2 Typical Application



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Figure 8-1. Low Voltage Data Retention With SN74LVC1G79

8.2.1 Design Requirements

The SN74LVC1G79 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

8.2.2 Detailed Design Procedure

- Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in [Section 5.3](#).
 - For specified high and low levels, see V_{IH} and V_{IL} in [Section 5.3](#).
 - Input voltages are recommended to not go below 0V and not exceed 5.5V for any V_{CC} . See [Section 5.3](#).
- Recommended output conditions:
 - Load currents must not exceed $\pm 50\text{mA}$. See [Section 5.1](#).
 - Output voltages are recommended to not go below 0V and not exceed the V_{CC} voltage. See [Section 5.3](#).

8.2.3 Application Curve

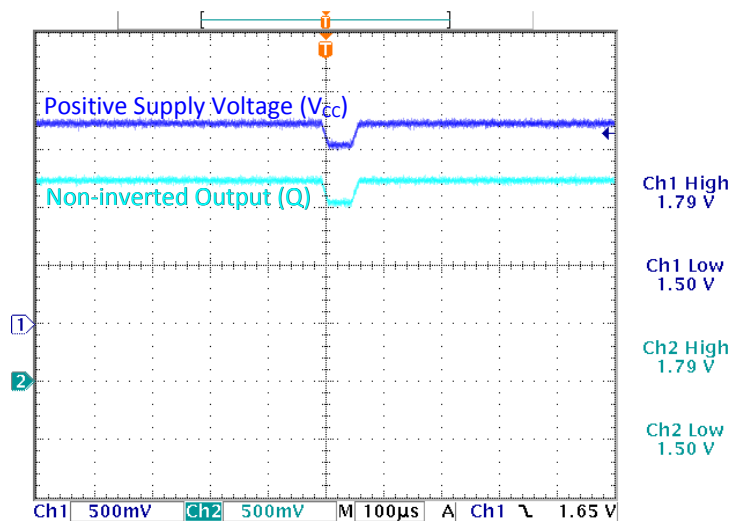


Figure 8-2. Data Retention With V_{CC} Glitch Down to 1.5V

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in [Section 5.3](#). A 0.1µF bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8-3](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

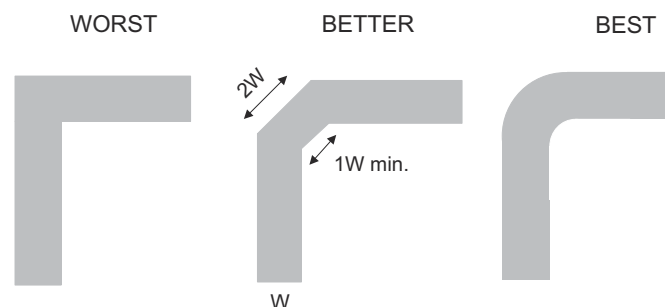


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [Understanding and Interpreting Standard Logic Data Sheets](#)
- Texas Instruments, [Power-Up Behavior of Clocked Devices](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

9.4 Trademarks

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 1, 2017 to August 12, 2026 (from Revision U (April 2017) to Revision V (August 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed Junction-to-ambient thermal resistance value for DBV package from: 247.2°C/W to: 357.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 154.5°C/W to: 263.7°C/W..	5
• Changed Junction-to-board characterization value for DBV package from: 86.8°C/W to: 264.4°C/W.....	5
• Changed Junction-to-top characterization value for DBV package from: 58°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DBV package from: 86.4°C/W to: 262.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DCK package from: 277.6°C/W to: 371°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 179.5°C/W to: 297.5°C/W..	5
• Changed Junction-to-board characterization value for DCK package from: 75.9°C/W to: 258.6°C/W.....	5
• Changed Junction-to-top characterization value for DCK package from: 49.7°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DCK package from: 75.1°C/W to: 256.2°C/W.....	5
• Changed Junction-to-ambient thermal resistance value for DRL package from: 294.3°C/W to: 364.1°C/W.....	5
• Changed Junction-to-case (top) thermal resistance value for DRL package from: 129.9°C/W to: 280.6°C/W..	5
• Changed Junction-to-board characterization value for DRL package from: 143.4°C/W to: 261.5°C/W.....	5
• Changed Junction-to-top characterization value for DRL package from: 14.3°C/W to: 195.6°C/W.....	5
• Changed Junction-to-board characterization value for DRL package from: 144°C/W to: 259.2°C/W.....	5
• Added <i>Thermal Information</i> table.....	5

Changes from Revision T (December 2013) to Revision U (April 2017)

	Page
• Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed thermal information to align with JEDEC standards.	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G79DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)
SN74LVC1G79DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)
SN74LVC1G79DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)
SN74LVC1G79DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)
SN74LVC1G79DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C795, C79F, C79J, C79R)
SN74LVC1G79DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C79F
SN74LVC1G79DBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C79F
SN74LVC1G79DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)
SN74LVC1G79DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)
SN74LVC1G79DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)
SN74LVC1G79DCKRG4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5
SN74LVC1G79DCKRG4.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5
SN74LVC1G79DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)
SN74LVC1G79DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CR5, CRF, CRJ, CR R)
SN74LVC1G79DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5
SN74LVC1G79DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CR5
SN74LVC1G79DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CR7, CRR)
SN74LVC1G79DRLR.A	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CR7, CRR)
SN74LVC1G79DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CR7, CRR)
SN74LVC1G79YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CR7, CRN)
SN74LVC1G79YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CR7, CRN)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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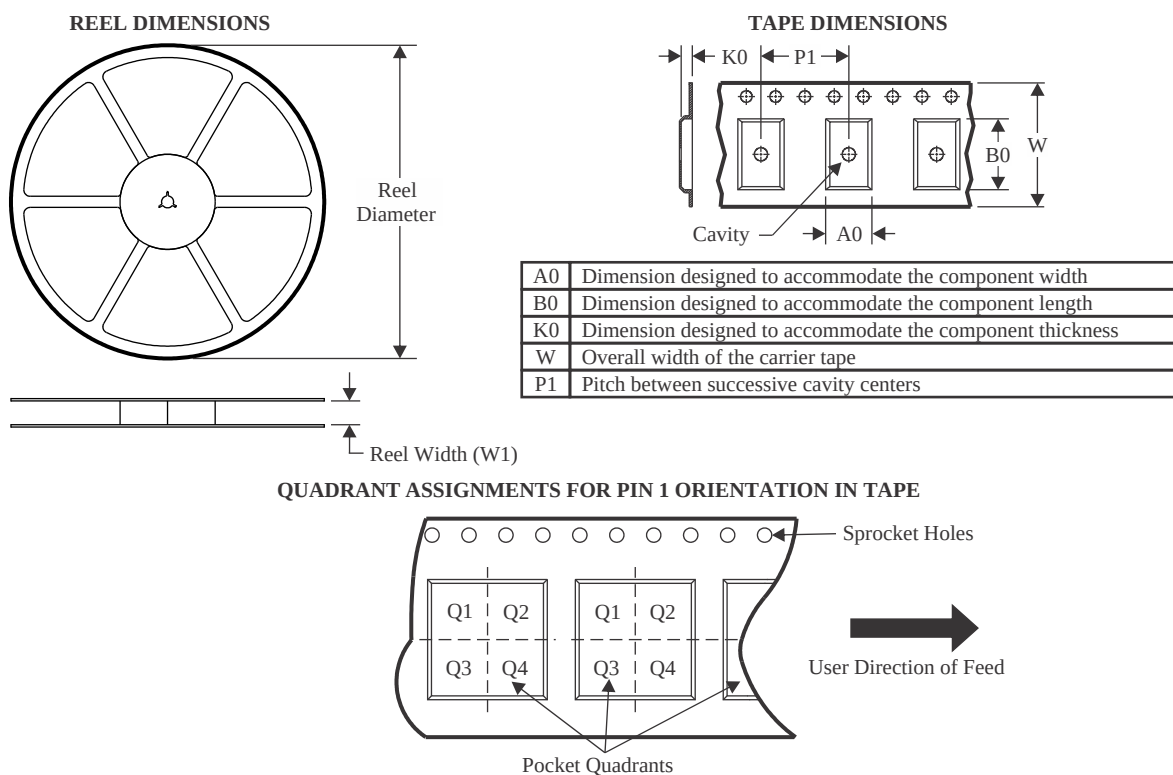
OTHER QUALIFIED VERSIONS OF SN74LVC1G79 :

- Automotive : [SN74LVC1G79-Q1](#)
- Enhanced Product : [SN74LVC1G79-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

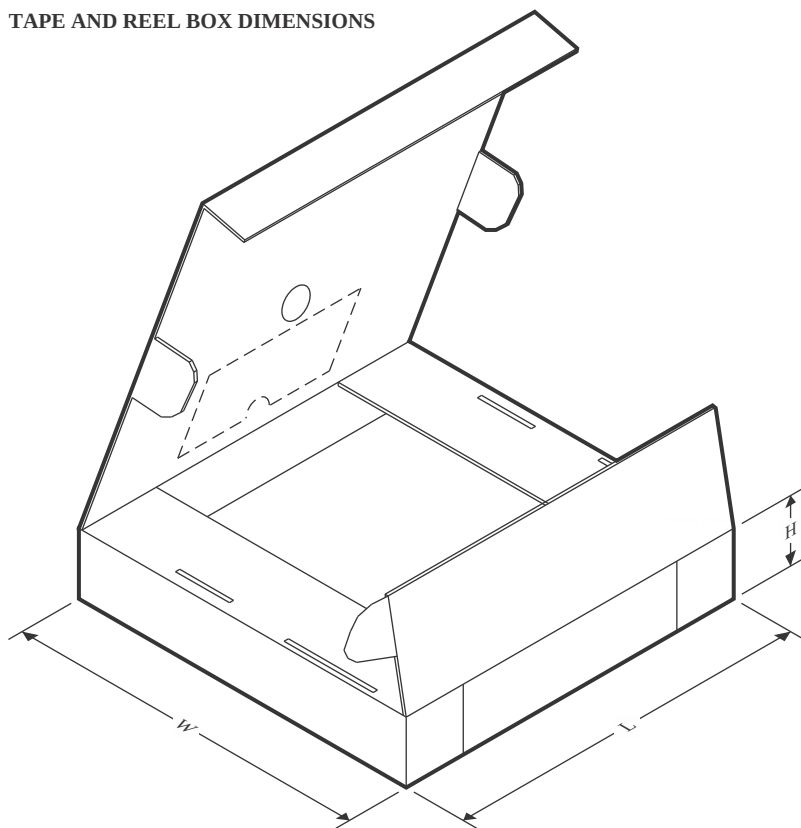


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G79DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G79DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G79DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G79DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G79DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G79DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G79DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G79YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G79DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G79DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G79DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G79DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DCKT	SC70	DCK	5	250	210.0	185.0	35.0
SN74LVC1G79DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G79DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G79DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G79YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

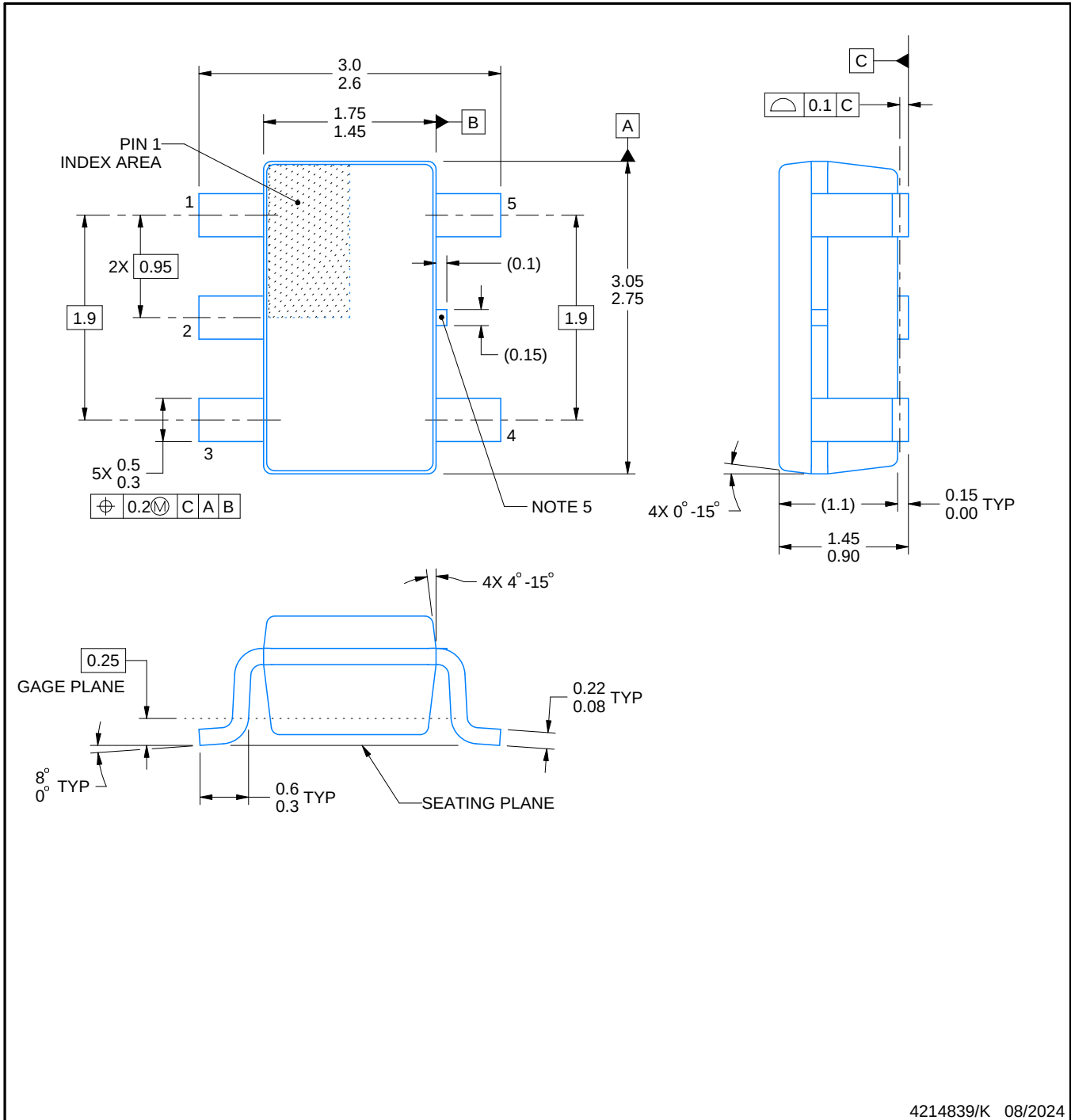


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

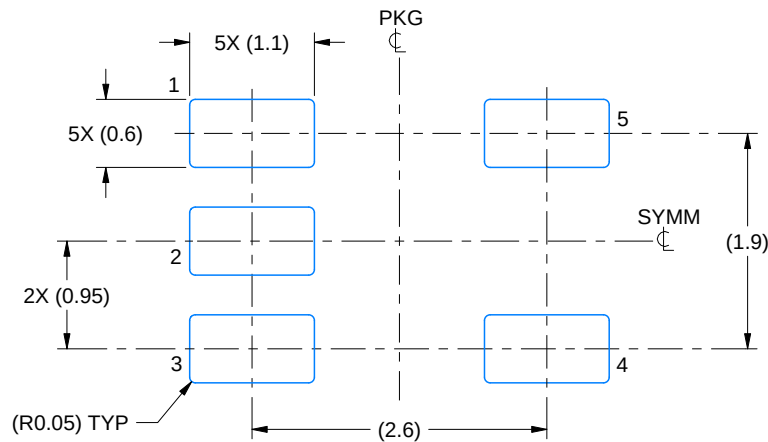
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

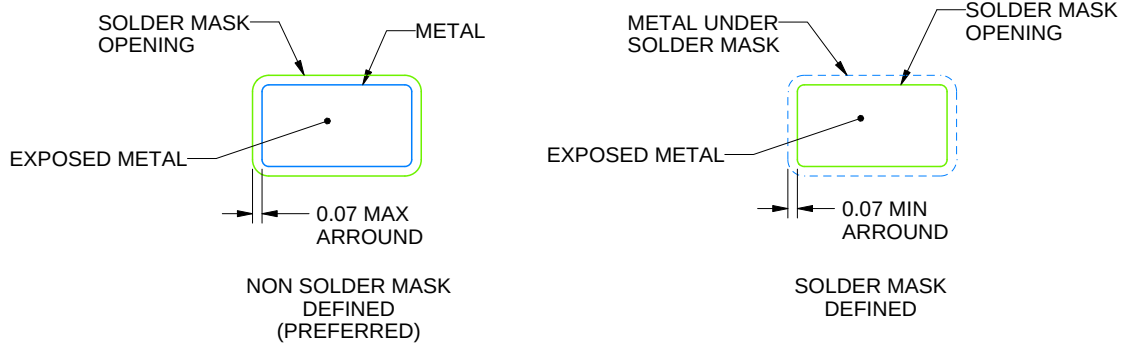
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

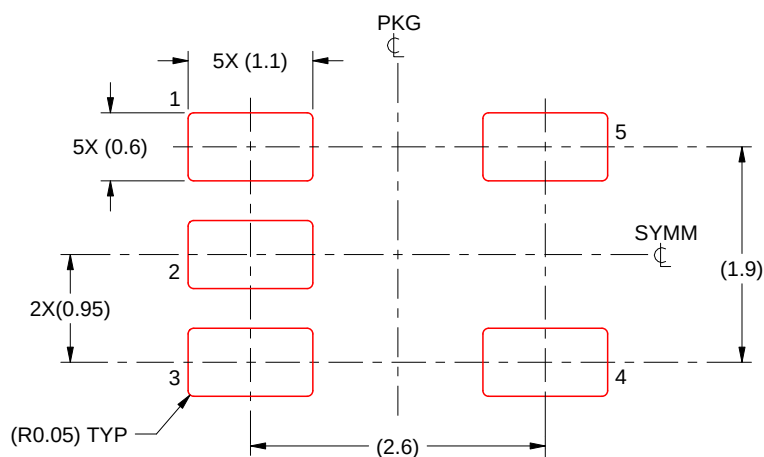
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

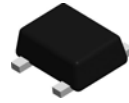
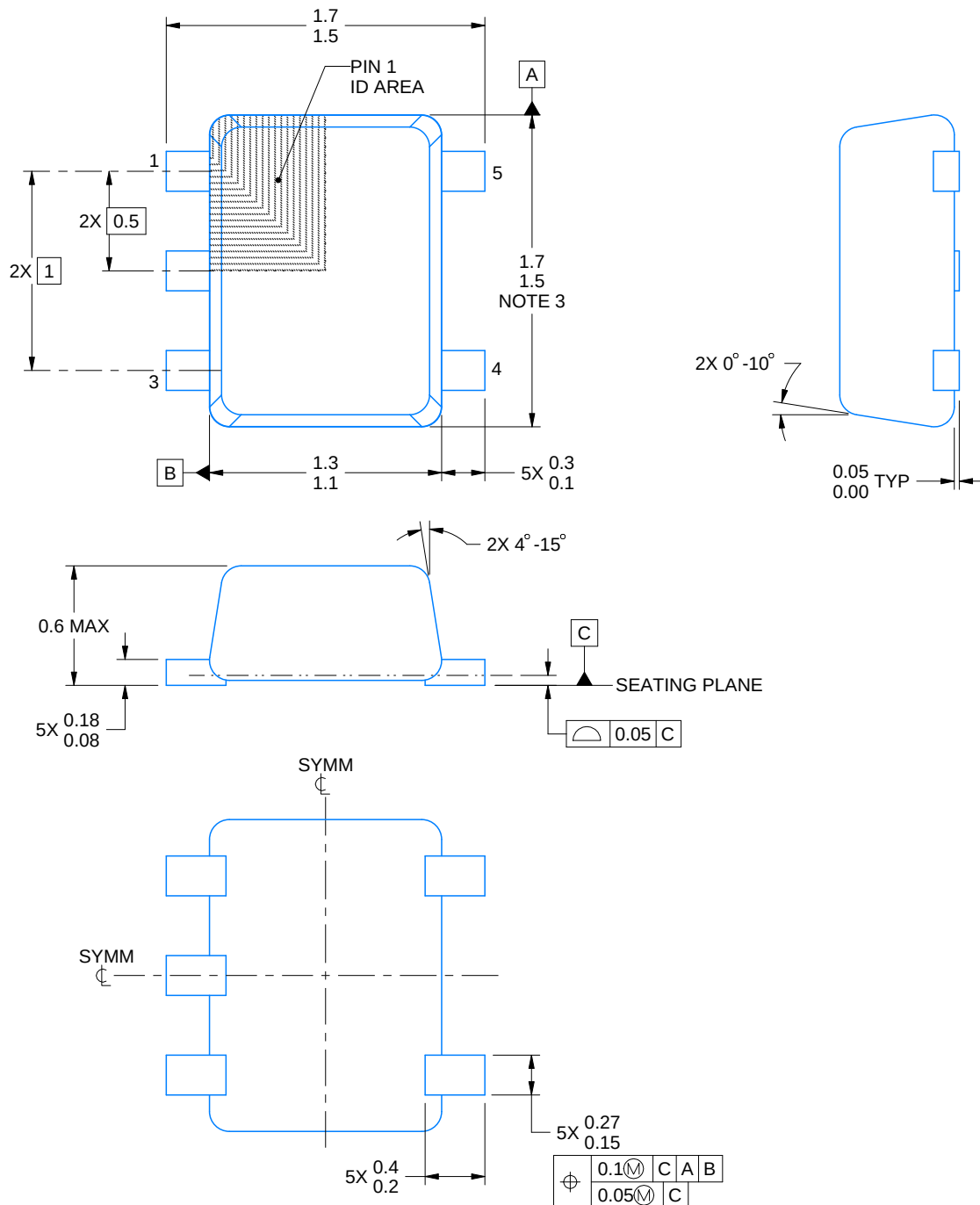


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220753/E 11/2024

NOTES:

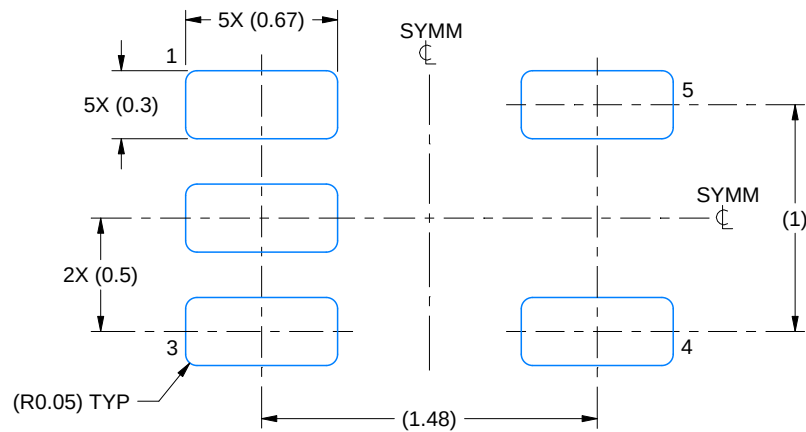
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

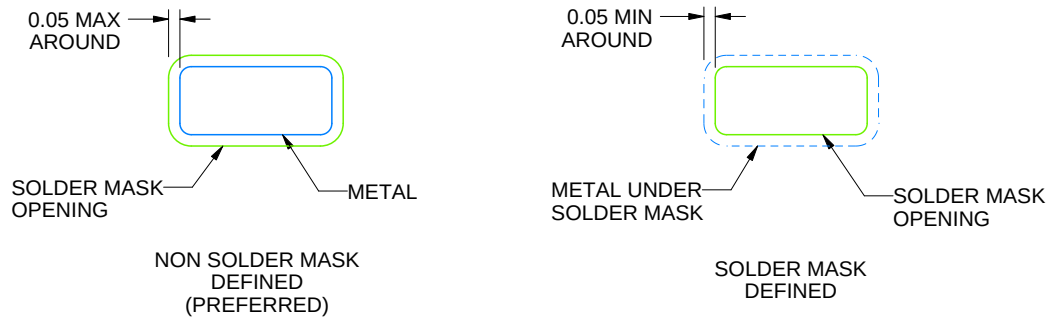
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

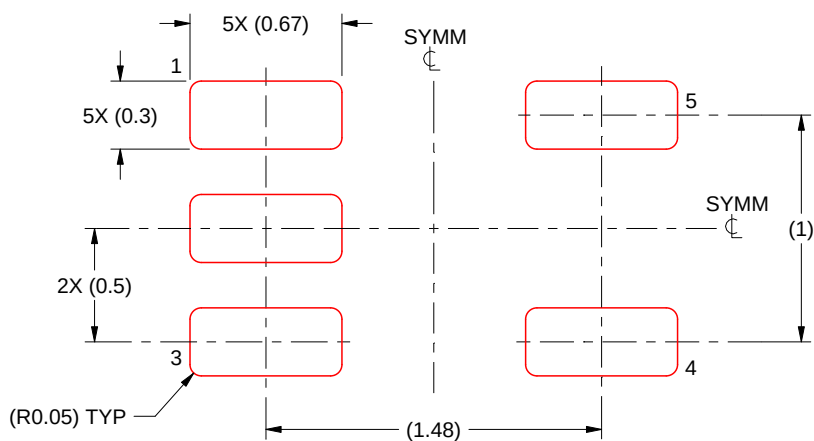
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

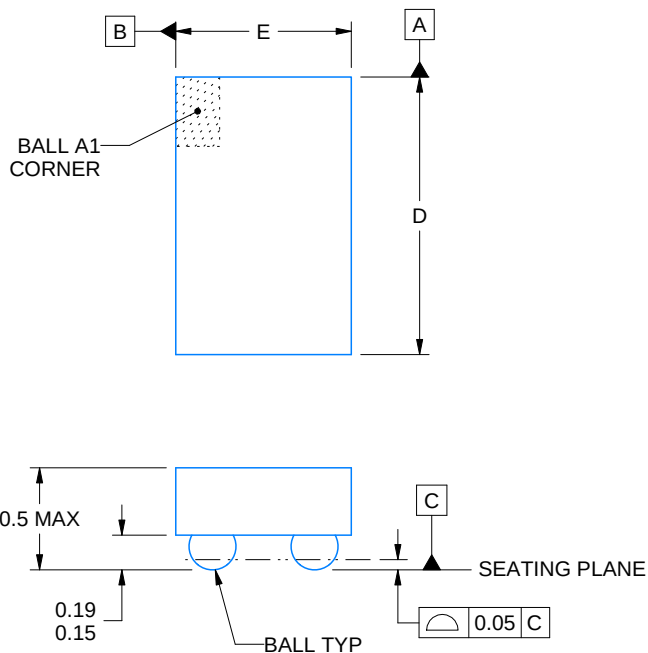
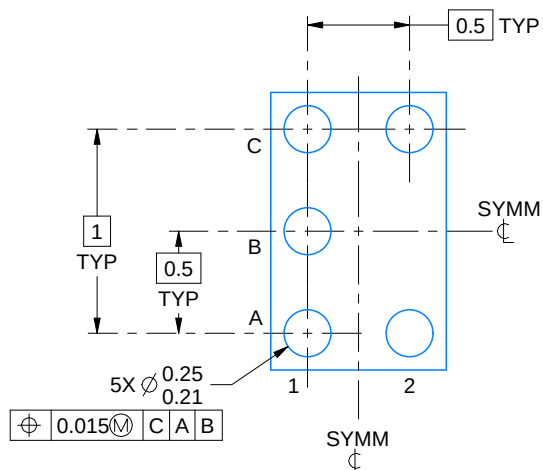
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm
E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

NOTES:

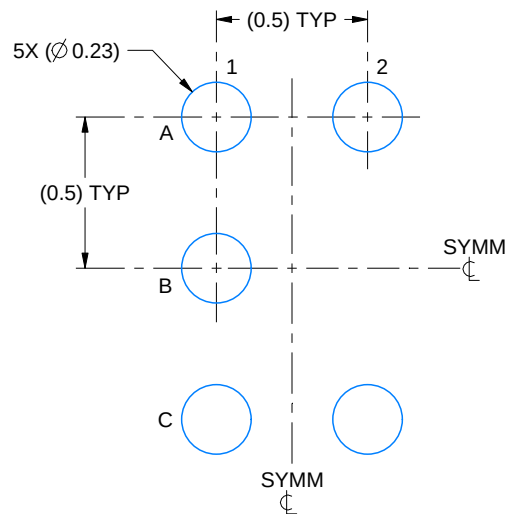
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

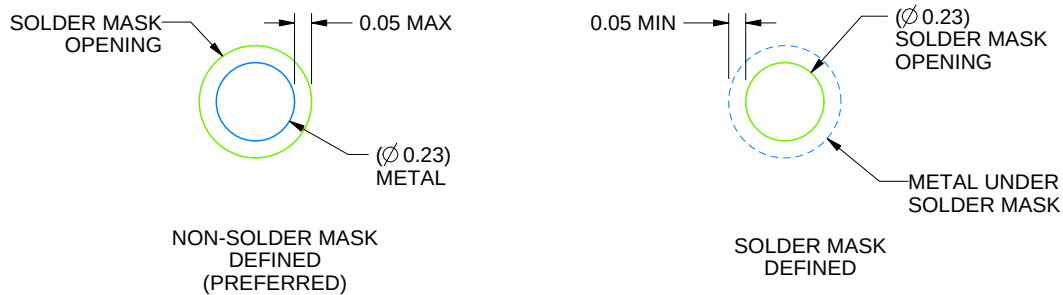
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

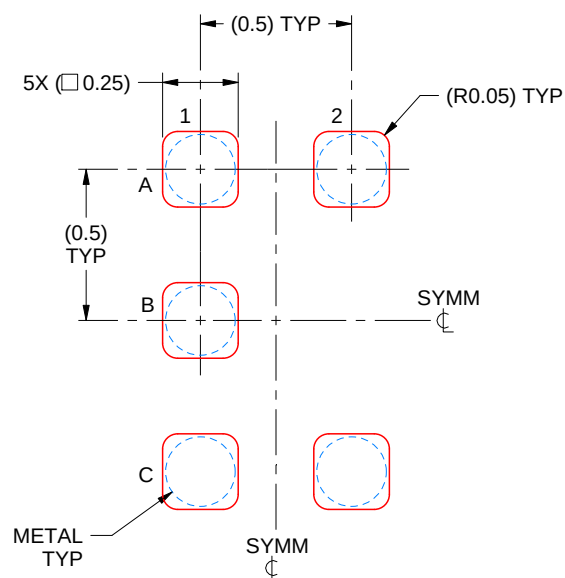
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

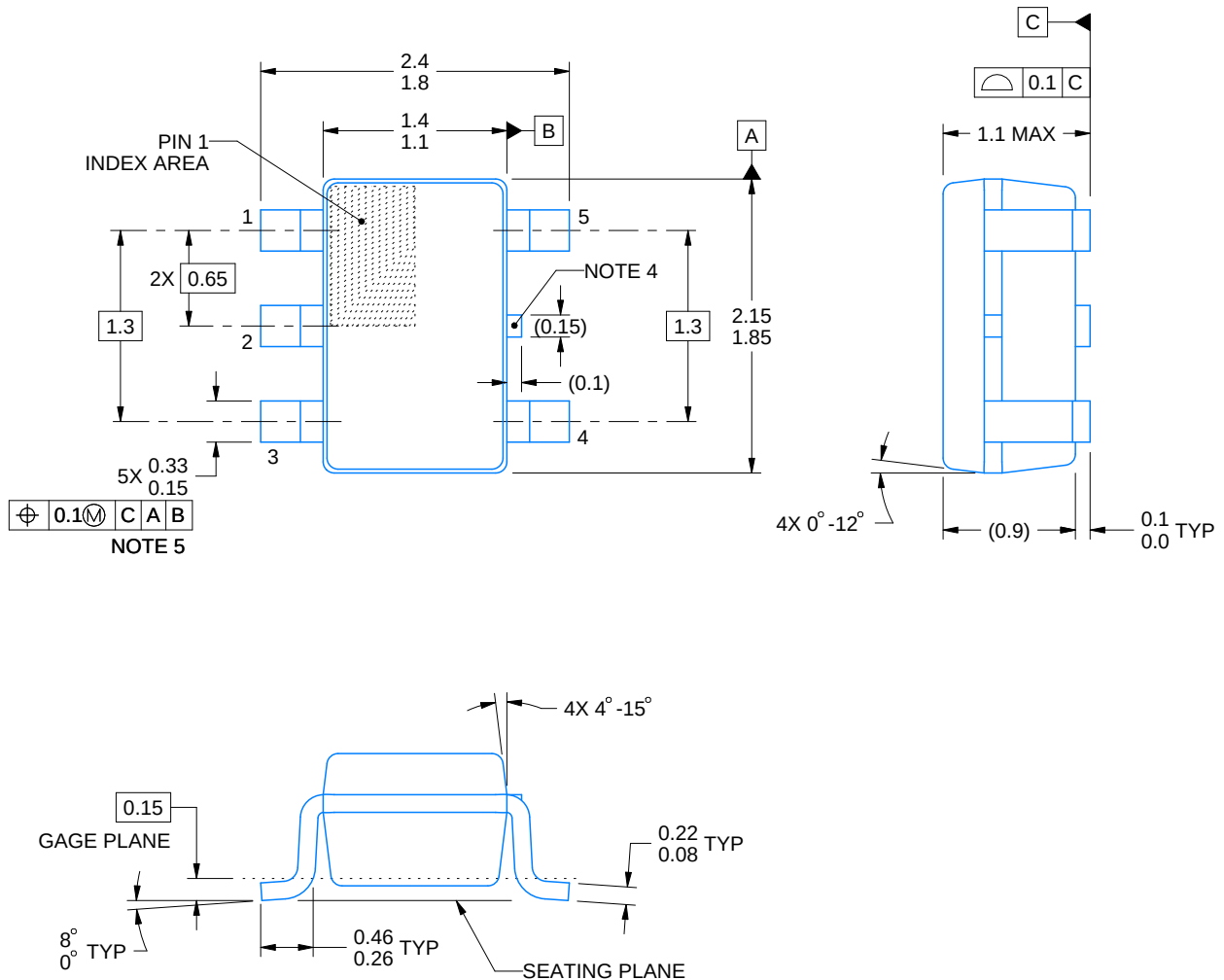


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

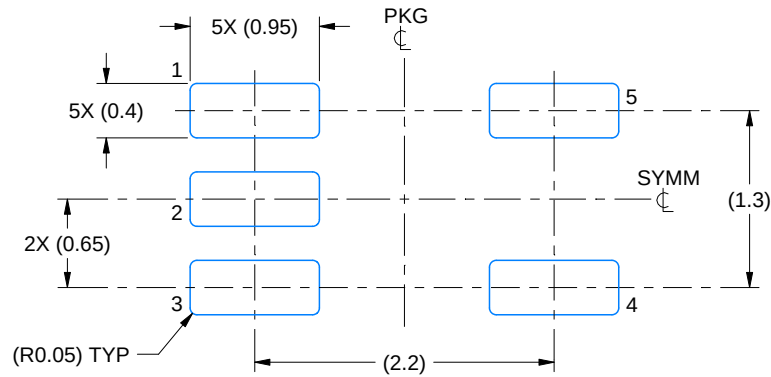
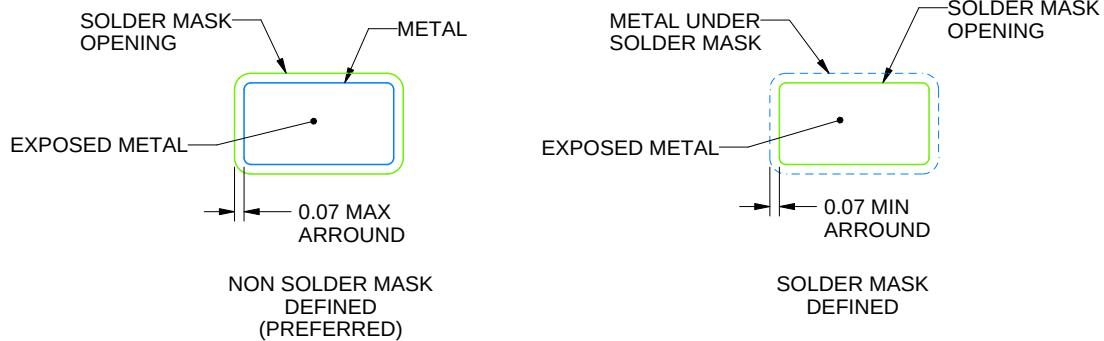
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4214834/G 11/2024

NOTES:

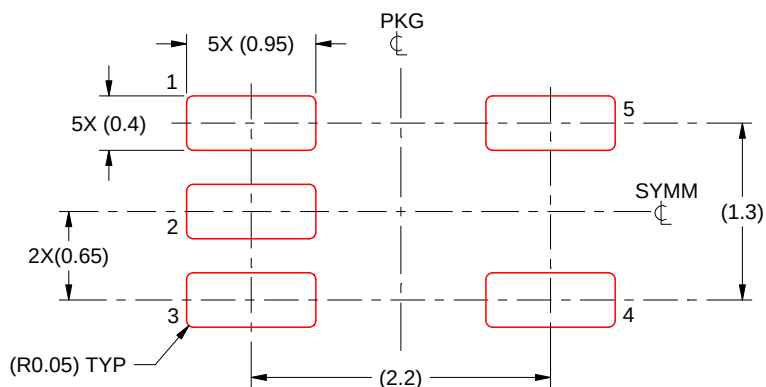
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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