SN74LVC1GX04 Crystal Oscillator Driver

1 Features

- Available in Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- One Unbuffered Inverter (SN74LVC1GU04) and One Buffered Inverter (SN74LVC1G04)
- Suitable for Commonly Used Clock Frequencies:
  - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Maximum t_{pd} of 2.4 ns at 3.3 V
- Low Power Consumption, 10-μA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Crystal Oscillators
- Clock Generation

3 Description

The SN74LVC1GX04 device is designed for 1.65-V to 5.5-V V_{CC} operation. This device incorporates the SN74LVC1GU04 (inverter with unbuffered output) and the SN74LVC1G04 (inverter) functions into a single device. The LVC1GX04 is optimized for use in crystal oscillator applications.

X1 and X2 can be connected to a crystal or resonator in oscillator applications. The device provides an additional buffered inverter (Y) for signal conditioning (see Figure 5). The additional buffered inverter improves the signal quality of the crystal oscillator output by making it rail to rail.

NanoStar and NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

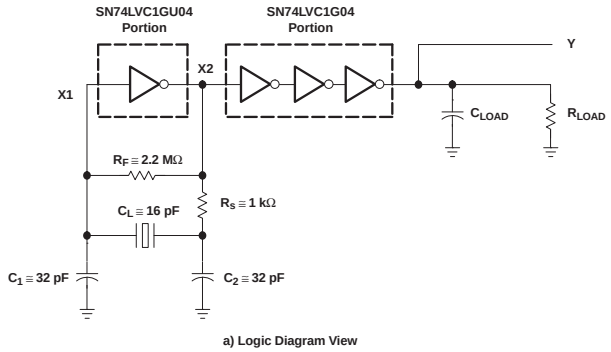
This device is fully specified for partial-power-down applications using I_{off} (Y output only). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1GX04DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LVC1GX04DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LVC1GX04DRL	SOT (6)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



a) Logic Diagram View

SN74LVC1GX04 includes both dotted portions

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

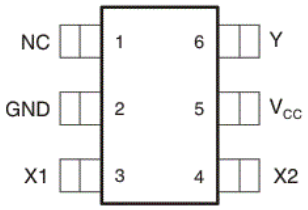
Changes from Revision C (December 2013) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

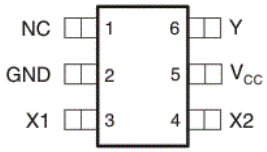
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5 Pin Configuration and Functions

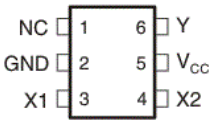
DBV Package
6-Pin SOT-23
Top View



DCK Package
6-Pin SC70
Top View



DRL Package
6-Pin SOT
Top View



See mechanical drawings for dimensions.

NC – No internal connection.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	–	Ground
NC	1	–	No internal connection
VCC	5	–	Supply power
X1	3	I	Amplifier input
X2	4	O	Amplifier output
Y	6	O	Main output to other logic

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to Y output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
		Crystal oscillator use	2		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 5.5 V	0.75 × V_{CC}		V
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 5.5 V		0.25 × V_{CC}	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	X2, Y	0	V_{CC}	V
		Y output only, Power-down mode, V_{CC} = 0 V	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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Recommended Operating Conditions[1] (continued)

			MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ±0.5 V		10	
T_A	Operating free-air temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1GX04			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	259	142	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	V_I = 5.5 V or GND	T_A = –40°C to 125°C	1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA			1.65 V	1.2			
		I_{OH} = –8 mA			2.3 V	1.9			
		I_{OH} = –16 mA			3 V	2.4			
		I_{OH} = –24 mA				2.3			
		I_{OH} = –32 mA			4.5 V	3.8			
V_{OL}		I_{OL} = 100 µA	V_I = 5.5 V or GND	T_A = –40°C to 125°C	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA			1.65 V			0.45	
		I_{OL} = 8 mA			2.3 V			0.3	
		I_{OL} = 16 mA		T_A = –40°C to 125°C	3 V			0.4	
		I_{OL} = 24 mA		T_A = –40°C to 85°C	3 V			0.55	
				T_A = –40°C to 125°C				0.63	
		I_{OL} = 32 mA		T_A = –40°C to 85°C	4.5 V			0.55	
				T_A = –40°C to 125°C				0.7	
I_I	X1	V_I = 5.5 V or GND	T_A = –40°C to 125°C		0 to 5.5 V			±5	µA
I_{off}	X1, Y	V_I or V_O = 5.5 V	T_A = –40°C to 125°C		0			±10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	T_A = –40°C to 125°C		1.65 V to 5.5 V			10	µA
C_i		V_I = V_{CC} or GND			3.3 V		7		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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6.6 Switching Characteristics, SN74LVC1GX04

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	V_{CC}	MIN	MAX	UNIT
t_{pd}	X1	X2	–40°C to 85°C	V_{CC} = 1.8 V ± 0.15 V	1	4	ns
				V_{CC} = 2.5 V ± 0.2 V	0.8	2.6	
				V_{CC} = 3.3 V ± 0.3 V	0.6	2.4	
				V_{CC} = 5 V ± 0.5 V	0.5	2	
		Y (1)	–40°C to 85°C	V_{CC} = 1.8 V ± 0.15 V	3.5	10	
				V_{CC} = 2.5 V ± 0.2 V	2.2	6	
				V_{CC} = 3.3 V ± 0.3 V	2	5	
				V_{CC} = 5 V ± 0.5 V	1.5	3.5	

(1) X2 – no external load

6.7 Switching Characteristics, SN74LVC1GX04

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	V_{CC}	MIN	MAX	UNIT
t_{pd}	X1	X2	–40°C to 85°C	V_{CC} = 1.8 V ± 0.15 V	1.1	7	ns
				V_{CC} = 2.5 V ± 0.2 V	0.8	4	
				V_{CC} = 3.3 V ± 0.3 V	0.8	3.7	
				V_{CC} = 5 V ± 0.5 V	0.8	3	
		Y (1)	–40°C to 85°C	V_{CC} = 1.8 V ± 0.15 V	3.8	18	
				V_{CC} = 2.5 V ± 0.2 V	2	7.4	
				V_{CC} = 3.3 V ± 0.3 V	2	7.8	
				V_{CC} = 5 V ± 0.5 V	2	5	

(1) X2 – no external load

6.8 Switching Characteristics, SN74LVC1GX04

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	V_{CC}	MIN	MAX	UNIT
t_{pd}	X1	X2	–40°C to 125°C	V_{CC} = 1.8 V ± 0.15 V	1.1	8	ns
				V_{CC} = 2.5 V ± 0.2 V	0.8	5	
				V_{CC} = 3.3 V ± 0.3 V	0.8	4.3	
				V_{CC} = 5 V ± 0.5 V	0.8	3.5	
		Y (1)	–40°C to 125°C	V_{CC} = 1.8 V ± 0.15 V	3.8	20	
				V_{CC} = 2.5 V ± 0.2 V	2	8.4	
				V_{CC} = 3.3 V ± 0.3 V	2	8.8	
				V_{CC} = 5 V ± 0.5 V	2	5.5	

(1) X2 – no external load

6.9 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	V_{CC} = 1.8 V	22	pF
			V_{CC} = 2.5 V	22	
			V_{CC} = 3.3 V	24	
			V_{CC} = 5 V	35	

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6.10 Typical Characteristics

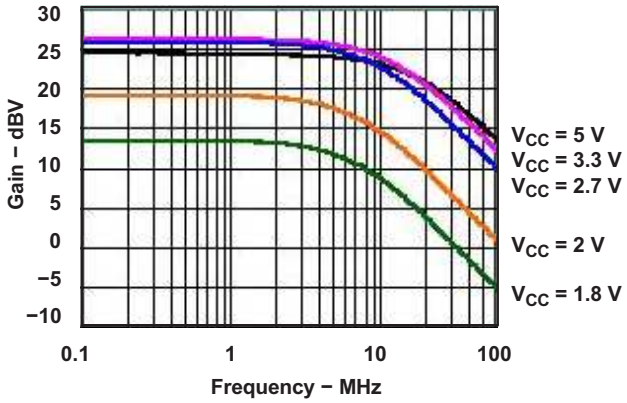
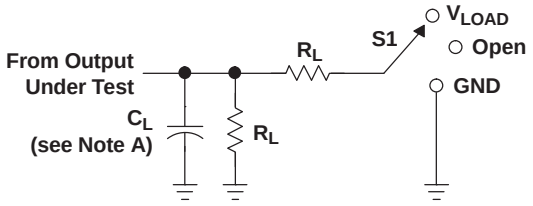


Figure 1. Open-Loop Gain Characteristics of Oscillator Amplifier

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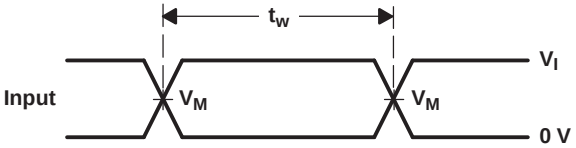
7 Parameter Measurement Information



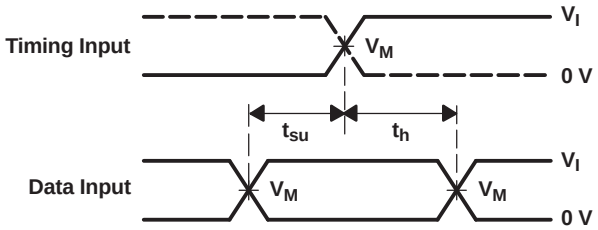
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

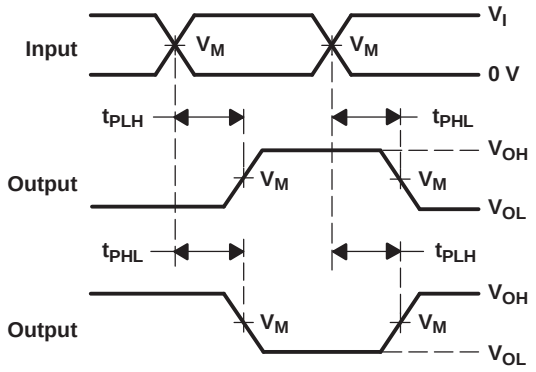
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V



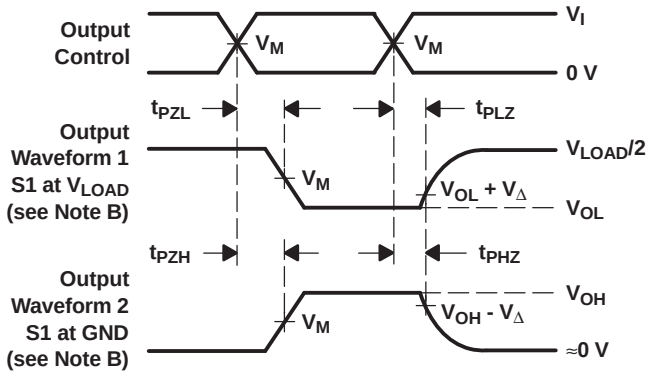
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



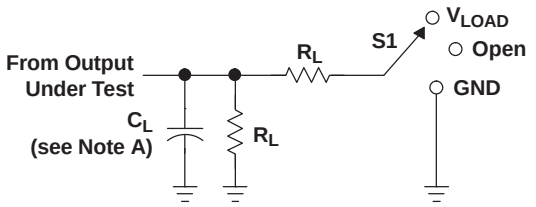
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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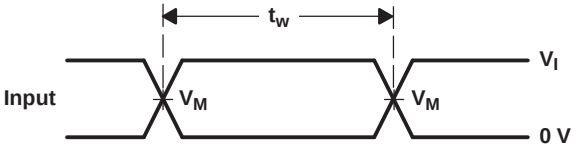
Parameter Measurement Information (continued)



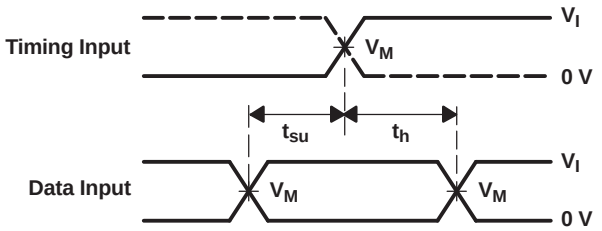
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

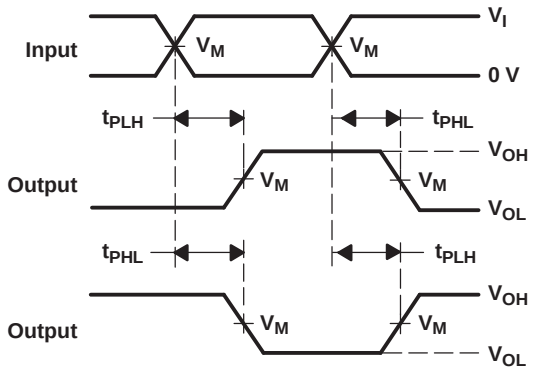
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



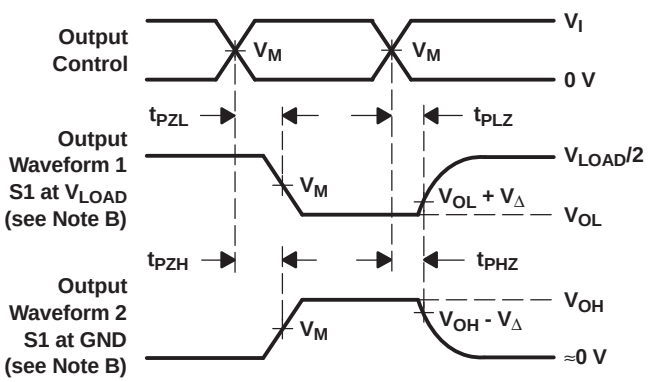
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



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ENABLE AND DISABLE TIMES
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NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

The SN74LVC1GX04 is optimized for creating a crystal oscillator circuit with a buffered square-wave output. This device is fully specified for partial-power-down applications using I_{off} (Y output only). The I_{off} circuitry disables the outputs, preventing damaging current back-flow through the device when it is powered down.

8.2 Functional Block Diagram

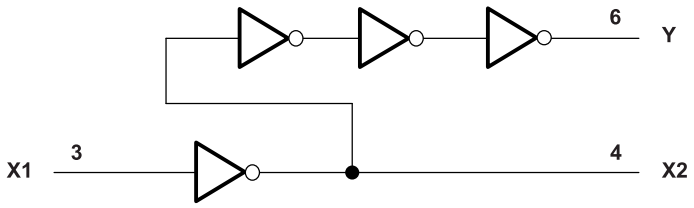


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

The first inverter is used as a linear amplifier for crystal oscillator.

The last three inverters ensure a fast edge square-wave at the Y output.

8.4 Device Functional Modes

The only intended device use is to generate a square-wave output using a crystal to set the operating frequency.

Table 1. Function Table

INPUT X1	OUTPUTS	
	X2	Y
H	L	H
L	H	L

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1GX04 contains a buffered and unbuffered inverter for the specific purpose of creating a crystal oscillator and driver with limited external components.

9.2 Typical Application

Figure 5 shows a typical application of the SN74LVC1GX04 in a Pierce oscillator circuit. The buffered inverter (SN74LVC1G04 portion) produces a rail-to-rail voltage waveform. The recommended load for the crystal shown in this example is 16 pF. The value of the recommended load (C_L) can be found in the crystal manufacturer's data sheet.

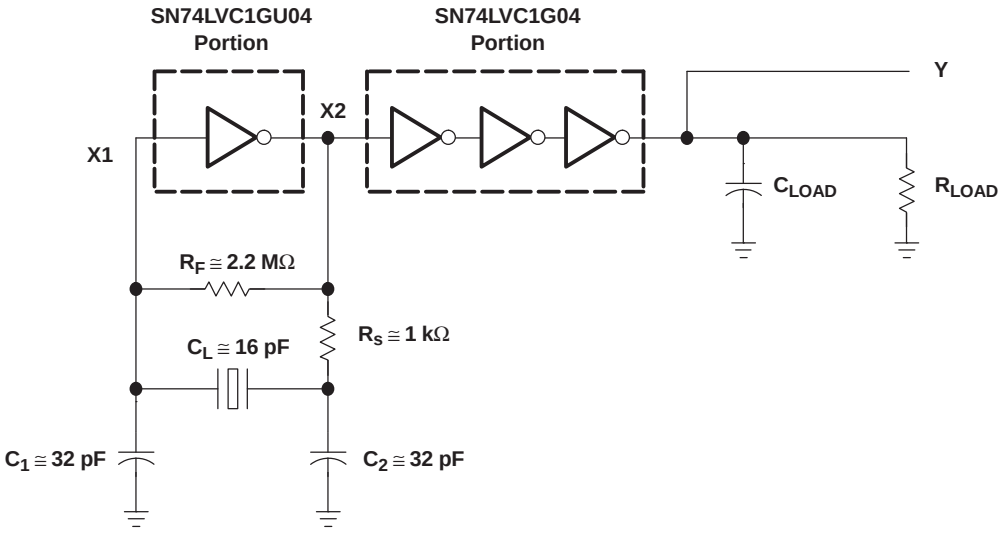
Values of C_1 and C_2 are chosen to calculate C_L in Equation 1 where $C_1 \equiv C_2$.

$$C_L = \frac{C_1 C_2}{C_1 + C_2} \quad (1)$$

R_S is the current-limiting resistor, and the value depends on the maximum power dissipation of the crystal. Generally, the recommended value of R_S is specified in the crystal manufacturer's data sheet and, usually, this value is approximately equal to the reactance of C_2 at resonance frequency, that is seen in Equation 2.

$$R_S = X_{C_2} \quad (2)$$

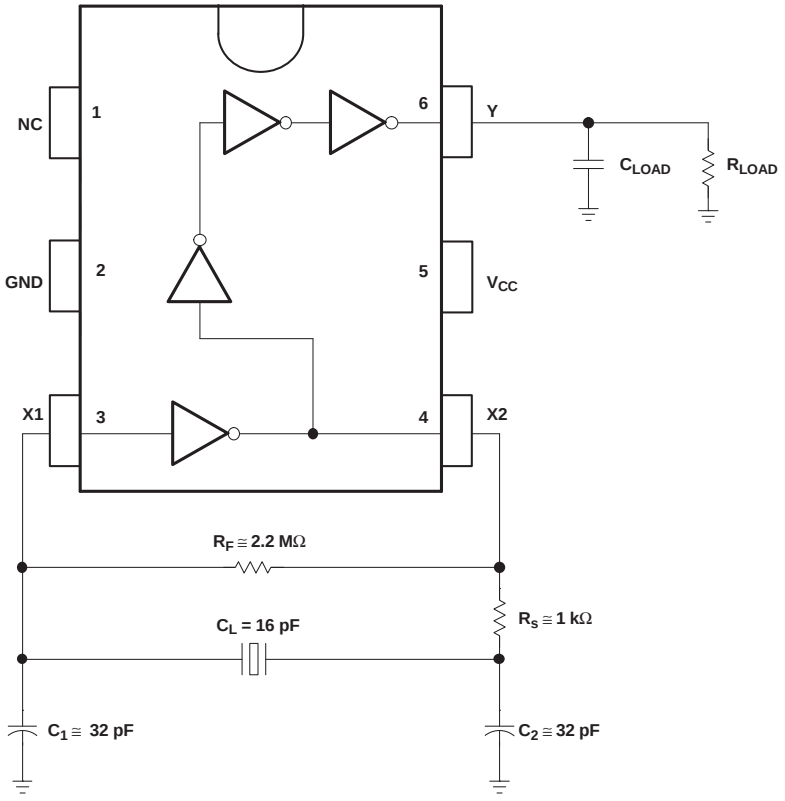
R_F is the feedback resistor that is used to bias the inverter in the linear region of operation. Usually, the value is chosen to be within 1 MΩ to 10 MΩ.



a) Logic Diagram View

Figure 5. Oscillator Circuit

Typical Application (continued)



b) Oscillator Circuit in DBV or DCK Pinout

Figure 6. Oscillator Circuit (Continued)

9.2.1 Design Requirements

The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases the closed-loop gain of the oscillator circuit. The value of R_s can be decreased to increase the closed-loop gain, while maintaining the power dissipation of the crystal within the maximum limit.

R_s and C_2 form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.

C_2 can be increased over C_1 to increase the phase shift and help in start-up of the oscillator. Increasing C_2 may affect the duty cycle of the output voltage.

At high frequency, phase shift due to R_s becomes significant. In this case, R_s can be replaced by a capacitor to reduce the phase shift.

9.2.2 Detailed Design Procedure

After the selection of proper component values, the oscillator circuit should be tested using these components. To ensure that the oscillator circuit performs within the *Recommended Operating Conditions*(1) , follow these steps:

1. Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
2. When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest V_{CC} and highest V_{CC}.
3. Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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Typical Application (continued)

9.2.3 Application Curve

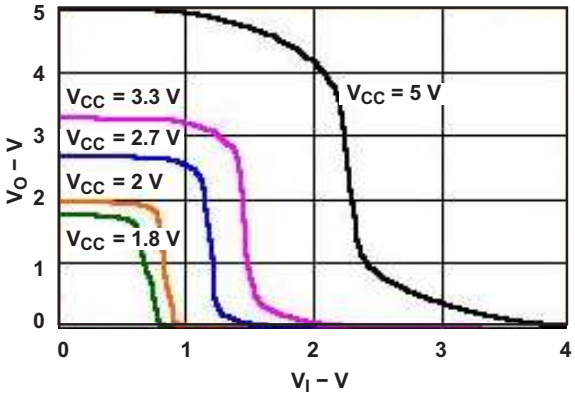


Figure 7. V_O vs V_I Characteristics of Oscillator Amplifier

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*(1) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01-µF or 0.022-µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

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11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

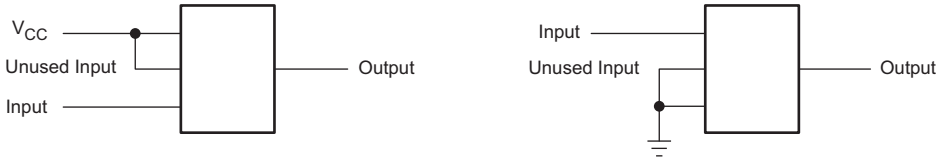


Figure 8. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoStar, NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1GX04DCKTG4	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D25, D2R)
74LVC1GX04DCKTG4.B	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D25, D2R)
SN74LVC1GX04DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX45, CX4R)
SN74LVC1GX04DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX45, CX4R)
SN74LVC1GX04DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX45
SN74LVC1GX04DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX45
SN74LVC1GX04DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX45, CX4R)
SN74LVC1GX04DBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX45, CX4R)
SN74LVC1GX04DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(D25, D2J, D2K, D2R)
SN74LVC1GX04DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(D25, D2J, D2K, D2R)
SN74LVC1GX04DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D25, D2K, D2R)
SN74LVC1GX04DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D25, D2K, D2R)
SN74LVC1GX04DCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(D25, D2J, D2R)
SN74LVC1GX04DCKT.B	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(D25, D2J, D2R)
SN74LVC1GX04DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(1K6, D27, D2R)
SN74LVC1GX04DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1K6, D27, D2R)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1GX04 :

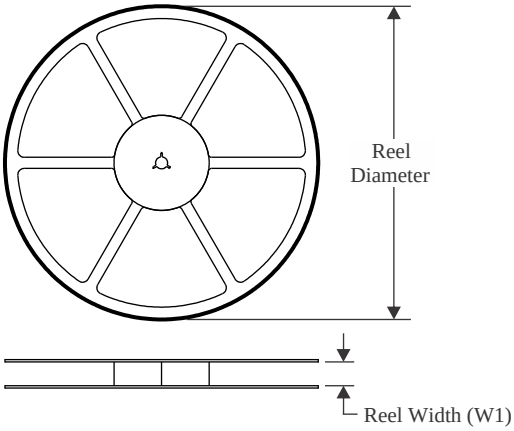
- Enhanced Product : SN74LVC1GX04-EP

NOTE: Qualified Version Definitions:

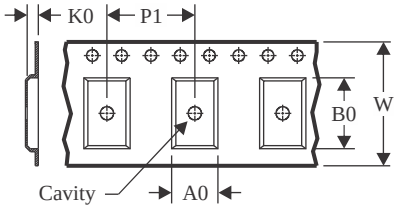
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

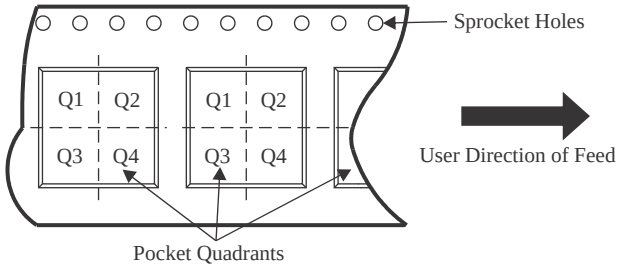


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

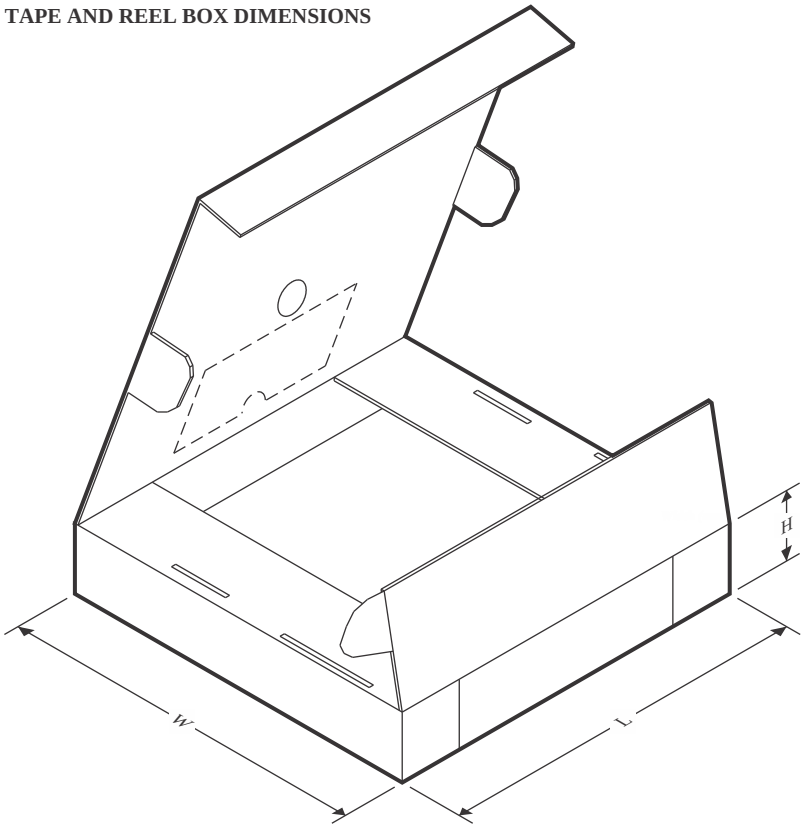


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1GX04DCKTG4	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1GX04DBVRG4	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1GX04DCKRG4	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1GX04DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1GX04DCKTG4	SC70	DCK	6	250	183.0	183.0	20.0
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1GX04DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1GX04DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1GX04DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1GX04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1GX04DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1GX04DCKRG4	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1GX04DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1GX04DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

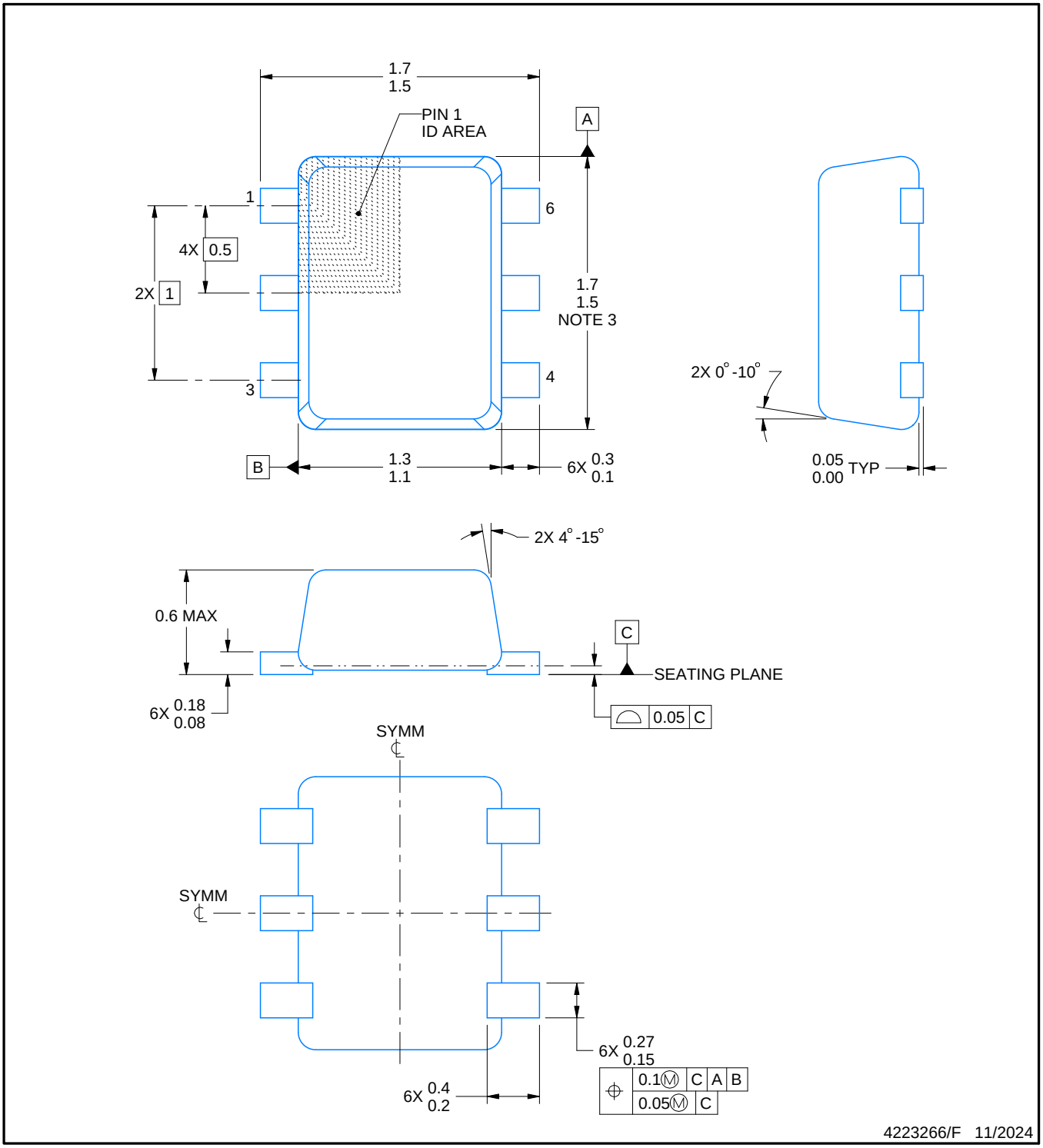


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

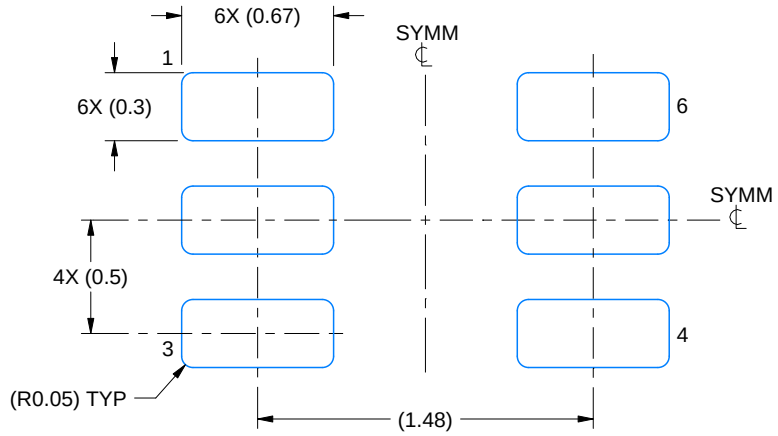
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

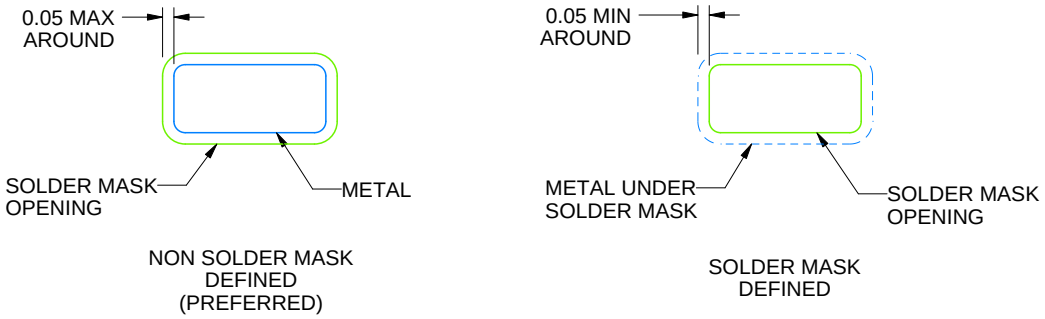
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

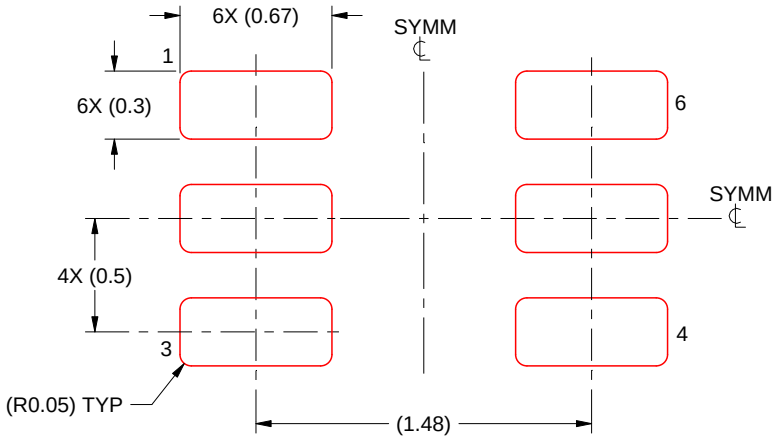
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

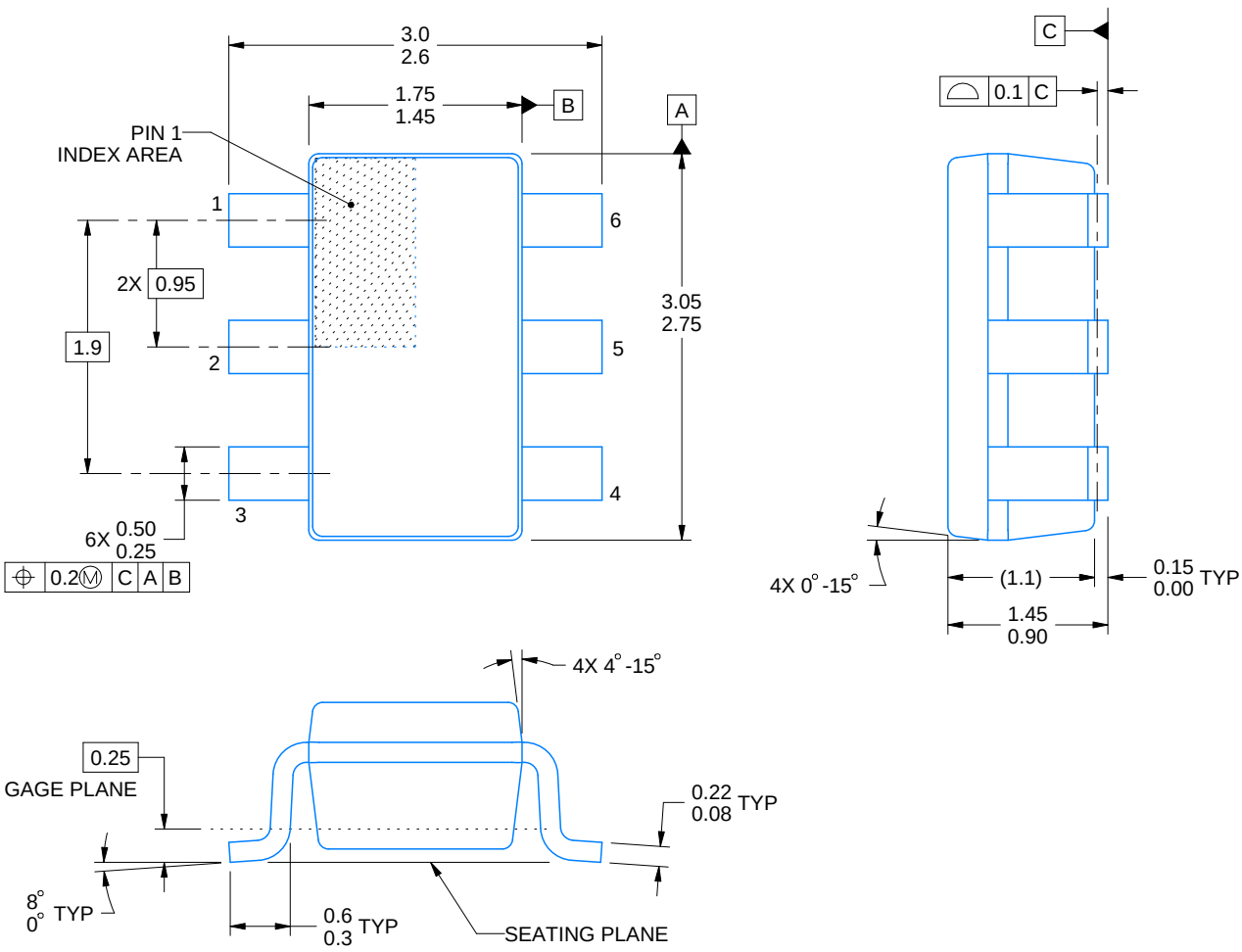
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

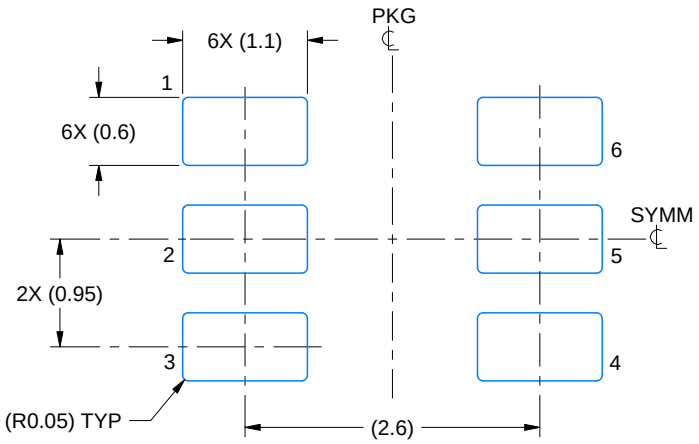
SMALL OUTLINE TRANSISTOR



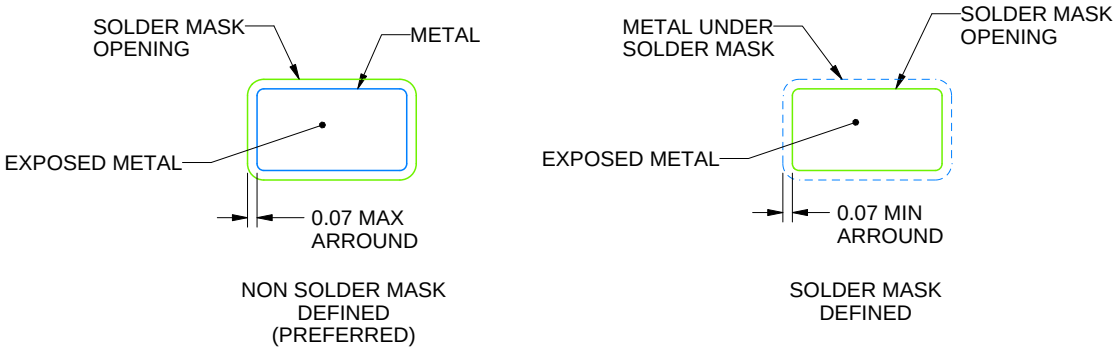
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

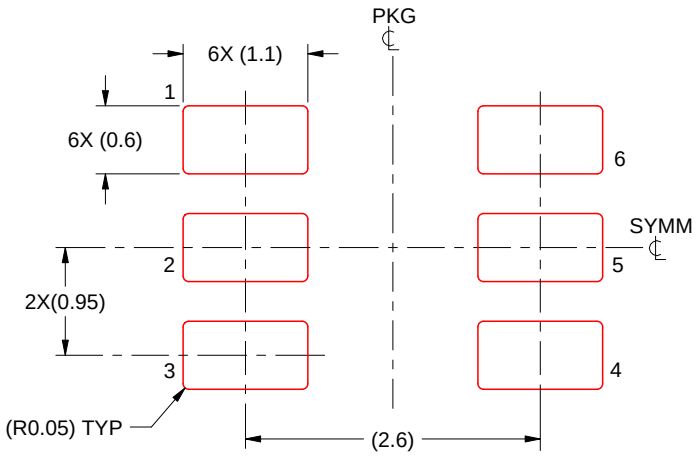


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

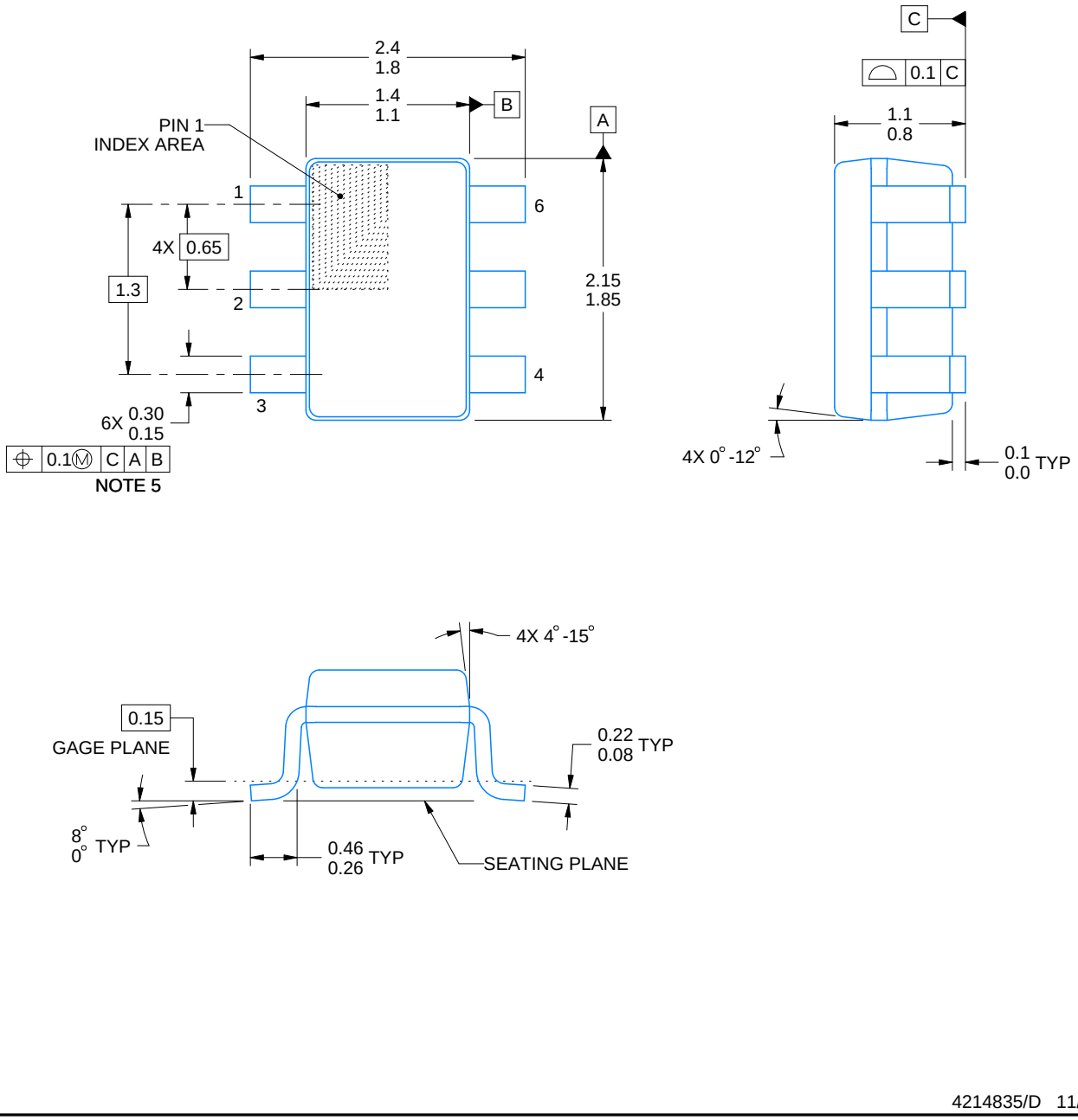
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

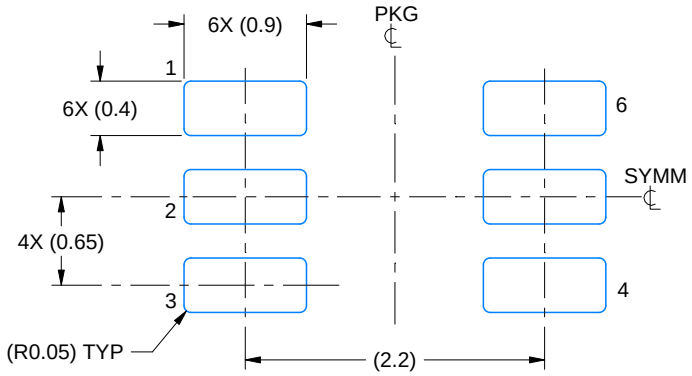
SMALL OUTLINE TRANSISTOR



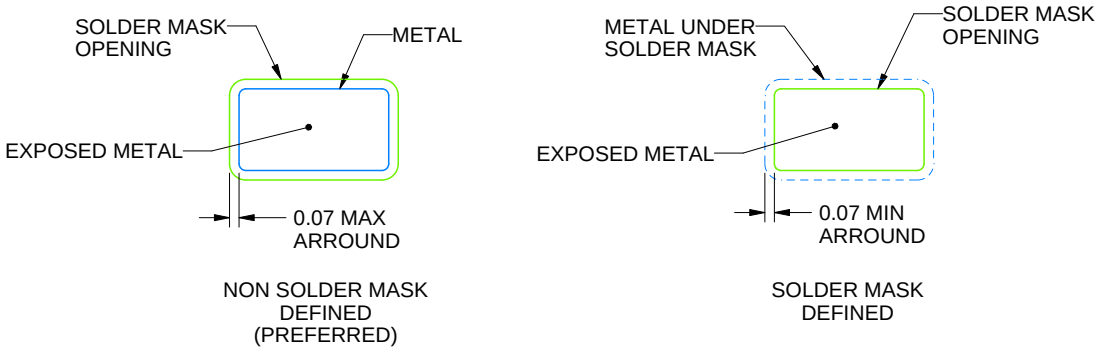
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

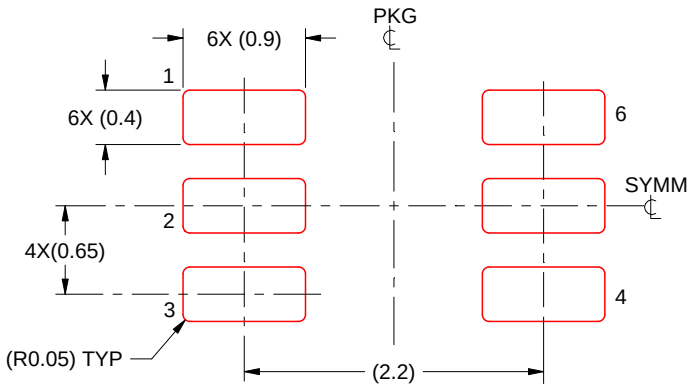


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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