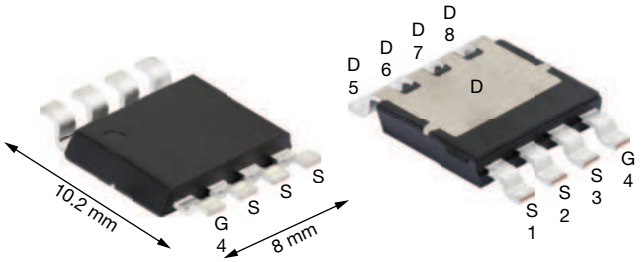
Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8LR



Top View | Bottom View

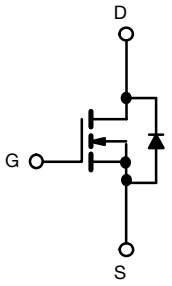
FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0015
I_D (A)	372
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ148ER (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C = 25 °C	I_D	372	A
	T_C = 125 °C		214	
Continuous source current (diode conduction)		I_S	360	
Pulsed drain current [b]		I_{DM}	670	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	46	
Single pulse avalanche energy		E_{AS}	105	mJ
Maximum power dissipation	T_C = 25 °C	P_D	394	W
	T_C = 125 °C		131	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	44	°C/W
Junction-to-case (drain)		R_{thJC}	0.38	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2	3	3.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	200	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	100	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A	-	0.00125	0.0015	Ω
		V_{GS} = 10 V	I_D = 20 A, T_J = 125 °C	-	-	0.0025	
		V_{GS} = 10 V	I_D = 20 A, T_J = 175 °C	-	-	0.0031	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 60 A		-	120	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	4170	5750	pF
Output capacitance	C_{oss}			-	1566	2193	
Reverse transfer capacitance	C_{rss}			-	131	184	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 20 A	-	68	102	nC
Gate-source charge [c]	Q_{gs}			-	20	-	
Gate-drain charge [c]	Q_{gd}			-	15	-	
Gate resistance	R_g	f = 1 MHz		0.8	1.6	2.4	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1 Ω I_D ≅ 20 A, V_{GEN} = 10 V, R_g = 1 Ω		-	17	26	ns
Rise time [c]	t_r			-	88	132	
Turn-off delay time [c]	$t_{d(off)}$			-	30	45	
Fall time [c]	t_f			-	12	18	
Source-Drain Diode Ratings and Characteristics [b]							
Reverse recovery time	t_{rr}	V_{DD} = 32 V, I_{FM} = 15 A, di/dt = 100 A/µs		-	47	94	ns
Reverse recovery charge	Q_{rr}			-	47	94	nC
Reverse recovery current	I_{RM}			-	-	1.8	A
Pulsed current [a]	I_{SM}			-	-	1600	A
Forward voltage	V_{SD}	I_F = 50 A, V_{GS} = 0		-	0.8	1.1	V

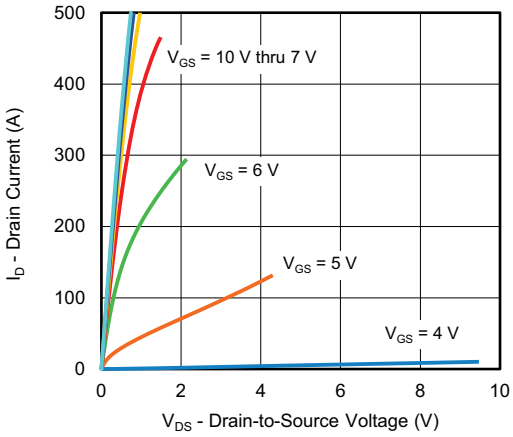
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

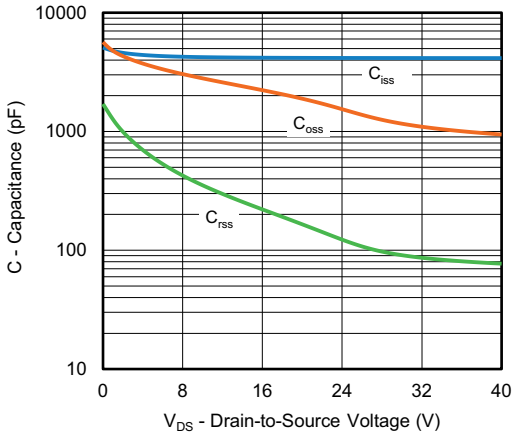
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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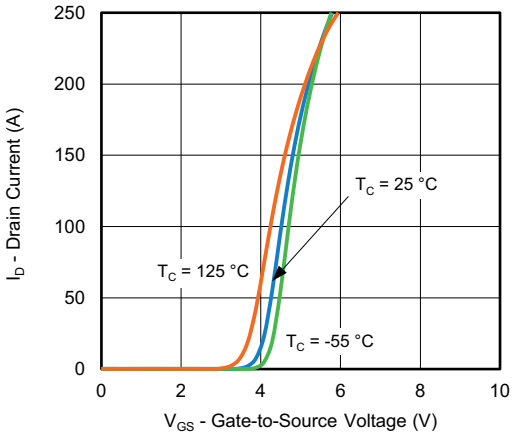
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



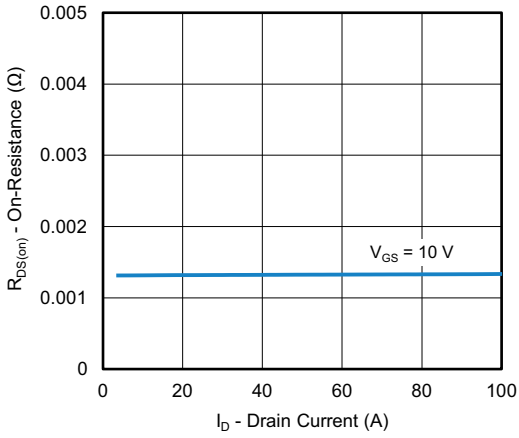
Output Characteristics



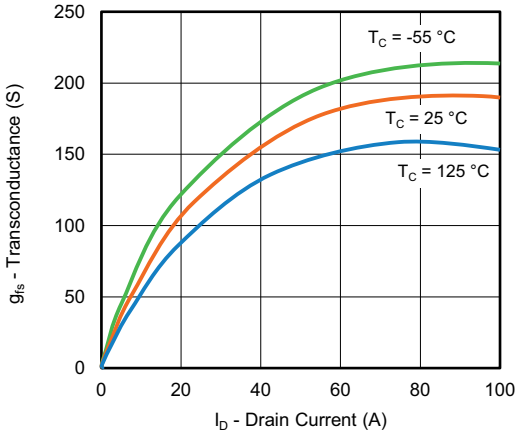
Capacitance



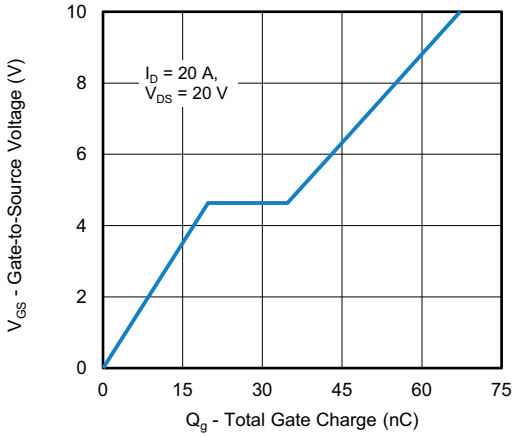
Transfer Characteristics



On-Resistance vs. Drain Current



Transconductance

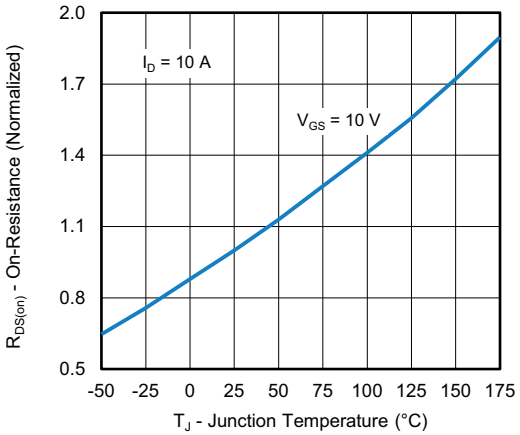


Gate Charge

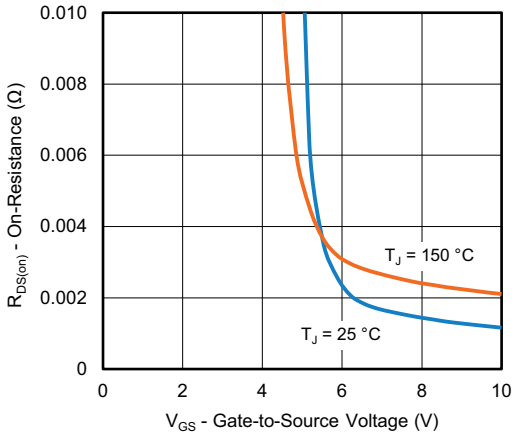
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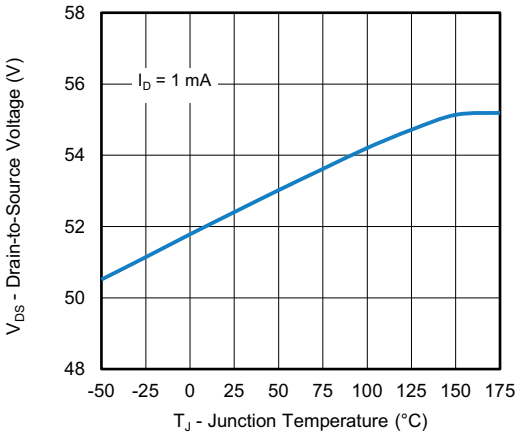
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



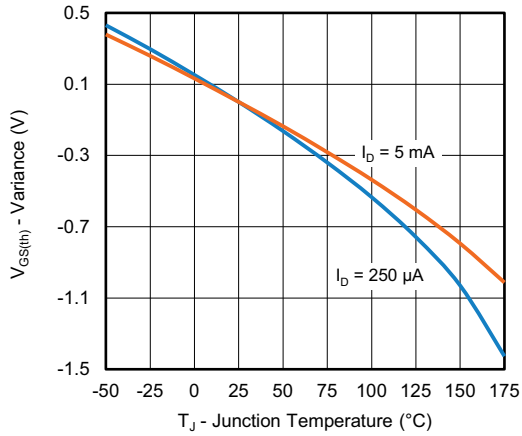
On-Resistance vs. Junction Temperature



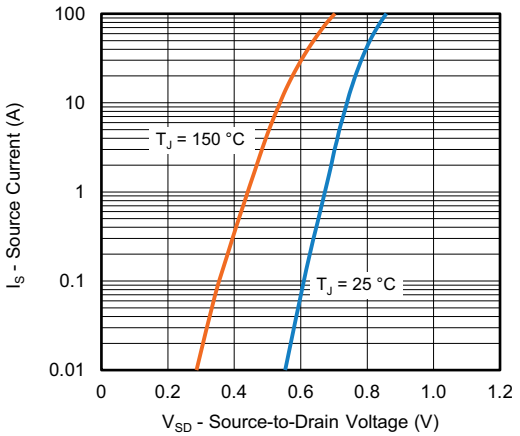
On-Resistance vs. Gate-to-Source Voltage



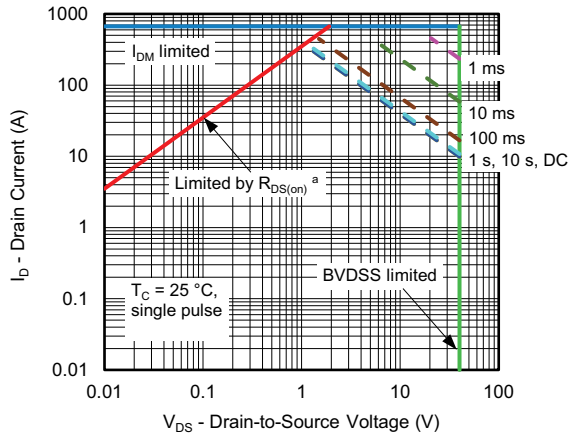
Drain Source Breakdown vs. Junction Temperature



Threshold Voltage



Source Drain Diode Forward Voltage



Safe Operating Area

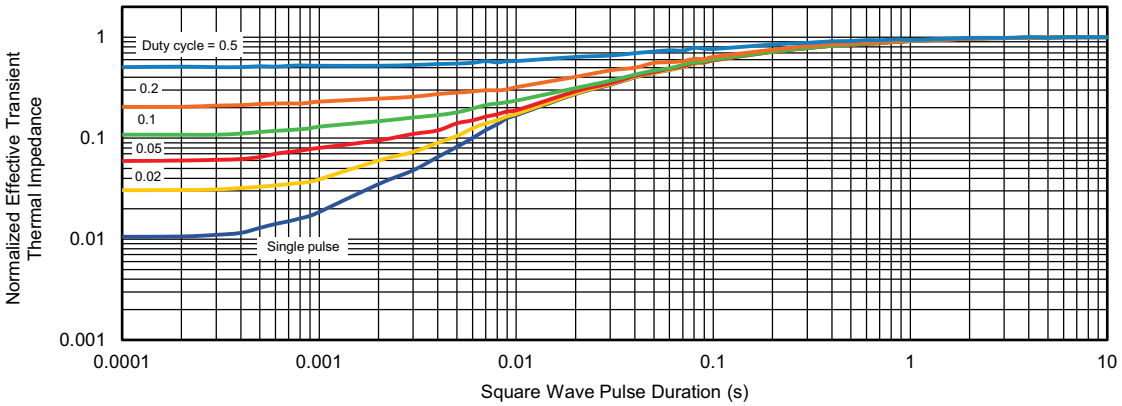
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

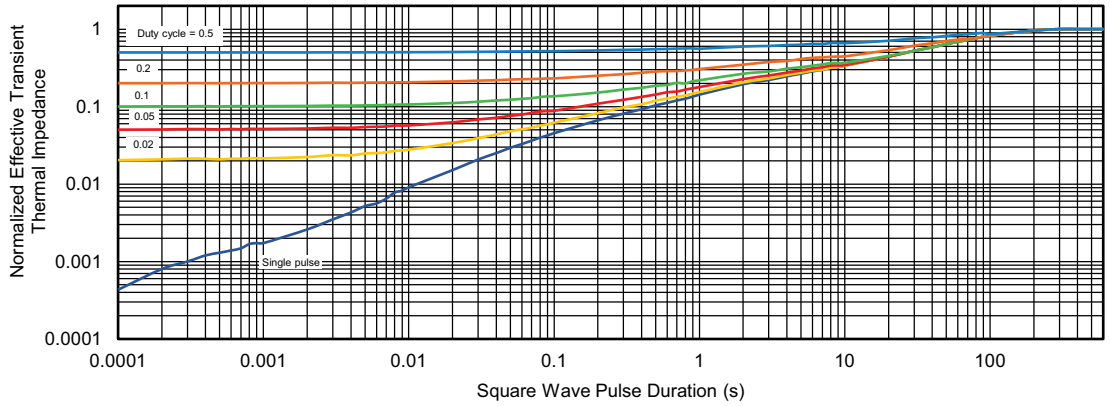
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



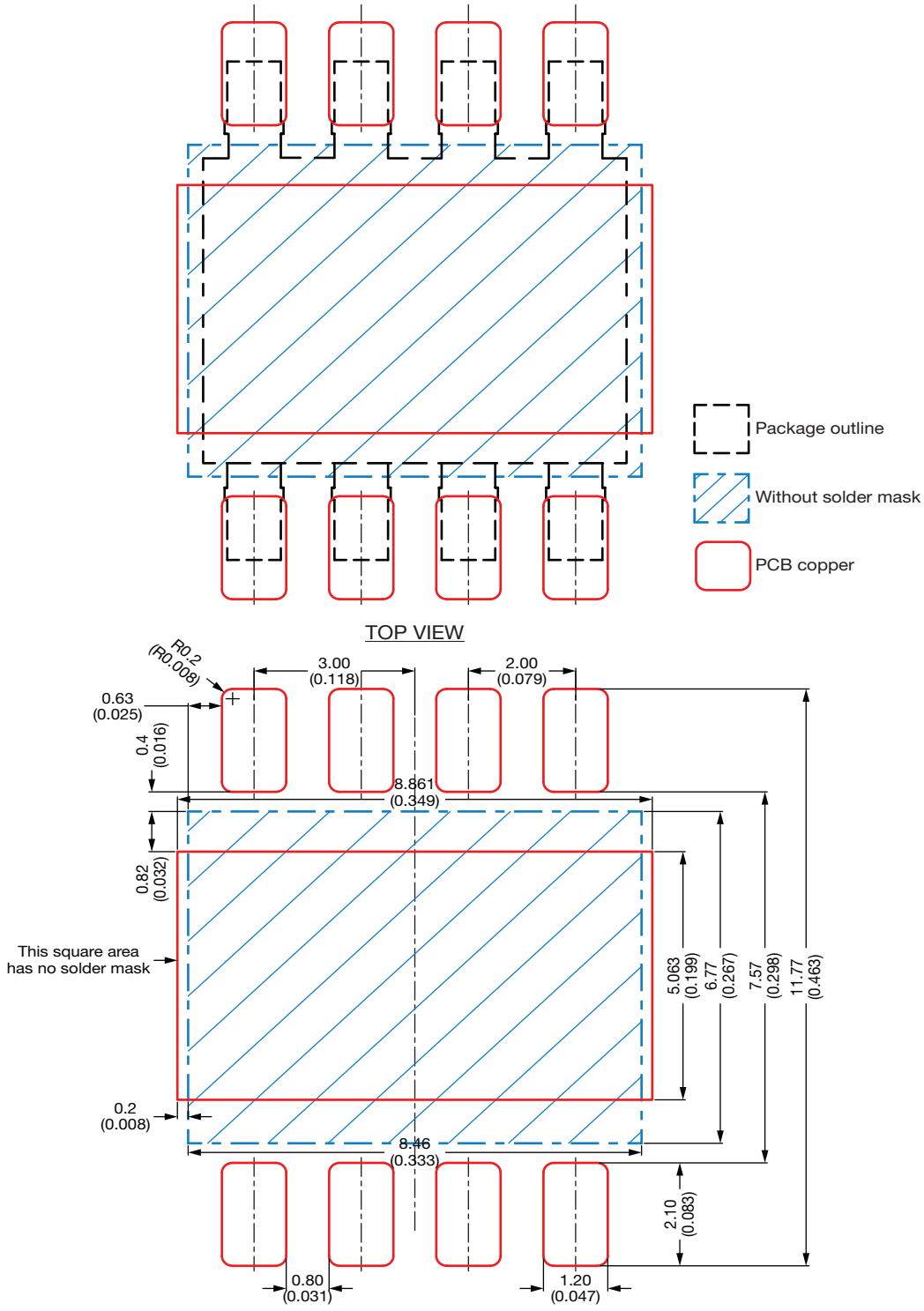
Normalized Thermal Transient Impedance, Junction-to-Ambient

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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023
DWG: 3002

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