SBFS030C – JANUARY 2006 – REVISED SEPTEMBER 2007

Two-Channel, Asynchronous Sample Rate Converter with Integrated Digital Audio Interface Receiver and Transmitter

FEATURES

- **Two-Channel Asynchronous Sample Rate Converter (SRC)**
  - **Dynamic Range with –60dB Input (A-Weighted): 128dB typical**
  - **Total Harmonic Distortion and Noise (THD+N) with Full-Scale Input: –125dB typical**
  - **Supports Audio Input and Output Data Word Lengths Up to 24 Bits**
  - **Supports Input and Output Sampling Frequencies Up to 216kHz**
  - **Automatic Detection of the Input-to-Output Sampling Ratio**
  - **Wide Input-to-Output Conversion Range: 16:1 to 1:16 Continuous**
  - **Excellent Jitter Attenuation Characteristics**
  - **Digital De-Emphasis Filtering for 32kHz, 44.1kHz, and 48kHz Input Sampling Rates**
  - **Digital Output Attenuation and Mute Functions**
  - **Output Word Length Reduction**
  - **Status Registers and Interrupt Generation for Sampling Ratio and Ready Flags**
- **Digital Audio Interface Transmitter (DIT)**
  - **Supports Sampling Rates Up to 216kHz**
  - **Includes Differential Line Driver and CMOS Buffered Outputs**
  - **Block-Sized Data Buffers for Both Channel Status and User Data**
  - **Status Registers and Interrupt Generation for Flag and Error Conditions**
- **User-Selectable Serial Host Interface: SPI or Philips I^{2}C™**
  - **Provides Access to On-Chip Registers and Data Buffers**

U.S. Patent No. 7,262,716

- **Digital Audio Interface Receiver (DIR)**
  - **PLL Lock Range Includes Sampling Rates from 20kHz to 216kHz**
  - **Includes Four Differential Input Line Receivers and an Input Multiplexer**
  - **Bypass Multiplexer Routes Line Receiver Outputs to Line Driver and Buffer Outputs**
  - **Block-Sized Data Buffers for Both Channel Status and User Data**
  - **Automatic Detection of Non-PCM Audio Streams (DTS CD/LD and IEC 61937 formats)**
  - **Audio CD Q-Channel Sub-Code Decoding and Data Buffer**
  - **Status Registers and Interrupt Generation for Flag and Error Conditions**
  - **Low Jitter Recovered Clock Output**
- **Two Audio Serial Ports (Ports A and B)**
  - **Synchronous Serial Interface to External Signal Processors, Data Converters, and Logic**
  - **Slave or Master Mode Operation with Sampling Rates up to 216kHz**
  - **Supports Left-Justified, Right-Justified, and Philips I^{2}S™ Data Formats**
  - **Supports Audio Data Word Lengths Up to 24 Bits**
- **Four General-Purpose Digital Outputs**
  - **Multifunction Programmable Via Control Registers**
- **Extensive Power-Down Support**
  - **Functional Blocks May Be Disabled Individually When Not In Use**
- **Operates From +1.8V Core and +3.3V I/O Power Supplies**
- **Small TQFP-48 Package, Compatible with the SRC4392 and DIX4192**

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APPLICATIONS

- **DIGITAL AUDIO RECORDERS AND MIXING DESKS**
- **DIGITAL AUDIO INTERFACES FOR COMPUTERS**
- **DIGITAL AUDIO ROUTERS AND DISTRIBUTION SYSTEMS**
- **BROADCAST STUDIO EQUIPMENT**
- **DVD/CD RECORDERS**
- **SURROUND SOUND DECODERS AND A/V RECEIVERS**
- **CAR AUDIO SYSTEMS**

DESCRIPTION

The SRC4382 is a highly-integrated CMOS device designed for use in professional and broadcast digital audio systems. The SRC4382 combines a high-performance, two-channel, asynchronous sample rate converter (SRC) with a digital audio interface receiver (DIR) and transmitter (DIT), two audio serial ports, and flexible distribution logic for interconnection of the function block data and clocks.

The DIR and DIT are compatible with the AES3, S/PDIF, IEC 60958, and EIAJ CP-1201 interface standards. The audio serial ports, DIT, and SRC may be operated at sampling rates up to 216kHz. The DIR lock range includes sampling rates from 20kHz to 216kHz.

The SRC4382 is configured using on-chip control registers and data buffers, which are accessed through either a 4-wire serial peripheral interface (SPI) port, or a 2-wire Philips I^2C bus interface. Status registers provide access to a variety of flag and error bits, which are derived from the various function blocks. An open drain interrupt output pin is provided, and is supported by flexible interrupt reporting and mask options via control register settings. A master reset input pin is provided for initialization by a host processor or supervisory functions.

The SRC4382 requires a +1.8V core logic supply, in addition to a +3.3V supply for powering portions of the DIR, DIT, and line driver and receiver functions. A separate logic I/O supply supports operation from +1.65V to +3.6V, providing compatibility with low voltage logic interfaces typically found on digital signal processors and programmable logic devices. The SRC4382 is available in a lead-free, TQFP-48 package, and is pin- and register-compatible with the Texas Instruments SRC4392 and DIX4192 products.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
SRC4382	TQFP-48	PFB	–40C to +85C	SRC4382I	SRC4382IPFBT	Tape and Reel, 250
					SRC4382IPFBR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supplies	
VDD18	–0.3V to +2.0V
VDD33	–0.3V to +4.0V
VIO	–0.3V to +4.0V
VCC	–0.3V to +4.0V
Digital Input Voltage: Digital Logic	
RXCKI, MUTE, CPM, $\overline{CS}$, CCLK, CDIN, CDOUT, $\overline{INT}$, $\overline{RST}$, MCLK, BLS, SYNC, BCKA, BCKB, LRCKA, LRCKB, SDINA, SDINB	–0.3V to (VIO + 0.3V)
Line Receiver Input Voltage (per pin)	
RX1+, RX1–, RX2+, RX2–, RX3+, RX3–, RX4+, RX4–	(VDD33 + 0.3) V_{PP}
Input Current (all pins except power and ground)	10mA
Ambient Operating Temperature	–40C to +85C
Storage Temperature	–65C to +150C

(1) These limits are stress ratings only. Stresses beyond these limits may result in permanent damage. Extended exposure to absolute maximum ratings may degrade device reliability. Normal operation or performance at or beyond these limits is not specified or ensured.

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ELECTRICAL CHARACTERISTICS: General, SRC, DIR, and DIT

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
DIGITAL I/O CHARACTERISTICS (All I/O Pins Except Line Receivers and Line Driver)					
High-Level Input Voltage, V_{IH}		0.7 ɪVIO		VIO	V
Low-Level Input Voltage, V_{IL}		0		0.3 ɪVIO	V
High-Level Input Current, I_{IH}			0.5	10	µA
Low-Level Input Current, V_{IL}			0.5	10	µA
High-Level Output Voltage, V_{OH}	I_O = –4mA	0.8 ɪVIO		VIO	V
Low-Level Output Voltage, V_{OL}	I_O = +4mA	0		0.2 ɪVIO	V
Input Capacitance, C_{IN}			3		pF
LINE RECEIVER INPUTS (RX1+, RX1–, RX2+, RX2–, RX3+, RX3–, RX4+, RX4–)					
Differential Input Sensitivity, V_{TH}	Voltage across a given differential input pair		150	200	mV
Input Hysteresis, V_{HY}		150			mV
LINE DRIVER OUTPUTS (TX+, TX–)					
Differential Output Voltage, V_{TXO}	R_L = 110Ω Across TX+ and TX–	5.4			V_{PP}
MASTER CLOCK INPUT					
Master Clock Input (MCLK) Frequency, f_{MCLK}		1		27.7	MHz
Master Clock Input (MCLK) Duty Cycle, f_{MCLKD}		45		55	%
ASYNCHRONOUS SAMPLE RATE CONVERTER (SRC)					
Input or Output Sampling Rate, f_{SIN} or f_{SOUT}		4		216	kHz
Input-to-Output Sampling Ratio		1:16		16:1	
Interchannel Gain Mismatch			0		dB
Interchannel Phase Mismatch			0		Degrees
Dynamic Range (no weighting filter applied)(1)	BW = 22Hz to f_{SOUT}/2, f = 997Hz at –60dBFS				
f_{SIN}:f_{SOUT} = 12kHz:192kHz			125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:44.1kHz			125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:48kHz			125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:96kHz			125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:192kHz			125		dB
f_{SIN}:f_{SOUT} = 48kHz:44.1kHz			125		dB
f_{SIN}:f_{SOUT} = 48kHz:48kHz			125		dB
f_{SIN}:f_{SOUT} = 48kHz:96kHz			125		dB
f_{SIN}:f_{SOUT} = 48kHz:192kHz			125		dB
f_{SIN}:f_{SOUT} = 96kHz:44.1kHz			125		dB
f_{SIN}:f_{SOUT} = 96kHz:48kHz			125		dB
f_{SIN}:f_{SOUT} = 96kHz:96kHz			125		dB
f_{SIN}:f_{SOUT} = 96kHz:192kHz			125		dB
f_{SIN}:f_{SOUT} = 192kHz:12kHz			125		dB
f_{SIN}:f_{SOUT} = 192kHz:44.1kHz			125		dB
f_{SIN}:f_{SOUT} = 192kHz:48kHz			125		dB
f_{SIN}:f_{SOUT} = 192kHz:96kHz			125		dB
f_{SIN}:f_{SOUT} = 192kHz:192kHz			125		dB

(1) Measured with an Audio Precision SYS-2722 192kHz test system with the input and output sampling frequencies asynchronous to one another. A-weighted dynamic range specifications will be improved by approximately 2dB to 3dB when compared to the results without A-weighting applied.

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ELECTRICAL CHARACTERISTICS: General, SRC, DIR, and DIT (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
Total Harmonic Distortion + Noise (THD+N)(2)	BW = 22Hz to $f_{SOUT}/2$, f = 997Hz at 0dBFS				
f_{SIN}:f_{SOUT} = 12kHz:192kHz			–125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:44.1kHz			–125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:48kHz			–125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:96kHz			–125		dB
f_{SIN}:f_{SOUT} = 44.1kHz:192kHz			–125		dB
f_{SIN}:f_{SOUT} = 48kHz:44.1kHz			–125		dB
f_{SIN}:f_{SOUT} = 48kHz:48kHz			–125		dB
f_{SIN}:f_{SOUT} = 48kHz:96kHz			–125		dB
f_{SIN}:f_{SOUT} = 48kHz:192kHz			–125		dB
f_{SIN}:f_{SOUT} = 96kHz:44.1kHz			–125		dB
f_{SIN}:f_{SOUT} = 96kHz:48kHz			–125		dB
f_{SIN}:f_{SOUT} = 96kHz:96kHz			–125		dB
f_{SIN}:f_{SOUT} = 96kHz:192kHz			–125		dB
f_{SIN}:f_{SOUT} = 192kHz:12kHz			–125		dB
f_{SIN}:f_{SOUT} = 192kHz:44.1kHz			–125		dB
f_{SIN}:f_{SOUT} = 192kHz:48kHz			–125		dB
f_{SIN}:f_{SOUT} = 192kHz:96kHz			–125		dB
f_{SIN}:f_{SOUT} = 192kHz:192kHz			–125		dB
Digital Interpolation Filter Characteristics					
Passband				0.4535 ƛf_{SIN}	Hz
Passband Ripple				0.007	dB
Transition Band		0.4535 ƛf_{SIN}		0.5465 ƛf_{SIN}	Hz
Stop Band		0.5465 ƛf_{SIN}			Hz
Stop Band Attenuation		–125			dB
Group Delay (64 samples pre-buffered)	Decimation filter enabled			102.53125/f_{SIN}	Seconds
Group Delay (64 samples pre-buffered)	Direct down-sampling enabled			102/f_{SIN}	Seconds
Group Delay (32 samples pre-buffered)	Decimation filter enabled			70.53125/f_{SIN}	Seconds
Group Delay (32 samples pre-buffered)	Direct down-sampling enabled			70/f_{SIN}	Seconds
Group Delay (16 samples pre-buffered)	Decimation filter enabled			54.53125/f_{SIN}	Seconds
Group Delay (16 samples pre-buffered)	Direct down-sampling enabled			54/f_{SIN}	Seconds
Group Delay (8 samples pre-buffered)	Decimation filter enabled			46.53125/f_{SIN}	Seconds
Group Delay (8 samples pre-buffered)	Direct down-sampling enabled			46/f_{SIN}	Seconds
Digital Decimation Filter Characteristics					
Passband				0.4535 ƛf_{SOUT}	Hz
Passband Ripple				0.008	dB
Transition Band		0.4535 ƛf_{SOUT}		0.5465 ƛf_{SOUT}	Hz
Stop Band		0.5465 ƛf_{SOUT}			Hz
Stop Band Attenuation		–125			dB
Group Delay	Decimation filter enabled			36.46875/f_{SOUT}	Seconds
Group Delay	Direct down-sampling enabled			0	Seconds
Digital De-Emphasis Filter Characteristics					
Filter Error for All Settings	De-emphasis filter enabled			0.001	dB

(2) Measured with an Audio Precision SYS-2722 192kHz test system with the input and output sampling frequencies asynchronous to one another.

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ELECTRICAL CHARACTERISTICS: General, SRC, DIR, and DIT (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
DIGITAL AUDIO INTERFACE RECEIVER (DIR)					
PLL Lock Range		20		216	kHz
Reference Clock Input (RXCKI) Frequency, f_{RXCKI}		3.5		27.7	MHz
Reference Clock Input (RXCKI) Duty Cycle, f_{RXCKID}		45		55	%
Recovered Clock Output (RXCKO) Frequency, f_{RXCKO}		3.5		27.7	MHz
Recovered Clock Output (RXCKO) Duty Cycle, f_{RXCKOD}		45		55	%
Recovered Clock Output (RXCKO) Intrinsic Jitter	Measured cycle-to-cycle		250		ps RMS
DIGITAL AUDIO INTERFACE TRANSMITTER (DIT)					
Intrinsic Output Jitter	Measured cycle-to-cycle		200		ps RMS

ELECTRICAL CHARACTERISTICS: Audio Serial Ports

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
AUDIO SERIAL PORTS (Port A and Port B)					
LRCK Clock Frequency, f_{LRCK}		0		216	kHz
LRCK Clock Duty Cycle, t_{LRCKD}			50		%
BCK Clock Frequency, f_{BCK}		0		13.824	MHz
BCK High Pulse Width, t_{BCKH}		10			ns
BCK Low Pulse Width, t_{BCKL}		10			ns
Audio Data Input (SDIN) Setup Time, t_{AIS}		10			ns
Audio Data Input (SDIN) Hold Time, t_{AISH}		10			ns
Audio Data Output (SDOUT) Delay, t_{ADD}				10	ns

ELECTRICAL CHARACTERISTICS: SPI Interface

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
HOST INTERFACE: SPI Mode					
Serial Clock (CCLK) Frequency, f_{CCLK}		0		40	MHz
$\overline{CS}$ Falling to CCLK Rising, t_{CSCR}		8			ns
CCLK Falling to $\overline{CS}$ Rising, t_{CFCS}		7			ns
CDIN Data Setup Time, t_{CDS}		7			ns
CDIN Data Hold Time, t_{CDH}		6			ns
CCLK Falling to CDOUT Data Valid, t_{CFDO}				3	ns
$\overline{CS}$ Rising to CDOUT High-Impedance, t_{CSZ}				3	ns

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ELECTRICAL CHARACTERISTICS: I²C Standard and Fast Modes

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
HOST INTERFACE: I²C Standard Mode(1)					
SCL Clock Frequency, f_{SCL}		0		100	kHz
Hold Time Repeated START Condition, t_{HDSTA}		4			µs
Low Period of SCL Clock, t_{LOW}		4.7			µs
High Period of SCL Clock, t_{HIGH}		4			µs
Setup Time Repeated START Condition, t_{SUSTA}		4.7			µs
Data Hold Time, t_{HDDAT}		0(2)		3.45(3)	µs
Data Setup Time, t_{SUDAT}		250			ns
Rise Time for Both SDA and SDL, t_R				1000	ns
Fall Time for Both SDA and SDL, t_F				300	ns
Setup Time for STOP Condition, t_{SUSTO}		4			µs
Bus Free Time Between START and STOP, t_{BUF}		4.7			µs
Capacitive Load for Each Bus Line, C_B				400	pF
Noise Margin at Low Level (including hysteresis), V_{NL}		0.1 ɔVIO			V
Noise Margin at High Level (including hysteresis), V_{NH}		0.2 ɔVIO			V
HOST INTERFACE: I²C Fast Mode(1)					
SCL Clock Frequency, f_{SCL}		0		400	kHz
Hold Time Repeated START Condition, t_{HDSTA}		0.6			µs
Low Period of SCL Clock, t_{LOW}		1.3			µs
High Period of SCL Clock, t_{HIGH}		0.6			µs
Setup Time Repeated START Condition, t_{SUSTA}		0.6			µs
Data Hold Time, t_{HDDAT}		0(2)		0.9(3)	µs
Data Setup Time, t_{SUDAT}		100(4)			ns
Rise Time for Both SDA and SDL, t_R		$20 + 0.2C_B$(5)		300	ns
Fall Time for Both SDA and SDL, t_F		$20 + 0.2C_B$(5)		300	ns
Setup Time for STOP Condition, t_{SUSTO}		0.6			µs
Bus Free Time Between START and STOP, t_{BUF}		1.3			µs
Spike Pulse Width Suppressed by Input Filter, t_{SP}		0		50	ns
Capacitive Load for Each Bus Line, C_B				400	pF
Noise Margin at Low Level (including hysteresis), V_{NL}		0.1 ɔVIO			V
Noise Margin at High Level (including hysteresis), V_{NH}		0.2 ɔVIO			V

(1) All values referred to the V_{IH} minimum and V_{IL} maximum levels listed in the Digital I/O Characteristics section of the *Electrical Characteristics: General, SRC, DIR, and DIT* table.
(2) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH} minimum input level) to bridge the undefined region of the falling edge of SCL.
(3) The maximum t_{HDDAT} has only to be met if the device does not stretch the Low period (t_{LOW}) of the SCL signal.
(4) A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement that t_{SUDAT} be 250ns minimum must then be met. For the SRC4382, this is automatically the case, since the device does not stretch the Low period of the SCL signal.
(5) C_B is defined as the total capacitance of one bus line in picofarads (pF). If mixed with High-Speed mode devices, faster fall times are allowed.

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ELECTRICAL CHARACTERISTICS: Power Supplies

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

PARAMETER	CONDITIONS	SRC4382			UNITS
		MIN	TYP	MAX	
POWER SUPPLIES					
Recommended Supply Voltage Range					
VDD18		+1.65	+1.8	+1.95	V
VDD33		+3.0	+3.3	+3.6	V
VIO		+1.65	+3.3	+3.6	V
VCC		+3.0	+3.3	+3.6	V
Supply Current: Initial Startup	All Blocks Powered Down by Default				
IDD18S	VDD18 = +1.8V		90		µA
IDD33S	VDD33 = +3.3V		1		µA
IIOS	VIO = +3.3V		270		µA
ICCS	VCC = +3.3V		1		µA
Supply Current: Quiescent	All Blocks Powered Up with No Clocks Applied				
IDD18Q	VDD18 = +1.8V		3.1		mA
IDD33Q	VDD33 = +3.3V		0.5		mA
IIOQ	VIO = +3.3V		0.27		mA
ICCQ	VCC = +3.3V		6.6		mA
Supply Current: Dynamic	All Blocks Powered Up, f_S = 48kHz				
IDD18D	VDD18 = +1.8V		23		mA
IDD33D	VDD33 = +3.3V		14		mA
IIOD(1)	VIO = +3.3V		43		mA
ICCD	VCC = +3.3V		8		mA
Supply Current: High Sampling Rate	All Blocks Powered Up, f_S = 192kHz				
IDD18H	VDD18 = +1.8V		58		mA
IDD33H	VDD33 = +3.3V		15		mA
IIOH(1)	VIO = +3.3V		44		mA
ICCH	VCC = +3.3V		8		mA
Total Power Dissipation: Initial Startup	All Blocks Powered Down by Default		1		mW
Total Power Dissipation: Quiescent	All Blocks Powered Up with No Clocks Applied		30		mW
Total Power Dissipation: Dynamic	All Blocks Powered Up, f_S = 48kHz		256		mW
Total Power Dissipation: High Sampling Rate	All Blocks Powered Up, f_S = 192kHz		326		mW

(1) The typical VIO supply current is measured using the SRC4382EVM evaluation module with loading from the DAIMB mother-board circuitry. VIO supply current will be dependent upon the loading on the logic output pins.

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TIMING DIAGRAMS

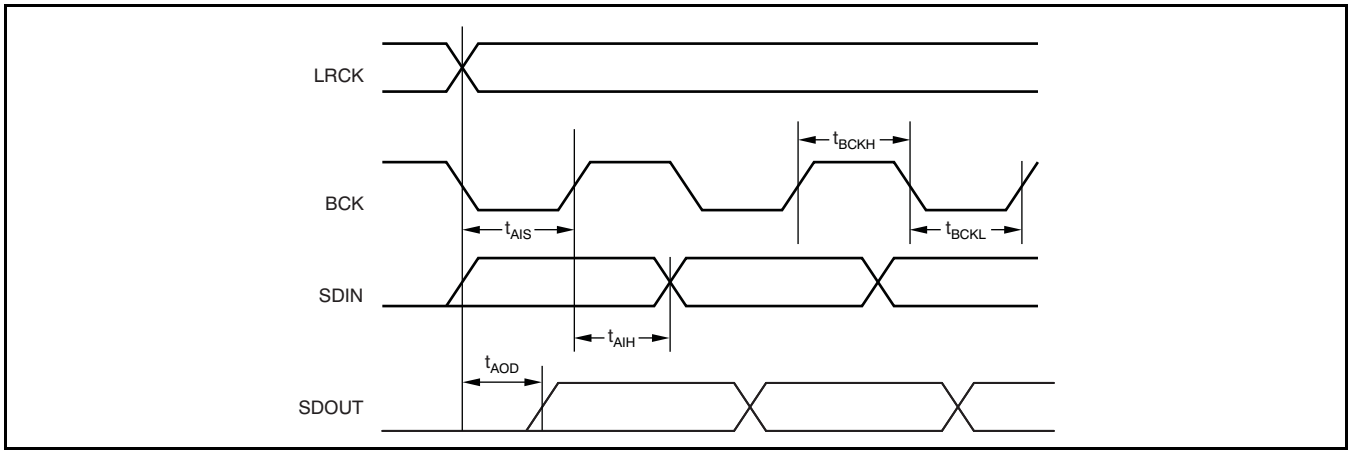


Figure 1. Audio Serial Port Timing

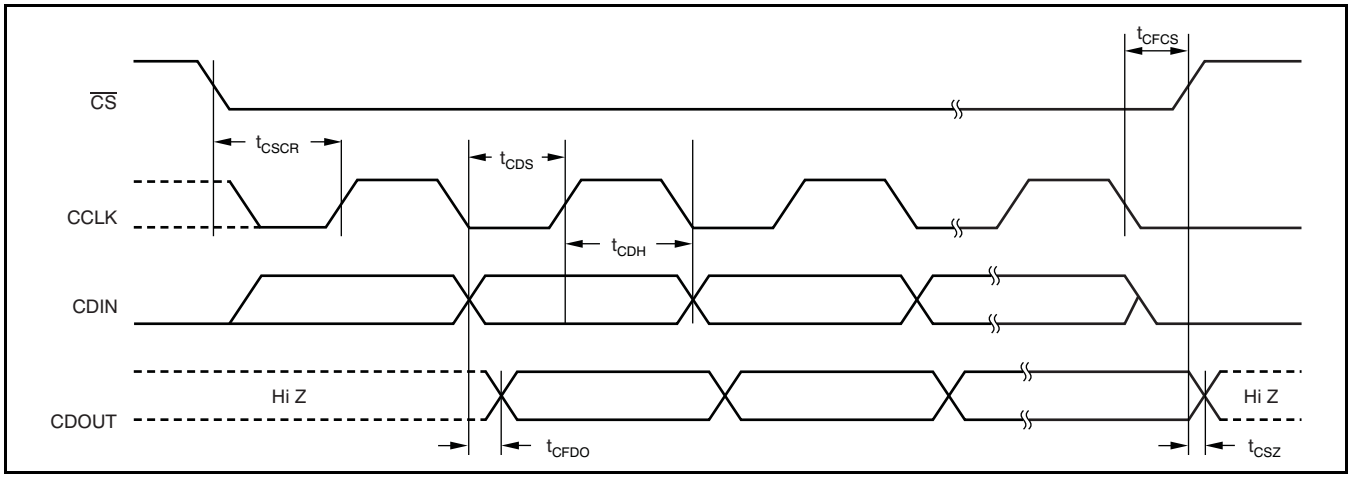


Figure 2. SPI Interface Timing

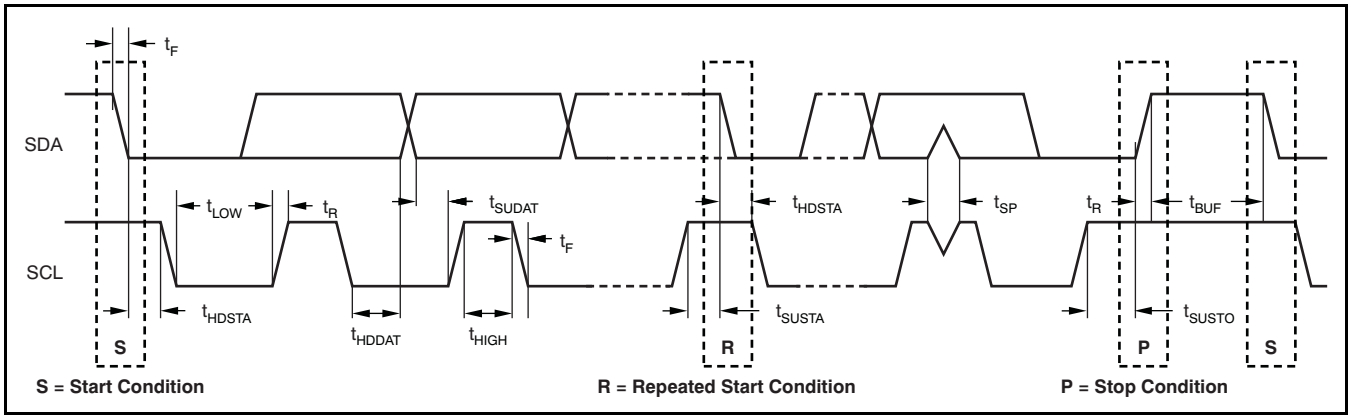
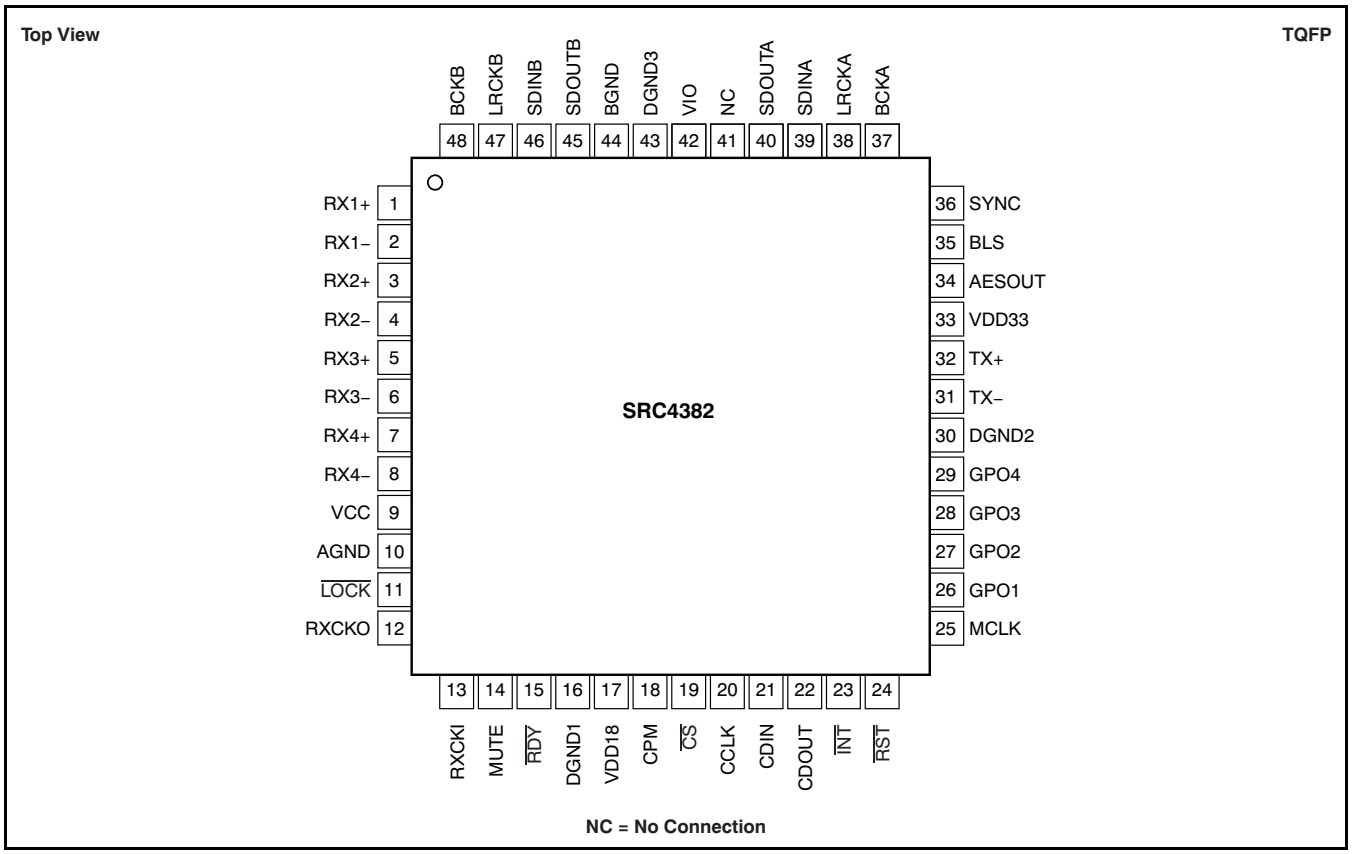


Figure 3. I²C Standard and Fast Mode Timing

PIN CONFIGURATION



PIN DESCRIPTIONS

NAME	PIN NUMBER	I/O	DESCRIPTION
RX1+	1	Input	Line Receiver 1, Noninverting Input
RX1–	2	Input	Line Receiver 1, Inverting Input
RX2+	3	Input	Line Receiver 2, Noninverting Input
RX2–	4	Input	Line Receiver 2, Inverting Input
RX3+	5	Input	Line Receiver 3, Noninverting Input
RX3–	6	Input	Line Receiver 3, Inverting Input
RX4+	7	Input	Line Receiver 4, Noninverting Input
RX4–	8	Input	Line Receiver 4, Inverting Input
VCC	9	Power	DIR Comparator and PLL Power Supply, +3.3V Nominal
AGND	10	Ground	DIR Comparator and PLL Power-Supply Ground
$\overline{\text{LOCK}}$	11	Output	DIR PLL Lock Flag (active Low)
RXCKO	12	Output	DIR Recovered Master Clock (tri-state output)
RXCKI	13	Input	DIR Reference Clock
MUTE	14	Input	SRC Output Mute (active High)
$\overline{\text{RDY}}$	15	Output	SRC Ready Flag (active Low)
DGND1	16	Ground	Digital Core Ground
VDD18	17	Power	Digital Core Supply, +1.8V Nominal
CPM	18	Input	Control Port Mode, 0 = SPI Mode, 1 = I^2C Mode
$\overline{\text{CS}}$ or A0	19	Input	Chip Select (active Low) for SPI Mode or Programmable Slave Address for I^2C Mode
CCLK or SCL	20	Input	Serial Data Clock for SPI Mode or I^2C Mode
CDIN orA1	21	Input	SPI Port Serial Data input or Programmable Slave Address for I^2C Mode
CDOUT or SDA	22	I/O	SPI Port Serial Data Output (tri-state output) or Serial Data I/O for I^2C Mode

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PIN DESCRIPTIONS (continued)

NAME	PIN NUMBER	I/O	DESCRIPTION
$\overline{\text{INT}}$	23	Output	Interrupt Flag (open-drain, active Low)
$\overline{\text{RST}}$	24	Input	Reset (active Low)
MCLK	25	Input	Master Clock
GPO1	26	Output	General-Purpose Output 1
GPO2	27	Output	General-Purpose Output 2
GPO3	28	Output	General-Purpose Output 3
GPO4	29	Output	General-Purpose Output 4
DGND2	30	Ground	DIR Line Receiver Bias and DIT Line Driver Digital Ground
TX–	31	Output	DIT Line Driver Inverting Output
TX+	32	Output	DIT Line Driver Noninverting Output
VDD33	33	Power	DIR Line Receiver Bias and DIT Line Driver Supply, +3.3V Nominal
AESOUT	34	Output	DIT Buffered AES3-Encoded Data
BLS	35	I/O	DIT Block Start Clock
SYNC	36	Output	DIT internal Sync Clock
BCKA	37	I/O	Audio Serial Port A Bit Clock
LRCKA	38	I/O	Audio Serial Port A Left/Right Clock
SDINA	39	Input	Audio Serial Port A Data Input
SDOUTA	40	Output	Audio Serial Port A Data Output
NC	41	—	No Internal Signal Connection, Internally Bonded to ESD Pad
VIO	42	Power	Logic I/O Supply, +1.65V to +3.6V
DGND3	43	Ground	Logic I/O Ground
BGND	44	Ground	Substrate Ground, Connect to AGND (pin 10)
SDOUTB	45	Output	Audio Serial Port B Data Output
SDINB	46	Input	Audio Serial Port B Data Input
LRCKB	47	I/O	Audio Serial Port B Left/Right Clock
BCKB	48	I/O	Audio Serial Port B Bit Clock

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TYPICAL CHARACTERISTICS

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

THD+N vs INPUT SAMPLING RATE (f_{SOUT} = 44.1kHz and f_{IN} = 997Hz at 0dBFS)

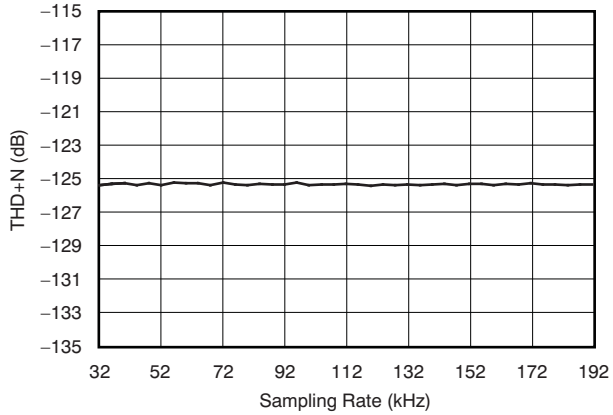

Figure 4.

THD+N vs INPUT SAMPLING RATE (f_{SOUT} = 48kHz and f_{IN} = 997Hz at 0dBFS)

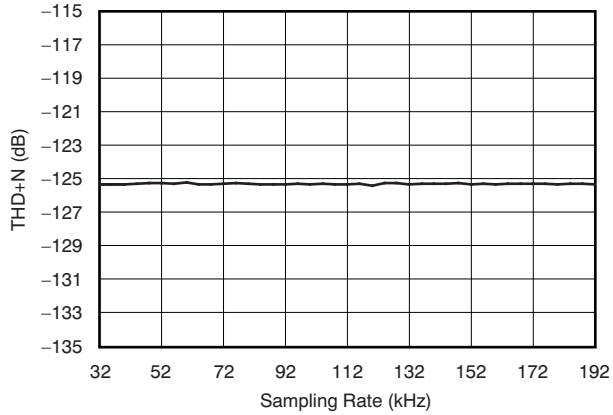

Figure 5.

THD+N vs INPUT SAMPLING RATE (f_{SOUT} = 96kHz and f_{IN} = 997Hz at 0dBFS)

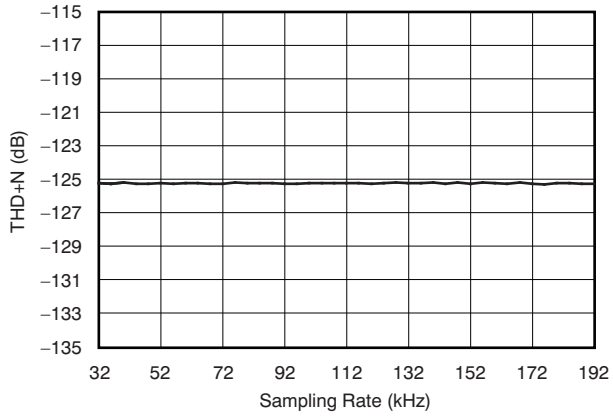

Figure 6.

THD+N vs INPUT SAMPLING RATE (f_{SOUT} = 192kHz and f_{IN} = 997Hz at 0dBFS)

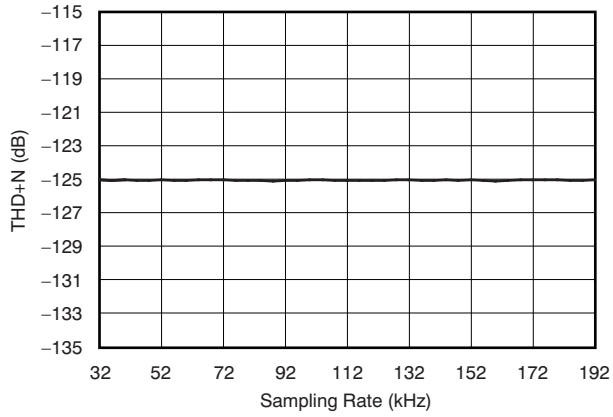

Figure 7.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 44.1kHz:44.1kHz and Input Amplitude = 0dBFS)

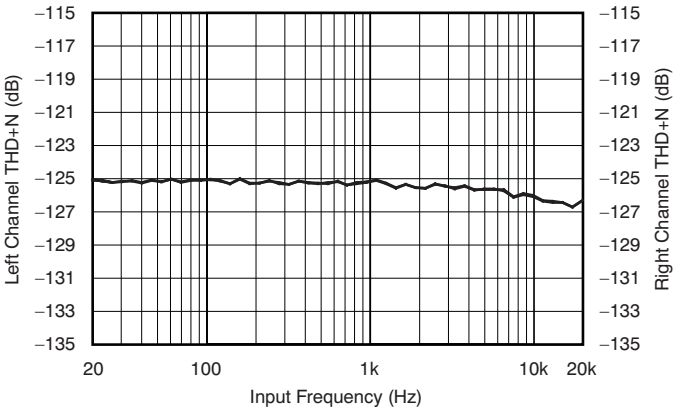

Figure 8.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 44.1kHz:48kHz and Input Amplitude = 0dBFS)

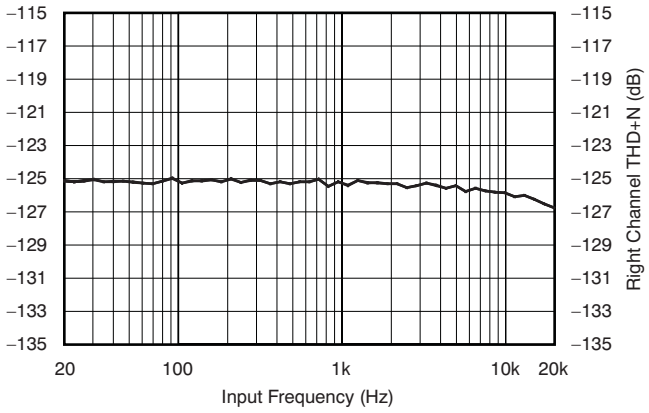

Figure 9.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 44.1kHz:96kHz and Input Amplitude = 0dBFS)

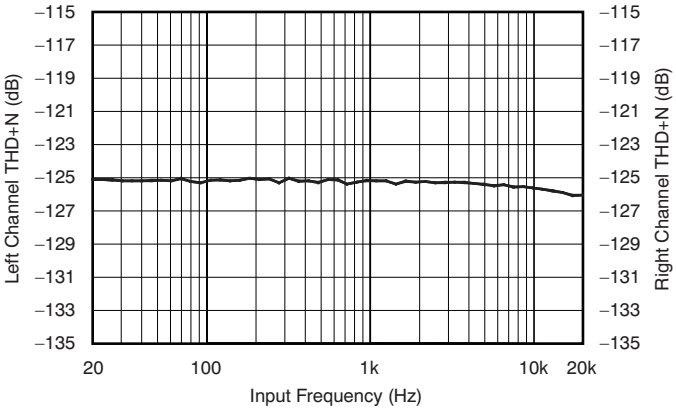

Figure 10.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 44.1kHz:192kHz and Input Amplitude = 0dBFS)

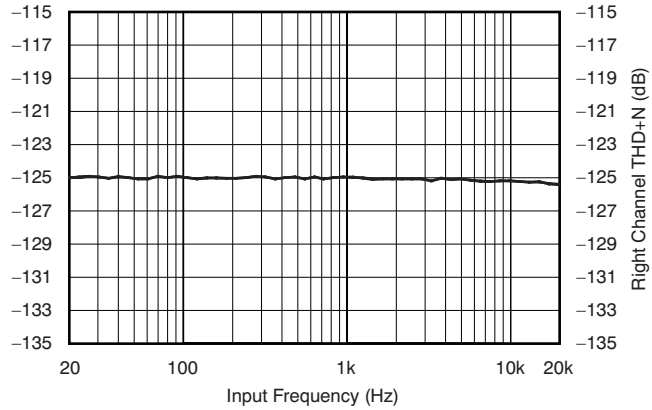

Figure 11.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 48kHz:44.1kHz and Input Amplitude = 0dBFS)

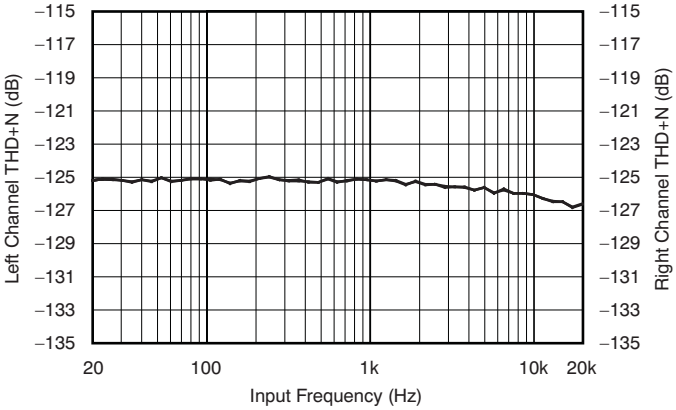

Figure 12.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 48kHz:48kHz and Input Amplitude = 0dBFS)

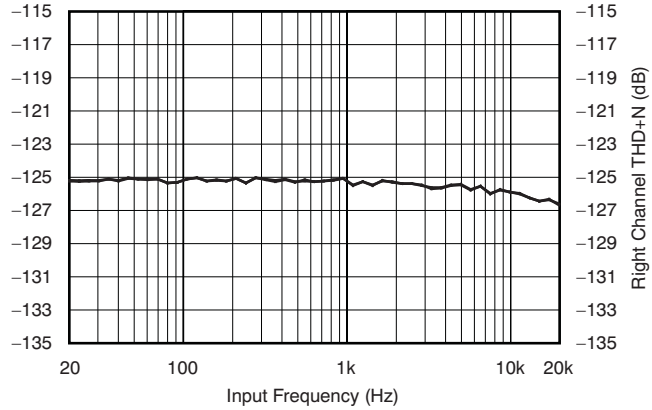

Figure 13.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 48kHz:96kHz and Input Amplitude = 0dBFS)

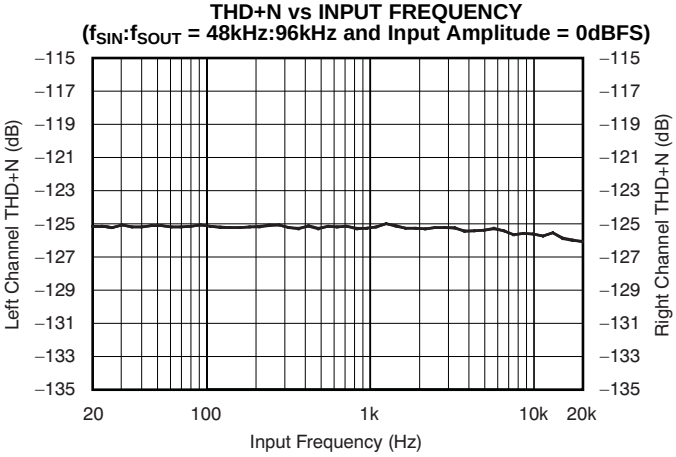

Figure 14.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 48kHz:192kHz and Input Amplitude = 0dBFS)

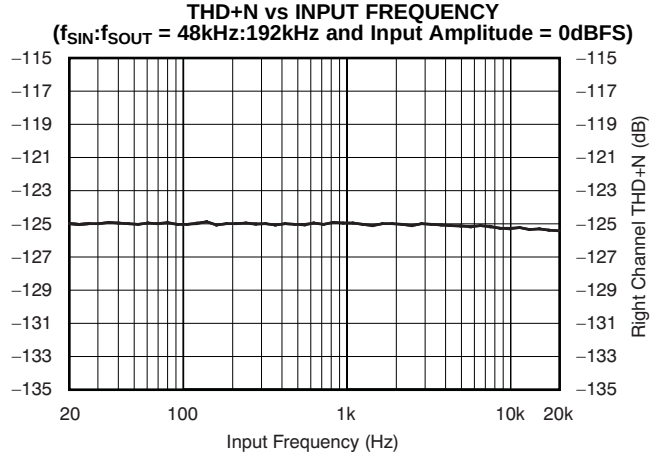

Figure 15.

TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 96kHz:44.1kHz and Input Amplitude = 0dBFS)

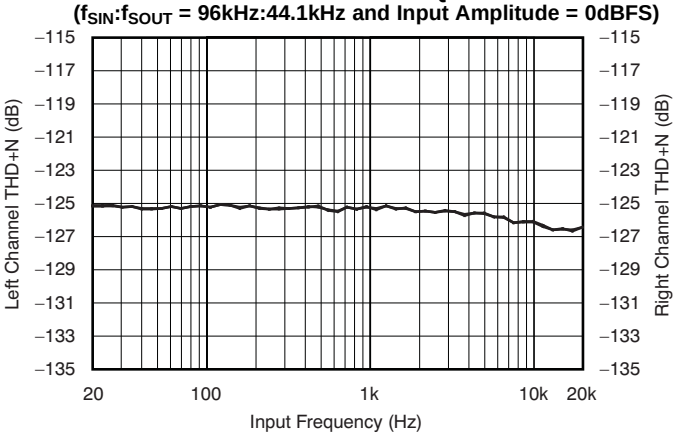

Figure 16.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 96kHz:48kHz and Input Amplitude = 0dBFS)

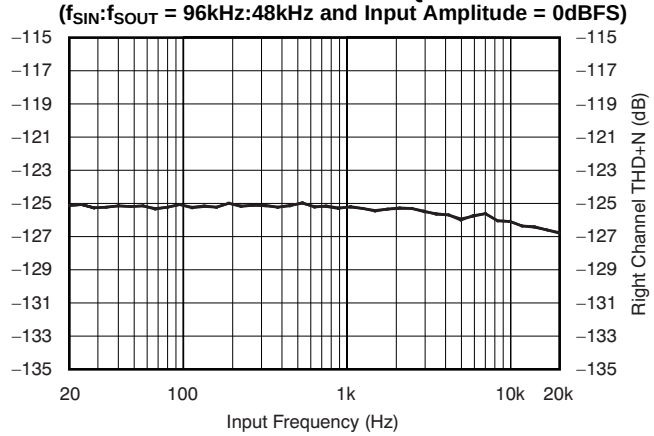

Figure 17.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 96kHz:96kHz and Input Amplitude = 0dBFS)

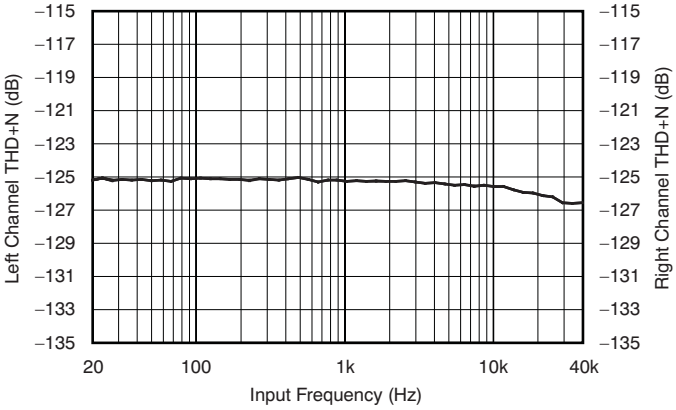

Figure 18.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 96kHz:192kHz and Input Amplitude = 0dBFS)

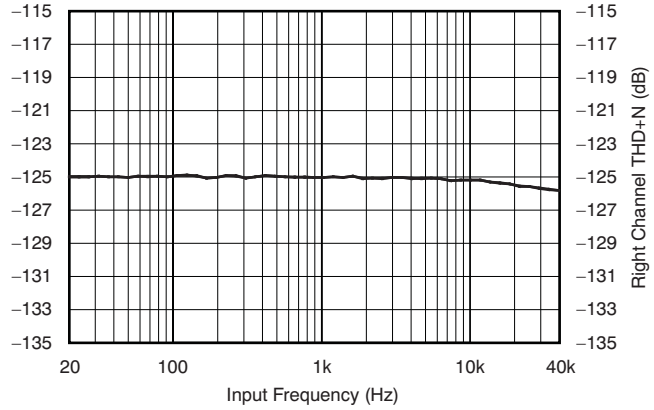

Figure 19.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 192kHz:44.1kHz and Input Amplitude = 0dBFS)

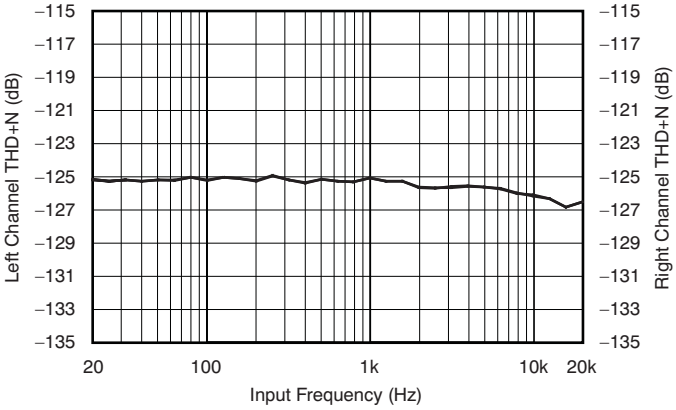

Figure 20.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 192kHz:48kHz and Input Amplitude = 0dBFS)

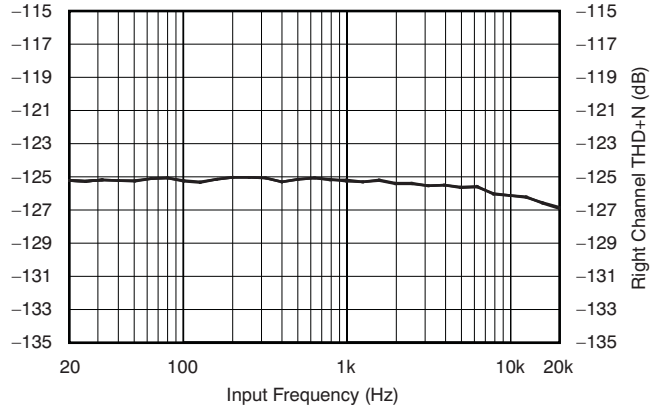

Figure 21.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 192kHz:96kHz and Input Amplitude = 0dBFS)

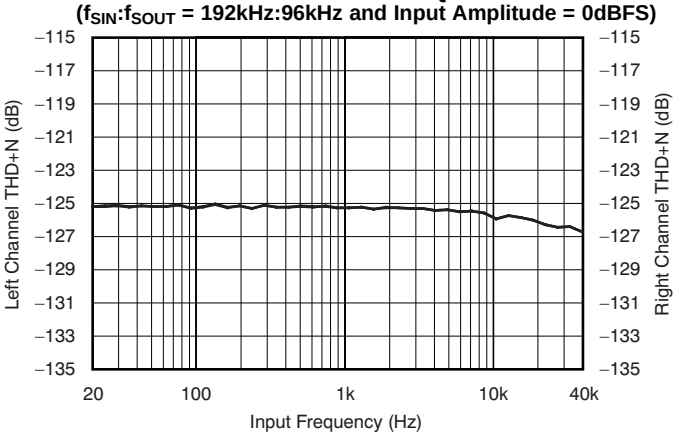

Figure 22.

THD+N vs INPUT FREQUENCY (f_{SIN}:f_{SOUT} = 192kHz:192kHz and Input Amplitude = 0dBFS)

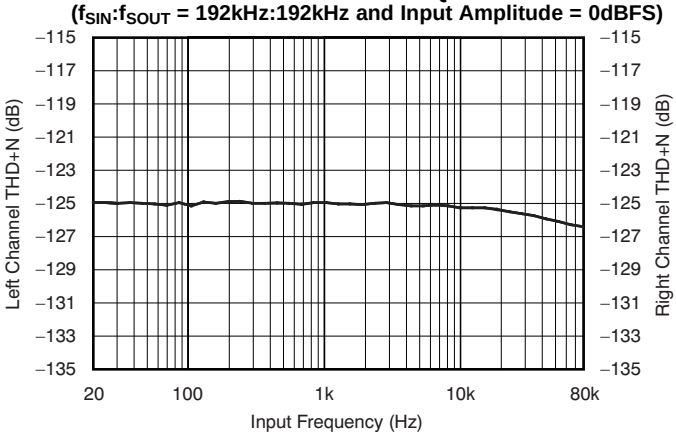

Figure 23.

THD+N vs INPUT AMPLITUDE (f_{SIN}:f_{SOUT} = 44.1kHz:44.1kHz and Input Frequency = 997Hz)

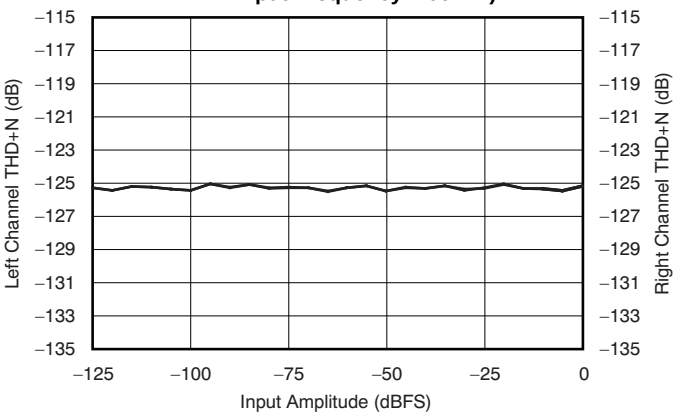

Figure 24.

THD+N vs INPUT AMPLITUDE (f_{SIN}:f_{SOUT} = 44.1kHz:48kHz and Input Frequency = 997Hz)

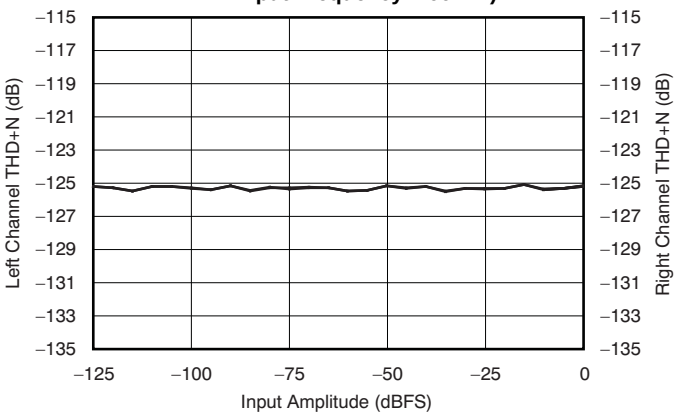

Figure 25.

THD+N vs INPUT AMPLITUDE (f_{SIN}:f_{SOUT} = 44.1kHz:96kHz and Input Frequency = 997Hz)

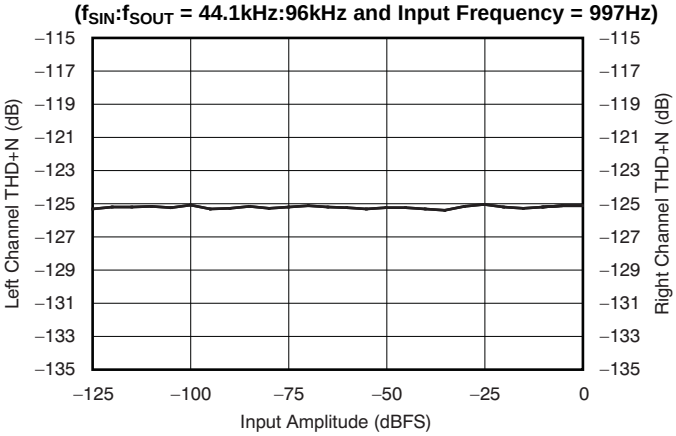

Figure 26.

THD+N vs INPUT AMPLITUDE (f_{SIN}:f_{SOUT} = 44.1kHz:192kHz and Input Frequency = 997Hz)

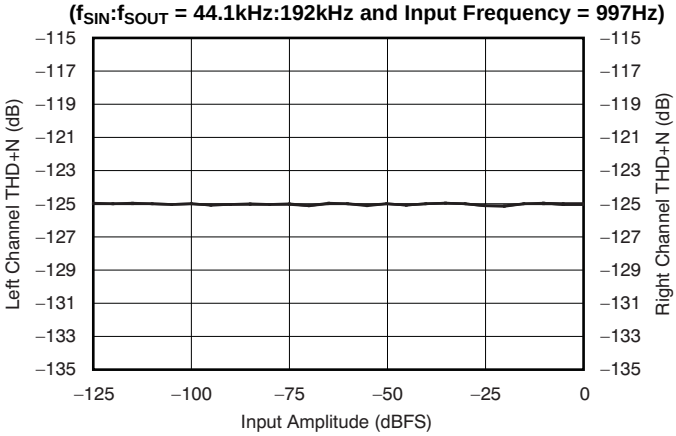

Figure 27.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 48kHz:44.1kHz and Input Frequency = 997Hz)

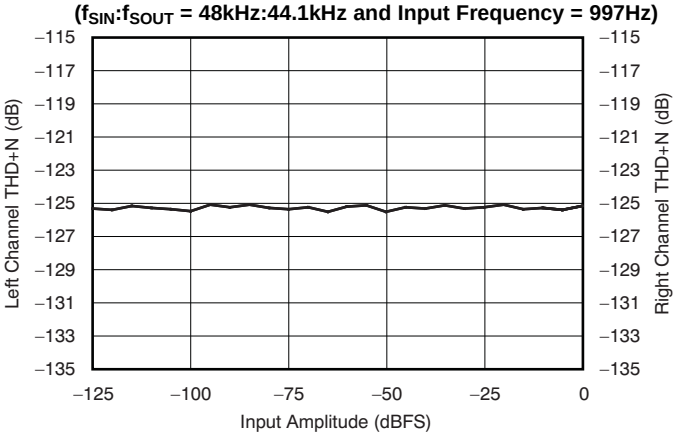

Figure 28.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 48kHz:48kHz and Input Frequency = 997Hz)

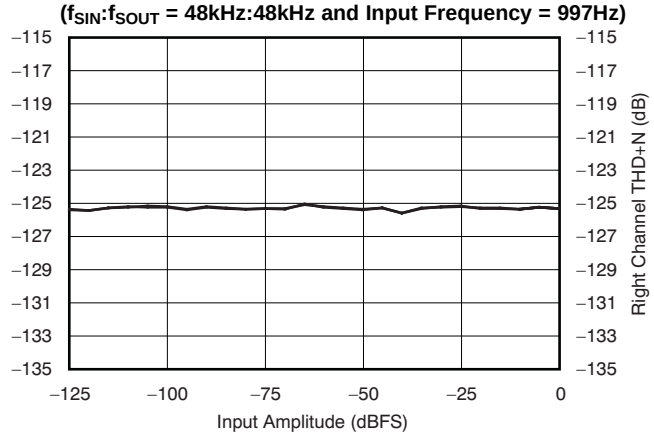

Figure 29.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 48kHz:96kHz and Input Frequency = 997Hz)

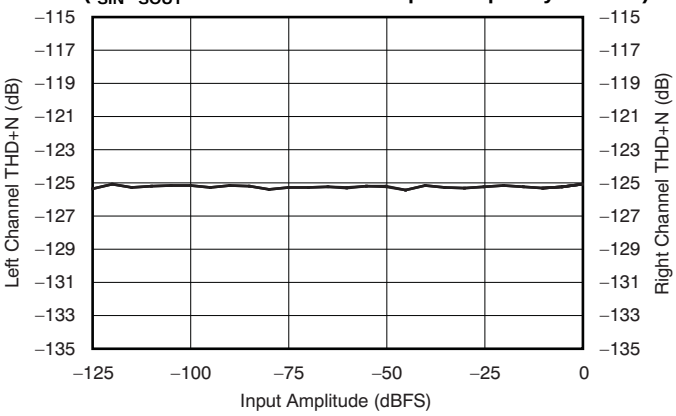

Figure 30.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 48kHz:192kHz and Input Frequency = 997Hz)

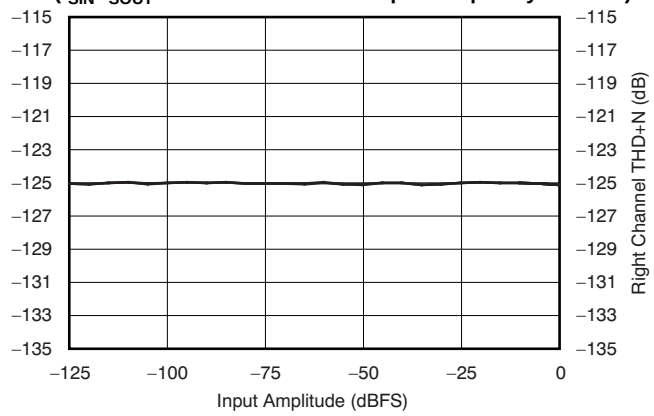

Figure 31.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 96kHz:44.1kHz and Input Frequency = 997Hz)

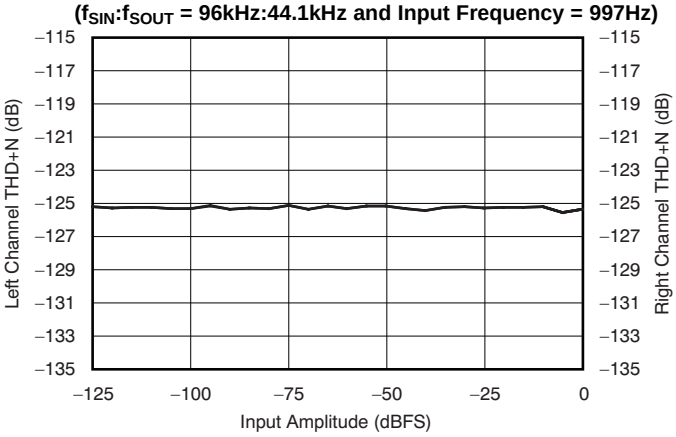

Figure 32.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 96kHz:48kHz and Input Frequency = 997Hz)

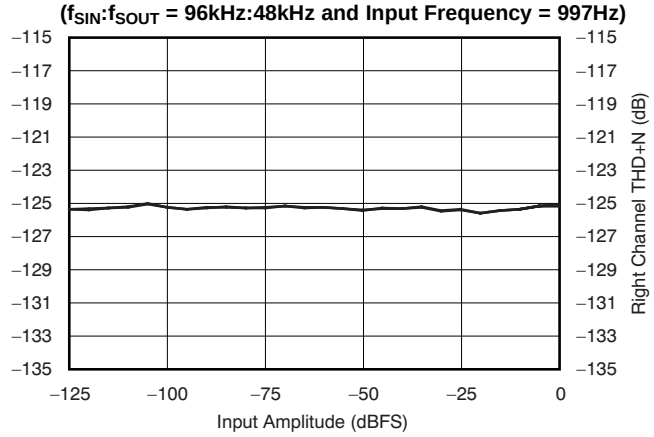

Figure 33.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 96kHz:96kHz and Input Frequency = 997Hz)

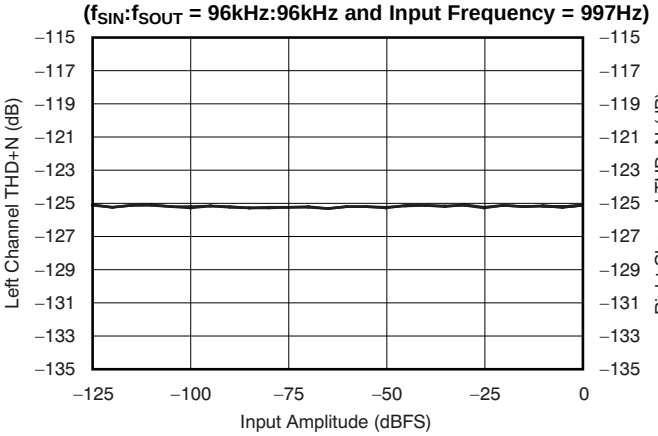

Figure 34.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 96kHz:192kHz and Input Frequency = 997Hz)

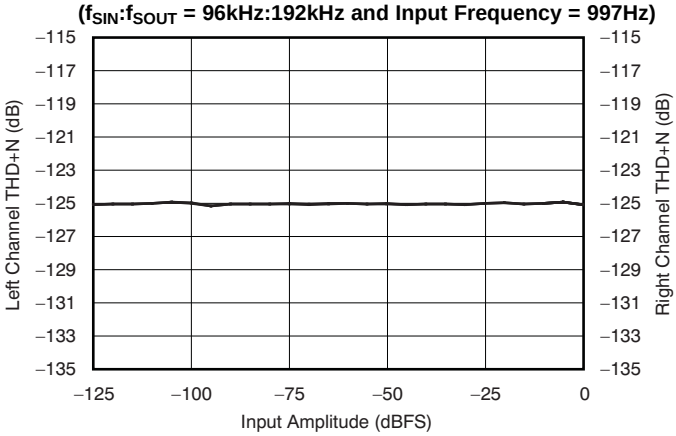

Figure 35.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 192kHz:44.1kHz and Input Frequency = 997Hz)

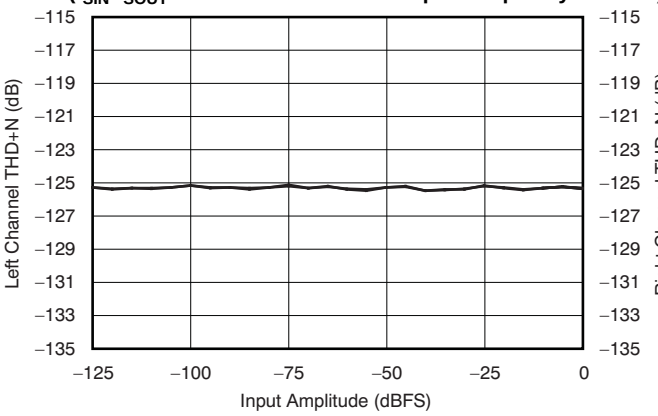

Figure 36.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 192kHz:48kHz and Input Frequency = 997Hz)

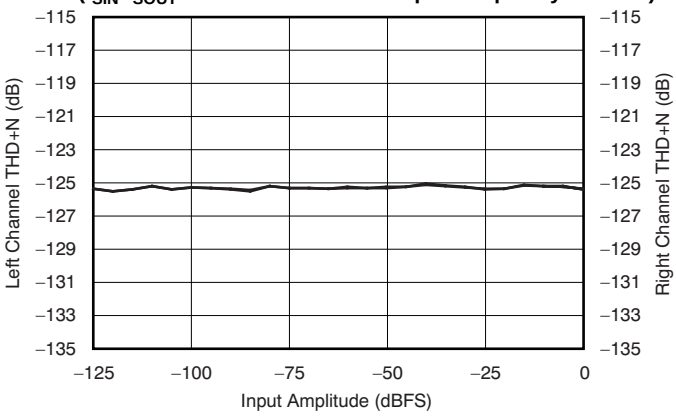

Figure 37.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 192kHz:96kHz and Input Frequency = 997Hz)

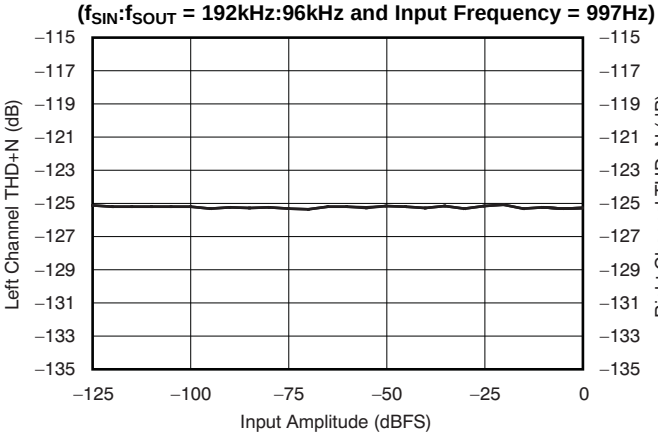

Figure 38.

THD+N vs INPUT AMPLITUDE
(f_{SIN}:f_{SOUT} = 192kHz:192kHz and Input Frequency = 997Hz)

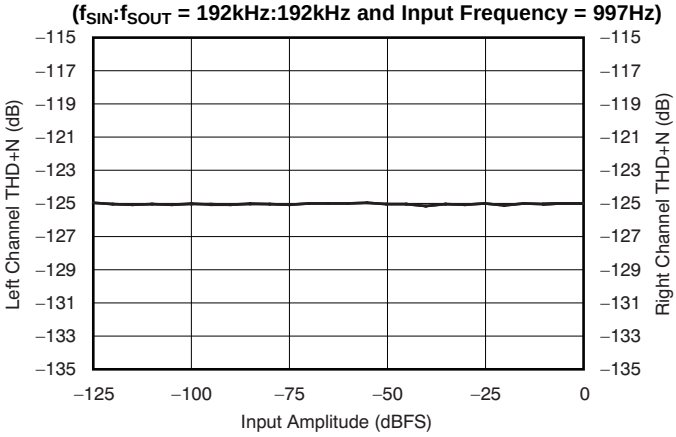

Figure 39.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

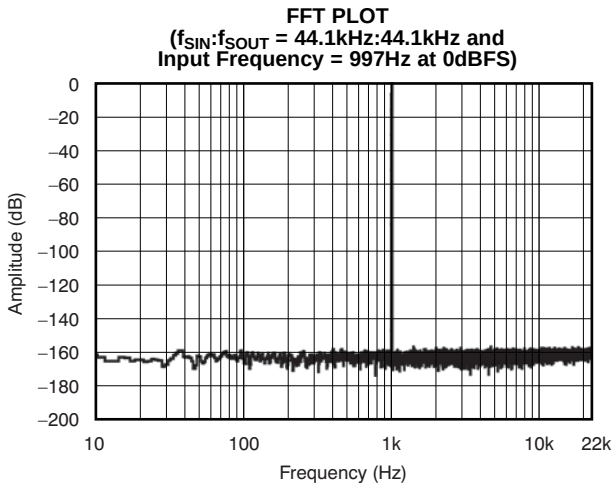

Figure 40.

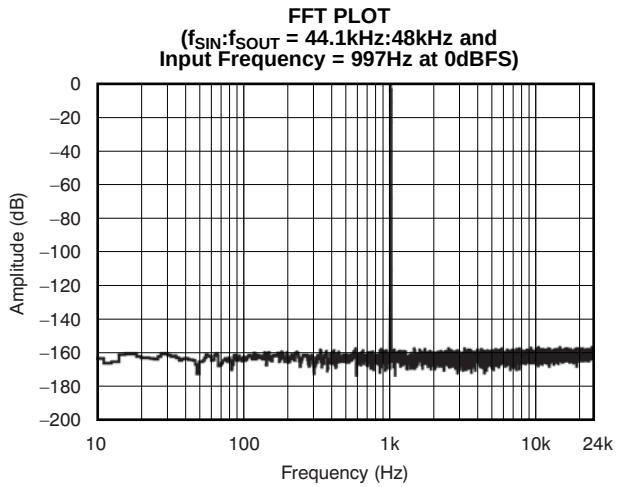

Figure 41.

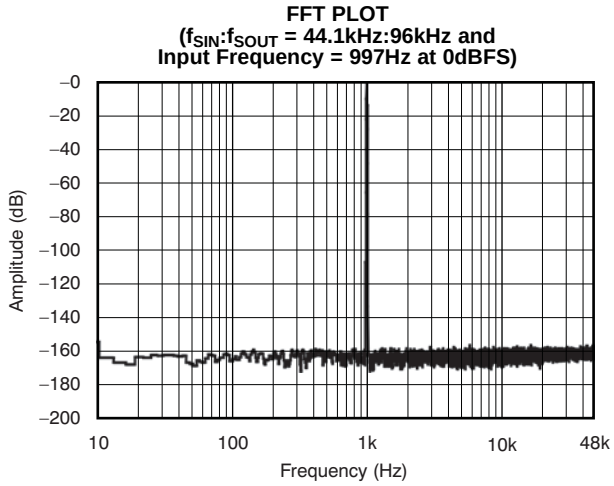

Figure 42.

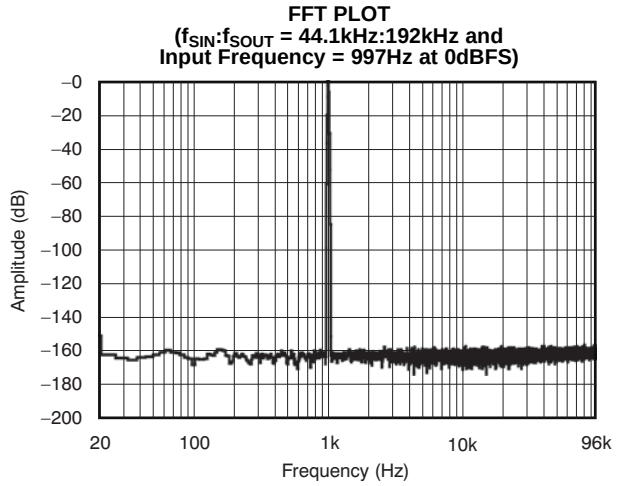

Figure 43.

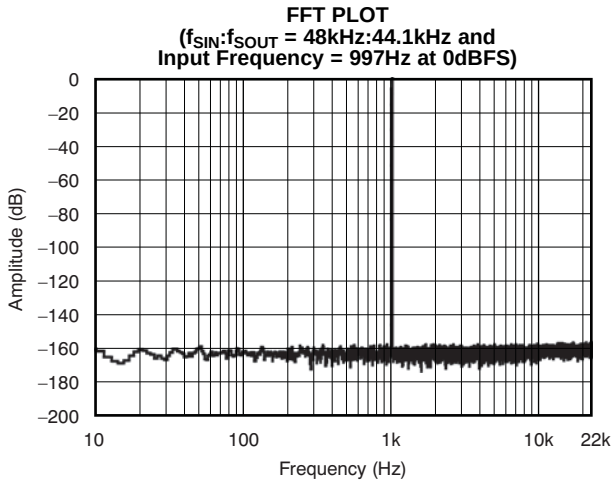

Figure 44.

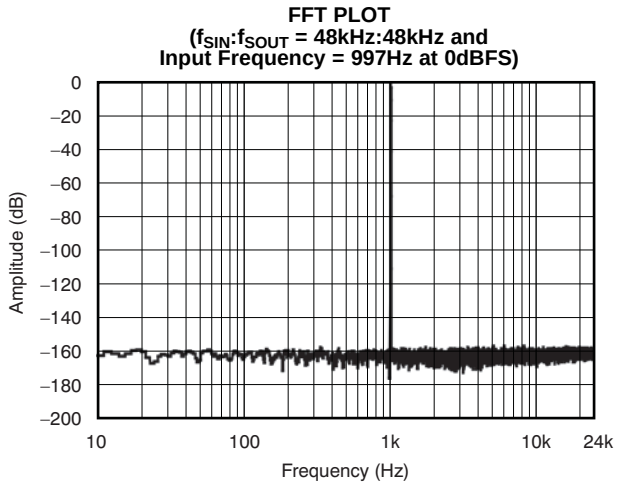

Figure 45.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

FFT PLOT
(f_{SIN}:f_{SOUT} = 48kHz:96kHz and Input Frequency = 997Hz at 0dBFS)

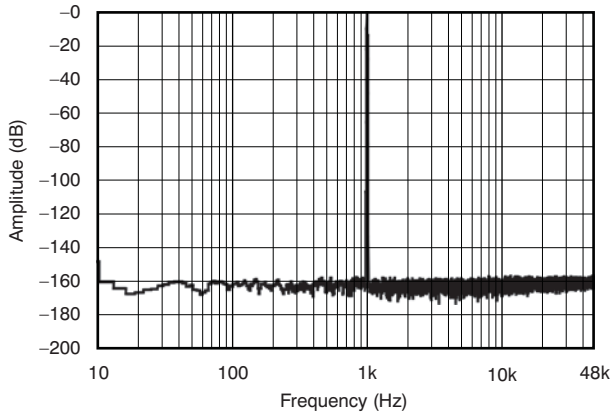

Figure 46.

FFT PLOT
(f_{SIN}:f_{SOUT} = 48kHz:192kHz and Input Frequency = 997Hz at 0dBFS)

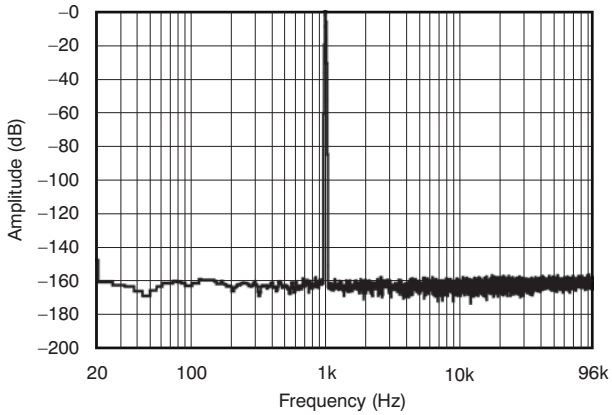

Figure 47.

FFT PLOT
(f_{SIN}:f_{SOUT} = 96kHz:44.1kHz and Input Frequency = 997Hz at 0dBFS)

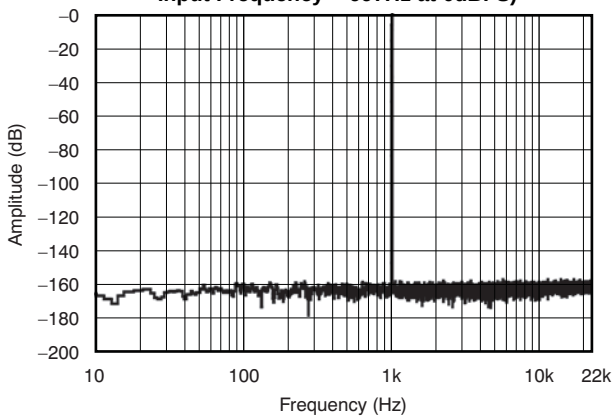

Figure 48.

FFT PLOT
(f_{SIN}:f_{SOUT} = 96kHz:48kHz and Input Frequency = 997Hz at 0dBFS)

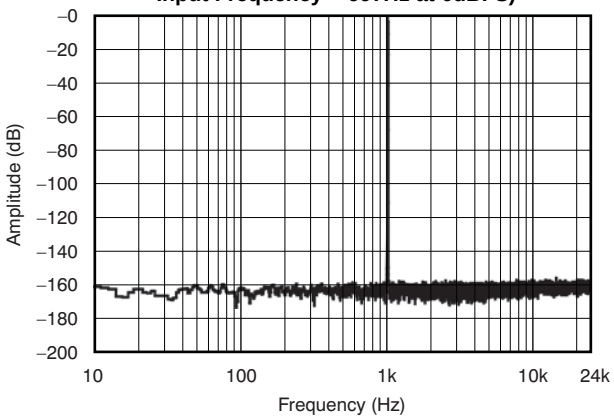

Figure 49.

FFT PLOT
(f_{SIN}:f_{SOUT} = 96kHz:96kHz and Input Frequency = 997Hz at 0dBFS)

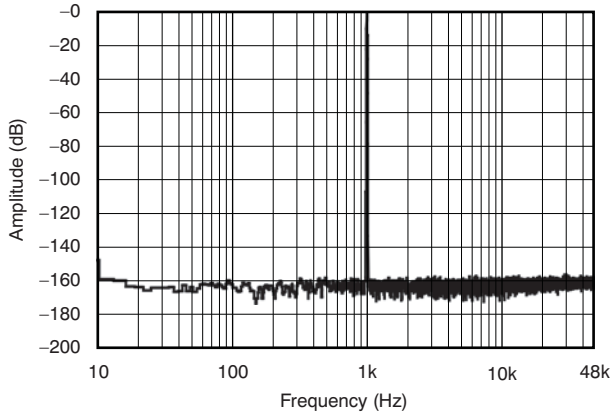

Figure 50.

FFT PLOT
(f_{SIN}:f_{SOUT} = 96kHz:192kHz and Input Frequency = 997Hz at 0dBFS)

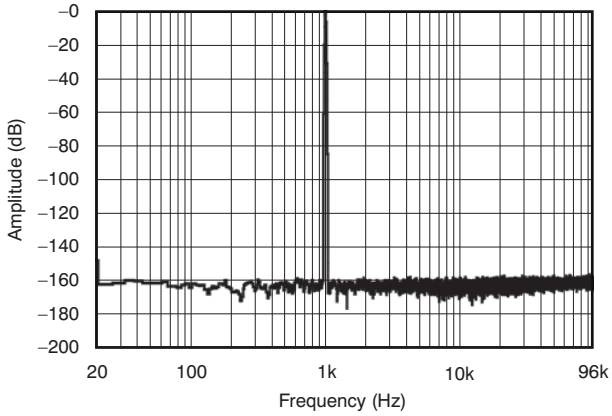

Figure 51.

TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

FFT PLOT
(f_{SIN}:f_{SOUT} = 192kHz:44.1kHz and Input Frequency = 997Hz at 0dBFS)

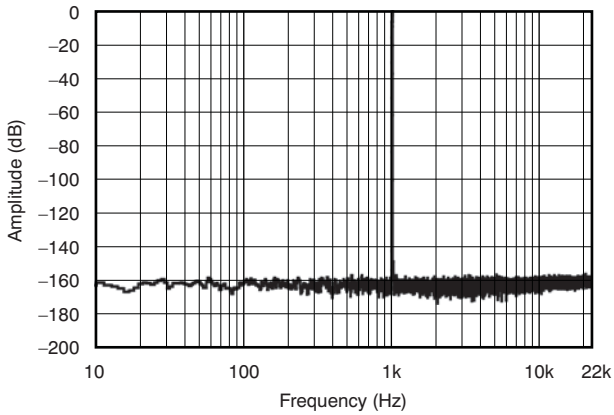

Figure 52.

FFT PLOT
(f_{SIN}:f_{SOUT} = 192kHz:48kHz and Input Frequency = 997Hz at 0dBFS)

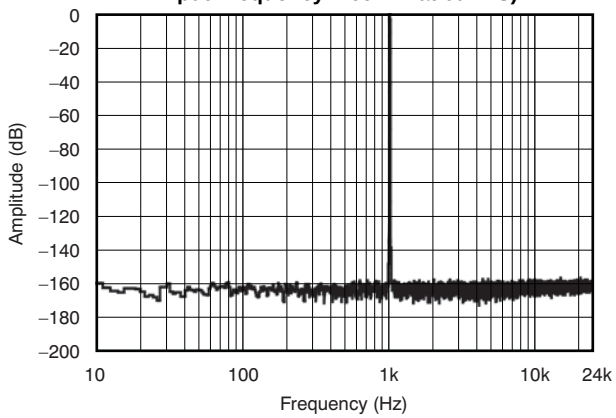

Figure 53.

FFT PLOT
(f_{SIN}:f_{SOUT} = 192kHz:96kHz and Input Frequency = 997Hz at 0dBFS)

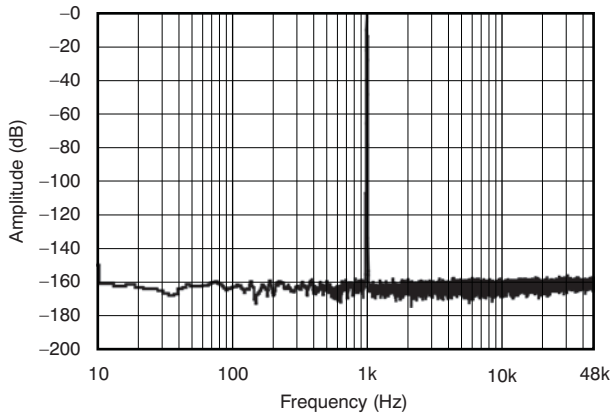

Figure 54.

FFT PLOT
(f_{SIN}:f_{SOUT} = 192kHz:192kHz and Input Frequency = 997Hz at 0dBFS)

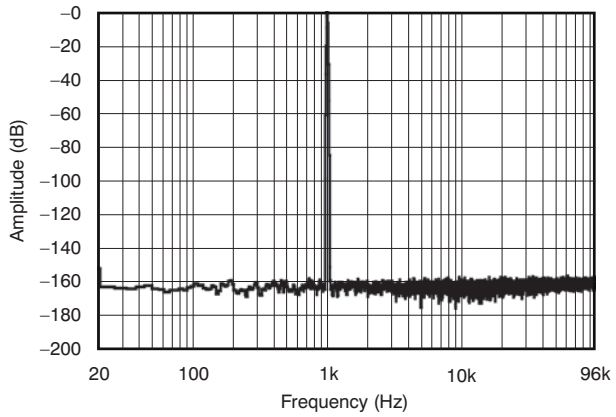

Figure 55.

IMD
(f_{SIN}:f_{SOUT} = 44.1kHz:48kHz, SMPTE/DIN 1:1, 10kHz and 11kHz, and –0.1dB Input Amplitude)

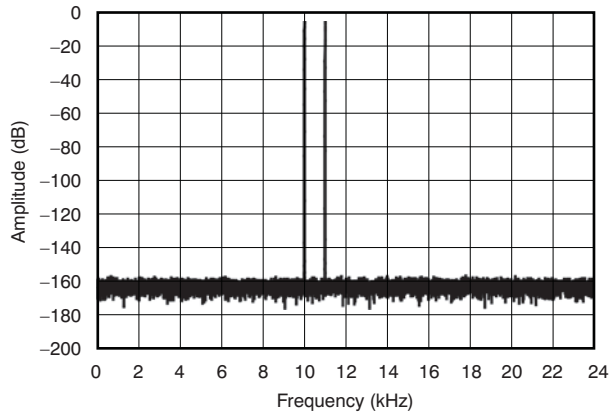

Figure 56.

IMD
(f_{SIN}:f_{SOUT} = 48kHz:44.1kHz, SMPTE/DIN 1:1, 10kHz and 11kHz, and –0.1dB Input Amplitude)

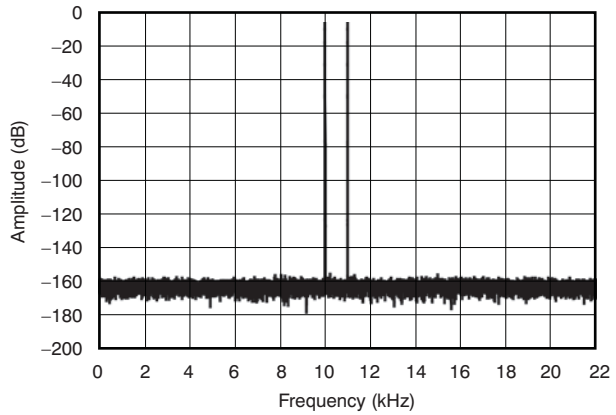

Figure 57.

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TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = +25C, VDD18 = +1.8V, VDD33 = +3.3V, VIO = +3.3V, and VCC = +3.3V, unless otherwise noted.

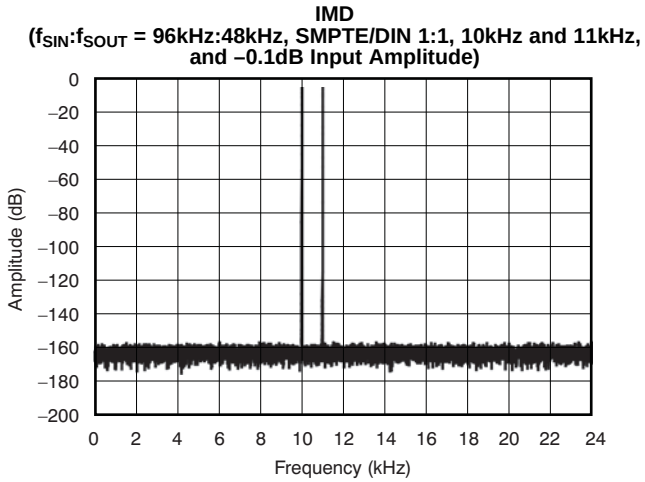

Figure 58.

PRODUCT OVERVIEW

The SRC4382 is a two-channel asynchronous sample rate converter (SRC) with an integrated digital audio interface receiver and transmitter (DIR and DIT). Two audio serial ports, Port A and Port B, support input and output interfacing to external data converters, signal processors, and logic devices. On-chip routing logic provides for flexible interconnection between the five functional blocks. The audio serial ports, DIT, and SRC may be operated at sampling rates up to 216kHz. The DIR is specified for a PLL lock range that includes sampling rates from 20kHz to 216kHz. All function blocks support audio data word lengths up to 24 bits.

The SRC4382 requires an external host processor or logic for configuration control. The SRC4382 includes a user-selectable serial host interface, which operates as either a 4-wire serial peripheral interface (SPI) port or a 2-wire Philips I^2C bus interface. The SPI port operates at bit rates up to 40MHz. The I^2C bus interface may be operated in standard or fast modes, supporting operation at 100kbps and 400kbps, respectively. The SPI and I^2C interfaces provide access to internal control and status registers, as well as the buffers utilized for the DIR and DIT channel status and user data.

The asynchronous SRC is based upon the successful SRC4192 core from Texas Instruments. The SRC in the SRC4382 has been further enhanced to provide exceptional jitter attenuation characteristics, helping to improve overall application performance. The SRC operates over a wide input-to-output sampling ratio range, from 1:16 to 16:1 continuous. The input-to-output sampling ratio is determined automatically by the SRC rate estimation circuitry, with the digital re-sampler parameters being updated in real-time without the need for programming. Interpolation and decimation filter delay are user-selectable. Additional SRC features include de-emphasis filtering, output word length reduction, output attenuation and muting, and input-to-output sampling ratio readback via status registers.

The digital interface receiver (DIR) includes four differential input line receiver circuits, suitable for balanced or unbalanced cable interfaces. Interfacing to optical receiver modules and CMOS logic devices is also supported. The outputs of the line receivers are connected to a 1-of-4 data selector, referred to as the receiver input multiplexer, which is utilized to select one of the four line receiver outputs for processing by the DIR core. The outputs of the line receivers are also connected to a second data selector, the bypass multiplexer, which may be used to route input data streams to the DIT CMOS output buffer and differential line driver functions. This configuration provides a bypass signal path for AES3-encoded input data streams.

The DIR core decodes the selected input stream data and separates the audio, channel status, user, validity, and parity data. Channel status and user data is stored in block-sized buffers, which may be accessed via the SPI or I^2C serial host interface, or routed directly to the general-purpose output pins (GPO1 through GPO4). The validity and parity bits are processed to determine error status. The DIR core recovers a low jitter master clock, which may be utilized to generate word and bit clocks using on-chip or external logic circuitry.

The digital interface transmitter (DIT) encodes digital audio input data into an AES3 formatted output data stream. Two DIT outputs are provided, including a differential line driver and a CMOS output buffer. Both the line driver and buffer include 1-of-2 input data selectors, which are utilized to choose either the output of the DIT AES3 encoder, or the output of the bypass multiplexer. The line driver output is suitable for balanced or unbalanced cable interfaces, while the CMOS output buffer supports interfacing to optical transmitter modules and external logic or line drivers. The DIT includes block-sized data buffers for both channel status and user data. These buffers are accessed via either the SPI or I^2C host interface, or may be loaded directly from the DIR channel status and user data buffers.

The SRC4382 includes four general-purpose digital outputs, or GPO pins. The GPO pins may be configured as simple logic outputs, which may be programmed to either a low or high state. Alternatively, the GPO pins may be connected to one of 14 internal logic nodes, allowing them to serve as functional, status, or interrupt outputs. The GPO pins provide added utility in applications where hardware access to selected internal logic signals may be necessary.

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Figure 59 shows a simplified functional block diagram for the SRC4382. Additional details for each function block will be covered in respective sections of this datasheet.

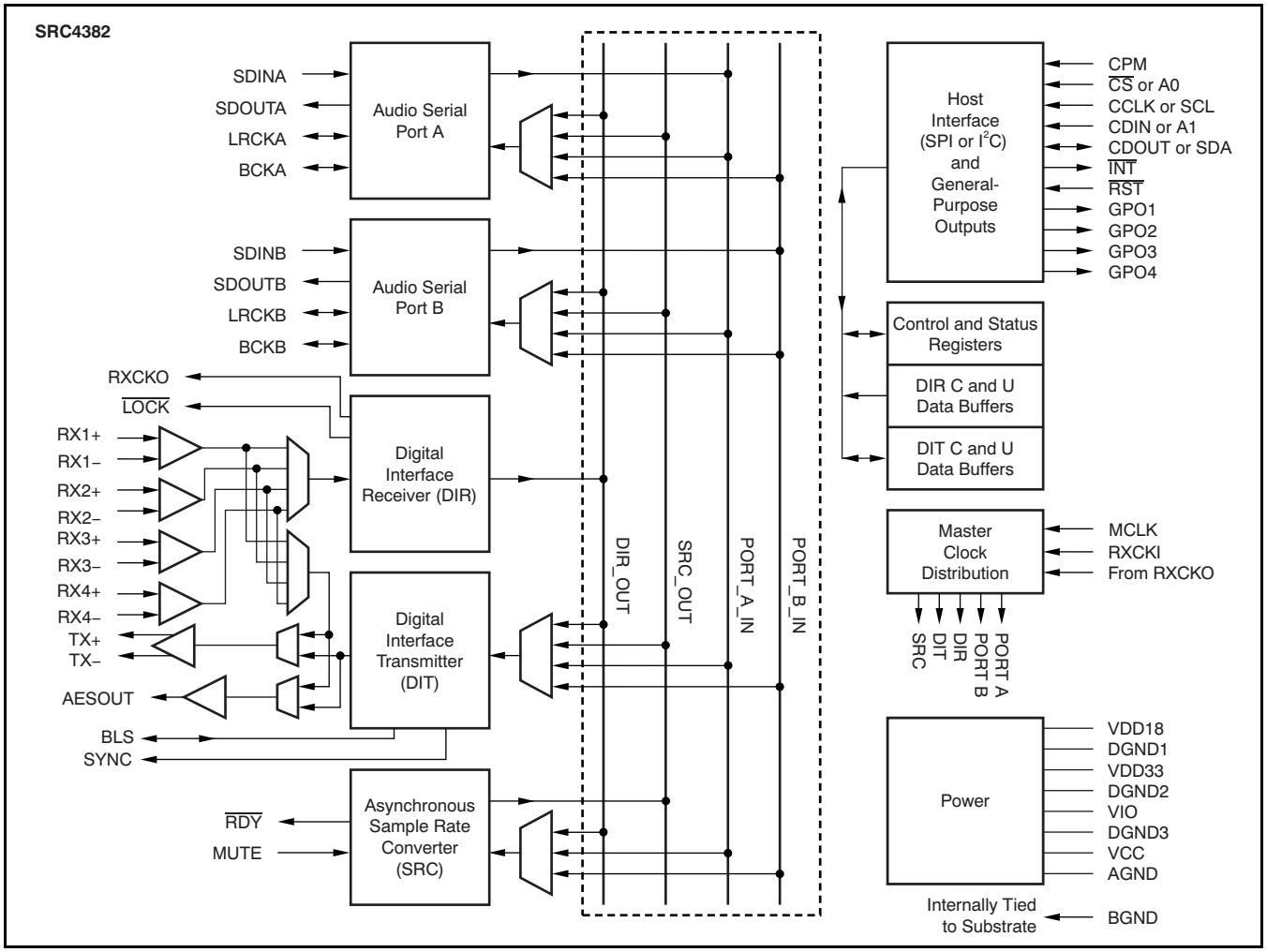

Figure 59. Functional Block Diagram

RESET OPERATION

The SRC4382 includes an asynchronous active low reset input, $\overline{RST}$ (pin 24), which may be used to initialize the internal logic at any time. The reset sequence forces all registers and buffers to their default settings. The reset low pulse width must be a minimum of 500ns in length. The user should not attempt a write or read operation using either the SPI or I^2C port for at least 500µs after the rising edge of $\overline{RST}$. See Figure 60 for the reset timing sequence of the SRC4382.

In addition to reset input, the RESET bit in control register 0x01 may be used to force an internal reset, whereby all registers and buffers are forced to their default settings. Refer to the Control Registers section for details regarding the RESET bit function.

Upon reset initialization, all functional blocks of the SRC4382 default to the powered-down state, with the exception of the SPI or I^2C host interface and the corresponding control registers. The user may then program the SRC4382 to the desired configuration, and then release the desired function blocks from the power-down state utilizing the corresponding bits in control register 0x01.

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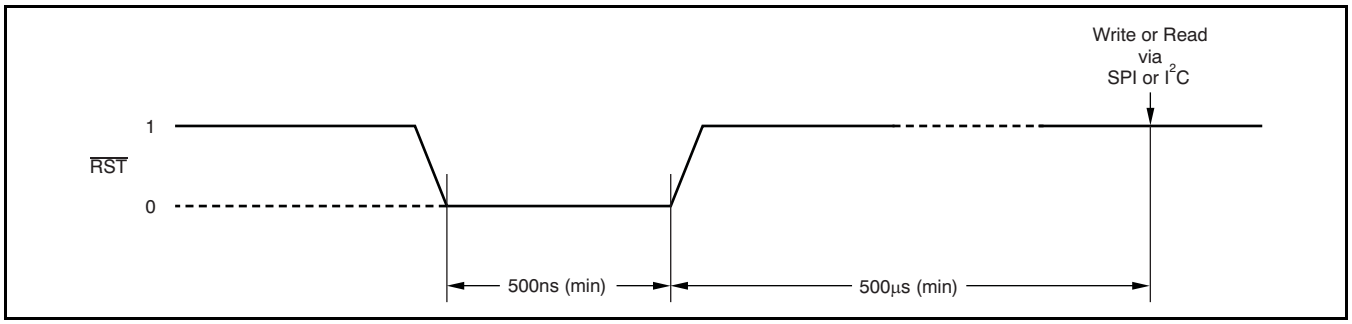

Figure 60. Reset Sequence Timing

MASTER AND REFERENCE CLOCKS

The SRC4382 includes two clock inputs, MCLK (pin 25) and RXCKI (pin 13). The MCLK clock input is typically used as the master clock source for the audio serial ports, the DIT, and/or the SRC. The MCLK may also be utilized as the reference clock for the DIR. The RXCKI clock input is typically used for the DIR reference clock source, although it may also be used as the master or reference clock source for the audio serial ports and/or the SRC.

In addition to the MCLK and RXCKI clock sources, the DIR core recovers a master clock from the AES3-encoded input data stream. This clock is suitable for use as a master or system clock source in many applications. The recovered master clock output, RXCKO (pin 12), may be utilized as the master or reference clock source for the audio serial ports, the DIT, and/or the SRC, as well as external audio devices.

The master clock frequency for the audio serial ports (Port A and Port B) depends on the Slave or Master mode configuration of the port. In Slave mode, the ports do not require a master clock, as the left/right word and bit clocks are inputs, sourced from an external audio device serving as the serial bus timing master. In Master mode, the serial ports derive the left/right word and bit clock outputs from the selected master clock source, MCLK, RXCKI, or RXCKO. The left/right word clock rate is derived from the selected master clock source using one of four clock divider settings (divide by 128, 256, 384, or 512). Refer to the Audio Serial Port Operation section for additional details.

The DIT always requires a master clock source, which may be either the MCLK input, or the DIR recovered clock output, RXCKO. Like the audio serial ports, the DIT output frame rate is derived from the selected master clock using one of four clock divider settings (divide by 128, 256, 384, or 512). Refer to the Digital Interface Transmitter (DIT) Operation section for additional details.

The DIR reference clock may be any frequency that meets the PLL1 setup requirements, described in the Control Registers section. Typically, a common audio system clock rate, such as 11.2896MHz, 12.288MHz, 22.5792MHz, or 24.576MHz, may be used for this clock.

The SRC reference clock rate may be any frequency up to 27.7MHz, and does not have to be related to or synchronous with the input or output sampling rates. The MCLK, RXCKI, or RXCKO clocks may be utilized as the reference clock source for the SRC. Refer to the Asynchronous Sample Rate Converter (SRC) Operation section for additional details.

It is recommended that the clock sources for MCLK and RXCKI input be generated by low-jitter crystal oscillators for optimal performance. In general, phase-locked loop (PLL) clock synthesizers should be avoided, unless they are designed and/or specified for low clock jitter.

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AUDIO SERIAL PORT OPERATION

The SRC4382 includes two audio serial ports, Port A and Port B. Both ports are 4-wire synchronous serial interfaces, supporting simultaneous input and output operation. Since each port has only one pair of left/right word and bit clocks, the input and output sampling rates are identical. A simplified block diagram is shown in Figure 61.

The audio serial ports may be operated at sampling rates up to 216kHz, and support audio data word lengths up to 24 bits. Philips I^2S, Left-Justified, and Right-Justified serial data formats are supported. Refer to Figure 62.

The left/right word clock (LRCKA or LRCKB) and the bit clock (BCKA or BCKB) may be configured for either Master or Slave mode operation. In Master mode these clocks are outputs, derived from the selected master clock source using internal clock dividers. The master clock source may be 128, 256, 384, or 512 times the audio input/output sampling rate, with the clock divider being selected using control register bits for each port. In Slave mode the left/right word and bit clocks are inputs, being sourced from an external audio device acting as the serial bus master.

The LRCKA or LRCKB clocks operate at the input/output sampling rate, f_S. The BCKA and BCKB clock rates are fixed at 64 times the left/right word clock rate in Master mode. For Slave mode, the minimum BCKA and BCKB clock rate is determined by the audio data word length multiplied by two, since there are two audio data channels per left/right word clock period. For example, if the audio data word length is 24 bits, the bit clock rate must be at least 48 times the left/right word clock rate, allowing one bit clock period for each data bit in the serial bit stream.

Serial audio data is clocked into the port on the rising edge of the bit clock, while data is clocked out of the port on the falling edge of the bit clock. Refer to the Electrical Characteristics: *Audio Serial Ports* table for parametric information and Figure 1 for a timing diagram related to audio serial port operation.

The audio serial ports are configured using control registers 0x03 through 0x06. Refer to the Control Registers section for descriptions of the control register bits.

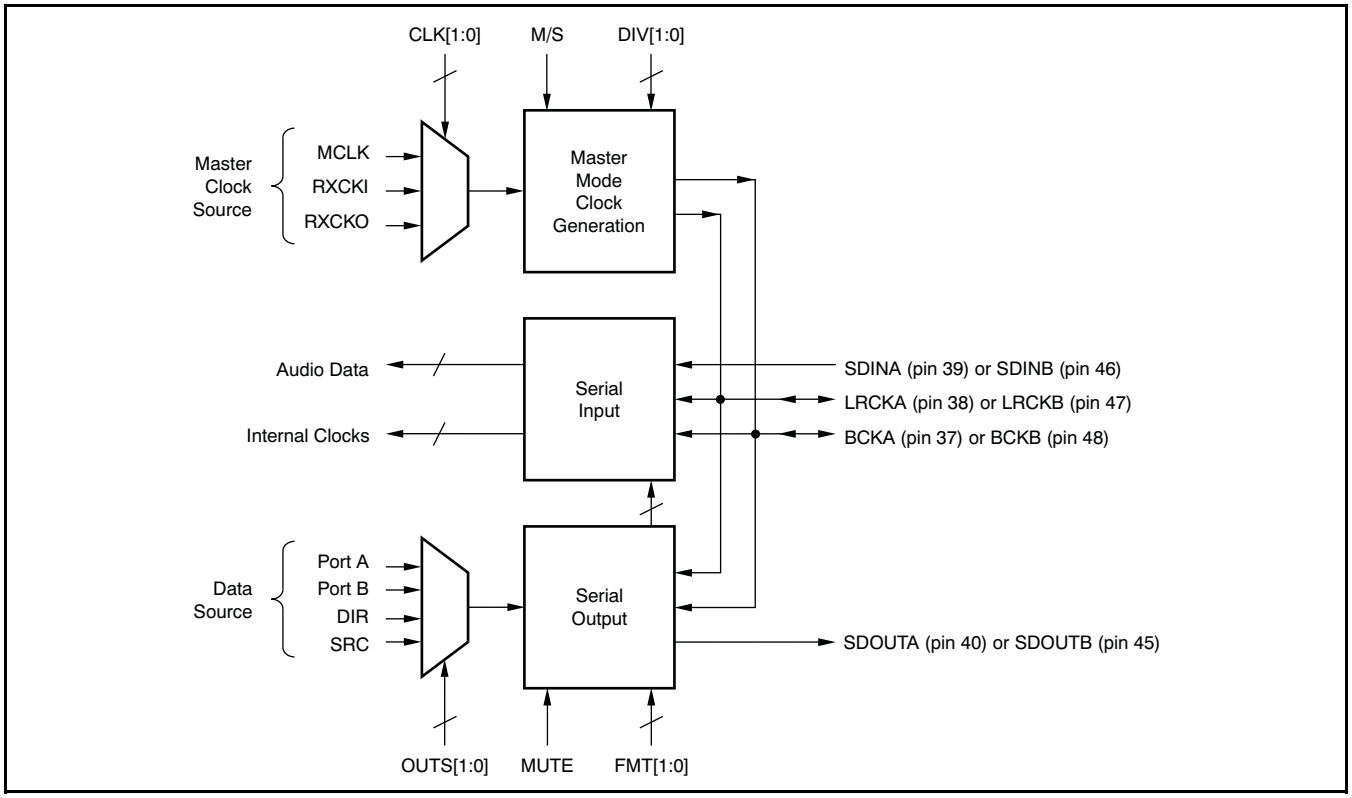

Figure 61. Audio Serial Port Block Diagram

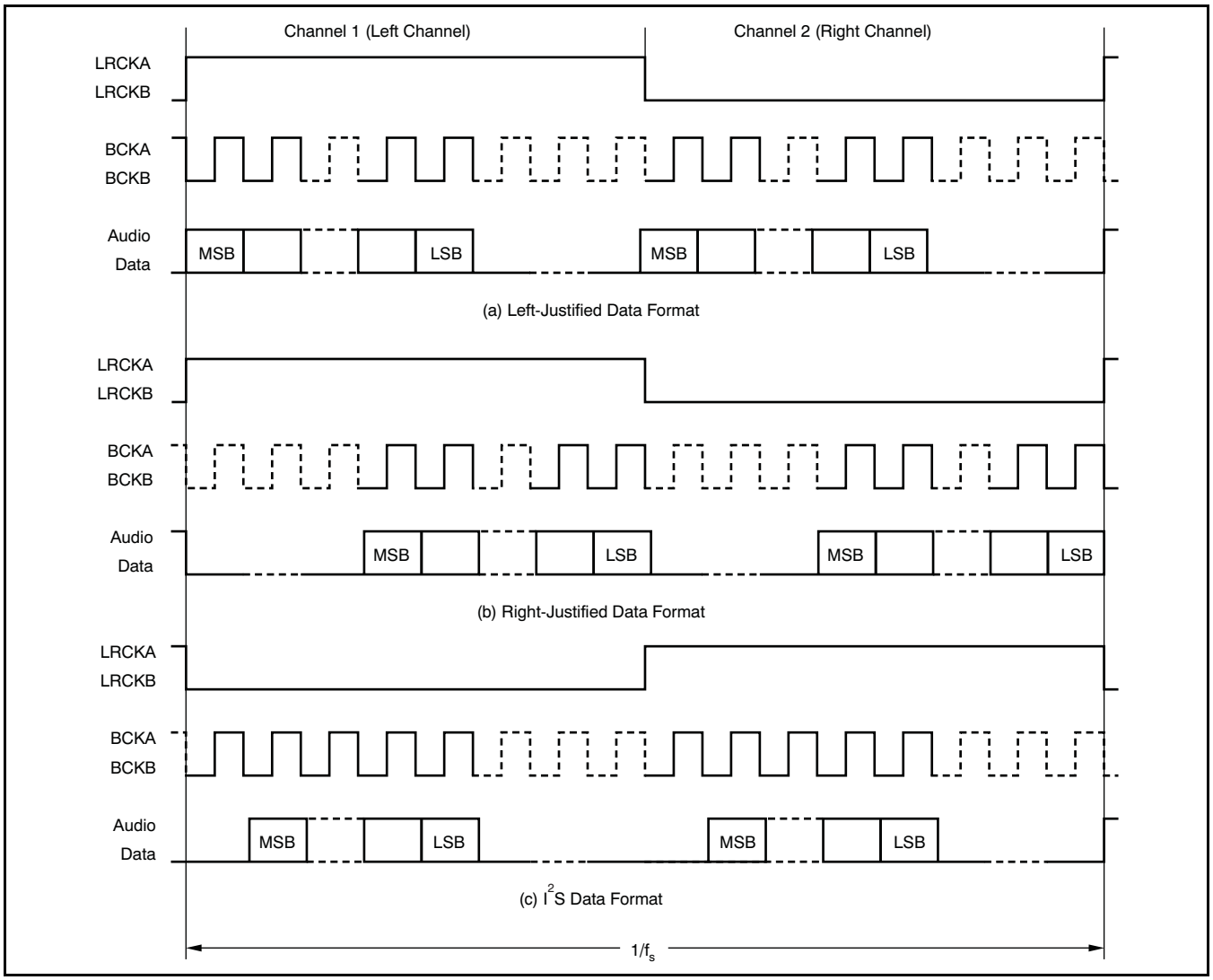

Figure 62. Audio Data Formats

OVERVIEW OF THE AES3 DIGITAL AUDIO INTERFACE PROTOCOL

This section introduces the basics of digital audio interface protocols pertaining to the transmitter (DIT) and receiver (DIR) blocks of the SRC4382. Emphasis is placed upon defining the basic terminology and characteristics associated with the AES3-2003 standard protocol, the principles of which may also be applied to a number of consumer-interface variations, including S/PDIF, IEC-60958, and EIAJ CP-1201. It is assumed that the reader is familiar with the AES3 and S/PDIF interface formats. Additional information is available from the sources listed in the Reference Documents section.

The AES3-2003 standard defines a technique for two-channel linear PCM data transmission over 110Ω shielded twisted-pair cable. The AES-3id document extends the AES3 interface to applications employing 75Ω coaxial cable connections. In addition, consumer transmission variants, such as those defined by the S/PDIF, IEC 60958, and CP-1201 standards, utilize the same encoding techniques but with different physical interfaces or transmission media. Channel status data definitions also vary between professional and consumer interface implementations.

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For AES3 transmission, data is encoded into frames, with each frame containing two subframes of audio and status data, corresponding to audio Channels 1 and 2 (or Left and Right, respectively, for stereophonic audio). Figure 63 shows the AES3 frame and subframe formatting. Each subframe includes four bits for the preamble, up to 24 bits for audio and/or auxiliary data, one bit indicating data validity (V), one bit for channel status data (C), one bit for user data (U), and one bit for setting parity (P).

The 4-bit preamble is used for synchronization and identification of blocks and subframes. The X and Y preamble codes are used to identify the start of the Channel 1 and Channel 2 subframes, as shown in Figure 63. However, the X preamble for the first subframe of every 192 frames is replaced by the Z preamble, which identifies the start of a new block of channel status and user data.

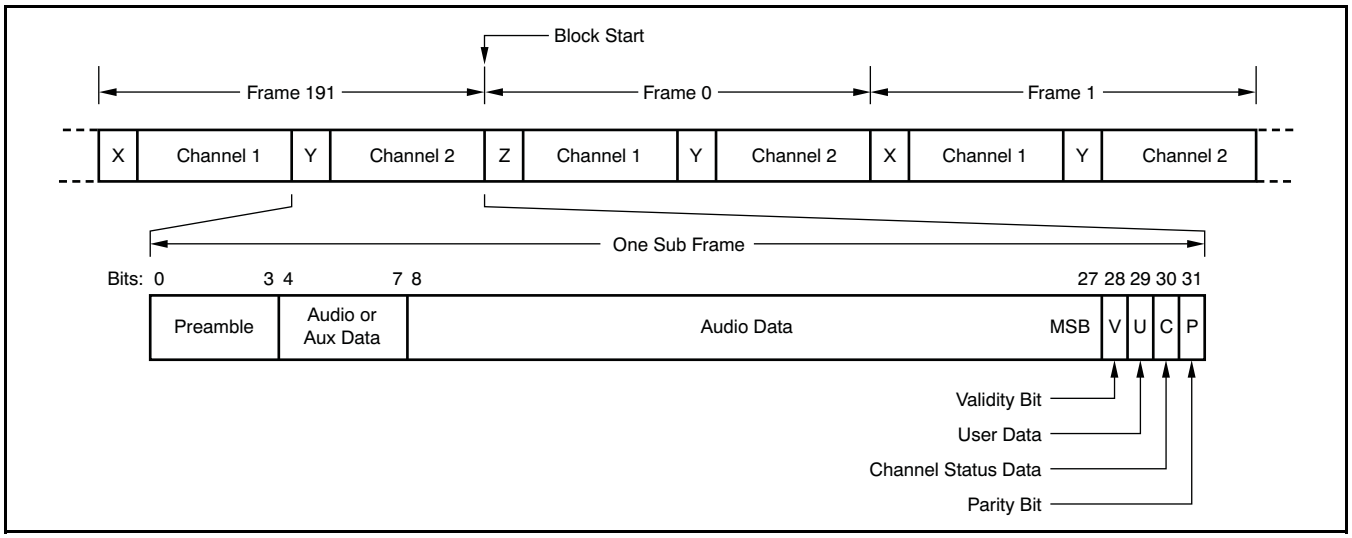

Figure 63. AES3 Frame and Subframe Encoding

One block is comprised of 192 frames of data. This format translates to 192 bits each for channel status and user data for each channel. The 192 bits are organized into 24 data bytes, which are defined by the AES3-2003 and consumer standards documents. The AES18 standard defines recommended usage and formatting of the user data bits, while consumer applications may utilize the user data for other purposes. The SRC4382 also includes block-sized transmitter and receiver channel status and user data buffers, which have 24 bytes each for the channel status and user data assigned to audio Channels 1 and 2. Refer to the Channel Status and User Data Buffer Maps section for the organization of the buffered channel status and user data for the receiver and transmitter functions.

The audio data for Channel 1 and Channel 2 may be up to 24 bits in length, and occupies bits 4 through 27 of the corresponding subframe. Bit 4 is the LSB while bit 27 is the MSB. If only 20 bits are required for audio data, then bits 8 through 27 are utilized for audio data, while bits 4 though 7 are utilized for auxiliary data bits.

The validity (V) bit indicates whether or not the audio sample word being transmitted is suitable for digital-to-analog (D/A) conversion or further digital processing at the receiver end of the connection. If the validity bit is 0, then the audio sample is suitable for conversion or additional processing. If the validity bit is 1, then the audio sample is not suitable for conversion or additional processing.

The parity (P) bit is set to either a 0 or 1, such that bits 4 through 31 carry an even number of ones and zeros for even parity. The DIT block in the SRC4382 automatically manages the parity bit, setting it to a 0 or 1 as needed. The DIR block checks the parity of bits 4 though 31 and generates a parity error if odd parity is detected.

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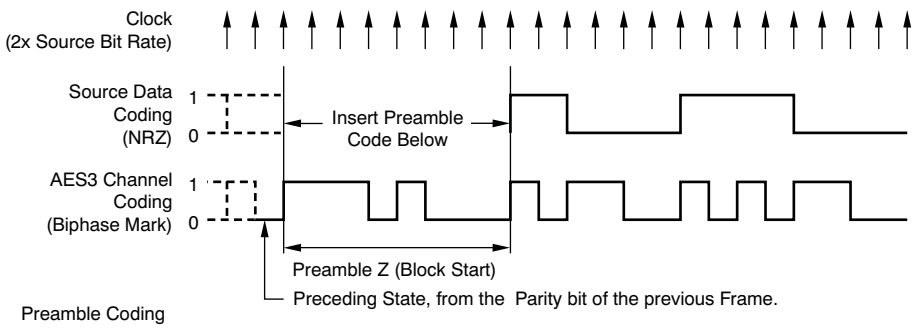
The binary non-return to zero (NRZ) formatted audio and status source data for bits 4 through 31 of each subframe are encoded utilizing a Biphase Mark format for transmission. This format allows for clock recovery at the receiver end, as well as making the interface insensitive to the polarity of the balanced cable connections. The preambles at the start of each subframe are encoded to intentionally violate the Biphase Mark formatting, making their detection by the receiver reliable, as well as avoiding the possibility of audio and status data imitating the preambles. Figure 64 shows the Biphase Mark and preamble encoding.

Although the AES3 standard originally defined transmission for sampling rates up to 48kHz, the interface is capable of handling higher sampling rates, given that attention is paid to cable length and impedance matching. Equalization at the receiver may also be required, depending on the cable and matching factors. It is also possible to transmit and decode more than two channels of audio data utilizing the AES3 or related consumer interfaces. Special encoding and/or compression algorithms are utilized to support multiple channels, including the Dolby® AC-3, DTS, MPEG-1/2, and other data reduced audio formats.



Preamble Coding

Preceding State:	0	1	
Preamble:	Channel Coding:	Channel Coding:	Description:
X	11100010	00011101	Channel 1 Subframe
Y	11100100	00011011	Channel 2 Subframe
Z	11101000	00010111	Channel 1 Subframe and Block Start

Figure 64. Biphase Mark Encoding

DIGITAL INTERFACE TRANSMITTER (DIT) OPERATION

The DIT encodes a given two-channel or data-reduced audio input stream into an AES3-encoded output stream. In addition to the encoding function, the DIT includes differential line driver and CMOS buffered output functions. The line driver is suitable for driving balanced or unbalanced line interfaces, while the CMOS buffered output is designed to drive external logic or line drivers, as well as optical transmitter modules. Figure 65 illustrates the functional block diagram for the DIT.

The input of the DIT receives the audio data for Channels 1 and 2 from one of four possible sources: Port A, Port B, the DIR, or the SRC. By default, Port A is selected as the source. The DIT also requires a master clock source, which may be provided by either the MCLK input (pin 25) or RXCKO (the DIR recovered master clock output). A master clock divider is utilized to select the frame rate for the AES3-encoded output data. The TXDIV[1:0] bits in control register 0x07 are utilized to select divide by 128, 256, 384, or 512 operation.

Channel status and user data for Channels 1 and 2 are input to the AES3 encoder via the corresponding Transmitter Access (TA) data buffers. The TA data buffers are in turn loaded from the User Access (UA) buffers, which are programmed via the SPI or I^2C host interface, or loaded from the DIR Receiver Access (RA) data buffers. The source of the channel status and user data is selected utilizing the TXCUS[1:0] bits in control register 0x09. When the DIR is selected as the input source, the channel status and user data output from the DIT is delayed by one block in relation to the audio data.

The validity (V) bit may be programmed using one of two sources. The VALSEL bit in control register 0x09 is utilized to select the validity data source for the DIT block. The default source is the VALID bit in control register 0x07, which is written via the SPI or I^2C host interface. The validity bit may also be transferred from the AES3 decoder output of the DIR, where the V bit for the DIT subframes tracks the decoded DIR value frame by frame.

The parity (P) bit will always be generated by the AES3 encoder internal parity generator logic, such that bits 4 through 31 of the AES3-encoded subframe are even parity.

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The AES3 encoder output is connected to the output line driver and CMOS buffer source multiplexers. As shown in Figure 65, the source multiplexers allow the line driver or buffer to be driven by the AES3-encoded data from the DIT, or by the bypass multiplexer, which is associated with the outputs of the four differential input line receivers preceding the DIR core. The bypass multiplexer allows for one of the four line receiver outputs to be routed to the line driver or buffer output, thereby providing a bypass mode of operation. Both the line driver and CMOS output buffer include output disables, set by the TXOFF and AESOFF bits in control register 0x08. When the outputs are disabled, they are forced to a low logic state.

The AES3 encoder includes an output mute function that sets all bits for both the Channel 1 and 2 audio and auxiliary data to zero. The preamble, V, U, and C bits are unaffected, while the P bit is recalculated. The mute function is controlled using the TXMUTE bit in control register 0x08.

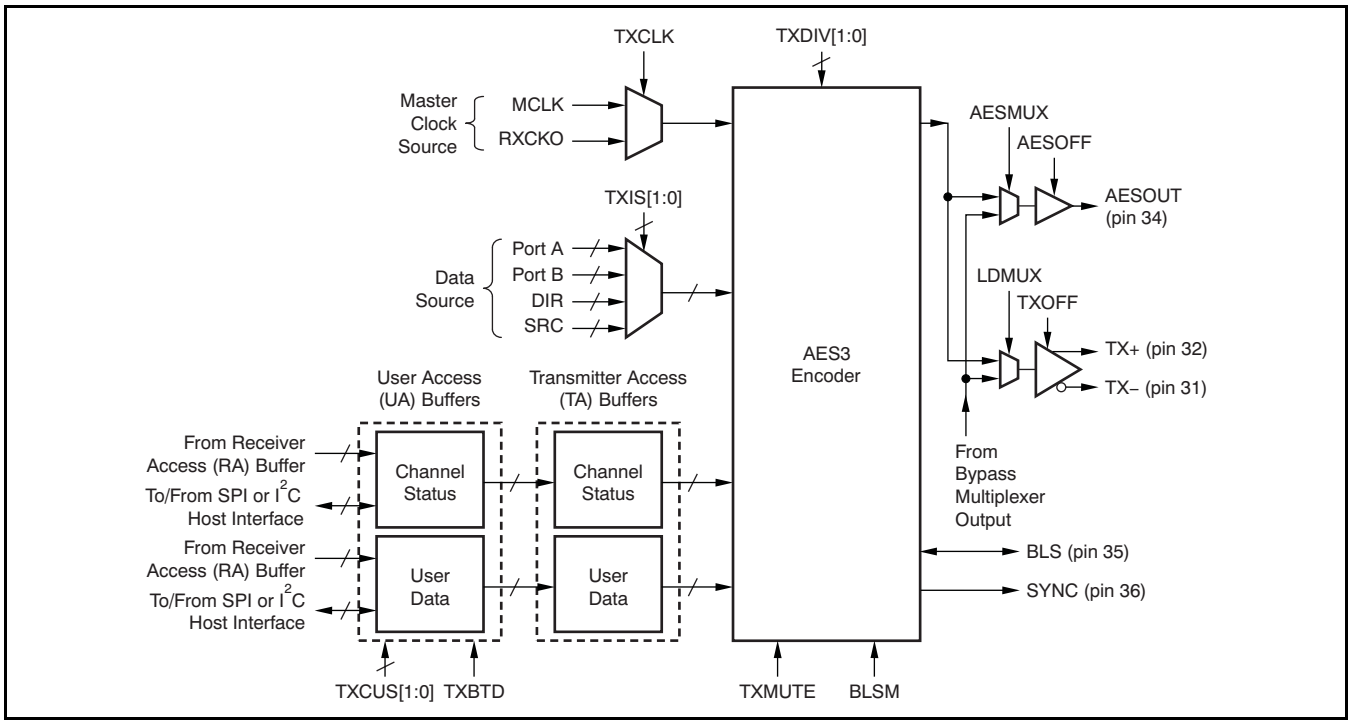

Figure 65. Digital Interface Transmitter (DIT) Functional Block Diagram

The AES3 encoder includes a block start input/output pin, BLS (pin 35). The BLS pin may be programmed as an input or output. The input/output state of the BLS pin is programmed using the BLSM bit in control register 0x07. By default, the BLS pin is configured as an input.

As an input, the BLS pin may be utilized to force a block start condition, whereby the start of a new block of channel status and user data is initiated by generating a Z preamble for the next frame of data. The BLS input must be synchronized with the DIT internal SYNC clock. This clock is output on SYNC (pin 36). The SYNC clock rising edge is aligned with the start of each frame for the AES3-encoded data output by the DIT. Figure 66 illustrates the format required for an external block start signal, as well as indicating the format when the BLS pin is configured as an output. When the BLS pin is an output, the DIT generates the block start signal based upon the internal SYNC clock.

For details regarding DIT control and status registers, as well as channel status and user data buffers, refer to the Control Registers and Channel Status and User Data Buffer Maps sections.

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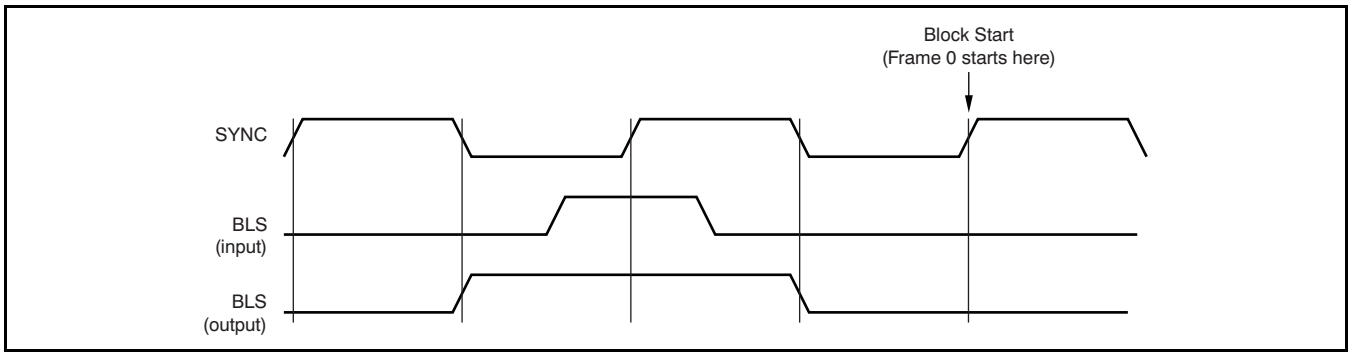

Figure 66. DIT Block Start Timing

DIGITAL INTERFACE RECEIVER (DIR) OPERATION

The DIR performs AES3 decoding and clock recovery and provides the differential line receiver functions. The lock range of the DIR includes frame/sampling rates from 20kHz to 216kHz. Figure 67 shows the functional block diagram for the DIR.

Four differential line receivers are utilized for signal conditioning the encoded input data streams. The receivers can be externally configured for either balanced or unbalanced cable interfaces, as well as interfacing with CMOS logic level inputs from optical receivers or external logic circuitry. See Figure 68 for a simplified schematic for the line receiver. External connections are discussed in the Receiver Input Interfacing section.

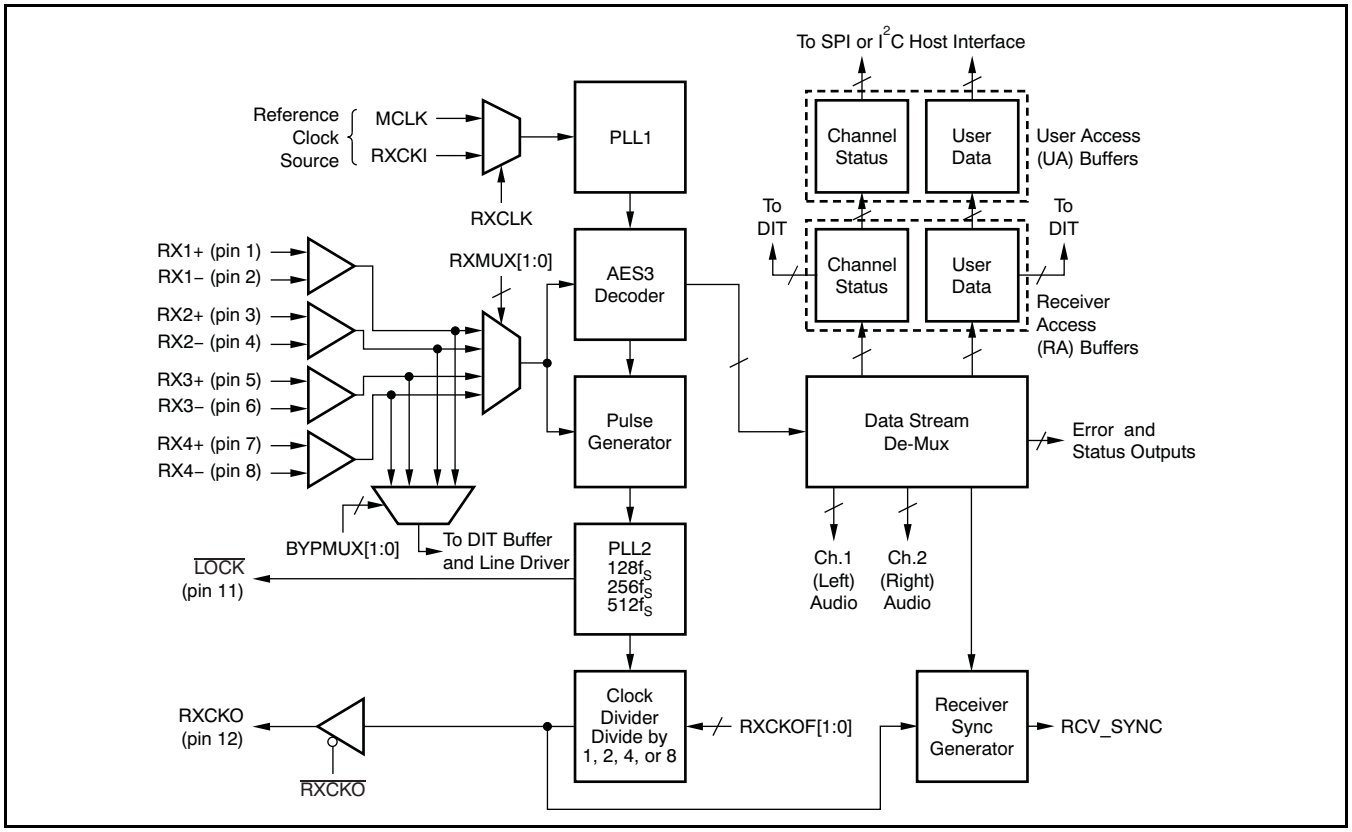

Figure 67. Digital Interface Receiver (DIR) Functional Block Diagram

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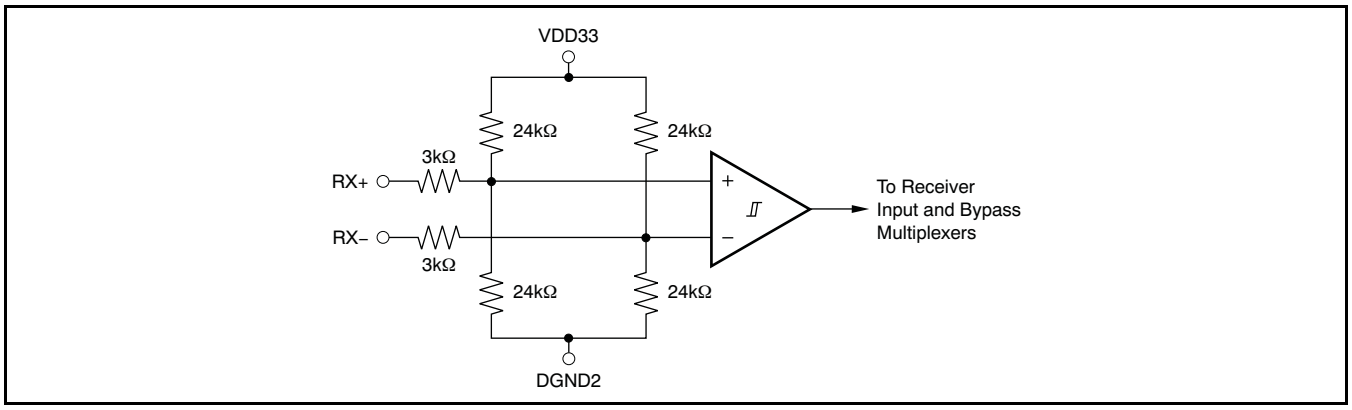

Figure 68. Differential Line Receiver Circuit

The outputs of the four line receivers are connected to two 1-of-4 data selectors: the receiver input multiplexer and the bypass multiplexer. The input multiplexer selects one of the four line receiver outputs as the source for the AES3-encoded data stream to be processed by the DIR core. The bypass multiplexer is utilized to route a line receiver output to either the DIT line driver or CMOS buffered outputs, thereby bypassing all other internal circuitry. The bypass function is useful for simple signal distribution and routing applications.

The DIR requires a reference clock, supplied by an external source applied at either the RXCKI (pin 13) or MCLK (pin 25) clock inputs. PLL1 multiplies the reference clock to a higher rate, which is utilized as the oversampling clock for the AES3 decoder. The decoder samples the AES3-encoded input stream in order to extract all of the audio and status data. The decoded data stream is sent on to a de-multiplexer, where audio and status data are separated for further processing and buffering. The pulse generator circuitry samples the encoded input data stream and generates a clock that is 16 times the frame/sampling rate (or f_S). The $16f_S$ clock is then processed by PLL2, which further multiplies the clock rate and provides low-pass filtering for jitter attenuation. The available PLL2 output clock rates include $512f_S$, $256f_S$, and $128f_S$. The maximum available PLL2 output clock rate for a given input sampling rate is estimated by internal logic and made available for readback via status register 0x13.

The output of PLL2 may be divided by a factor of two, four, or eight, or simply passed through to the recovered master clock output, RXCKO (pin 12). The RXCKO clock is also be routed internally to other function blocks, where it may be further divided to create left/right word and bit clocks. The RXCKO output may be disabled and forced to a high-impedance state by means of a control register bit, allowing other tri-state buffered clocks to be tied to the same external circuit node, if needed. By default, the RXCKO output (pin 12) is disabled and forced to a high-impedance state.

Figure 69 illustrates the frequency response of PLL2. Jitter attenuation starts at approximately 50kHz. Peaking is nominally 1dB, which is within the 2dB maximum allowed by the AES3 standard. The receiver jitter tolerance plot for the DIR is illustrated in Figure 70, along with the required AES3 jitter tolerance template. The DIR jitter tolerance satisfies the AES3 requirements, as well as the requirements set forth by the IEC60958-3 specification. Figure 70 was captured using a full-scale 24-bit, two-channel, AES3-encoded input stream with a 48kHz frame rate.

The decoded audio data, along with the internally-generated sync clocks, may be routed to other function blocks, including Port A, Port B, the SRC, and/or the DIT. The decoded channel status and user data is buffered in the corresponding Receiver Access (RA) data buffers, then transferred to the corresponding User Access (UA) data buffers, where it may be read back through either the SPI or I^2C serial host interface. The contents of the RA buffers may also be transferred to the DIT UA data buffers; see Figure 65. The channel status and user data bits may also be output serially through the general-purpose output pins, GPO[4:1]. Figure 71 illustrates the output format for the GPO pins when used for this purpose, along with the DIR block start (BLS) and frame synchronization (SYNC) clocks. The rising edges of the DIR SYNC clock output are aligned with the start of each frame for the received AES3 data.

The DIR includes a dedicated, active low AES3 decoder and PLL2 lock output, named $\overline{\text{LOCK}}$ (pin 11). The lock output is active only when both the AES3 decoder and PLL2 indicate a lock condition. Additional DIR status flags may be output at the general-purpose output (GPO) pins, or accessed through the status registers via the SPI or I^2C host interface. Refer to the General-Purpose Digital Outputs and Control Registers sections for additional information regarding the DIR status functions.

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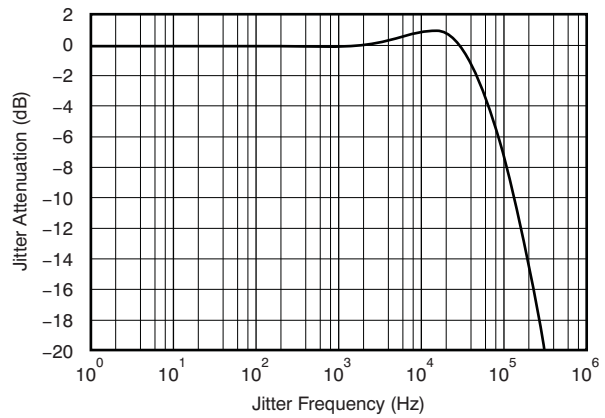

Figure 69. DIR Jitter Attenuation Characteristics

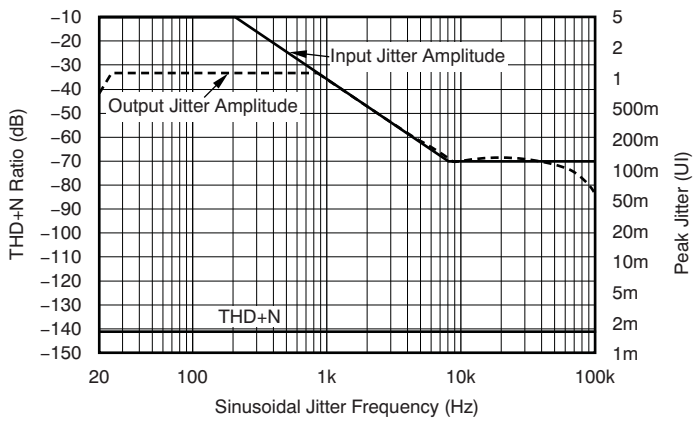

Figure 70. DIR Jitter Tolerance Plot

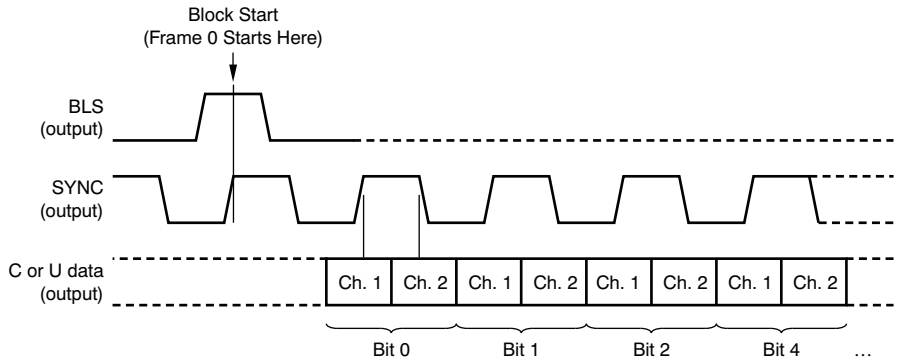

Figure 71. DIR Channel Status and User Data Serial Output Format Via the GPO Pins

ASYNCHRONOUS SAMPLE RATE CONVERTER (SRC) OPERATION

The asynchronous SRC provides conversion from an arbitrary input sampling rate to a desired output sampling rate. The input and output sampling rates may be equal or different, within the bounds of a 1:16 to 16:1

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input-to-output sampling ratio range. The input and output data sources may be completely asynchronous to one another; synchronous operation is also supported. The input-to-output sampling ratio is determined automatically using internal rate estimation logic, with the re-sampler being updated in real time without the need for programming. The SRC supports input and output sampling rates up to 216kHz, with audio data word lengths up to 24 bits. A functional block diagram for the SRC is shown in Figure 72.

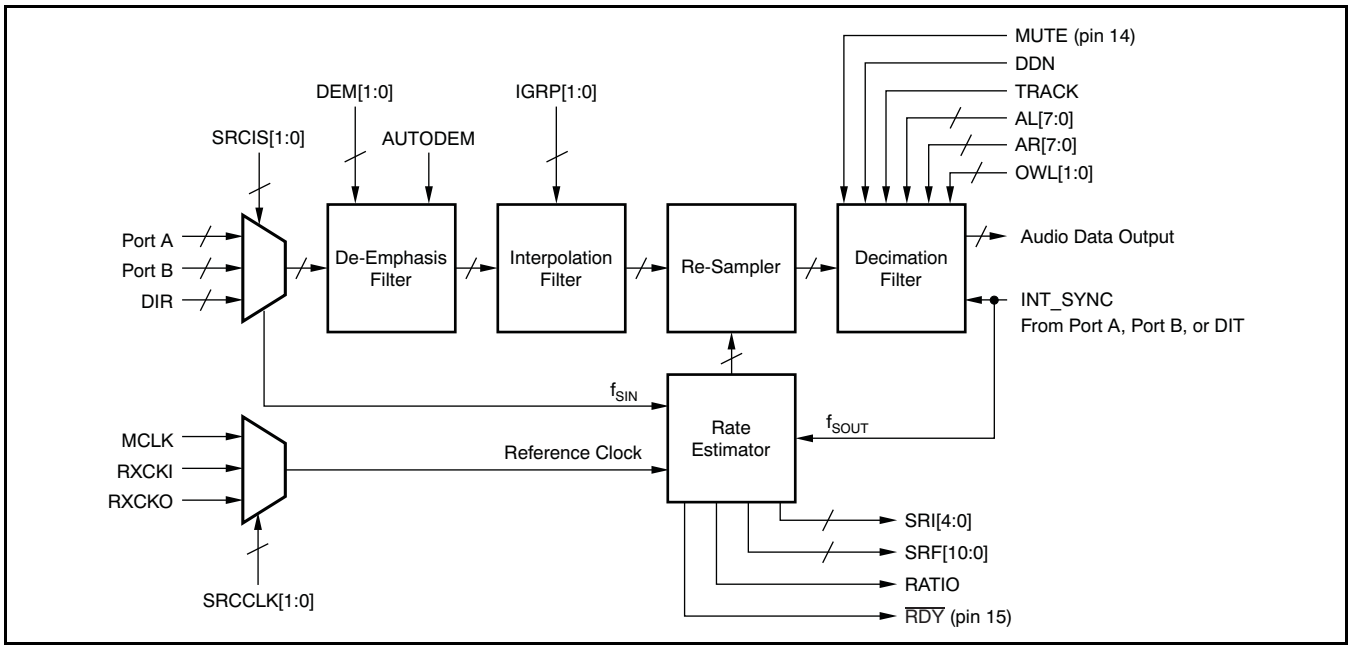

Figure 72. Asynchronous Sample Rate Converter (SRC) Functional Block Diagram

The SRC receives a digital audio input from one of three data sources: Port A, Port B, or the DIR. By default, Port A is selected as the input source for the SRC. The output of the SRC may be connected to Port A, Port B, and/or the DIT.

The SRC requires a reference clock, which may be sourced from either the MCLK (pin 25) or RXCKI (pin 13) clock inputs, or from the RXCKO recovered master clock output from the DIR block. The reference clock is utilized by the rate estimator to determine the input-to-output sampling ratio. By default, MCLK is selected as the reference clock source for the SRC.

As part of the SRC rate estimation and re-sampling functions, two digital servo loops are employed, one for the input side and one for the output side. The servo loops operate in two modes: Fast and Slow. When a change in one or both of the sampling rates occurs, the servo loop(s) enter(s) Fast mode operation. When a servo loop has settled in Fast mode, it will then switch to Slow mode. When both the input and output servo loops have switched to Slow mode, the $\overline{RDY}$ output (pin 15) is forced low, indicating that the SRC has completed the rate estimation process.

The input and output servo-loop frequency responses are shown in Figure 73 and Figure 74, respectively. The filter response for each servo loop rolls off at 80dB per decade. The servo loop corner frequencies scale proportionally with input or output sampling rates. The low corner frequency and sharp roll-off provide excellent jitter attenuation for the SRC block.

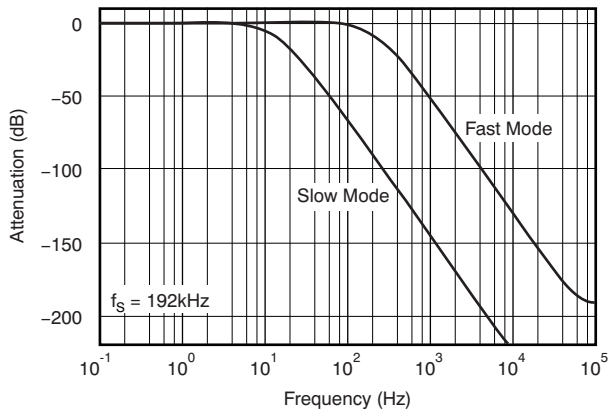

Figure 73. Input Digital Servo-Loop Frequency Response

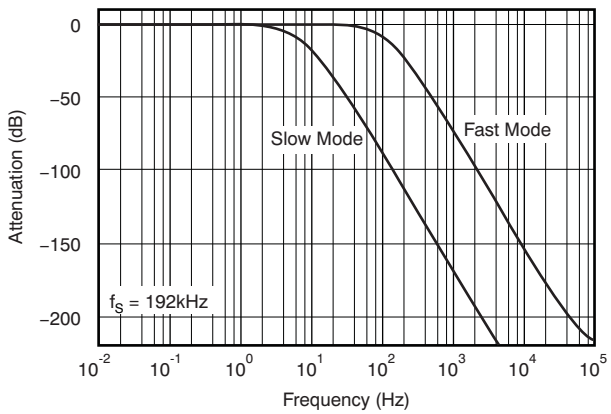

Figure 74. Output Digital Servo-Loop Frequency Response

The SRC includes output soft muting and digital attenuation functions, providing artifact-free muting and output level control for the SRC output data. The mute function forces the SRC output data low by stepping the output attenuation from the current setting to an all-zero data output state. The mute function may be controlled by the MUTE input (pin 14), or the MUTE bit in control register 0x2D. Both the pin and control bit are active high, with the signals being combined by a logic OR function internally to generate the SRC output mute control signal. The MUTE control bit in control register 0x2D is disabled by default.

The digital attenuation is programmable over a 0dB to –127.5dB range in 0.5dB steps, and may be controlled independently for the Left and Right channels. The attenuation level is set using control registers; by default, the level is 0dB. A tracking function is available, allowing the Left and Right channel attenuation data to be set to the same value by simply programming the Left channel attenuation register. The tracking mode is enabled or disabled using a control register bit. The tracking function is disabled by default.

The SRC includes digital de-emphasis filtering for the audio input data. The de-emphasis filter provides normalization for 50/15µs pre-emphasized audio data. The de-emphasis filter supports 32kHz, 44.1kHz, and 48kHz input sampling rates. The filter is controlled by the DEM0, DEM1, and AUTODEM bits in control register 0x2E. The DEM0 and DEM1 bits allow the user to manually configure the de-emphasis filter operation. By default, the de-emphasis filtering is disabled. The AUTODEM bit, when enabled, overrides the setting of the

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DEM0 and DEM1 bits. The AUTODEM function automatically enables and disables the de-emphasis filter for the required sampling rate based upon the setting of the pre-emphasis and sampling frequency channel status bits in the AES3 or S/PDIF input data stream, which are decoded by the DIR block. The AUTODEM feature functions only when both 50/15µs pre-emphasis and one of the three supported sampling rates (32kHz, 44.1kHz, or 48kHz) are decoded by the DIR. By default, the de-emphasis filter, including the AUTODEM function, is disabled.

The group delay of the SRC interpolation function can be programmed to one of four settings. The actual length of the interpolation filter is unaltered, but the number of samples pre-buffered in the FIFO prior to the re-sampler function can be set to 64, 32, 16, or 8. The FIFO length directly impacts the latency and group delay. By default, the number of samples pre-buffered is set to 64.

The decimation filter includes a direct down-sampling option. This option should only be used in cases where the output sampling rate is higher than the input sampling rate. The advantage of using the direct down-sampling option is that it results in zero latency operation, as it simply selects one out of every 16 samples from the re-sampler output without applying low-pass anti-aliasing filtering. By contrast, the decimation filter response adds 36.46875 samples of group delay. The disadvantage of the direct down-sampling option is that it cannot be used in cases where the output sampling rate is equal to or lower than the input sampling rate, since the lack of low-pass filtering results in aliasing. By default, the decimation filter is enabled, as the initial values of the input and output sampling rates may be unknown.

The SRC includes two status registers that contain the integer and fractional parts of the input-to-output sampling ratio, which is derived by the SRC rate estimator circuitry. These registers can be read back any time the $\overline{\text{RDY}}$ output is low. When either the input or output sampling rate is known, the unknown sampling rate can be calculated using the contents of these status registers.

The SRC provides a simple word length reduction mechanism for reducing 24-bit audio data to 20-, 18-, or 16-bit output word lengths. Word length reduction is performed utilizing triangular probability density function (or TPDF) dither. The OWL0 and OWL1 bits in control register 0x2F are utilized to set the SRC output word length.

One note concerning the SRC output word length setting: when using the SRC output as the data source for either the Port A or Port B serial data outputs, and the audio serial port data format is set to Right-Justified, the word length set for the audio serial port format must match the word length set for the SRC output data.

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GENERAL-PURPOSE DIGITAL OUTPUTS

The SRC4382 includes four general-purpose digital outputs, GPO1 through GPO4 (pins 26 through 29, respectively). A GPO pin may be programmed to a static high or low state. Alternatively, a GPO pin may be connected to one of 14 internal logic nodes, allowing the GPO pin to inherit the function of the selected signal. Control registers 0x1B through 0x1E are utilized to select the function of the GPO pins. For details regarding GPO output configuration, refer to the Control Registers section. Table 1 summarizes the available output options for the GPO pins.

Table 1. General-Purpose Output Pin Configurations

GPOn3	GPOn2	GPOn1	GPOn0	GPOn FUNCTION
0	0	0	0	GPOn is forced Low (default).
0	0	0	1	GPOn is forced High.
0	0	1	0	SRC Interrupt Flag; Active Low
0	0	1	1	DIT Interrupt Flag; Active Low
0	1	0	0	DIR Interrupt Flag; Active Low
0	1	0	1	DIR 50/15µs Emphasis Flag; Active Low
0	1	1	0	DIR Non-Audio Data Flag; Active High
0	1	1	1	DIR Non-Valid Data Flag; Active High
1	0	0	0	DIR Channel Status Data Serial Output
1	0	0	1	DIR User Data Serial Output
1	0	1	0	DIR Block Start Clock Output
1	0	1	1	DIR COPY Bit Output (0 = Copyright Asserted, 1 = Copyright Not Asserted)
1	1	0	0	DIR L (or Origination) Bit Output (0 = 1st Generation or Higher,1 = Original)
1	1	0	1	DIR Parity Error Flag; Active High
1	1	1	0	DIR Internal Sync Clock Output; may be used as the data clock for the Channel Status and User Data serial outputs.
1	1	1	1	DIT Internal Sync Clock

HOST INTERFACE OPERATION: SERIAL PERIPHERAL INTERFACE (SPI) MODE

The SRC4382 supports a 4-wire SPI port when the CPM input (pin 18) is forced low or tied to ground. The SPI port supports high-speed serial data transfers up to 40Mbps. Register and data buffer write and read operations are supported.

The $\overline{CS}$ input (pin 19) serves as the active low chip select for the SPI port. The $\overline{CS}$ input must be forced low in order to write or read registers and data buffers. When $\overline{CS}$ is forced high, the data at the CDIN input (pin 21) is ignored, and the CDOUT output (pin 22) is forced to a high-impedance state. The CDIN input serves as the serial data input for the port; the CDOUT output serves as the serial data output.

The CCLK input (pin 20) serves as the serial data clock for both the input and output data. Data is latched at the CDIN input on the rising edge of CCLK, while data is clocked out of the CDOUT output on the falling edge of CCLK.

Figure 75 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit (or MSB) is the read/write bit. For the R/W bit, a '0' indicates a write operation, while a '1' indicates a read operation. The remaining seven bits of the command byte are utilized for the register address targeted by the write or read operation. Byte 1 is a *don't care* byte, and may be set to all zeroes. This byte is included in order to retain protocol compatibility with earlier Texas Instruments digital audio interface and sample rate converter products, including the DIT4096, DIT4192, the SRC418x series devices, and the SRC419x series devices.

The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in Figure 75, the auto-increment mode is invoked by simply holding the $\overline{CS}$ input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte.

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Refer to the Electrical Characteristics: *SPI Interface* table and Figure 2 for specifications and a timing diagram that highlight the key parameters for SPI interface operation.

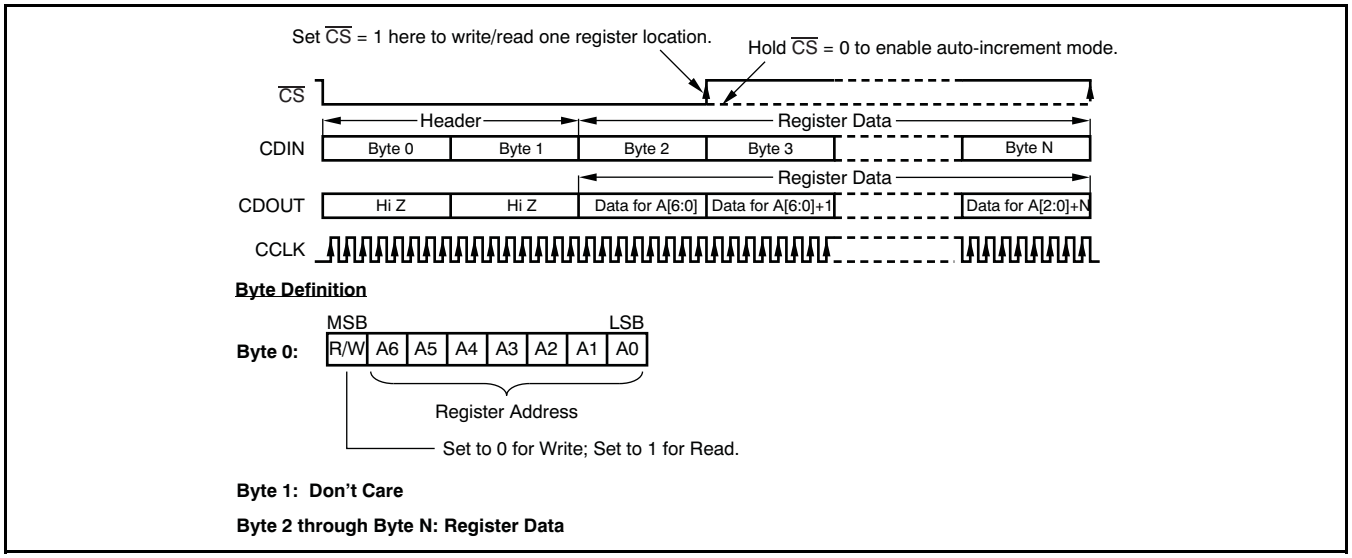

Figure 75. Serial Peripheral Interface (SPI) Protocol for the SRC4382

HOST INTERFACE OPERATION: PHILIPS I²C MODE

The SRC4382 supports a 2-wire Philips I²C bus interface when CPM (pin 18) is forced high or pulled up to the VIO supply rail. The SRC4382 functions as a Slave-only device on the bus. Standard and Fast modes of operation are supported. Standard mode supports data rates up to 100kbps, while Fast mode supports data rates up to 400kbps. Fast mode is downward compatible with Standard mode, and these modes are sometimes referred to as Fast/Standard, or F/S mode. The I²C Bus Specification (Version 2.1, January 2000), available from Philips Semiconductor, provides the details for the bus protocol and implementation. It is assumed that the reader is familiar with this specification. Refer to the Electrical Characteristics: *I²C Standard and Fast Modes* table and Figure 3 for specifications and a timing diagram that highlight the key parameters for I²C interface operation.

When the I²C mode is invoked, pin 20 becomes SCL (which serves as the bus clock) and pin 22 becomes SDA (which carries the bi-directional serial data for the bus). Pins 19 and 21 become A0 and A1, respectively, and function as the hardware configurable portion of the 7-bit slave address.

The SRC4382 utilizes a 7-bit Slave address, see Figure 76(a). Bits A2 through A6 are fixed and bits A0 and A1 are hardware programmable using pins 19 and 21, respectively. The programmable bits allow for up to four SRC4382 devices to be connected to the same bus. The slave address is followed by the Register Address Byte, which points to a specific register or data buffer location in the SRC4382 register map. The register address byte is comprised of seven bits for the address, and one bit for enabling or disabling auto-increment operation, see Figure 76(b). Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations.

Figure 77 illustrates the protocol for Standard and Fast mode Write operations. When writing a single register address, or multiple non-sequential register addresses, the single register write operation of Figure 77(a) may be used one or more times. When writing multiple sequential register addresses, the auto-increment mode of Figure 77(b) improves efficiency. The register address is automatically incremented by one for each successive byte of data transferred.

Figure 78 illustrates the protocol for Standard and Fast mode Read operations. The current address read operation of Figure 78(a) assumes the value of the register address from the previously executed write or read operation, and is useful for polling a register address for status changes. Figure 78(b) and Figure 78(c) illustrate read operations for one or more random register addresses, with or without auto-increment mode enabled.

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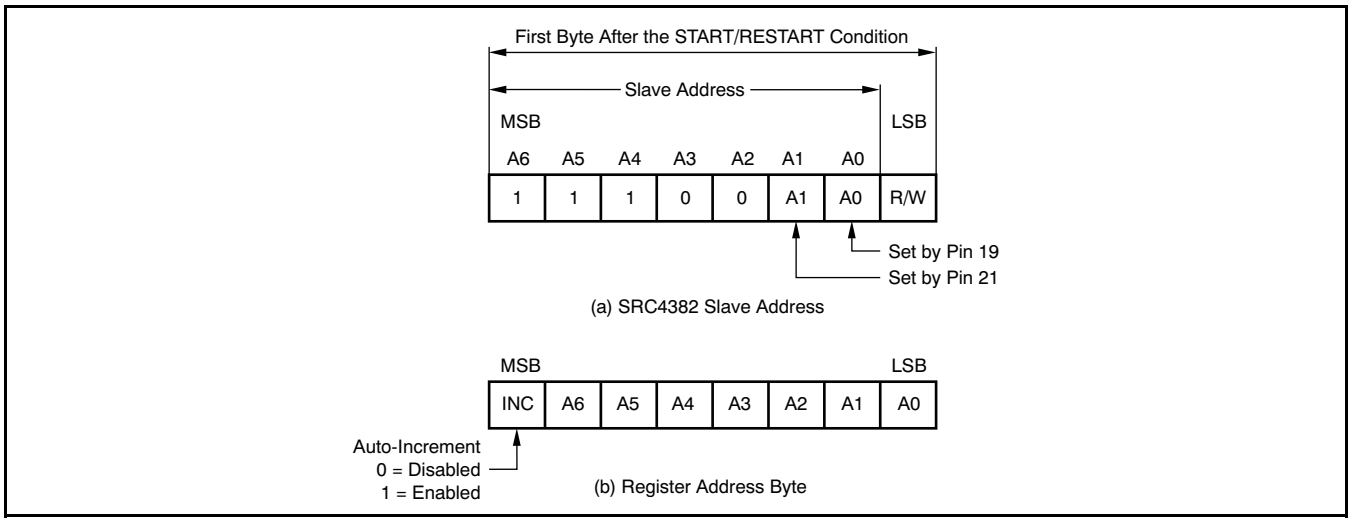

Figure 76. SRC4382 Slave Address and Register Address Byte Definitions

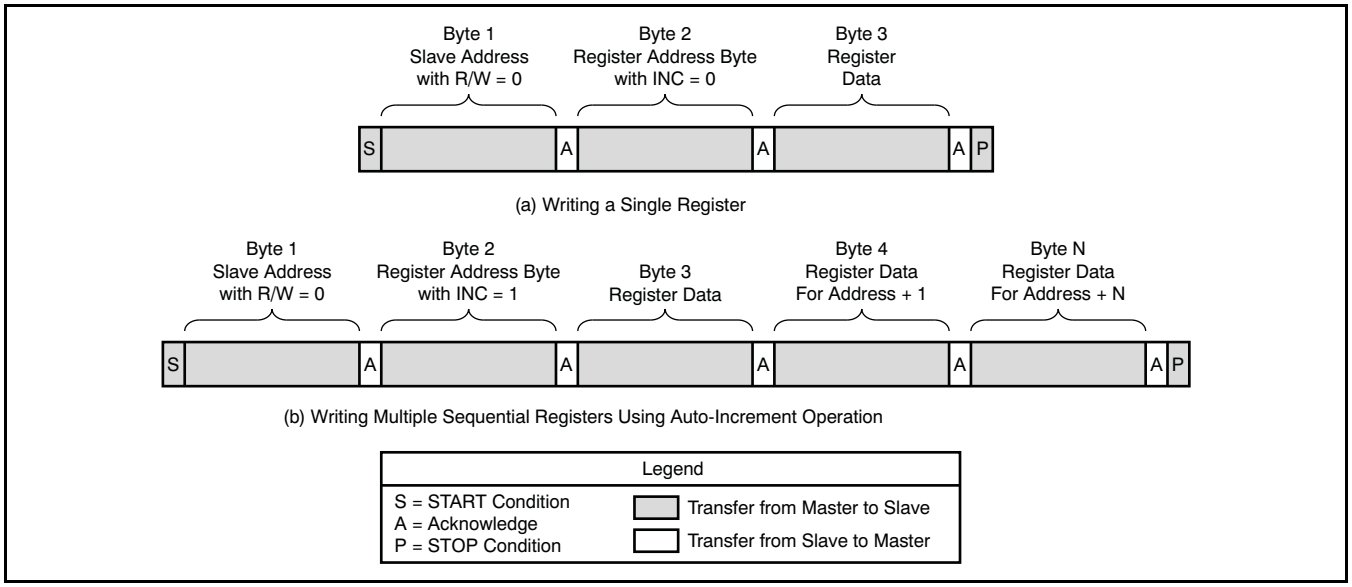

Figure 77. Fast/Standard Mode Write Operations

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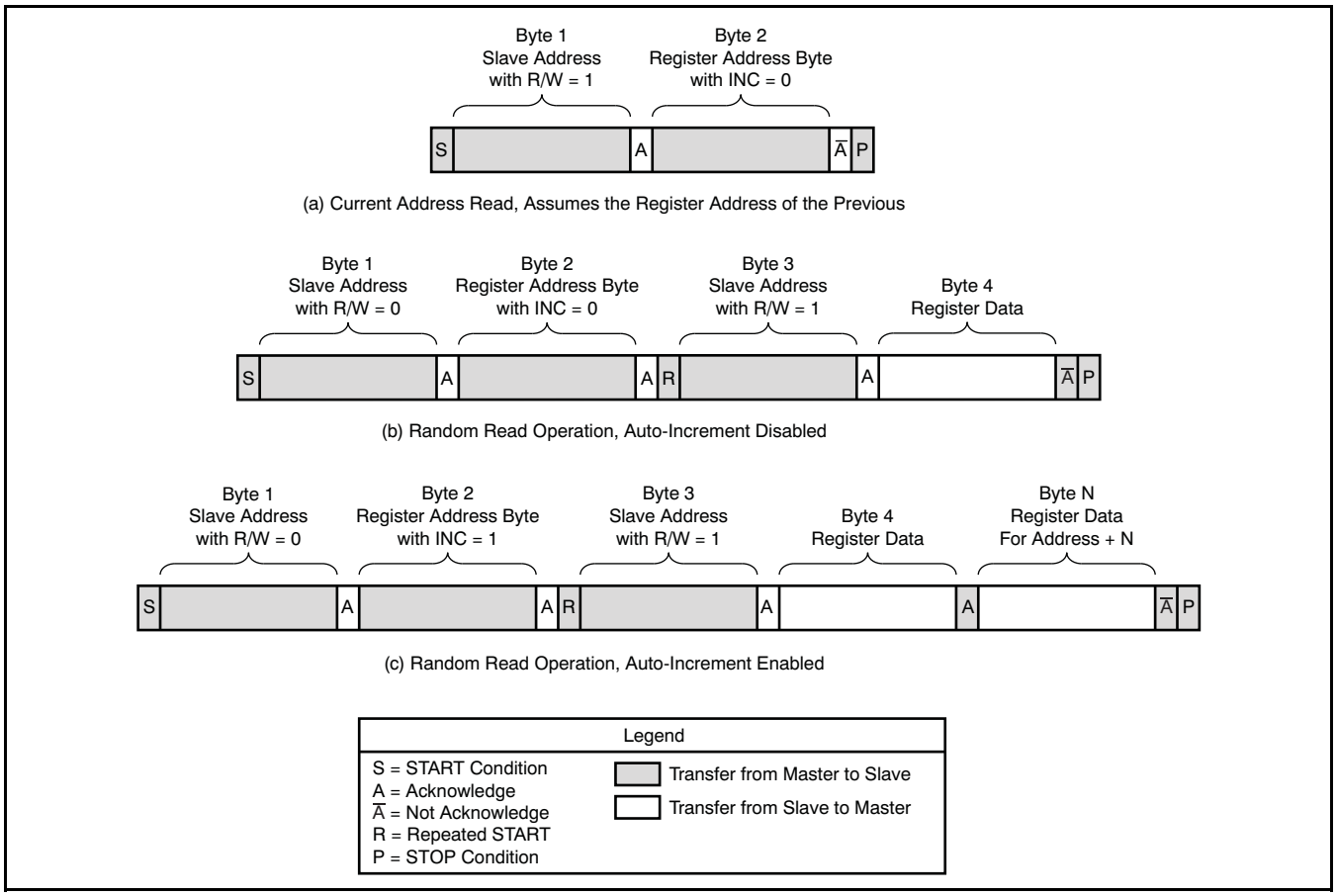

Figure 78. Fast/Standard Mode Read Operations

INTERRUPT OUTPUT

The SRC4382 includes multiple internal status bits, many of which may be set to trigger an interrupt signal. The interrupt signal is output at $\overline{INT}$ (pin 23), which is an active low, open-drain output. The $\overline{INT}$ pin requires a pull-up resistor to the VIO supply rail. The value of the pull-up is not critical, but a 10kΩ device should be sufficient for most applications. Figure 79 shows the interrupt output pin connection. The open-drain output allows interrupt pins from multiple SRC4382 devices to be connected in a wired OR configuration.

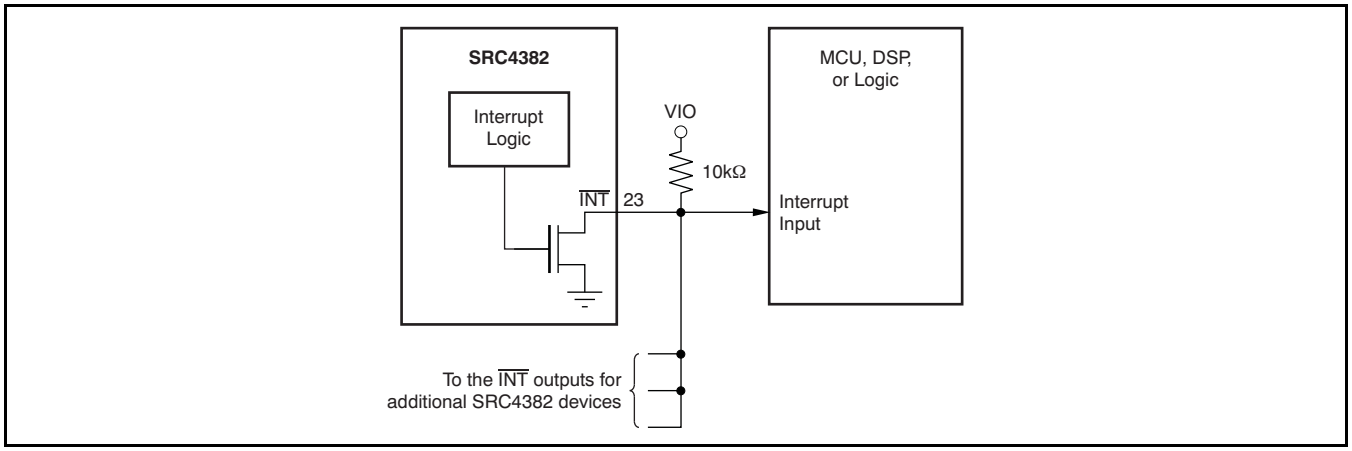

Figure 79. Interrupt Output Pin Connections

APPLICATIONS INFORMATION

Typical application diagrams and power-supply connections are presented in this section to aid the customer in hardware designs employing the SRC4382 device.

Figure 80 illustrates typical application connections for the SRC4382 using an SPI host interface. The SPI host will typically be a microcontroller, digital signal processor, or a programmable logic device. In addition to providing the SPI bus master, the host may be utilized to process interrupt and flag outputs from the SRC4382. The audio serial ports are connected to external digital audio devices, which may include data converters, digital signal processors, digital audio interface receivers/transmitters, or other logic devices. The DIR inputs and DIT outputs are connected to line, optical, or logic interfaces (see the Receiver Input Interfacing and Transmitter Output Interfacing sections). Master and DIR reference clock sources are also shown.

Figure 81 illustrates typical application connections for the SRC4382 using an I^2C bus interface. The I^2C bus master will typically be a microcontroller, digital signal processor, or a programmable logic device. In addition to providing the I^2C bus master, the host may be used to process interrupt and flag outputs from the SRC4382. Pull-up resistors are connected from SCL (pin 20) and SDA (pin 22) to the VIO supply rail. These pull-up resistors are required for the open drain outputs of the I^2C interface. All other connections to the SRC4382 are the same as the SPI host case discussed previously.

Figure 82 illustrates the recommended power-supply connections and bypassing for the SRC4382. In this case, it is assumed that the VIO, VDD33, and VCC supplies are powered from the same +3.3V power source. The VDD18 core supply is powered from a separate supply, or derived from the +3.3V supply using a linear voltage regulator, as illustrated with the optional regulator circuitry of Figure 82.

The 0.1µF bypass capacitors are surface-mount X7R ceramic, and should be located as close to the device as possible. These capacitors should be connected directly between the supply and corresponding ground pins of the SRC4382. The ground pin is then connected directly to the ground plane of the printed circuit board (PCB). The larger value capacitors, shown connected in parallel to the 0.1µF capacitors, are recommended. At a minimum, there should at least be footprints on the PCB for installation of these larger capacitors, so that experiments can be run with and without the capacitors installed, in order to determine the effect on the measured performance of the SRC4382. The larger value capacitors can be surface-mount X7R multilayer ceramic or tantalum chip.

The substrate ground, BGND (pin 44), should be connected by a PCB trace to AGND (pin 10). The AGND pin is then connected directly to the ground plane. This connection helps to reduce noise in the DIR section of the device, aiding the overall jitter and noise tolerance for the receiver.

A series resistor is shown between the +3.3V supply and VCC (pin 9) connection. This resistor combines with the bypass capacitors to create a simple RC filter to remove higher frequency components from the VCC supply. The series resistor should be a metal film type for best filtering characteristics. As a substitute for the resistor, a ferrite bead can be utilized, although it may have to be physically large in order to contribute to the filtering.

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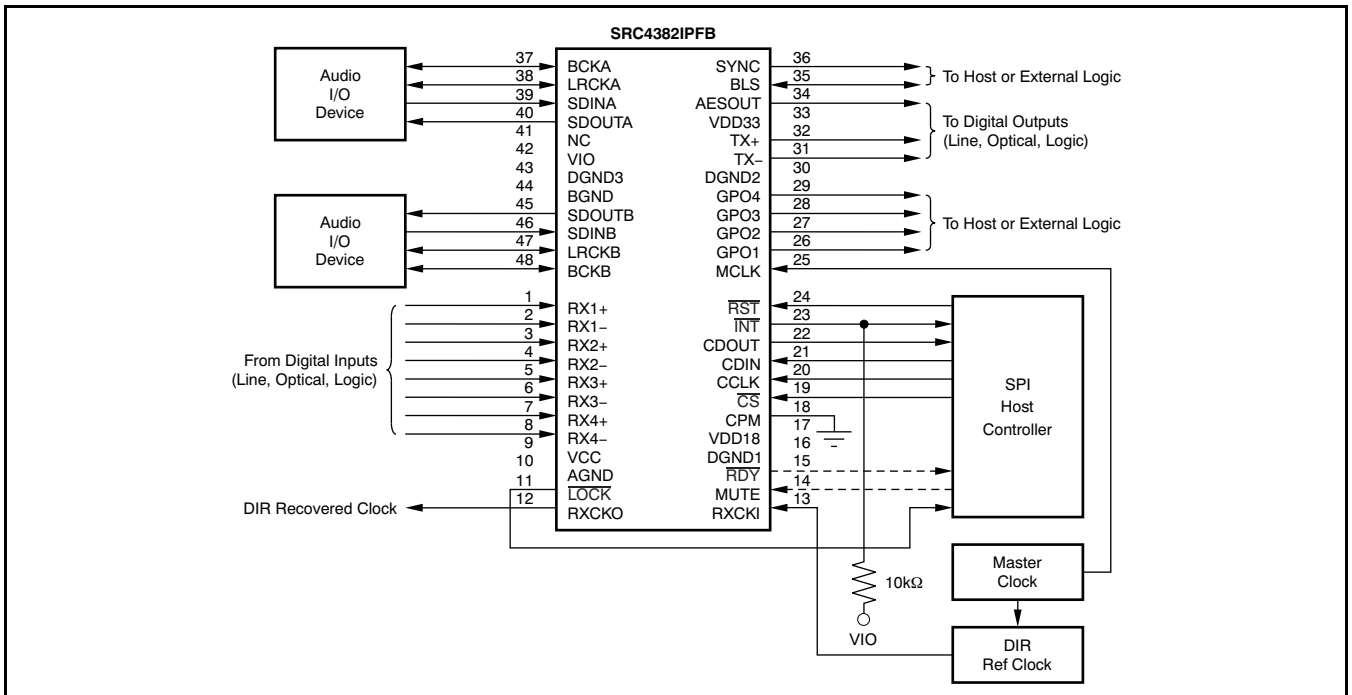

Figure 80. Typical Application Diagram Using SPI Host Interface

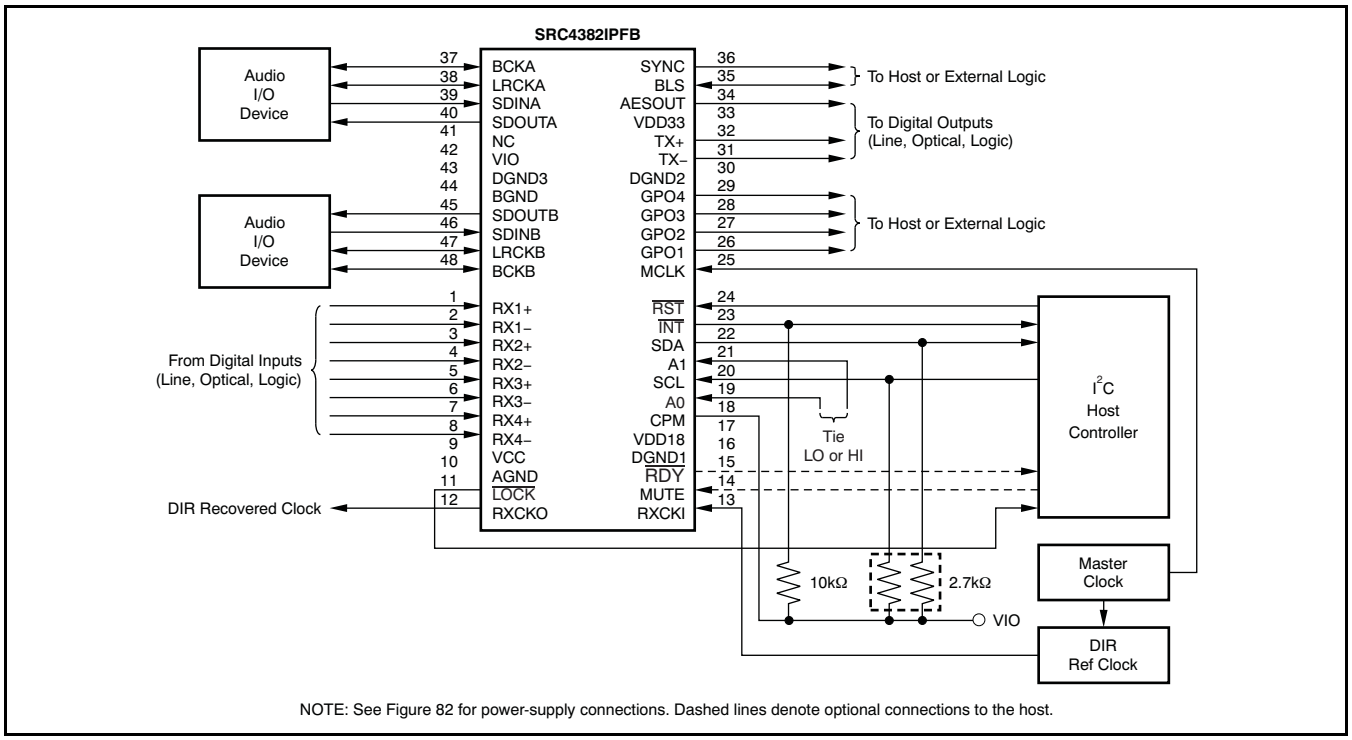

Figure 81. Typical Application Diagram Using I^2C Host Interface

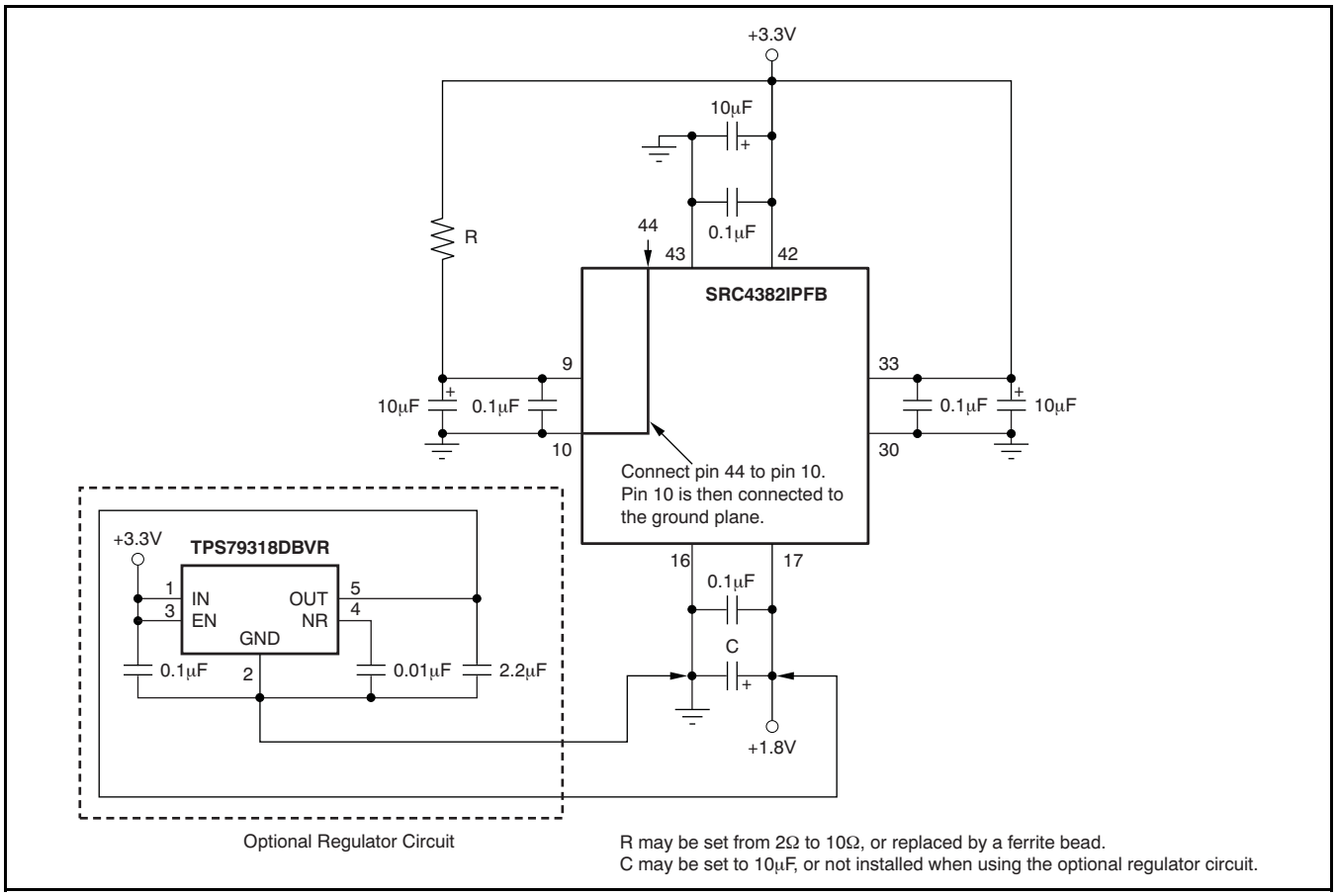

Figure 82. Recommended Power-Supply Connections

DIGITAL AUDIO TRANSFORMER VENDORS

Transformers are shown in this data sheet for both receiver and transmitter balanced and unbalanced line interface implementations. For the Texas Instruments Pro Audio evaluation modules, transformers from Scientific Conversion are utilized. In addition to Scientific Conversion, there are other vendors that offer transformer products for digital audio interface applications. Please refer to the following manufacturer web sites for details regarding their products and services. Other transformer vendors may also be available by searching catalog and/or Internet resources.

- Scientific Conversion: http://scientificconversion.com
- Schott Corporation: http://schottcorp.com
- Pulse Engineering: http://pulseeng.com

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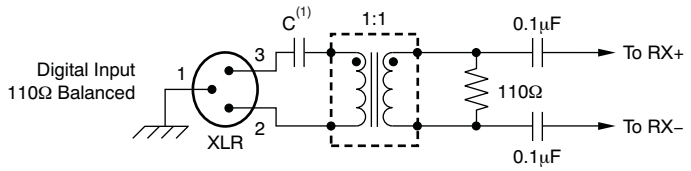
RECEIVER INPUT INTERFACING

This section details the recommended interfaces for the SRC4382 line receiver inputs. Balanced and unbalanced line interfaces, in addition to optical receiver and external logic interfacing, will be discussed.

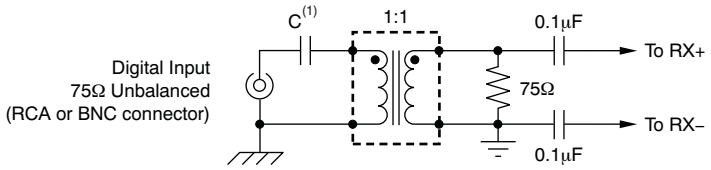
For professional digital audio interfaces, 110Ω balanced line interfaces are either required or preferred. Transformer coupling is commonly employed to provide isolation and to improve common-mode noise rejection. Figure 83 shows the recommended transformer-coupled balanced line receiver interface for the SRC4382. The transformer is specified for a 1:1 turn ratio, and should exhibit low inter-winding capacitance for best performance. Due to the DC bias on the line receiver inputs, 0.1µF capacitors are utilized for AC-coupling the transformer to the line receiver inputs. On the line side of the transformer, an optional 0.1µF capacitor is shown for cases where a DC bias may be applied at the transmitter side of the connection. The coupling capacitors should be surface-mount ceramic chip type with an X7R or C0G dielectric.



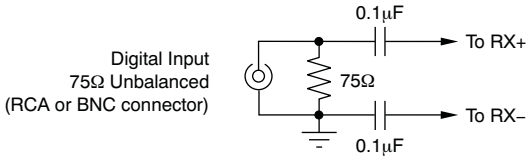
(1) Insert a 0.1µF capacitor when blocking common-mode DC voltage.

Figure 83. Transformer-Coupled Balanced Input Interface

Unbalanced 75Ω coaxial cable interfaces are commonly employed in consumer and broadcast audio applications. Designs with and without transformer line coupling may be utilized. Figure 84(a) shows the recommended 75Ω transformer-coupled line interface, which shares many similarities to the balanced design shown in Figure 83. Once again, the transformer provides isolation and improved noise rejection. Figure 84(b) shows the transformer-free interface, which is commonly used for S/PDIF consumer connections.



(a) Transformer-Coupled Unbalanced Line Interface

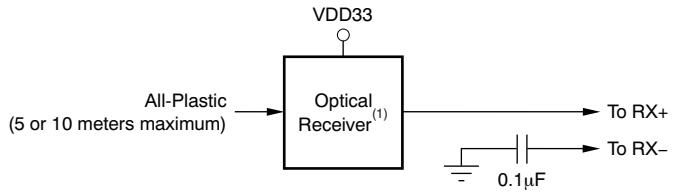


(b) Unbalanced Line Interface Without Transformer

(1) Insert a 0.1µF capacitor when blocking common-mode DC components.

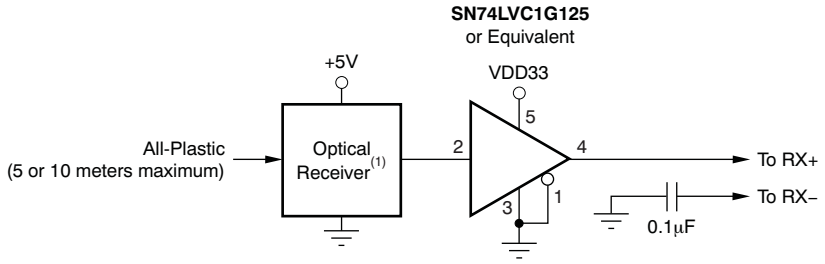
Figure 84. Unbalanced Line Input Interfaces

Optical interfaces utilizing all-plastic fiber are commonly employed for consumer audio equipment where interconnections are less than 10m in length. Optical receiver modules utilized for a digital audio interface operate from either a single +3.3V or +5V supply and have a TTL-, CMOS-, or low-voltage CMOS-compatible logic output. Interfacing to +3.3V optical receivers is straightforward when the optical receiver supply is powered from the SRC4382 VDD33 power source, as shown in Figure 85. For the +5V optical receivers, the output high logic level may exceed the SRC4382 line receiver absolute maximum input voltage. A level translator is required, placed between the optical receiver output and the SRC4382 line receiver input. Figure 86 shows the recommended input circuit when interfacing a +5V optical receiver to the SRC4382 line receiver inputs. The Texas Instruments SN74LVC1G125 single buffer IC is operated from the same +3.3V supply used for SRC4382 VDD33 supply. This buffer includes a +5V tolerant digital input, and provides the logic level translation required for the interface.



(1) Toshiba TORX141 or equivalent.

Figure 85. Interfacing to a +3.3V Optical Receiver Module



(1) Toshiba TORX173, TORX176, TORX179, or equivalent.

Figure 86. Interfacing to a +5V Optical Receiver Module

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The SRC4382 line receivers may also be driven directly from external logic or line receiver devices with TTL or CMOS outputs. If the logic driving the line receiver is operated from +3.3V, then logic level translation is not be required. However, if the external logic is operated from a power-supply voltage that exceeds the maximum VDD33 supply voltage of the SRC4382, or operates from a supply voltage lower than +3.3V, then level translation is required. Figure 87 shows the recommended logic level translation methods, utilizing buffers and level translators available from Texas Instruments.

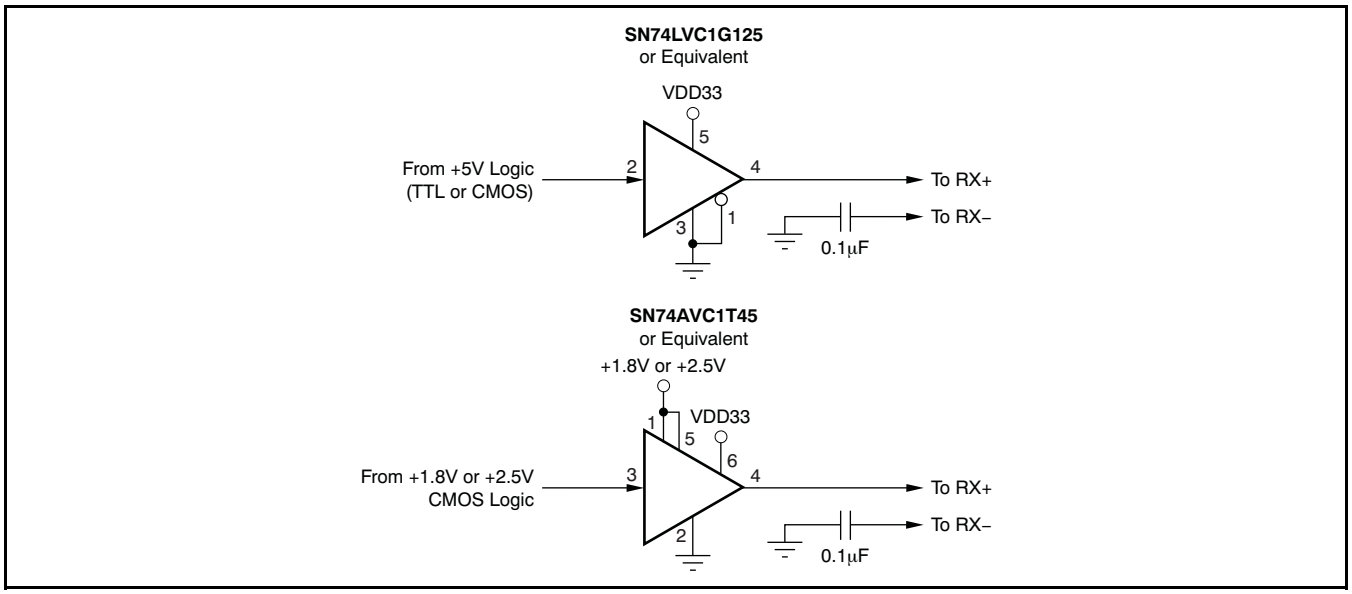

Figure 87. CMOS/TTL Input Logic Interface

TRANSMITTER OUTPUT INTERFACING

This section details the recommended interfaces for the SRC4382 transmitter line driver and CMOS buffered outputs. Balanced and unbalanced line interfaces, in addition to optical transmitter and external logic interfacing, will be discussed.

For professional digital audio interfaces, 110Ω balanced line interfaces are either required or preferred. Transformer coupling is commonly employed to provide isolation and to improve common-mode noise performance. Figure 88 shows the recommended transformer-coupled balanced line driver interface for the SRC4382. The transformer is specified for a 1:1 turn ratio, and should exhibit low inter-winding capacitance for best performance. To eliminate residual DC bias, a 0.1µF capacitor is utilized for AC-coupling the transformer to the line driver outputs. The coupling capacitor should be a surface-mount ceramic chip type with an X7R or C0G dielectric.

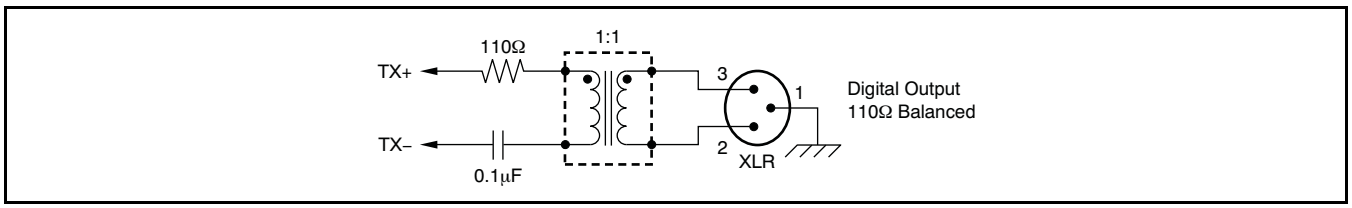

Figure 88. Transformer-Coupled Balanced Output Interface

Unbalanced 75Ω coaxial cable interfaces are commonly employed in consumer and broadcast audio applications. Designs with and without transformer line coupling may be utilized. Figure 89(a) illustrates the recommended 75Ω transformer-coupled line driver interface, which shares many similarities to the balanced design shown in Figure 88. Figure 89(b) illustrates the transformer-free line driver interface, which is commonly used for S/PDIF consumer connections.

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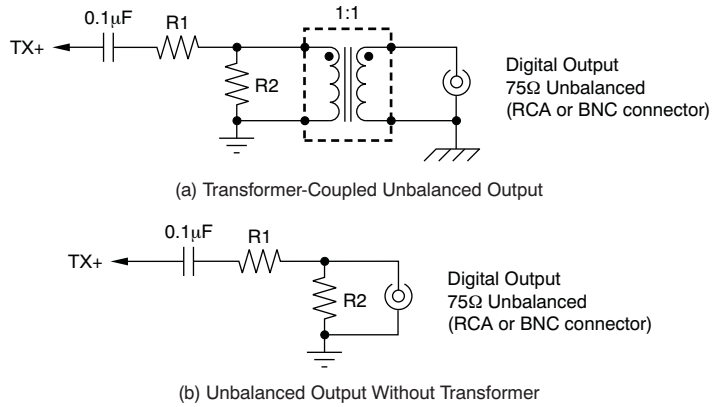
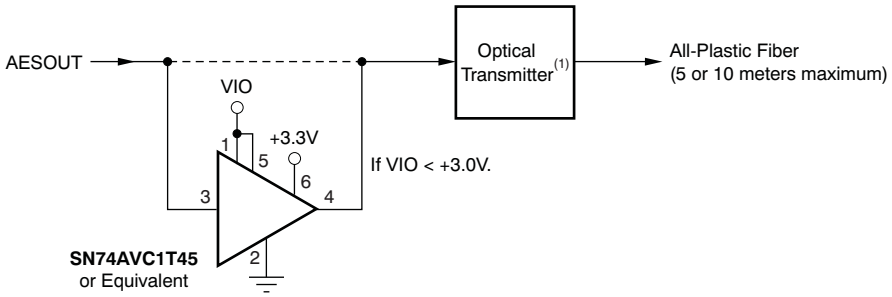


R1 and R2 are selected to achieve the desired output voltage level while maintaining the required 75Ω transmitter output impedance. The TX+ output impedance is negligible.

Figure 89. Unbalanced Line Output Interfaces

Optical interfaces utilizing all-plastic fiber are commonly employed for consumer audio equipment where interconnections are less than 10m in length. Most optical transmitter modules utilized for a digital audio interface operate from a single +3.3V or +5V supply and have a TTL-compatible logic input. The CMOS buffered transmitter output of the SRC4382, AESOUT (pin 34), is capable of driving the optical transmitter with VIO supply voltages down to +3.0V. If the VIO supply voltage is less than +3.0V, then level translation logic is required to drive the optical transmitter input. A good choice for this application is the Texas Instruments SN74AVC1T45 single bus transceiver. This device features two power-supply rails, one for the input side and one for the output side. For this application, the input side supply is powered from the VIO supply, while the output side is powered from a +3.3V supply. This will boost the logic high level to a voltage suitable for driving the TTL compatible input configuration. Figure 90 shows the recommended optical transmitter interface circuits.



(1) Toshiba TOTX141, TOTX173, TOTX176, TOTX179, or equivalent.

Figure 90. Interfacing to an Optical Transmitter Module

The AESOUT output may also be used to drive external logic or line driver devices directly. Figure 91 illustrates the recommended logic interface techniques, including connections with and without level translation. Figure 92 illustrates an external line driver interface utilizing the Texas Instruments SN75ALS191 dual differential line driver. If the VIO supply of the SRC4382 is set from +3.0V to +3.3V, no logic level translation is required between the AESOUT output and the line driver input. If the VIO supply voltage is below this range, then the optional logic level translation logic of Figure 92 is required. The SN75ALS191 dual line driver is especially useful in applications where simultaneous 75Ω and 110Ω line interfaces are required.

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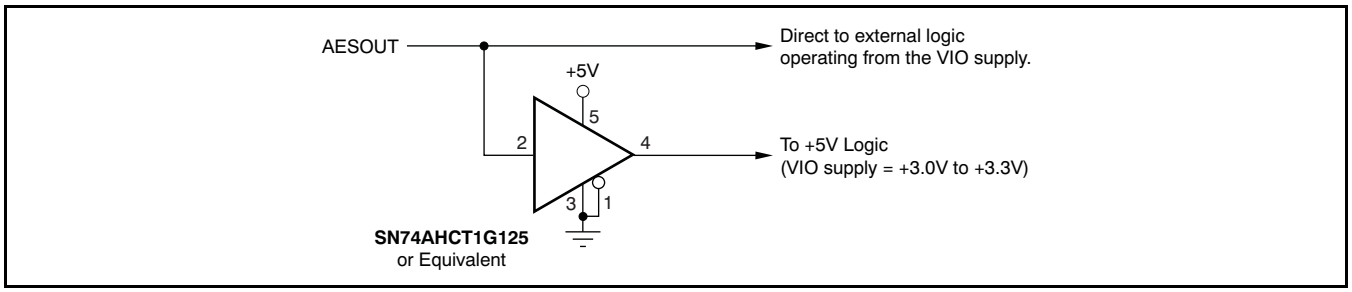

Figure 91. CMOS/TTL Output Logic Interface

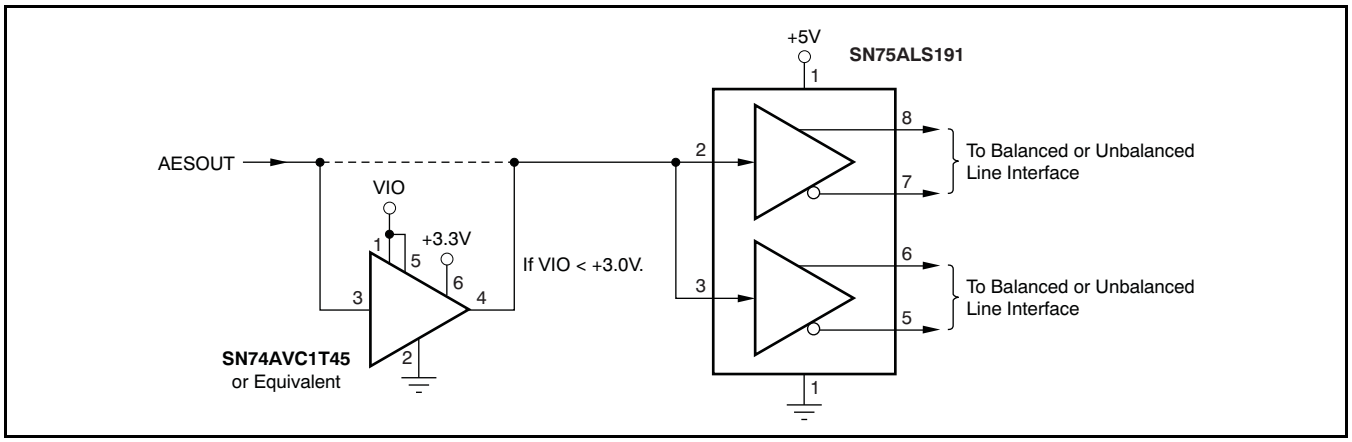

Figure 92. External Line Driver Interface

REGISTER AND DATA BUFFER ORGANIZATION

The SRC4382 organizes the on-chip registers and data buffers into four pages. The currently active page is chosen by programming the Page Selection Register to the desired page number. The Page Selection Register is available on every register page at address 0x7F, allowing easy movement between pages. Table 2 indicates the page selection corresponding to the Page Selection Register value.

Table 2. Register Page Selection

Page Selection Register Value (Hex)	Selected Register Page
00	Page 0, Control and Status Registers
01	Page 1, DIR Channel Status and User Data Buffers
02	Page 2, DIT Channel Status and User Data Buffers
03	Page 3, Reserved

Register Page 0 contains the control registers utilized to configure the various function blocks within the SRC4382. In addition, status registers are provided for flag and error conditions, with many of the status bits capable of generating an interrupt signal when enabled. See Table 3 for the control and status register map.

Register Page 1 contains the digital interface receiver (or DIR) channel status and user data buffers. These buffers correspond to the data contained in the C and U bits of the previously received block of the AES3-encoded data stream. The contents of these buffers may be read through the SPI or I^2C serial host interface and processed as needed by the host system. See Table 5 for the DIR channel status buffer map, and Table 6 for the DIR user data buffer map.

Register Page 2 contains the digital interface transmitter (or DIT) channel status and user data buffers. These buffers correspond to the data contained in the C and U bits of the transmitted AES3-encoded data stream. The contents of these buffers may be written through the SPI or I^2C serial host interface to configure the C and U bits of the transmitted AES3 data stream. The buffers may also be read for verification by the host system. See Table 7 for the DIT channel status buffer map, and Table 8 for the DIT user data buffer map.

Register Page 3 is reserved for factory test and verification purposes, and cannot be accessed without an unlock code. The unlock code remains private; the test modes disable normal operation of the device, and are not useful in customer applications.

CONTROL REGISTERS

See Table 3 for the control and status register map of the SRC4382. Register addresses 0x00 and 0x34 through 0x7E are reserved for factory or future use. All register addresses are expressed as hexadecimal numbers. The following pages provide detailed descriptions for each control and status register.

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Table 3. Control and Status Register Map (Register Page 0)

ADDRESS (Hex)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	REGISTER GROUP
01	RESET	0	$\overline{\text{PDALL}}$	$\overline{\text{PDPA}}$	$\overline{\text{PDPB}}$	$\overline{\text{PDTX}}$	$\overline{\text{PDRX}}$	$\overline{\text{PDSRC}}$	Power-Down and Reset
02	0	0	0	0	0	TX	RX	SRC	Global Interrupt Status
03	0	AMUTE	AOUTS1	AOUTS0	AM/S	AFMT2	AFMT1	AFMT0	Port A Control
04	0	0	0	0	ACLK1	ACLK0	ADIV1	ADIV0	Port A Control
05	0	BMUTE	BOUTS1	BOUTS0	BM/S	BFMT2	BFMT1	BFMT0	Port B Control
06	0	0	0	0	BCLK1	BCLK0	BDIV1	BDIV0	Port B Control
07	TXCLK	TXDIV1	TXDIV0	TXIS1	TXIS0	BLSM	VALID	BSSL	Transmitter Control
08	BYPMUX1	BYPMUX0	AESMUX	LDMUX	TXBTD	AESOFF	TXMUTE	TXOFF	Transmitter Control
09	0	0	0	0	0	VALSEL	TXCUS1	TXCUS0	Transmitter Control
0A	0	0	RATIO	READY	0	0	TSLIP	TBTI	SRC and DIT Status
0B	0	0	MRATIO	MREADY	0	0	MTSLIP	MTBTI	SRC and DIT Interrupt Mask
0C	RATIOM1	RATIOM0	READYM1	READYM0	TSLIPM1	TSLIPM0	TBTIM1	TBTIM0	SRC and DIT Interrupt Mode
0D	0	0	0	RXBTD	RXCLK	0	RXMUX1	RXMUX	Receiver Control
0E	0	0	0	LOL	RXAMLL	RXCKOD1	RXCKOD0	RXCKOE	Receiver Control
0F	P3	P2	P1	P0	J5	J4	J3	J2	Receiver PLL Configuration
10	J1	J0	D13	D12	D11	D10	D9	D8	Receiver PLL Configuration
11	D7	D6	D5	D4	D3	D2	D1	D0	Receiver PLL Configuration
12	0	0	0	0	0	0	DTS CD/LD	IEC61937	Non-PCM Audio Detection
13	0	0	0	0	0	0	RXCKR1	RXCKR0	Receiver Status
14	CSCRC	PARITY	VBIT	BPERR	QCHG	UNLOCK	QCRC	RBTI	Receiver Status
15	0	0	0	0	0	0	0	OSLIP	Receiver Status
16	MCSCRC	MPARITY	MVBIT	MBPERR	MQCHG	MUNLOCK	MQCRC	MRBTI	Receiver Interrupt Mask
17	0	0	0	0	0	0	0	MOSLIP	Receiver Interrupt Mask
18	QCHGM1	QCHGM0	UNLOCKM1	UNLOCKM0	QCRCM1	QCRCM0	RBTIM1	RBTIM0	Receiver Interrupt Mode
19	CSCRCM1	CSCRCM0	PARITYM1	PARITYM0	VBITM1	VBITM0	BPERRM1	BPERRM0	Receiver Interrupt Mode
1A	0	0	0	0	0	0	OSLIPM1	OSLIPM0	Receiver Interrupt Mode
1B	0	0	0	0	GPO13	GPO12	GPO11	GPO10	General-Purpose Out (GPO1)
1C	0	0	0	0	GPO23	GPO22	GPO21	GPO20	General-Purpose Out (GPO2)
1D	0	0	0	0	GPO33	GPO32	GPO31	GPO30	General-Purpose Out (GPO3)
1E	0	0	0	0	GPO43	GPO42	GPO41	GPO40	General-Purpose Out (GPO4)
1F	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Audio CD Q-Channel Sub-Code
20	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Audio CD Q-Channel Sub-Code
21	Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23	Audio CD Q-Channel Sub-Code
22	Q24	Q25	Q26	Q27	Q28	Q29	Q30	Q31	Audio CD Q-Channel Sub-Code
23	Q32	Q33	Q34	Q35	Q36	Q37	Q38	Q39	Audio CD Q-Channel Sub-Code
24	Q40	Q41	Q42	Q43	Q44	Q45	Q46	Q47	Audio CD Q-Channel Sub-Code
25	Q48	Q49	Q50	Q51	Q52	Q53	Q54	Q55	Audio CD Q-Channel Sub-Code
26	Q56	Q57	Q58	Q59	Q60	Q61	Q62	Q63	Audio CD Q-Channel Sub-Code
27	Q64	Q65	Q66	Q67	Q68	Q69	Q70	Q71	Audio CD Q-Channel Sub-Code
28	Q72	Q73	Q74	Q75	Q76	Q77	Q78	Q79	Audio CD Q-Channel Sub-Code
29	PC15	PC14	PC13	PC12	PC11	PC10	PC09	PC08	PC Burst Preamble, High Byte
2A	PC07	PC06	PC05	PC04	PC03	PC02	PC01	PC00	PC Burst Preamble, Low Byte
2B	PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08	PD Burst Preamble, High Byte
2C	PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00	PD Burst Preamble, Low Byte
2D	0	TRACK	0	MUTE	SRCCLK1	SRCCLK0	SRCIS1	SRCIS0	SRC Control
2E	0	0	AUTODEM	DEM1	DEM0	DDN	IGRP1	IGRP0	SRC Control
2F	OWL1	OWL0	0	0	0	0	0	0	SRC Control
30	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0	SRC Control
31	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0	SRC Control
32	SRI4	SRI3	SRI2	SRI1	SRI0	SRF10	SRF9	SRF8	SRC Input: Output Ratio
33	SRF7	SRF6	SRF5	SRF4	SRF3	SRF2	SRF1	SRF0	SRC Input: Output Ratio
7F	0	0	0	0	0	0	PAGE1	PAGE0	Page Selection

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Register 01: Power-Down and Reset

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RESET	0	$\overline{\text{PDALL}}$	$\overline{\text{PDPA}}$	$\overline{\text{PDPB}}$	$\overline{\text{PDTX}}$	$\overline{\text{PDRX}}$	$\overline{\text{PDSRC}}$

$\overline{\text{PDSRC}}$ **Power-Down for the SRC Function Block**

This bit is utilized to power-down the SRC and associated functions.

$\overline{\text{PDSRC}}$	SRC Power-Down Mode
0	Enabled (Default)
1	Disabled; the SRC function block will operate normally based upon the applicable control register settings.

$\overline{\text{PDRX}}$ **Power-Down for the Receiver Function Block**

This bit is utilized to power-down the DIR and associated functions. All receiver outputs are forced low.

$\overline{\text{PDRX}}$	Receiver Power-Down Mode
0	Enabled (Default)
1	Disabled; the Receiver function block will operate normally based upon the applicable control register settings.

$\overline{\text{PDTX}}$ **Power-Down for the Transmitter Function Block**

This bit is utilized to power-down the DIT and associated functions. All transmitter outputs are forced low.

$\overline{\text{PDTX}}$	Transmitter Power-Down Mode
0	Enabled (Default)
1	Disabled; the Transmitter function block will operate normally based upon the applicable control register settings.

$\overline{\text{PDPB}}$ **Power-Down for Serial Port B**

This bit is utilized to power-down the audio serial I/O Port B. All port outputs are forced low.

$\overline{\text{PDPB}}$	Port B Power-Down Mode
0	Enabled (Default)
1	Disabled; Port B will operate normally based upon the applicable control register settings.

$\overline{\text{PDPA}}$ **Power-Down for Serial Port A**

This bit is utilized to power-down the audio serial I/O Port A. All port outputs are forced low.

$\overline{\text{PDPA}}$	Port A Power-Down Mode
0	Enabled (Default)
1	Disabled; Port A will operate normally based upon the applicable control register settings.

$\overline{\text{PDALL}}$ **Power-Down for All Functions**

This bit is utilized to power-down all function blocks except the host interface port and the control and status registers.

$\overline{\text{PDALL}}$	All Function Power-Down Mode
0	Enabled (Default)
1	Disabled; all function blocks will operate normally based upon the applicable control register settings.

RESET **Software Reset**

This bit is used to force a reset initialization sequence, and is equivalent to forcing an external reset via the $\overline{\text{RST}}$ input (pin 24).

RESET	Reset Function
0	Disabled (Default)
1	Enabled; all control registers will be reset to the default state.

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Register 02: Global Interrupt Status (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	TX	RX	SRC

SRC — **SRC Function Block Interrupt Status (Active High)**

When set to 1, this bit indicates an active interrupt from the SRC function block. This bit is active high. The user should then read status register 0x0A in order to determine which of the sources has generated an interrupt.

RX — **Receiver Function Block Interrupt Status (Active High)**

When set to 1, this bit indicates an active interrupt from the DIR function block. This bit is active high. The user should then read status registers 0x14 and 0x15 in order to determine which of the sources has generated an interrupt.

TX — **Transmitter Function Block Interrupt Status (Active High)**

When set to 1, this bit indicates an active interrupt from the DIT function block. This bit is active high. The user should then read status register 0x0A in order to determine which of the sources has generated an interrupt.

Register 03: Port A Control Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	AMUTE	AOUTS1	AOUTS0	AM/S	AFMT2	AFMT1	AFMT0

AFMT[2:0] — **Port A Audio Data Format**

These bits are used to set the audio input and output data format for Port A. Refer to the Audio Serial Port Operation section for illustrations of the supported data formats. Refer to the Electrical Characteristics: *Audio Serial Ports* table and Figure 1 for an applicable timing diagram and parameters.

AFMT2	AFMT1	AFMT0	Audio Data Format
0	0	0	24-Bit Left-Justified (Default)
0	0	1	24-Bit Philips I^2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right-Justified
1	0	1	18-Bit Right-Justified
1	1	0	20-Bit Right-Justified
1	1	1	24-Bit Right-Justified

Note: When the SRC is selected as the output data source for Port A and the data format for the port is set to Right-Justified, the proper word length must be selected in the Port A control registers such that it matches the corresponding SRC output data word length. Refer to control register 0x2F for the SRC output word length selection.

AM/S — **Port A Slave/Master Mode**

This bit is used to set the audio clock mode for Port A to either Slave or Master.

AM/S	Slave/Master Mode
0	Slave mode; the LRCK and BCK clocks are inputs generated by an external digital audio source. (Default)
1	Master mode; the LRCK and BCK clocks are outputs, derived from the Port A master clock source.

AOUTS[1:0] — **Port A Output Data Source**

These bits are used to select the output data source for Port A. The data is output at SDOUTA (pin 40).

AOUTS1	AOUTS0	Output Data Source
0	0	Port A Input, for data loop back. (Default)
0	1	Port B Input
1	0	DIR
1	1	SRC

AMUTE — **Port A Output Mute**

This bit is used to mute the Port A audio data output.

AMUTE	Output Mute
0	Disabled; SDOUTA is driven by the output data source. (Default)
1	Enabled; SDOUTA is forced low.

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Register 04: Port A Control Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	ACLK1	ACLK0	ADIV1	ADIV0

ADIV[1:0] **Port A Master Clock Divider**

These bits are used to set the master clock divider for generating the LRCKA clock for Port A when configured for Master mode operation. BCKA is always set to 64 times the LRCKA clock rate in Master mode.

ADIV1	ADIV0	Master Mode Clock Divider
0	0	Divide By 128 (Default)
0	1	Divide By 256
1	0	Divide By 384
1	1	Divide By 512

ACLK[1:0] **Port A Master Clock Source**

These bits are used to set the master clock source for Port A when configured for Master mode operation.

ACLK1	ACLK0	Master Clock Source
0	0	MCLK (Default)
0	1	RXCKI
1	0	RXCKO
1	1	Reserved

Register 05: Port B Control Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	BMUTE	BOUTS1	BOUTS0	BM/S	BFMT2	BFMT1	BFMT0

BFMT[2:0] **Port B Audio Data Format**

These bits are used to set the audio input and output data format for Port B. Refer to the Audio Serial Port Operation section for illustrations of the supported data formats. Refer to the Electrical Characteristics: *Audio Serial Ports* table and Figure 1 for an applicable timing diagram and parameters.

BFMT2	BFMT1	BFMT0	Audio Data Format
0	0	0	24-Bit Left-Justified (Default)
0	0	1	24-Bit Philips I^2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right-Justified
1	0	1	18-Bit Right-Justified
1	1	0	20-Bit Right-Justified
1	1	1	24-Bit Right-Justified

Note: When the SRC is selected as the output data source for Port B and the data format for the port is set to Right-Justified, the proper word length must be selected in the Port B control registers such that it matches the corresponding SRC output data word length. Refer to control register 0x2F for the SRC output word length selection.

BM/S **Port B Slave/Master Mode**

This bit is used to set the audio clock mode for Port B to either Slave or Master.

BM/S	Slave/Master Mode
0	Slave mode; the LRCK and BCK clocks are generated by an external source. (Default)
1	Master mode; the LRCK and BCK clocks are derived from the Port A master clock source.

BOUTS[1:0] **Port B Output Source**

These bits are used to select the output data source for Port B. The data is output at SDOUTB (pin 45).

BOUTS1	BOUTS0	Output Data Source
0	0	Port B Input, for data loop back. (Default)
0	1	Port A Input
1	0	DIR
1	1	SRC

BMUTE **Port B Output Mute**

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This bit is used to mute the Port B audio data output.

BMUTE	Output Mute
0	Disabled; SDOUTB is driven by the output data source. (Default)
1	Enabled; SDOUTB is forced low.

Register 06: Port B Control Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	BCLK1	BCLK0	BDIV1	BDIV0

BDIV[1:0] **Port B Master Mode Clock Divider**

These bits are used to set the master clock divider for generating the LRCKB clock for Port B when configured for Master mode operation. BCKB is always set to 64 times the LRCKB clock rate in Master mode.

BDIV1	BDIV0	Master Mode Clock Divider
0	0	Divide By 128 (Default)
0	1	Divide By 256
1	0	Divide By 384
1	1	Divide By 512

BCLK[1:0] **Port B Master Clock Source**

These bits are used to set the master clock source for Port B when configured for Master mode operation.

BCLK1	BCLK0	Master Clock Source
0	0	MCLK (Default)
0	1	RXCKI
1	0	RXCKO
1	1	Reserved

Register 07: Transmitter Control Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TXCLK	TXDIV1	TXDIV0	TXIS1	TXIS0	BLSM	VALID	BSSL

BSSL **Block Start or Asynchronous Data Slip Interrupt Trigger Selection**

This bit is used to select the trigger source for the Transmitter TSLIP status and interrupt bit.

BSSL	TSLIP Interrupt Trigger Source
0	Data Slip Condition (Default)
1	Block Start Condition

VALID **Validity (V) Data Bit**

This bit may be used to set the validity (or V) data bit in the AES3-encoded output. Refer to the VALSEL bit in control register 0x09 for V-bit source selection.

VALID	Transmitted Validity (V) Bit Data
0	Indicates that the transmitted audio data is suitable for conversion to an analog signal or for further digital processing. (Default)
1	Indicates that the transmitted audio data is not suitable for conversion to an analog signal or for further digital processing.

BLSM **Transmitter Block Start Input/Output Mode**

This bit is used to select the input/output mode for the DIT block start pin, BLS (pin 35).

BLSM	BLS Pin Mode
0	Input (Default)
1	Output

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TXIS[1:0] **Transmitter Input Data Source**

These bits are used to select the audio data source for the DIT function block.

TXIS1	TXIS0	Output Word Length
0	0	Port A (Default)
0	1	Port B
1	0	DIR
1	1	SRC

TXDIV[1:0] **Transmitter Master Clock Divider**

These bits are used to select the Transmitter master clock divider, which determines the output frame rate.

TXDIV1	TXDIV0	Clock Divider
0	0	Divide the master clock by 128. (Default)
0	1	Divide the master clock by 256.
1	0	Divide the master clock by 384.
1	1	Divide the master clock by 512.

TXCLK **Transmitter Master Clock Source**

This bit is used to select the master clock source for the Transmitter block.

TXCLK	Transmitter Master Clock Source
0	MCLK Input (Default)
1	RXCKO; the recovered master clock from the DIR function block.

Register 08: Transmitter Control Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
BYPMUX1	BYPMUX0	AESMUX	LDMUX	TXBTD	AESOFF	TXMUTE	TXOFF

TXOFF **Transmitter Line Driver Output Enable**

This bit is used to enable or disable the TX+ (pin 32) and TX– (pin 31) line driver outputs.

TXOFF	Transmitter Line Driver
0	Enabled; the line driver outputs function normally. (Default)
1	Disabled; the line driver outputs are forced low.

TXMUTE **Transmitter Audio Data Mute**

This bit is used to set the 24 bits of audio and auxiliary data to all zeros for both Channels 1 and 2.

TXMUTE	Transmitter Audio Data Mute
0	Disabled (Default)
1	Enabled; the audio data for both Channels 1 and 2 are set to all zeros.

AESOFF **AESOUT Output Enable**

This bit is used to enable or disable the AESOUT (pin 34) buffered AES3-encoded CMOS logic level output.

AESOFF	AESOUT Output
0	Enabled; the AESOUT pin functions normally. (Default)
1	Disabled; the AESOUT pin is forced low.

TXBTD **Transmitter C and U Data Buffer Transfer Disable**

This bit is used to enable and disable buffer transfers between the DIT User Access (UA) and DIT Transmitter Access (TA) buffers for both channel status (C) and user (U) data.
Buffer transfers may be disabled, allowing the user to write new C and U data to the UA buffers via the SPI or I^2C serial host interface. Once updated, UA-to-TA buffer transfers may then be re-enabled, allowing the TA buffer to be updated and the new C and U data to be transmitted at the start of the next block.

TXBTD	User Access (UA) to Transmitter Access (TA) Buffer Transfers
0	Enabled (Default)
1	Disabled; allows the user to update DIT C and U data buffers.

Note: The TXCUS0 and TXCUS1 bits in control register 0x09 must be set to a non-zero value in order for DIT UA buffer updates to occur.

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LDMUX **Transmitter Line Driver Input Source Selection**

This bit is used to select the input source for the DIT differential line driver outputs.

LDMUX	Line Driver Input Source
0	DIT AES3 Encoder Output (Default)
1	Bypass Multiplexer Output

AESMUX **AESOUT CMOS Buffer Input Source Selection**

This bit is used to select the input source for the AESOUT CMOS logic level output.

AESMUX	AESOUT Buffer Input Source
0	DIT AES3 Encoder Output (Default)
1	Bypass Multiplexer Output

BYPMUX[1:0] **Bypass Multiplexer Source Selection**

These bits select the line receiver output to be utilized as the Bypass multiplexer data source.

BYPMUX1	BYPMUX0	Line Receiver Output Selection
0	0	RX1 (Default)
0	1	RX2
1	0	RX3
1	1	RX4

Register 09: Transmitter Control Register 3

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	VALSEL	TXCUS1	TXCUS0

TXCUS[1:0] **Transmitter Channel Status and User Data Source**

These bits select the source of the channel status (or C) data and user (or U) data which is used to load the DIT User Access (UA) buffers.

TXCUS1	TXCUS0	DIT UA Buffer Source
0	0	The buffers will not be updated. (Default)
0	1	The buffers are updated via the SPI or I^2C host interface.
1	0	The buffers are updated via the DIR RA buffers.
1	1	The first 10 bytes of the buffers are updated via the SPI or I^2C host, while the remainder of the buffers are updated via the DIR RA buffers.

VALSEL **Transmitter Validity Bit Source**

This bit is utilized to select the source for the validity (or V) bit in the AES3-encoded output data stream.

VALSEL	Validity (or V) Bit Source Selection
0	The VALID bit in control register 0x07.
1	The V bit is transferred from the DIR block with zero latency.

Register 0A: SRC and DIT Status (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	RATIO	READY	0	0	TSLIP	TBTI

TBTI **Transmitter Buffer Transfer Status, Active High**

When DIT User Access (UA) to Transmitter Access (TA) buffer transfers are enabled (the TXBTD bit in control register 0x08 is set to 0), and the TBTI interrupt is unmasked (the MTBTI bit in control register 0x0B is set to 1), the TBTI bit will be set to 1 when the UA-to-TA buffer transfer has completed. This configuration also causes the $\overline{INT}$ output (pin 23) to be driven low and the TX bit in status register 0x02 to be set to 1, indicating that an interrupt has occurred.

TSLIP **Transmitter Source Data Slip Status, Active High**

The TSLIP bit will be set to 1 when either an asynchronous data slip or block start condition is detected, and the TSLIP interrupt is unmasked (the MTSLIP bit in control register 0x0B is set to 1). The BSSL bit in control register 0x07 is used to set the source for this interrupt.
The TSLIP bit being forced to 1 will also cause the $\overline{INT}$ output (pin 23) to be driven low and the TX bit in status register 0x02 to be set to 1, indicating that an interrupt has occurred.

READY **SRC Rate Estimator Ready Status, Active High**

The READY bit will be set to 1 when the input and output rate estimators have completed the Fast mode portion of the rate estimation process, and the READY interrupt is unmasked (the MREADY bit in control register 0x0B is set to 1). This will also cause the $\overline{INT}$ output (pin 23) to be driven low and the SRC bit in status register 0x02 to be set to 1, indicating that an interrupt has occurred.

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RATIO **SRC Ratio Status, Active High**

The RATIO bit will be set to 1 when the input sampling rate is higher than the output sampling rate, and the RATIO interrupt is unmasked (the MRATIO bit in control register 0x0B is set to 1). This will also cause the $\overline{\text{INT}}$ output (pin 23) to be driven low and the SRC bit in status register 0x02 to be set to 1, indicating that an interrupt has occurred.

Register 0B: SRC and DIT Interrupt Mask Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	MRATIO	MREADY	0	0	MTSLIP	MTBTI

MBTI **Transmitter Buffer Transfer Interrupt Mask**

MTBI	BTI Interrupt Mask
0	BTI interrupt is masked. (Default)
1	BTI interrupt is enabled.

MTSLIP **Transmitter TSLIP Interrupt Mask**

MTSLIP	TSLIP Interrupt Mask
0	TSLIP interrupt is masked. (Default)
1	TSLIP interrupt is enabled.

MREADY **SRC Ready Interrupt Mask**

MREADY	READY Interrupt Mask
0	READY interrupt is masked. (Default)
1	READY interrupt is enabled.

MRATIO **SRC Ratio Interrupt Mask**

MRATIO	RATIO Interrupt Mask
0	RATIO interrupt is masked. (Default)
1	RATIO interrupt is enabled.

Register 0C: SRC and DIT Interrupt Mode Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RATIOM1	RATIOM0	READYM1	READYM0	TSLIPM1	TSLIPM0	TBTIM1	TBTIM0

TBTIM[1:0] **Transmitter Buffer Transfer Interrupt Mode**

These bits are utilized to select the active trigger state for the BTI interrupt.

TBTIM1	TBTIM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

TSLIPM[1:0] **Transmitter Data Source Slip Interrupt Mode**

These bits are utilized to select the active trigger state for the TSLIP interrupt.

TSLIPM1	TSLIPM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

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READYM[1:0] **SRC Ready Interrupt Mode**

These bits are utilized to select the active trigger state for the READY interrupt.

READYM1	READYM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

RATIOM[1:0] **SRC Ratio Interrupt Mode**

These bits are utilized to select the active trigger state for the RATIO interrupt.

RATIOM1	RATIOM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

Register 0D: Receiver Control Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	RXBTD	RXCLK	0	RXMUX1	RXMUX0

RXMUX[1:0] **Receiver Input Source Selection**

These bits are used to select the output of the line receiver to be used as the input data source for the DIR core.

RXMUX1	RXMUX0	Input Selection
0	0	RX1 (Default)
0	1	RX2
1	0	RX3
1	1	RX4

RXCLK **Receiver Reference Clock Source**

This bit is used to select the reference clock source for PLL1 in the DIR core.

RXCLK	Receiver Reference Clock
0	RXCKI (Default)
1	MCLK

RXBTD **Receiver C and U Data Buffer Transfer Disable**

This bit is used to enable and disable buffer transfers between the Receiver Access (RA) and User Access (UA) buffers for both channel status (C) and user (U) data.
Buffer transfers are typically disabled to allow the customer to read C and U data from the DIR UA buffer via the SPI or I^2C serial host interface. Once read, the RA-to-UA buffer transfer can be re-enabled to allow the RA buffer to update the contents of the UA buffer in real time.

RXBTD	Receiver Access (RA) to User Access (UA) Buffer Transfers
0	Enabled (Default)
1	Disabled; the user may read C and U data from the DIR UA buffers.

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Register 0E: Receiver Control Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	LOL	RXAMLL	RXCKOD1	RXCKOD0	RXCKOE

RXCKOE **RXCKOE Output Enable**

This bit is used to enable or disable the recovered clock output, RXCKO (pin 12). When disabled, the output is set to a high-impedance state.

RXCKOE	RXCKO Output State
0	Disabled; the RXCKO output is set to high-impedance. (Default)
1	Enabled; the recovered master clock is available at RXCKO.

RXCKOD[1:0] **RXCKO Output Clock Divider**

These bits are utilized to set the clock divider at the output of PLL2. The output of the divider is the RXCKO clock, available internally or at the RXCKO output (pin 12).

RXCKOD1	RXCKOD0	RXCKO Output Divider
0	0	Passthrough, no division is performed. (Default)
0	1	Divide the PLL2 clock output by 2.
1	0	Divide the PLL2 clock output by 4.
1	1	Divide the PLL2 clock output by 8.

RXAMLL **Receiver Automatic Mute for Loss of Lock**

This bit is used to set the automatic mute function for the DIR block when a loss of lock is indicated by both the AES3 decoder and PLL2.

RXAMLL	Receiver Auto-Mute Function
0	Disabled (Default)
1	Enabled; audio data output from the DIR block is forced low for a loss of lock condition.

LOL **Receiver Loss of Lock Mode for the Recovered Clock (output from PLL2)**

This bit is used to set the mode of operation for PLL2 when a loss of lock condition occurs.

LOL	Receiver PLL2 Operation
0	The PLL2 output clock is stopped for a loss of lock condition. (Default)
1	The PLL2 output clock free runs when a loss of lock condition occurs.

Register 0F: Receiver PLL1 Configuration Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
P3	P2	P1	P0	J5	J4	J3	J2

Register 10: Receiver PLL1 Configuration Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
J1	J0	D13	D12	D11	D10	D9	D8

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Register 11: Receiver PLL1 Configuration Register 3

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
D7	D6	D5	D4	D3	D2	D1	D0

Registers 0x0F through 0x11 are utilized to program PLL1 in the DIR core. PLL1 multiplies the DIR reference clock source to an oversampling rate which is adequate for AES3 decoder operation. PLL1 is programmed using the following relationship:

(CLOCK ɹK) / P = 98.304MHz

where:
CLOCK = frequency of the DIR reference clock source.

K = J.D, where the integer part J = 1 to 63, and the fractional part D = 0 to 9999.
P = the pre-divider value, which may be set to any 4-bit value that meets the conditions stated below.
The following conditions must be met for the values of P, J, and D:

If D = 0, then:	**If D ≠ 0, then:**
2 MHz ≤ (CLOCK / P) ≤ 20 MHz and 4 ≤ J ≤ 55.	10 MHz ≤ (CLOCK / P) ≤ 20 MHz and 4 ≤ J ≤11.

Referring to registers 0x0F through 0x11:
P is programmed using bits P[3:0].
J is programmed using bits J[5:0].
D is programmed using bits D[13:0].
Table 4 shows values for P, J, and D for common DIR reference clock rates.

Table 4. PLL1 Register Values for Common Reference Clock Rates

REFERENCE CLOCK RATE (MHz)	P	J	D	ERROR (%)
8.1920	1	12	0	0.0000
11.2896	1	8	7075	0.0002
12.2880	1	8	0	0.0000
16.3840	1	6	0	0.0000
22.5792	2	8	7075	0.0002
24.5760	2	8	0	0.0000
27.0000	2	7	2818	0.0003

Register 12: Non-PCM Audio Detection Status Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	DTS CD/LD	IEC61937

IEC61937 This bit is utilized to indicate the detection of an IEC 61937 data reduced audio format (includes Dolby AC-3, DTS, etc.) for DVD playback or general transmission purposes.

IEC61937	Status
0	Data is not an IEC61937 format.
1	Data is an IEC61937 format. Refer to the PC and PD preamble registers (addresses 0x29 through 0x2C) for data type and burst length.

DTS CD/LD This bit is used to indicate the detection of a DTS encoded audio compact disc (CD) or Laserdisc (LD) playback.

DTS CD/LD	Status
0	The CD/LD is not DTS encoded.
1	DTS CD/LD playback detected.

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Register 13: Receiver Status Register 1 (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	RXCKR1	RXCKR0

RXCKR[1:0] **Maximum Available Recovered Clock Rate**

These two bits indicate the maximum available RXCKO clock rate based upon the DIR detection circuitry, which determines the frame rate of the incoming AES3-encoded bit stream. Based upon the estimated frame rate, a maximum rate for the recovered clock output (RXCKO) is determined and output from PLL2, as well as being loaded into the RXCKR0 and RXCKR1 status bits.
The status of the RXCKR0 and RXCKR1 bits may be utilized to determine the programmed value for the PLL2 output clock divider, set by the RXCKOD0 and RXCKOD1 bits in control register 0x0E.

RXCKR1	RXCKR0	Maximum Available RXCKO Rate
0	0	Clock rate not determined.
0	1	$128f_S$
1	0	$256f_S$
1	1	$512f_S$

Register 14: Receiver Status Register 2 (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
CSCRC	PARITY	VBIT	BPERR	QCHG	UNLOCK	QCRC	RBTI

Note: Status bits must be unmasked in control register 0x16 in order for the status interrupts to be generated.

CSCRC **Channel Status CRC Status**

CSCRC	CRC Status
0	No Error
1	CRC Error Detected

PARITY **Parity Status**

PARITY	Parity Status
0	No Error
1	Parity Error Detected

VBIT **Validity Bit Status**

VBIT	Validity Bit
0	Valid Audio Data Indicated
1	Non-Valid Data Indicated

BPERR **Bipolar Encoding Error Status**

BPERR	Bipolar Encoding Status
0	No Error
1	Bipolar Encoding Error Detected

QCHG **Q-Channel Sub-Code Data Change Status**

QCHG	Q-Channel Data Status
0	No change in Q-channel sub-code data.
1	Q-channel data has changed. May be used to trigger a read of the Q-channel sub-code data, registers 0x1F through 0x28.

UNLOCK **DIR Unlock Error Status**

UNLOCK	DIR Lock Status
0	No error; the DIR AES3 decoder and PLL2 are locked.
1	DIR lock error; the AES3 decoder and PLL2 are unlocked.

QCRC **Q-Channel Sub-Code CRC Status**

QCRC	Q-Channel CRC Status
0	No Error
1	Q-channel sub-code data CRC error detected.

RBTI **Receiver Buffer Transfer Interrupt Status**

RBTI	DIR RA Buffer-to-UA Buffer Transfer Status
0	Buffer Transfer Incomplete, or No Buffer Transfer Interrupt Indicated

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1	Buffer Transfer Completed

Register 15: Receiver Status Register 3 (Read-Only)

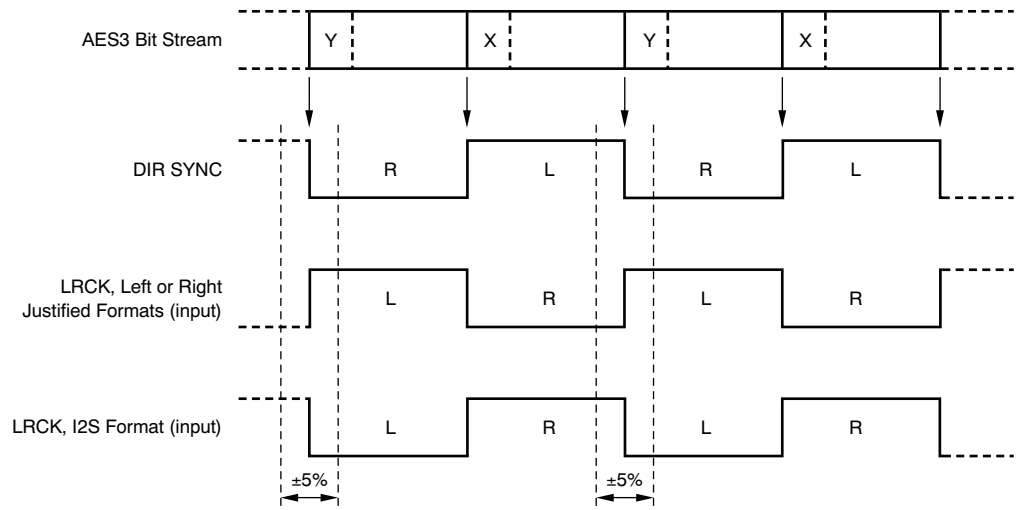
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	0	OSLIP

Note: Status bits must be unmasked in control register 0x17 in order for the status interrupts to be generated.

OSLIP **Receiver Output Data Slip Error Status**

OSLIP	Receiver OSLIP Error Status
0	No Error
1	DIR Output Data Slip/Repeat Error Detected

An OSLIP interrupt is possible when the DIR output is used as the source for either the Port A or Port B audio serial port and the port is configured to operate in slave mode. Figure 93 shows the timing associated with the OSLIP interrupt.
When only one audio serial port (Port A or Port B) is sourced by the DIR output, then the OSLIP status bit and interrupt applies to that port. If both Port A and Port B are sourced by the DIR output, then the OSLIP status bit and interrupt applies to Port A only.



Data Slip or Repeat may occur when the LRCK edges indicated are within the ±5% window.

Figure 93. DIR Output Slip/Repeat (OSLIP) Behavior

Register 16: Receiver Interrupt Mask Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
MCSCRC	MPARITY	MVBIT	MBPERR	MQCHG	MUNLOCK	MQCRC	MRBTI

MCSCRC **Channel Status CRC Error Interrupt Mask**

MCSCRC	CRC Interrupt
0	Masked (Default)
1	Enabled

MPARITY **Parity Error Interrupt Mask**

MPARITY	Parity Error Interrupt
0	Masked (Default)
1	Enabled

MVBIT **Validity Error Interrupt Mask**

MVBIT	Validity Error Interrupt
0	Masked (Default)
1	Enabled

MBPERR **Bipolar Encoding Error Interrupt Mask**

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MBPERR	**Bipolar Error Interrupt**
0	Masked (Default)
1	Enabled

MQCHG **Q-Channel Sub-Code Data Change Interrupt Mask**

MQCHG	**Q-Channel Data Change Interrupt**
0	Masked (Default)
1	Enabled

MUNLOCK **DIR Unlock Error Interrupt Mask**

MUNLOCK	**DIR Unlock Interrupt**
0	Masked (Default)
1	Enabled

MQCRC **Q-Channel Sub-Code CRC Error Interrupt Mask**

MQCRC	**Q-Channel CRC Error Interrupt**
0	Masked (Default)
1	Enabled

MRBTI **Receiver Buffer Transfer Interrupt Mask**

MRBTI	**Receiver Buffer Transfer Interrupt**
0	Masked (Default)
1	Enabled

Register 17: Receiver Interrupt Mask Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	0	MOSLIP

MOSLIP **Receiver Output Data Slip Error Mask**

MOSLIP	**Receiver OSLIP Error Interrupt**
0	Masked (Default)
1	Enabled

Register 18: Receiver Interrupt Mode Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
QCHGM1	QCHGM0	UNLOCKM1	UNLOCKM0	QCRCM1	QCRCM0	RBTIM1	RBTIM0

QCHGM[1:0] **Q-Channel Sub-Code Data Change Interrupt Mode**

QCHGM1	**QCHGM0**	**Interrupt Active State**
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

UNLOCKM[1:0] **DIR Unlock Error Interrupt Mode**

UNLOCKM1	**UNLOCKM0**	**Interrupt Active State**
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

QCRCM[1:0] **Q-Channel Sub-Code CRC Error Interrupt Mode**

QCRCM1	**QCRCM0**	**Interrupt Active State**
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

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RBTIM[1:0] **Receive Buffer Transfer Interrupt Mode**

RBTIM1	RBTIM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

Register 19: Receiver Interrupt Mode Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
CSCRCM1	CSCRCM0	PARITYM1	PARITYM0	VBITM1	VBITM0	BPERRM1	BPERRM0

CSCRCM[1:0] **Channel Status CRC Error Interrupt Mode**

CSCRCM1	CSCRCM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

PARITYM[1:0] **Parity Error Interrupt Mode**

PARITYM1	PARITYM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

VBITM[1:0] **Validity Error Interrupt Mode**

VBITM1	VBITM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

BPERRM[1:0] **Bipolar Encoding Error Interrupt Mode**

BPERRM1	BPERRM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

Register 1A: Receiver Interrupt Mode Register 3

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	OSLIPM1	OSLIPM0

OSLIPM[1:0] **Receiver Output Data Slip Error Interrupt Mode**

OSLIPM1	OSLIPM0	Interrupt Active State
0	0	Rising Edge Active (Default)
0	1	Falling Edge Active
1	0	Level Active
1	1	Reserved

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Register 1B: General-Purpose Output 1 (GPO1) Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	GPO13	GPO12	GPO11	GPO10

GPO[13:10] **General-Purpose Output 1 (GPO1) Configuration**

These bits are used to set the state or data source for the general-purpose digital output pin GPO1.

GPO13	GPO12	GPO11	GPO10	GPO1 Function
0	0	0	0	GPO1 is Forced Low (Default)
0	0	0	1	GPO1 is Forced High
0	0	1	0	SRC Interrupt, Active Low
0	0	1	1	Transmitter Interrupt, Active Low
0	1	0	0	Receiver Interrupt, Active Low
0	1	0	1	Receiver 50/15µs Pre-Emphasis, Active Low
0	1	1	0	Receiver Non-Audio Data, Active High
0	1	1	1	Receiver Non-Valid Data, Active High
1	0	0	0	Receiver Channel Status Bit
1	0	0	1	Receiver User Data Bit
1	0	1	0	Receiver Block Start Clock
1	0	1	1	Receiver COPY Bit (0 = Copyright Asserted, 1 = Copyright Not Asserted)
1	1	0	0	Receiver L-Bit (0 = First Generation or Higher, 1 = Original)
1	1	0	1	Receiver Parity Error, Active High
1	1	1	0	Receiver Internal Sync Clock
1	1	1	1	Transmitter Internal Sync Clock

Register 1C: General-Purpose Output 2 (GPO2) Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	GPO23	GPO22	GPO21	GPO20

GPO[23:20] **General-Purpose Output 2 (GPO2) Configuration**

These bits are used to set the state or data source for the general-purpose digital output pin GPO2.

GPO23	GPO22	GPO21	GPO20	GPO2 Function
0	0	0	0	GPO2 is Forced Low (Default)
0	0	0	1	GPO2 is Forced High
0	0	1	0	SRC Interrupt, Active Low
0	0	1	1	Transmitter Interrupt, Active Low
0	1	0	0	Receiver Interrupt, Active Low
0	1	0	1	Receiver 50/15µs Pre-Emphasis, Active Low
0	1	1	0	Receiver Non-Audio Data, Active High
0	1	1	1	Receiver Non-Valid Data, Active High
1	0	0	0	Receiver Channel Status Bit
1	0	0	1	Receiver User Data Bit
1	0	1	0	Receiver Block Start Clock
1	0	1	1	Receiver COPY Bit (0 = Copyright Asserted, 1 = Copyright Not Asserted)
1	1	0	0	Receiver L-Bit (0 = First Generation or Higher, 1 = Original)
1	1	0	1	Receiver Parity Error, Active High
1	1	1	0	Receiver Internal Sync Clock
1	1	1	1	Transmitter Internal Sync Clock

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Register 1D: General-Purpose Output 3 (GPO3) Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	GPO33	GPO32	GPO31	GPO30

GPO[33:30] **General-Purpose Output 3 (GPO3) Configuration**

These bits are used to set the state or data source for the general-purpose digital output pin GPO3.

GPO33	GPO32	GPO31	GPO30	GPO3 Function
0	0	0	0	GPO3 is Forced Low (Default)
0	0	0	1	GPO3 is Forced High
0	0	1	0	SRC Interrupt, Active Low
0	0	1	1	Transmitter Interrupt, Active Low
0	1	0	0	Receiver Interrupt, Active Low
0	1	0	1	Receiver 50/15µs Pre-Emphasis, Active Low
0	1	1	0	Receiver Non-Audio Data, Active High
0	1	1	1	Receiver Non-Valid Data, Active High
1	0	0	0	Receiver Channel Status Bit
1	0	0	1	Receiver User Data Bit
1	0	1	0	Receiver Block Start Clock
1	0	1	1	Receiver COPY Bit (0 = Copyright Asserted, 1 = Copyright Not Asserted)
1	1	0	0	Receiver L-Bit (0 = First Generation or Higher, 1 = Original)
1	1	0	1	Receiver Parity Error, Active High
1	1	1	0	Receiver Internal Sync Clock
1	1	1	1	Transmitter Internal Sync Clock

Register 1E: General-Purpose Output 4 (GPO4) Control Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	GPO43	GPO42	GPO41	GPO40

GPO[43:40] **General-Purpose Output 4 (GPO4) Configuration**

These bits are used to set the state or data source for the general-purpose digital output pin GPO4.

GPO43	GPO42	GPO41	GPO40	GPO4 Function
0	0	0	0	GPO4 is Forced Low (Default)
0	0	0	1	GPO4 is Forced High
0	0	1	0	SRC Interrupt, Active Low
0	0	1	1	Transmitter Interrupt, Active Low
0	1	0	0	Receiver Interrupt, Active Low
0	1	0	1	Receiver 50/15µs Pre-Emphasis, Active Low
0	1	1	0	Receiver Non-Audio Data, Active High
0	1	1	1	Receiver Non-Valid Data, Active High
1	0	0	0	Receiver Channel Status Bit
1	0	0	1	Receiver User Data Bit
1	0	1	0	Receiver Block Start Clock
1	0	1	1	Receiver COPY Bit (0 = Copyright Asserted, 1 = Copyright Not Asserted)
1	1	0	0	Receiver L-Bit (0 = First Generation or Higher, 1 = Original)
1	1	0	1	Receiver Parity Error, Active High
1	1	1	0	Receiver Internal Sync Clock
1	1	1	1	Transmitter Internal Sync Clock

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Registers 1F through 28: Q-Channel Sub-Code Data Registers

Registers 0x1F through 0x28 comprise the Q-channel sub-code buffer, which may be accessed for audio CD playback. The Q-channel data provides information regarding the playback status for the current disc. The buffer data is decoded by the DIR block.

Register 1F: Q-Channel Sub-Code Data Register 1 (Read-Only), Bits[7:0], Control and Address

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7

Register 20: Q-Channel Sub-Code Data Register 2 (Read-Only), Bits[15:8], Track

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15

Register 21: Q-Channel Sub-Code Data Register 3 (Read-Only), Bits[23:16], Index

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q16	Q17	Q18	Q19	Q20	Q21	Q22	Q23

Register 22: Q-Channel Sub-Code Data Register 4 (Read-Only), Bits[31:24], Minutes

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q24	Q25	Q26	Q27	Q28	Q29	Q30	Q31

Register 23: : Q-Channel Sub-Code Data Register 5 (Read-Only), Bits[39:32], Seconds

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q32	Q33	Q34	Q35	Q36	Q37	Q38	Q39

Register 24: : Q-Channel Sub-Code Data Register 6 (Read-Only), Bits[47:40], Frame

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q40	Q41	Q42	Q43	Q44	Q45	Q46	Q47

Register 25: Q-Channel Sub-Code Data Register 7 (Read-Only), Bits[55:48], Zero

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q48	Q49	Q50	Q51	Q52	Q53	Q54	Q55

Register 26: Q-Channel Sub-Code Data Register 8 (Read-Only), Bits[63:56], AMIN

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q56	Q57	Q58	Q59	Q60	Q61	Q62	Q63

Register 27: Q-Channel Sub-Code Data Register 9 (Read-Only), Bits[71:64], ASEC

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q64	Q65	Q66	Q67	Q68	Q69	Q70	Q71

Register 28: Q-Channel Sub-Code Data Register 10 (Read-Only), Bits[79:72], AFRAME

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Q72	Q73	Q74	Q75	Q76	Q77	Q78	Q79

Registers 29 through 2C: IEC61937 PC/PD Burst Preamble

The PC and PD burst preambles are part of the IEC61937 standard for transmission of data reduced, non-PCM audio over a standard two-channel interface (IEC60958). Examples of data-reduced formats include Dolby AC-3, DTS, various flavors of MPEG audio (including AAC), and Sony ATRAC. The PA and PB preambles provide synchronization data, and are fixed values of 0xF872 and 0x4E1F, respectively. The PC preamble indicates the type of data being carried by the interface and the PD preamble indicates the length of the burst, given as number of bits.
Registers 0x29 through 0x2C contain the PC and PD preambles as decoded by the DIR block.

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Register 29: Burst Preamble PC High-Byte Status Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
PC15	PC14	PC13	PC12	PC11	PC10	PC09	PC08

Register 2A: Burst Preamble PC Low-Byte Status Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
PC07	PC06	PC05	PC04	PC03	PC02	PC01	PC00

PC[4:0], Hex	Data Type
00	Null
01	Dolby AC-3
02	Reserved
03	Pause
04	MPEG-1 Layer 1
05	MPEG-1 Layer 2 or 3, or MPEG-2 Without Extension
06	MPEG-2 Data With Extension
07	MPEG-2 AAC ADTS
08	MPEG-2 Layer 1 Low Sample Rate
09	MPEG-2 Layer 2 or 3 Low Sample Rate
0A	Reserved
0B	DTS Type 1
0C	DTS Type 2
0D	DTS Type 3
0E	ATRAC
0F	ATRAC2/3
10-1F	Reserved

Bits PC[6:5] are both set to 0.
Bit PC[7] is an Error Flag, where: 0 = A valid burst-payload; 1 = Burst-payload may contain errors.
Bits PC[12:8] are data-type dependent.
Bits PC[15:13] indicate the stream number, which is set to 0.

Register 2B: Burst Preamble PD High-Byte Status Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
PD15	PD14	PD13	PD12	PD11	PD10	PD09	PD08

Register 2C: Burst Preamble PD Low-Byte Status Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
PD07	PD06	PD05	PD04	PD03	PD02	PD01	PD00

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Register 2D: SRC Control Register 1

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	TRACK	0	MUTE	SRCCLK1	SRCCLK0	SRCIS1	SRCIS0

SRCIS[1:0] **SRC Input Data Source**

These bits select the input data source for the SRC.

SRCIS1	SRCIS0	Input Source
0	0	Port A (Default)
0	1	Port B
1	0	DIR
1	1	Reserved

SRCCLK[1:0] **SRC Reference Clock Source**

These bits select the reference clock source for the SRC.

SRCCLK1	SRCCLK0	Reference Clock Source
0	0	MCLK (Default)
0	1	RXCKI
1	0	RXCKO
1	1	Reserved

MUTE **SRC Output Soft Mute Function**

This bit enables or disables the SRC output soft mute function.

MUTE	Mute Function
0	Mute Disabled (Default)
1	Mute enabled; output data set to all zeros.

TRACK **SRC Digital Output Attenuation Tracking**

This bit enables or disables left and right channel attenuation tracking.

TRACK	Output Attenuation Tracking
0	Tracking Disabled (Default) The Left and Right channel attenuation is programmed separately using registers 0x30 and 0x31, respectively.
1	Tracking Enabled The Left channel attenuation setting is also used for the Right channel. The Right channel tracks the Left channel setting.

Register 2E: SRC Control Register 2

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	AUTODEM	DEM1	DEM0	DDN	IGRP1	IGRP0

IGRP[1:0] **SRC Interpolation Filter Group Delay**

These bits select the interpolation filter group delay by configuring the number of samples which are pre-buffered prior to the re-sampler function.

IGRP1	IGRP0	Number of Samples Pre-Buffered
0	0	64 Samples (Default)
0	1	32 Samples
1	0	16 Samples
1	1	8 Samples

DDN **SRC Decimation Filter/Direct Down-Sampling Function**

This bit selects the mode of the decimation function, either true decimation filter or direct down-sampling without filtering.

DDN	Decimation Function
0	Decimation Filter (Default)
1	Direct Down Sampling

Note: Direct down-sampling should only be used when the output sampling rate is higher than the input sampling rate. When the output sampling rate is equal to or lower than the input sampling rate, the Decimation Filter must be used in order to avoid aliasing.

DEM[1:0] **Digital De-Emphasis Filter, Manual Configuration**

These bits are utilized to enable or disable the digital de-emphasis filter manually. The de-emphasis filter is intended to process 50/15µs pre-emphasized audio material at the following input sampling rates:

DEM1	DEM0	De-Emphasis Filter Function
0	0	De-Emphasis Disabled (Default)
0	1	De-Emphasis Enabled for f_S = 48kHz
1	0	De-Emphasis Enabled for f_S = 44.1kHz
1	1	De-Emphasis Enabled for f_S = 32kHz

Note: When the AUTODEM bit is set to 1, the setting of the DEM0 and DEM1 bits are ignored.

AUTODEM **Automatic De-Emphasis Configuration**

This bit enables or disables the automatic de-emphasis function, which monitors the channel status bits from the DIR function block and determines whether de-emphasis is enabled and for which sampling frequency. This function is valid for only 50/15µs pre-emphasized data and one of the three supported sampling rates (32kHz, 44.1kHz, or 48kHz).

AUTODEM	Automatic De-Emphasis Function
0	Disabled (Default)
1	Enabled

Register 2F: SRC Control Register 3

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
OWL1	OWL0	0	0	0	0	0	0

OWL[1:0] **SRC Output Word Length**

These bits select the word length for the SRC output data. The word length reduction is performed by utilizing triangular PDF dithering.

OWL1	OWL0	SRC Output Word Length
0	0	24 Bits (Default)
0	1	20 Bits
1	0	18 Bits
1	1	16 Bits

Note: When the SRC is selected as the output data source for Port A or B and the data format for the port is set to Right-Justified, the proper word length must be selected in the Port A or B control registers such that it matches the corresponding SRC output data word length set by the OWL0 and OWL1 bits.

Register 30: SRC Control Register 4

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

These bits are utilized to configure the SRC digital output attenuation for the Left Channel when the TRACK bit in register 0x2D is set to 0. The attenuation setting for the Left channel also applies to the Right channel when TRACK bit in register 0x2D is set to 1.
Output Attenuation (dB) = –N ɹ0.5, where N = $AL[7:0]_{DEC}$.

Register 31: SRC Control Register 5

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

These bits are utilized to configure the SRC digital output attenuation for the Right Channel when the TRACK bit in register 0x2D is set to 0.
Output Attenuation (dB) = –N ɹ0.5, where N = $AR[7:0]_{DEC}$.

Register 32: SRC Ratio Readback Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
SRI4	SRI3	SRI2	SRI1	SRI0	SRF10	SRF9	SRF8

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Register 33: SRC Ratio Readback Register (Read-Only)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
SRF7	SRF6	SRF5	SRF4	SRF3	SRF2	SRF1	SRF0

SRI[4:0] **Integer Part of the Input-to-Output Sampling Ratio**

SRF[10:0] **Fractional Part of the Input-to-Output Sampling Ratio**

In order to properly read back the ratio, these registers must be read back in sequence, starting with register 0x32.

Register 7F: Page Selection Register

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	0	0	0	0	PAGE1	PAGE0

PAGE[1:0] **Page Selection**

These bits are utilized to select one of three register pages for write and/or read access via the SPI or I^2C serial host interface. The Page Selection Register is present on every register page at address 0x7F, allowing movement between pages as necessary.

PAGE1	PAGE0	Register/Buffer Page Selection
0	0	Page 0, Control and Status Registers (Default)
0	1	Page 1, DIR Channel Status and User Data Buffers
1	0	Page 2, DIT Channel Status and User Data Buffers
1	1	Page 3, Reserved

CHANNEL STATUS AND USER DATA BUFFER MAPS

Table 5 through Table 8 show the buffer maps for the DIR and DIT channel status and user data buffers.

For Table 5, the channel status byte definitions are dependent on the transmission mode, either Professional or Consumer. Bit 0 of Byte 0 defines the transmission mode, 0 for Consumer mode, and 1 for Professional mode. This is applicable for Table 5 and Table 6.

For Table 7, the channel status byte definitions are dependent on the transmission mode, either Professional or Consumer. Bit 0 of Byte 0 defines the transmission mode, 0 for Consumer mode, and 1 for Professional mode. In Professional mode, Byte 23 for each channel is reserved for CRC data, which is automatically calculated and encoded by the DIT. There is no need to program Byte 23 for either channel in Professional mode.

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Table 5. DIR Channel Status Data Buffer Map (Register Page 1)

ADDRESS (Hex)	CHANNEL	BYTE	BIT 0 (MSB)	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
0	1	0	D0	D1	D2	D3	D4	D5	D6	D7
1	2	0	D0	D1	D2	D3	D4	D5	D6	D7
2	1	1	D0	D1	D2	D3	D4	D5	D6	D7
3	2	1	D0	D1	D2	D3	D4	D5	D6	D7
4	1	2	D0	D1	D2	D3	D4	D5	D6	D7
5	2	2	D0	D1	D2	D3	D4	D5	D6	D7
6	1	3	D0	D1	D2	D3	D4	D5	D6	D7
7	2	3	D0	D1	D2	D3	D4	D5	D6	D7
8	1	4	D0	D1	D2	D3	D4	D5	D6	D7
9	2	4	D0	D1	D2	D3	D4	D5	D6	D7
A	1	5	D0	D1	D2	D3	D4	D5	D6	D7
B	2	5	D0	D1	D2	D3	D4	D5	D6	D7
C	1	6	D0	D1	D2	D3	D4	D5	D6	D7
D	2	6	D0	D1	D2	D3	D4	D5	D6	D7
E	1	7	D0	D1	D2	D3	D4	D5	D6	D7
F	2	7	D0	D1	D2	D3	D4	D5	D6	D7
10	1	8	D0	D1	D2	D3	D4	D5	D6	D7
11	2	8	D0	D1	D2	D3	D4	D5	D6	D7
12	1	9	D0	D1	D2	D3	D4	D5	D6	D7
13	2	9	D0	D1	D2	D3	D4	D5	D6	D7
14	1	10	D0	D1	D2	D3	D4	D5	D6	D7
15	2	10	D0	D1	D2	D3	D4	D5	D6	D7
16	1	11	D0	D1	D2	D3	D4	D5	D6	D7
17	2	11	D0	D1	D2	D3	D4	D5	D6	D7
18	1	12	D0	D1	D2	D3	D4	D5	D6	D7
19	2	12	D0	D1	D2	D3	D4	D5	D6	D7
1A	1	13	D0	D1	D2	D3	D4	D5	D6	D7
1B	2	13	D0	D1	D2	D3	D4	D5	D6	D7
1C	1	14	D0	D1	D2	D3	D4	D5	D6	D7
1D	2	14	D0	D1	D2	D3	D4	D5	D6	D7
1E	1	15	D0	D1	D2	D3	D4	D5	D6	D7
1F	2	15	D0	D1	D2	D3	D4	D5	D6	D7
20	1	16	D0	D1	D2	D3	D4	D5	D6	D7
21	2	16	D0	D1	D2	D3	D4	D5	D6	D7
22	1	17	D0	D1	D2	D3	D4	D5	D6	D7
23	2	17	D0	D1	D2	D3	D4	D5	D6	D7
24	1	18	D0	D1	D2	D3	D4	D5	D6	D7
25	2	18	D0	D1	D2	D3	D4	D5	D6	D7
26	1	19	D0	D1	D2	D3	D4	D5	D6	D7
27	2	19	D0	D1	D2	D3	D4	D5	D6	D7
28	1	20	D0	D1	D2	D3	D4	D5	D6	D7
29	2	20	D0	D1	D2	D3	D4	D5	D6	D7
2A	1	21	D0	D1	D2	D3	D4	D5	D6	D7
2B	2	21	D0	D1	D2	D3	D4	D5	D6	D7
2C	1	22	D0	D1	D2	D3	D4	D5	D6	D7
2D	2	22	D0	D1	D2	D3	D4	D5	D6	D7
2E	1	23	D0	D1	D2	D3	D4	D5	D6	D7
2F	2	23	D0	D1	D2	D3	D4	D5	D6	D7

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Table 6. DIR User Data Buffer Map (Register Page 1)

ADDRESS (Hex)	CHANNEL	BYTE	BIT 0 (MSB)	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
40	1	0	D0	D1	D2	D3	D4	D5	D6	D7
41	2	0	D0	D1	D2	D3	D4	D5	D6	D7
42	1	1	D0	D1	D2	D3	D4	D5	D6	D7
43	2	1	D0	D1	D2	D3	D4	D5	D6	D7
44	1	2	D0	D1	D2	D3	D4	D5	D6	D7
45	2	2	D0	D1	D2	D3	D4	D5	D6	D7
46	1	3	D0	D1	D2	D3	D4	D5	D6	D7
47	2	3	D0	D1	D2	D3	D4	D5	D6	D7
48	1	4	D0	D1	D2	D3	D4	D5	D6	D7
49	2	4	D0	D1	D2	D3	D4	D5	D6	D7
4A	1	5	D0	D1	D2	D3	D4	D5	D6	D7
4B	2	5	D0	D1	D2	D3	D4	D5	D6	D7
4C	1	6	D0	D1	D2	D3	D4	D5	D6	D7
4D	2	6	D0	D1	D2	D3	D4	D5	D6	D7
4E	1	7	D0	D1	D2	D3	D4	D5	D6	D7
4F	2	7	D0	D1	D2	D3	D4	D5	D6	D7
50	1	8	D0	D1	D2	D3	D4	D5	D6	D7
51	2	8	D0	D1	D2	D3	D4	D5	D6	D7
52	1	9	D0	D1	D2	D3	D4	D5	D6	D7
53	2	9	D0	D1	D2	D3	D4	D5	D6	D7
54	1	10	D0	D1	D2	D3	D4	D5	D6	D7
55	2	10	D0	D1	D2	D3	D4	D5	D6	D7
56	1	11	D0	D1	D2	D3	D4	D5	D6	D7
57	2	11	D0	D1	D2	D3	D4	D5	D6	D7
58	1	12	D0	D1	D2	D3	D4	D5	D6	D7
59	2	12	D0	D1	D2	D3	D4	D5	D6	D7
5A	1	13	D0	D1	D2	D3	D4	D5	D6	D7
5B	2	13	D0	D1	D2	D3	D4	D5	D6	D7
5C	1	14	D0	D1	D2	D3	D4	D5	D6	D7
5D	2	14	D0	D1	D2	D3	D4	D5	D6	D7
5E	1	15	D0	D1	D2	D3	D4	D5	D6	D7
5F	2	15	D0	D1	D2	D3	D4	D5	D6	D7
60	1	16	D0	D1	D2	D3	D4	D5	D6	D7
61	2	16	D0	D1	D2	D3	D4	D5	D6	D7
62	1	17	D0	D1	D2	D3	D4	D5	D6	D7
63	2	17	D0	D1	D2	D3	D4	D5	D6	D7
64	1	18	D0	D1	D2	D3	D4	D5	D6	D7
65	2	18	D0	D1	D2	D3	D4	D5	D6	D7
66	1	19	D0	D1	D2	D3	D4	D5	D6	D7
67	2	19	D0	D1	D2	D3	D4	D5	D6	D7
68	1	20	D0	D1	D2	D3	D4	D5	D6	D7
69	2	20	D0	D1	D2	D3	D4	D5	D6	D7
6A	1	21	D0	D1	D2	D3	D4	D5	D6	D7
6B	2	21	D0	D1	D2	D3	D4	D5	D6	D7
6C	1	22	D0	D1	D2	D3	D4	D5	D6	D7
6D	2	22	D0	D1	D2	D3	D4	D5	D6	D7
6E	1	23	D0	D1	D2	D3	D4	D5	D6	D7
6F	2	23	D0	D1	D2	D3	D4	D5	D6	D7

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Table 7. DIT Channel Status Data Buffer Map (Register Page 2)

ADDRESS (Hex)	CHANNEL	BYTE	BIT 0 (MSB)	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
0	1	0	D0	D1	D2	D3	D4	D5	D6	D7
1	2	0	D0	D1	D2	D3	D4	D5	D6	D7
2	1	1	D0	D1	D2	D3	D4	D5	D6	D7
3	2	1	D0	D1	D2	D3	D4	D5	D6	D7
4	1	2	D0	D1	D2	D3	D4	D5	D6	D7
5	2	2	D0	D1	D2	D3	D4	D5	D6	D7
6	1	3	D0	D1	D2	D3	D4	D5	D6	D7
7	2	3	D0	D1	D2	D3	D4	D5	D6	D7
8	1	4	D0	D1	D2	D3	D4	D5	D6	D7
9	2	4	D0	D1	D2	D3	D4	D5	D6	D7
A	1	5	D0	D1	D2	D3	D4	D5	D6	D7
B	2	5	D0	D1	D2	D3	D4	D5	D6	D7
C	1	6	D0	D1	D2	D3	D4	D5	D6	D7
D	2	6	D0	D1	D2	D3	D4	D5	D6	D7
E	1	7	D0	D1	D2	D3	D4	D5	D6	D7
F	2	7	D0	D1	D2	D3	D4	D5	D6	D7
10	1	8	D0	D1	D2	D3	D4	D5	D6	D7
11	2	8	D0	D1	D2	D3	D4	D5	D6	D7
12	1	9	D0	D1	D2	D3	D4	D5	D6	D7
13	2	9	D0	D1	D2	D3	D4	D5	D6	D7
14	1	10	D0	D1	D2	D3	D4	D5	D6	D7
15	2	10	D0	D1	D2	D3	D4	D5	D6	D7
16	1	11	D0	D1	D2	D3	D4	D5	D6	D7
17	2	11	D0	D1	D2	D3	D4	D5	D6	D7
18	1	12	D0	D1	D2	D3	D4	D5	D6	D7
19	2	12	D0	D1	D2	D3	D4	D5	D6	D7
1A	1	13	D0	D1	D2	D3	D4	D5	D6	D7
1B	2	13	D0	D1	D2	D3	D4	D5	D6	D7
1C	1	14	D0	D1	D2	D3	D4	D5	D6	D7
1D	2	14	D0	D1	D2	D3	D4	D5	D6	D7
1E	1	15	D0	D1	D2	D3	D4	D5	D6	D7
1F	2	15	D0	D1	D2	D3	D4	D5	D6	D7
20	1	16	D0	D1	D2	D3	D4	D5	D6	D7
21	2	16	D0	D1	D2	D3	D4	D5	D6	D7
22	1	17	D0	D1	D2	D3	D4	D5	D6	D7
23	2	17	D0	D1	D2	D3	D4	D5	D6	D7
24	1	18	D0	D1	D2	D3	D4	D5	D6	D7
25	2	18	D0	D1	D2	D3	D4	D5	D6	D7
26	1	19	D0	D1	D2	D3	D4	D5	D6	D7
27	2	19	D0	D1	D2	D3	D4	D5	D6	D7
28	1	20	D0	D1	D2	D3	D4	D5	D6	D7
29	2	20	D0	D1	D2	D3	D4	D5	D6	D7
2A	1	21	D0	D1	D2	D3	D4	D5	D6	D7
2B	2	21	D0	D1	D2	D3	D4	D5	D6	D7
2C	1	22	D0	D1	D2	D3	D4	D5	D6	D7
2D	2	22	D0	D1	D2	D3	D4	D5	D6	D7
2E	1	23	D0	D1	D2	D3	D4	D5	D6	D7
2F	2	23	D0	D1	D2	D3	D4	D5	D6	D7

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Table 8. DIT User Data Buffer Map (Register Page 2)

ADDRESS (Hex)	CHANNEL	BYTE	BIT 0 (MSB)	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
40	1	0	D0	D1	D2	D3	D4	D5	D6	D7
41	2	0	D0	D1	D2	D3	D4	D5	D6	D7
42	1	1	D0	D1	D2	D3	D4	D5	D6	D7
43	2	1	D0	D1	D2	D3	D4	D5	D6	D7
44	1	2	D0	D1	D2	D3	D4	D5	D6	D7
45	2	2	D0	D1	D2	D3	D4	D5	D6	D7
46	1	3	D0	D1	D2	D3	D4	D5	D6	D7
47	2	3	D0	D1	D2	D3	D4	D5	D6	D7
48	1	4	D0	D1	D2	D3	D4	D5	D6	D7
49	2	4	D0	D1	D2	D3	D4	D5	D6	D7
4A	1	5	D0	D1	D2	D3	D4	D5	D6	D7
4B	2	5	D0	D1	D2	D3	D4	D5	D6	D7
4C	1	6	D0	D1	D2	D3	D4	D5	D6	D7
4D	2	6	D0	D1	D2	D3	D4	D5	D6	D7
4E	1	7	D0	D1	D2	D3	D4	D5	D6	D7
4F	2	7	D0	D1	D2	D3	D4	D5	D6	D7
50	1	8	D0	D1	D2	D3	D4	D5	D6	D7
51	2	8	D0	D1	D2	D3	D4	D5	D6	D7
52	1	9	D0	D1	D2	D3	D4	D5	D6	D7
53	2	9	D0	D1	D2	D3	D4	D5	D6	D7
54	1	10	D0	D1	D2	D3	D4	D5	D6	D7
55	2	10	D0	D1	D2	D3	D4	D5	D6	D7
56	1	11	D0	D1	D2	D3	D4	D5	D6	D7
57	2	11	D0	D1	D2	D3	D4	D5	D6	D7
58	1	12	D0	D1	D2	D3	D4	D5	D6	D7
59	2	12	D0	D1	D2	D3	D4	D5	D6	D7
5A	1	13	D0	D1	D2	D3	D4	D5	D6	D7
5B	2	13	D0	D1	D2	D3	D4	D5	D6	D7
5C	1	14	D0	D1	D2	D3	D4	D5	D6	D7
5D	2	14	D0	D1	D2	D3	D4	D5	D6	D7
5E	1	15	D0	D1	D2	D3	D4	D5	D6	D7
5F	2	15	D0	D1	D2	D3	D4	D5	D6	D7
60	1	16	D0	D1	D2	D3	D4	D5	D6	D7
61	2	16	D0	D1	D2	D3	D4	D5	D6	D7
62	1	17	D0	D1	D2	D3	D4	D5	D6	D7
63	2	17	D0	D1	D2	D3	D4	D5	D6	D7
64	1	18	D0	D1	D2	D3	D4	D5	D6	D7
65	2	18	D0	D1	D2	D3	D4	D5	D6	D7
66	1	19	D0	D1	D2	D3	D4	D5	D6	D7
67	2	19	D0	D1	D2	D3	D4	D5	D6	D7
68	1	20	D0	D1	D2	D3	D4	D5	D6	D7
69	2	20	D0	D1	D2	D3	D4	D5	D6	D7
6A	1	21	D0	D1	D2	D3	D4	D5	D6	D7
6B	2	21	D0	D1	D2	D3	D4	D5	D6	D7
6C	1	22	D0	D1	D2	D3	D4	D5	D6	D7
6D	2	22	D0	D1	D2	D3	D4	D5	D6	D7
6E	1	23	D0	D1	D2	D3	D4	D5	D6	D7
6F	2	23	D0	D1	D2	D3	D4	D5	D6	D7

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REFERENCE DOCUMENTS

Throughout this data sheet, various standards and documents are repeatedly cited as references. Sources for these documents are listed here so that the reader may obtain the documents for further study.

Audio Engineering Society (AES) standards documents, including the AES3, AES11, AES18, and related specifications are available from the AES web site: http://www.aes.org.

International Electrotechnical Committee (IEC) standards, including the IEC60958 and IEC61937 are available from the IEC web site: http://www.iec.ch; or the ANSI web site: http://www.ansi.org.

The EIAJ CP-1212 (formerly CP-1201) standard is available from the Japanese Electronics and Information Technologies Industries Association (JEITA): http://www.jeita.or.jp/english.

The Philips I^2C bus specification is available from Philips: http://www.philips.com.The version utilized as a reference for this product is Version 2.1, published in January 2000.

Several papers regarding balanced and unbalanced transformer-coupled digital audio interfaces have been published and presented at past AES conventions by Jon D. Paul of Scientific Conversion, Inc. These papers are available for download from: http://www.scientificconversion.com.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REV	PAGE	SECTION	DESCRIPTION
4/06	B	—	—	Changed from Product Preview to Production Data.
		12	Typical Characteristics	Corrected spelling of *Typical.*
		35	Product Overview, Asynchronous Sample Rate Converter Operation	Figure 74: Corrected alignment of text.
		40	Product Overview, Interrupt Output	Figure 79: Changed reference to multiple SRC4392 devices. Corrected spelling error.
		45	Applications Information, Receiver Input Interfacing	Figure 85, Figure 86: Corrected spelling errors.
		47	Applications Information, Transmitter Output Interfacing	Figure 89, Figure 90: Corrected spelling errors. Figure 90: Renamed *Optical Receiver* block to *Optical Transmitter*.
		49	Applications Information, Control Registers	Changed wording in paragraph describing Control Registers to accurately explain which register addresses are reserved for factory or future use.
		Global	—	Corrected punctuation errors: *AES3-encoded*, *transformer-coupled*.

Changes from Revision B (April 2006) to Revision C **Page**

- Added U.S. patent number to front page. 1

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SRC4382IPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SRC4382I
SRC4382IPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SRC4382I
SRC4382IPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SRC4382I
SRC4382IPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SRC4382I
SRC4382IPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SRC4382I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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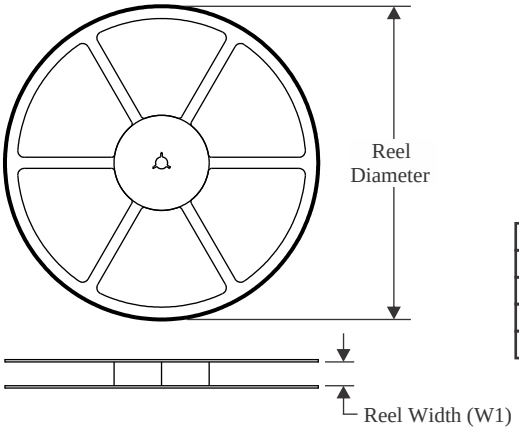
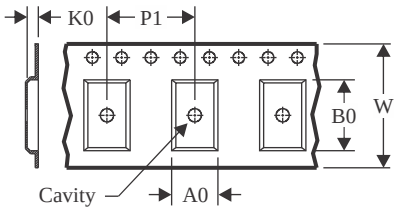
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

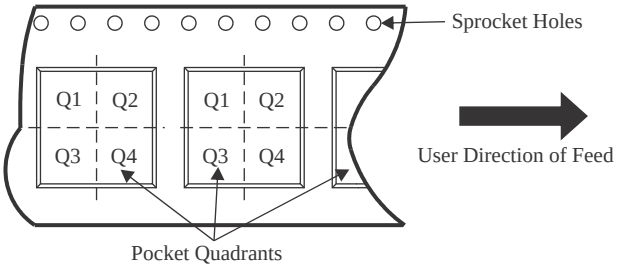


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

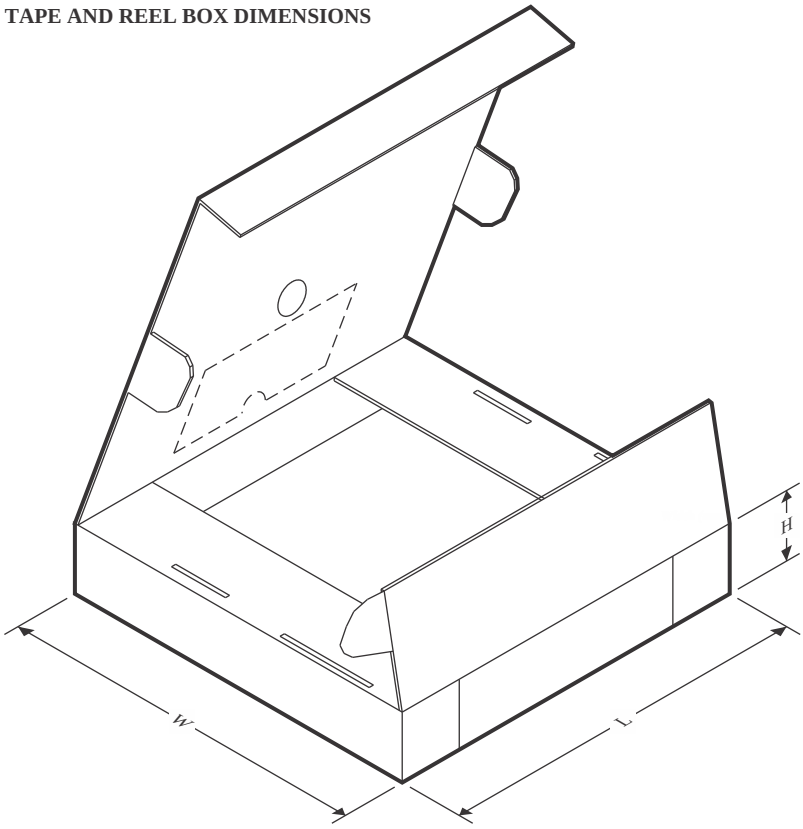
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SRC4382IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

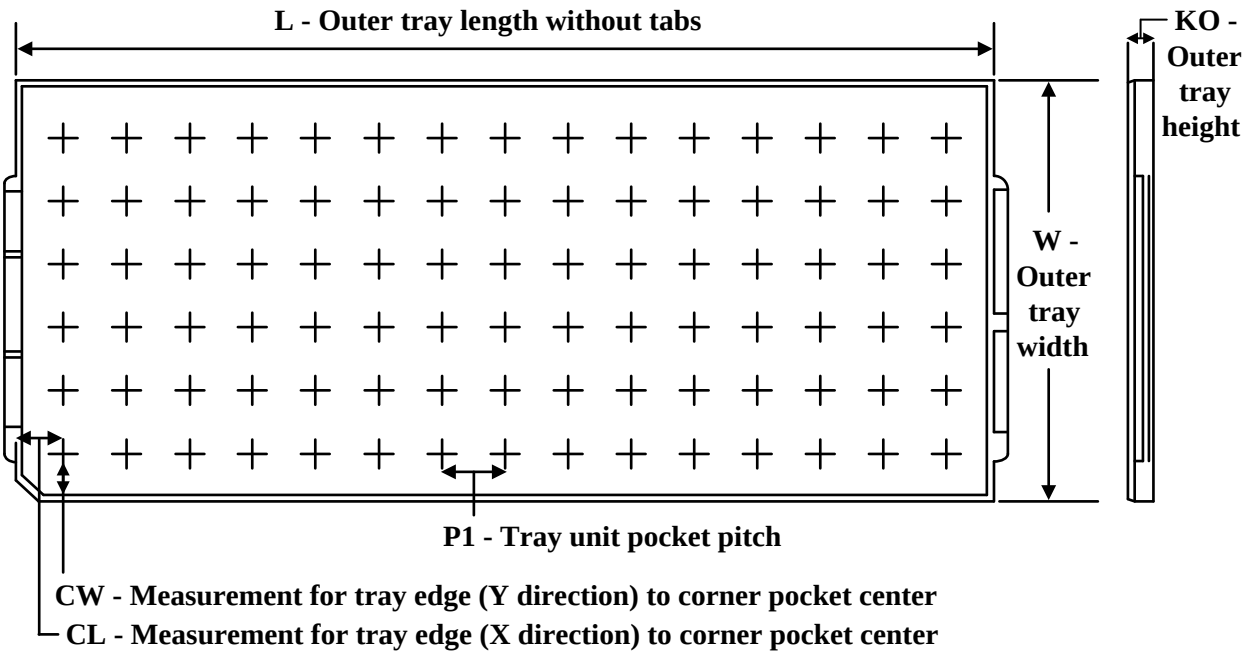
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SRC4382IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0

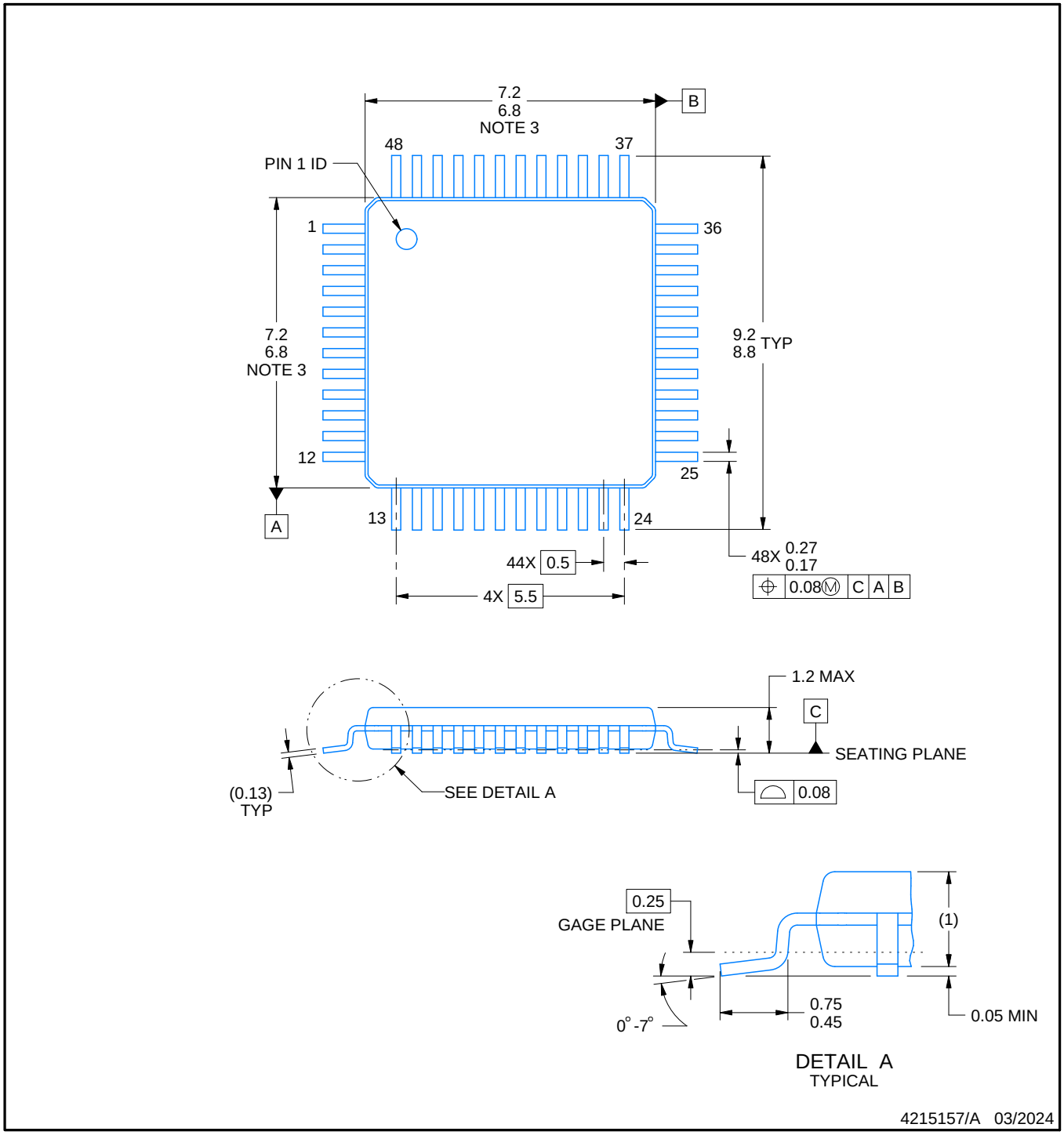
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

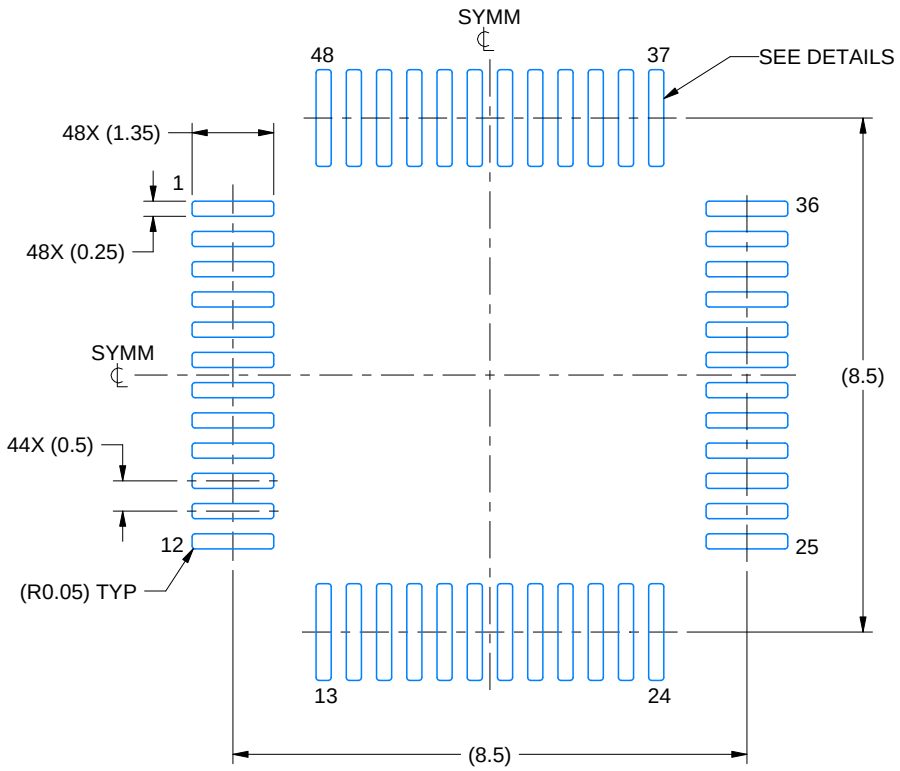
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SRC4382IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
SRC4382IPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
SRC4382IPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

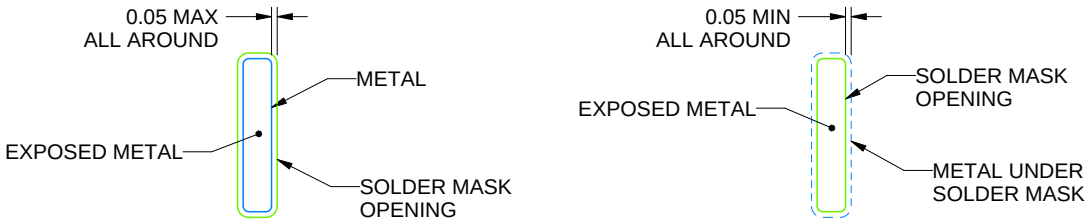


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

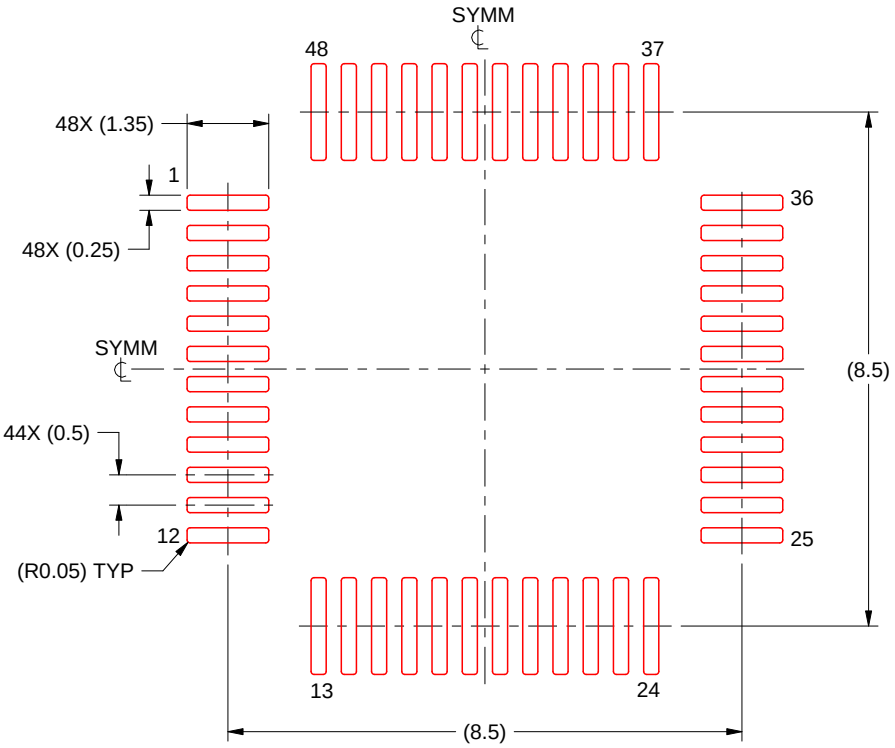


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025