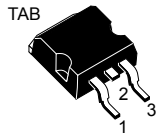
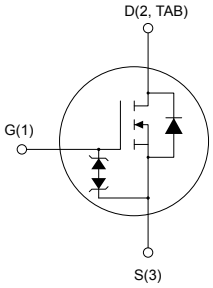
STB24N60M6

Datasheet

N-channel 600 V, 162 mΩ typ., 17 A, MDmesh M6 Power MOSFET in a D²PAK package



D²PAK



AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB24N60M6	600 V	190 mΩ	17 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link
STB24N60M6

Product summary	
Order code	STB24N60M6
Marking	24N60M6
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	17	A
	Drain current (continuous) at T_C = 100 °C	10.7	
I_{DM}(1)	Drain current (pulsed)	52.5	A
P_{TOT}	Total power dissipation at T_C = 25 °C	130	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 17 A, di/dt = 400 A/µs, V_{DS} < $V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.96	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{Jmax})	3.2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	250	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 8.5 A, V_{GS} = 10 V		162	190	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	960	-	pF
C_{oss}	Output capacitance		-	76	-	
C_{rss}	Reverse transfer capacitance		-	4.5	-	
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	181	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 17 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	23	-	nC
Q_{gs}	Gate-source charge		-	4.8	-	
Q_{gd}	Gate-drain charge		-	12.8	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	17.7	-	ns
t_r	Rise time		-	32	-	
$t_{d(off)}$	Turn-off delay time		-	38.3	-	
t_f	Fall time		-	9	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
I_{SDM}(1)	Source-drain current (pulsed)		-		52.5	A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	225		ns
Q_{rr}	Reverse recovery charge		-	2.3		µC
I_{RRM}	Reverse recovery current		-	20.4		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	387		ns
Q_{rr}	Reverse recovery charge		-	3.85		µC
I_{RRM}	Reverse recovery current		-	25.1		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

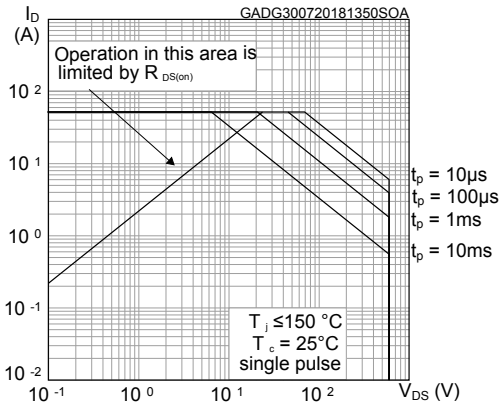


Figure 2. Thermal impedance

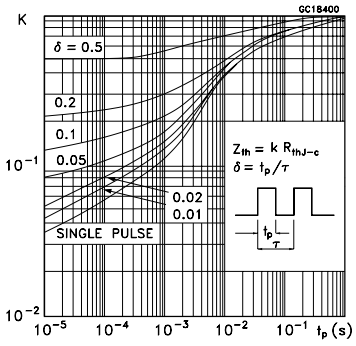


Figure 3. Output characteristics

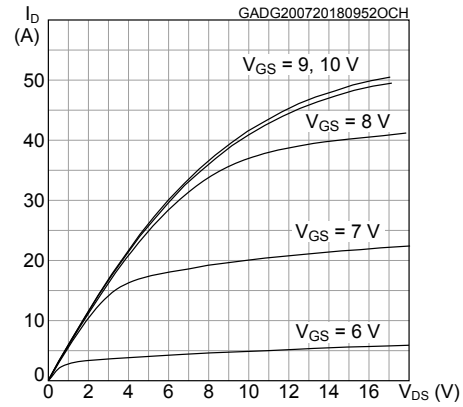


Figure 4. Transfer characteristics

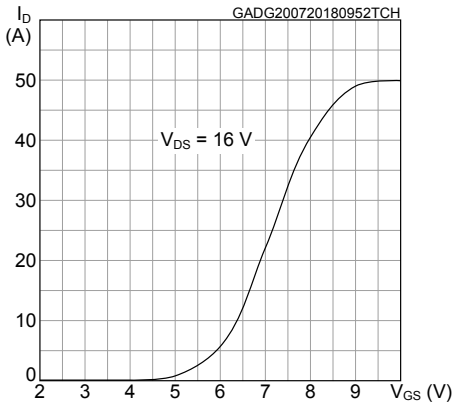


Figure 5. Gate charge vs gate-source voltage

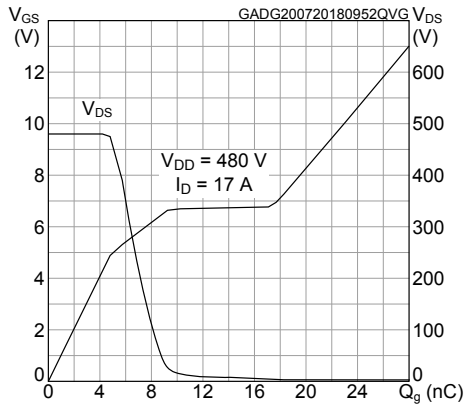


Figure 6. Static drain-source on-resistance

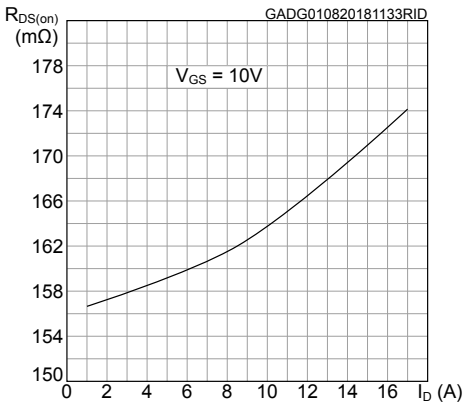


Figure 7. Capacitance variations

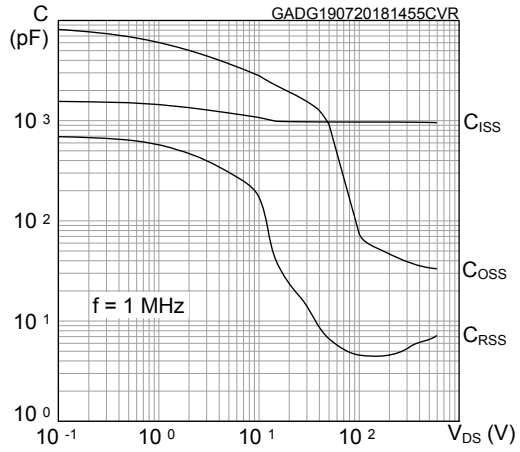


Figure 8. Output capacitance stored energy

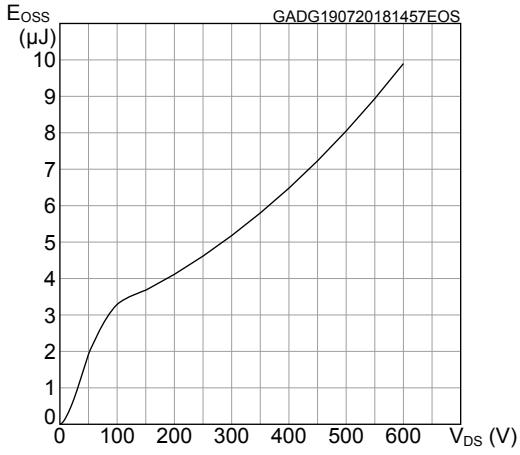


Figure 9. Normalized gate threshold voltage vs temperature

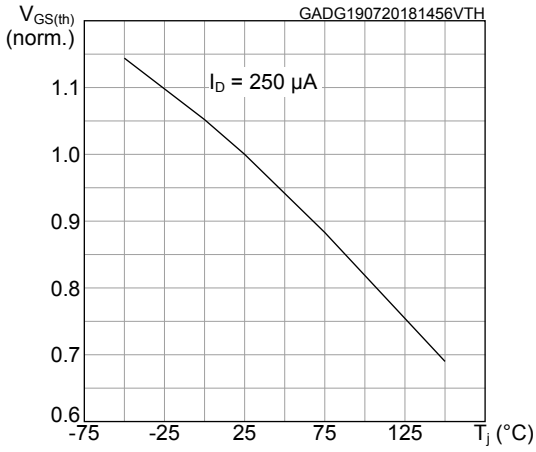


Figure 10. Normalized on-resistance vs temperature

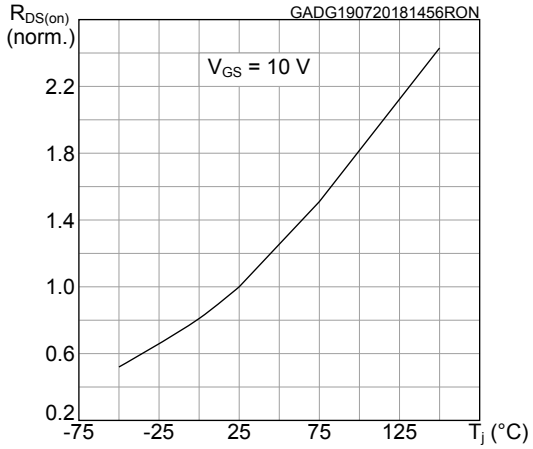


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

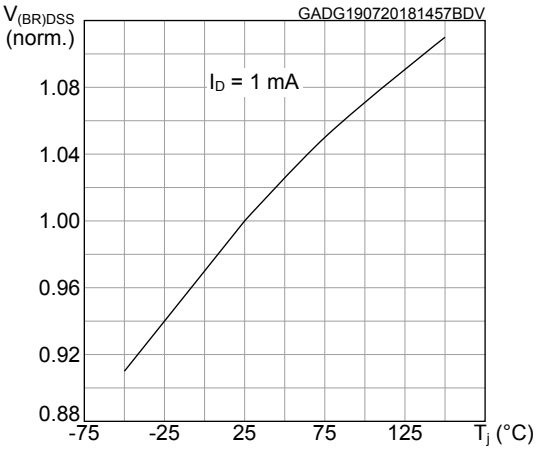
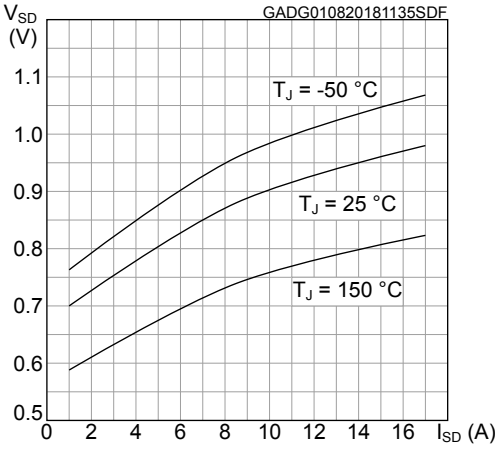
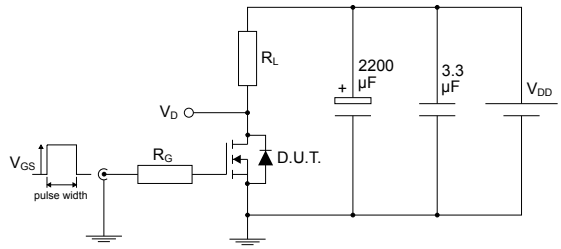


Figure 12. Source-drain diode forward characteristics



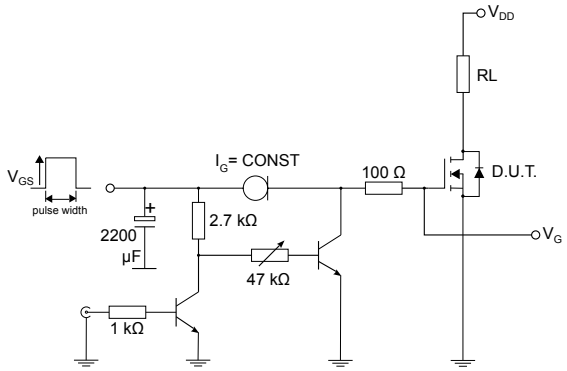
3 Test circuits

Figure 13. Test circuit for resistive load switching times



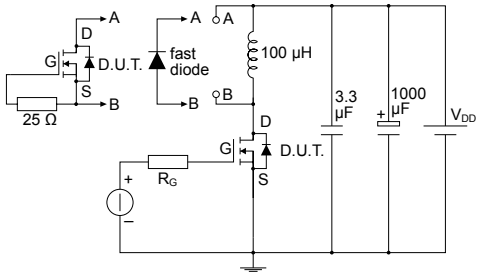
AM01468v1

Figure 14. Test circuit for gate charge behavior



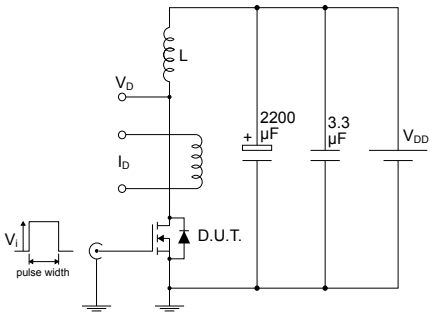
AM01469v10

Figure 15. Test circuit for inductive load switching and diode recovery times



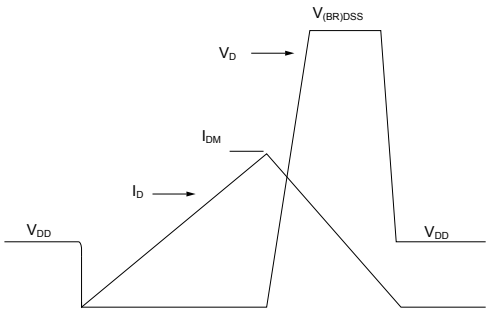
AM01470v1

Figure 16. Unclamped inductive load test circuit



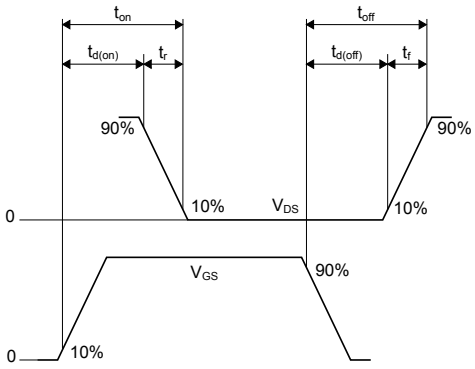
AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK package information

Figure 19. **D²PAK (TO-263) type A package outline**

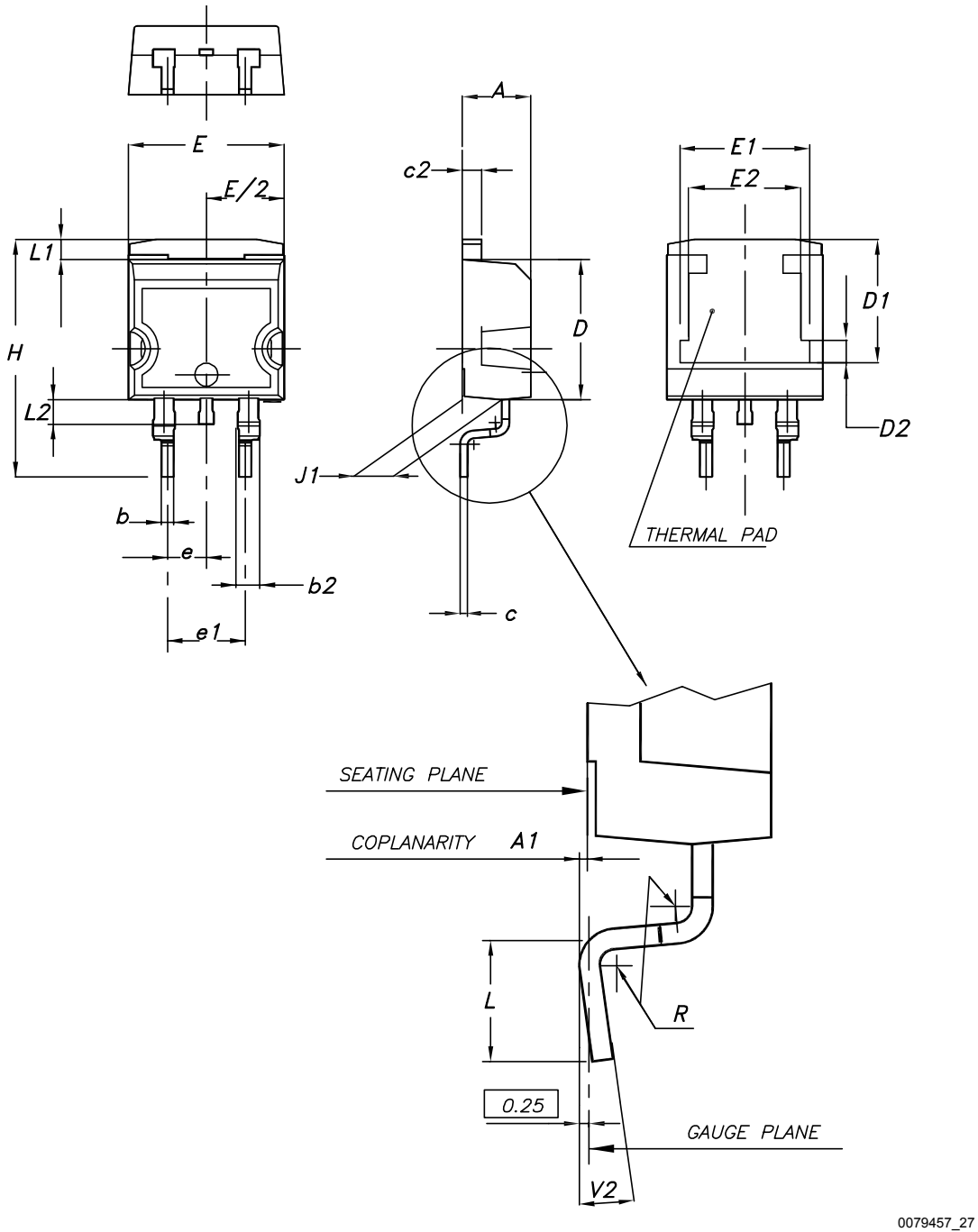
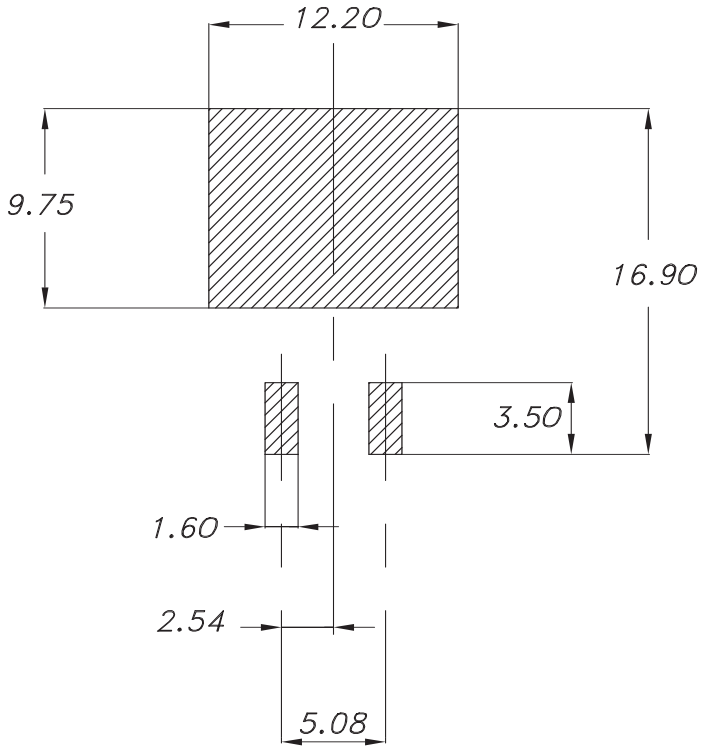


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

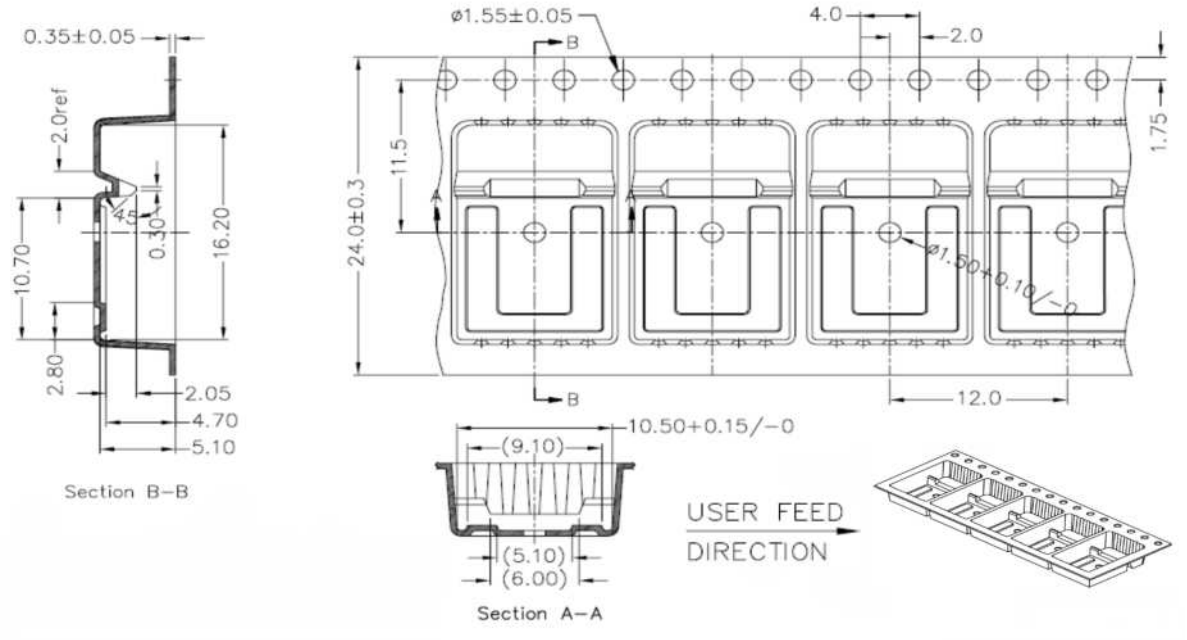
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 21. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. **Document revision history**

Date	Version	Changes
06-Aug-2018	1	Initial release.
14-Jul-2025	2	Updated Section 4.1: D²PAK (TO-263) type A package information. Updated Section 4.2: D²PAK packing information.

Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 7
4 **Package information** 8
4.1 D²PAK package information 8
4.2 D²PAK packing information 10
Revision history 11

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved