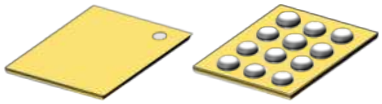
STBC15

Datasheet

Ultra-low current consumption linear battery charger



QFN12 1.7 x 2.0



Flip-chip12

Maturity status link
STBC15

Features

- Charges thin film battery with CC-CV algorithm
- L version suitable for Li-Ion batteries
- Charging current up to 40 mA (selectable by dedicated pins)
- 250 nA battery leakage current
- Reverse current protection from battery to supply input
- Programmable floating voltage with 0.5% accuracy
- Battery overcurrent protection
- Battery over-discharge protection switch totally disconnects battery for cell durability
- Shelf-mode supported, no battery mechanical switch needed
- Power-Good open-drain output
- Valid source open drain output
- Peak mode input to avoid over-discharge false triggering
- Available packages:
  - QFN12 1.7 x 2.0 mm, thickness 0.55 mm max.
  - Flip-chip12 1.1 x 1.4 mm, 300 µm pitch

Applications

- Fitness portable Internet of Things
- Energy harvesting application
- Smart cards
- Wireless sensor nodes
- Portable health care devices
- Fitness and wellness wearable devices

Description

The STBC15 is a linear charger thin film battery with a maximum charging current of 40 mA. The device uses a CC/CV algorithm to charge the battery. Thanks to the ultra-low consumption architecture, the charger is suitable for low-capacity cells such as thin film batteries and can use low energy sources such as energy harvesters. A 5 V input like a standard USB port can be used as a voltage source as well. A specific version (-L) is available to charge Li-Ion cells.

The STBC15 integrates an over-discharge and overcurrent protection circuitry to prevent the battery from being damaged under fault conditions. The floating voltage value can be set to four different values by using dedicated selection inputs. A higher set of floating voltages, suitable for Li-Ion batteries, is available in the -L version of the product. A dedicated pin allows the device to be set in shelf-mode. In this condition, the STBC15 consumes less than 10 nA, thus not discharging the battery before the final device is activated by the end user. The ultra-low power architecture allows the STBC15 to consume less than 250 nA when the input power source is removed and less than 10 nA in over-discharge-mode.

The device is available in a (1.7 × 2.0 mm) 12-lead QFN package, 400 µm pitch, 0.55 mm max. thickness or in Flip-chip 1.1 x 1.4 mm 12 bumps 300 µm pitch.

1 Application schematic

Figure 1. STBC15 application schematic

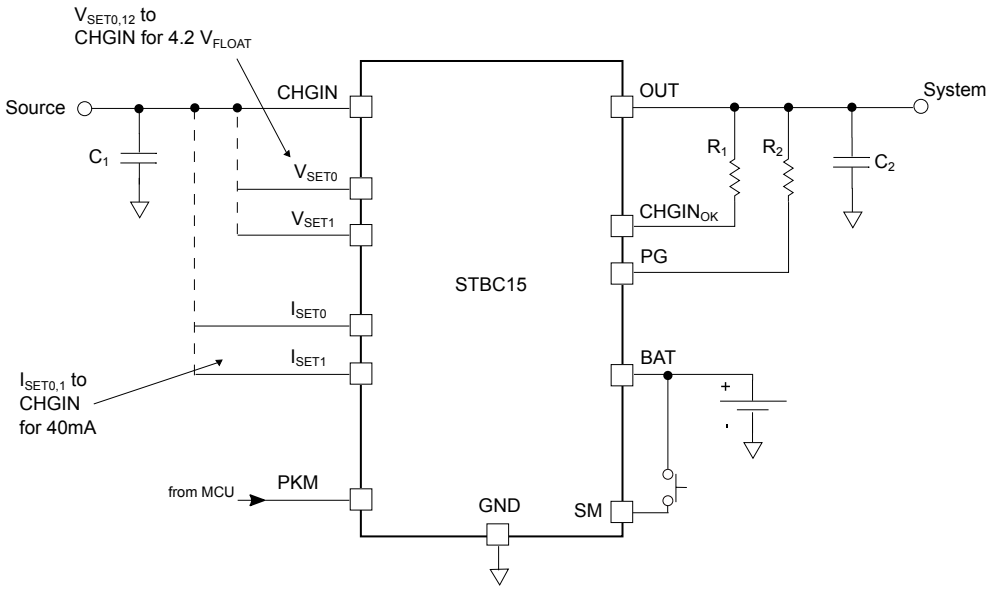


Table 1. Typical bill of material (BOM)

Symbol	Value	Description	Note
C1	10 µF (16 V)	Input supply voltage capacitor	Ceramic type
C2	10 µF (10 V)	System output capacitor	Ceramic type
R1, R2	10 kΩ	Pull-up resistors	Film type

2 Pin configuration

Figure 2. Pin connection (top through view)

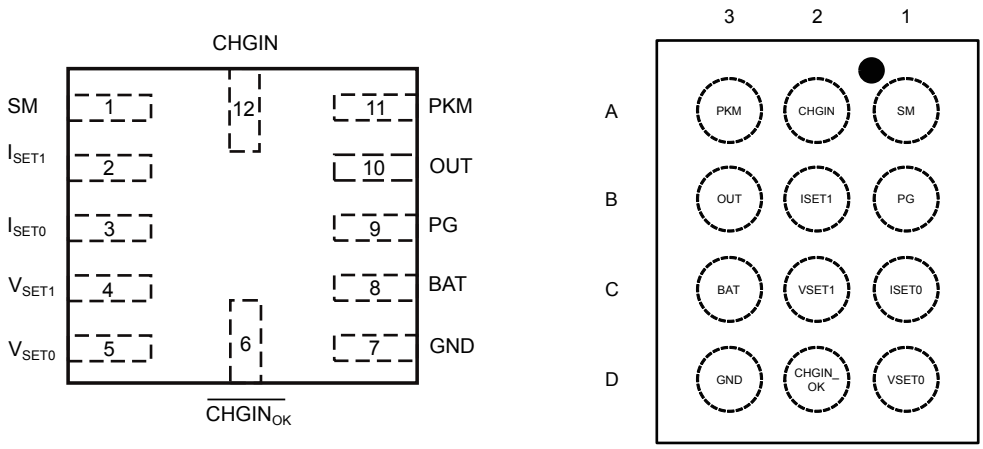


Table 2. Pin description

Bump		QFN12	Flip-chip12	Description
Power	CHGIN	12	A2	Input supply voltage. Bypass this pin to ground with a 10 µF capacitor
	BAT	8	C3	Battery positive terminal. Bypass this pin to GND with a 4.7 µF ceramic capacitor
	OUT	10	B3	System output. Bypass this pin to ground with 1 µF ceramic capacitor
	GND	7	D3	Ground
Programming	V_{SET0}	5	D1	VFLOAT selection input pins. Connect the pin to CHGIN or GND (no internal pull-up/down resistors). Pin must be tied to GND or CHGIN
	V_{SET1}	4	C2	
	I_{SET0}	3	C1	Charging current selection input pins. Pins must be tied to GND or CHGIN
	I_{SET1}	2	B2	
Digital I/Os	PKM	11	A3	Peak mode input
	PG	9	B1	Power-Good signal, active high-z open-drain output
	$\overline{CHGIN_{OK}}$	6	D2	Charging source status. It is an active high-z open drain output
	SM	1	A1	Shelf mode activation pin. Active high input with internal pull-down resistor. When high, the device enters shelf-mode

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
CHGIN	Input supply voltage pin	DC voltage	-0.3 to +7.0	V
BAT	Battery pin and system OUT pin	DC voltage	-0.3 to +5.5	V
		Non repetitive, 60 s pulse length	-0.3 to +6.0	V
OUT	Battery pin and system OUT pin	DC voltage	-0.3 to +6.0	V
$CHGIN_{OK}$, $V_{SET0,1}$, $I_{SET0,1}$, PG, SM, PKM	I/O pins	DC voltage	-0.3 to +7.0	V
ESD	Charged device model (CDM)		±500	V
	Human body model (all the others)		±2000	V
T_{AMB}	Operating ambient temperature		-40 to +85	°C
T_J	Maximum junction temperature		+125	°C
T_{STG}	Storage temperature		-65 to +150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	QFN12	Flip-chip12	Unit
R_{THJB}(1)	Junction-to-pcb board thermal resistance	100	160	°C/W

1. *Standard FR4 pcb board.*

4 Electrical characteristics

V_{CHGIN} = 5 V, V_{BAT} = 3.6 V, C_1 = 10 µF, C_2 = 10 µF, $V_{SET0,1}$ = 0 V; $I_{SET0,1}$ = 0 V, SM floating, T_A = 25 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
CHGIN	Operating input voltage	V_{float} set 4.2 V, I_{FAST} < 250 mA	V_{CHGIN_UVLO}		6.5 (1)	V
V_{BATMIN}	Minimum battery voltage		3.2			V
V_{CHGIN_UVLO}	CHGIN undervoltage lockout threshold - rising	V_{BAT} < V_{BAT_OVD}	3.3	3.5		V
$V_{CHGIN_UVLO_H}$	CHGIN undervoltage lockout hysteresis	V_{BAT} < V_{BAT_OVD}		150		mV
I_{CHARGE}	Battery charging current (CC mode)	0 V < V_{BAT} < V_{FLOAT} I_{SET0},1 = CHGIN	36	40	44	mA
		0 V < V_{BAT} < V_{FLOAT} I_{SET1} = CHGIN, I_{SET0} = GND	26	30	34	mA
		0 V < V_{BAT} < V_{FLOAT} I_{SET1} = GND, I_{SET0} = CHGIN	16	20	24	mA
		0 V < V_{BAT} < V_{FLOAT} $I_{SET0,1}$ = GND	8	10	12	mA
V_{FLOAT}	Battery float voltage (CV mode)	STBC15, I_{BAT} = 10 µA, $V_{SET0,1}$ 1 = CHGIN, T_A = 25 °C	4.180	4.2	4.221	V
		STBC15L, I_{BAT} = 10 µA, $V_{SET0,1}$ = CHGIN, T_A = 25 °C	4.378	4.4	4.422	V
	Battery float voltage (CV mode), temperature variation (1)	STBC15, I_{BAT} = 10 µA, $V_{SET0,1}$ = CHGIN, T_A = -40 to 85 °C	4.158	4.2	4.242	V
		STBC15L, I_{BAT}= 10 µA, $V_{SET0,1}$ = CHGIN, T_A= -40 to 85 °C	4.356	4.4	4.444	V
I_{CC}	IC supply current	T_A = -40 to 85 °C		580	1000	nA
I_{BAT}	Leakage on BAT pin	V_{CHGIN} = 0 V, V_{BAT} < V_{BAT_OVD}		4	10	nA
		V_{CHGIN} = 0 V, I_{OUT} = 0 A, V_{BAT} > V_{BAT_OVD}		250	380	nA
		Shelf-mode, V_{CHGIN} = 0 V, V_{BAT} = 4 V		4	10	nA
V_{BAT_OVD}	Battery over discharge disconnection threshold	STBC15, V_{CHGIN} = 0 V, I_{OUT} = 0 A, PKM = 0 (peak mode disabled)	3.15	3.25	3.3	V
		STBC15, V_{CHGIN} = 0 V, I_{OUT} = 0 A,	2.15	2.25	2.3	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BAT_OVD}	Battery over discharge disconnection threshold	PKM=1 (peak mode enabled)				V
		STBC15L, V_{CHGIN} = 0 V, I_{OUT} = 0 A, PKM = 0 or 1	2.60	2.7	2.75	
V_{BAT_FF}	Battery disconnected FF retention voltage	V_{CHGIN} = 0 V, $V_{BAT} < V_{BAT_OVD}$	1.8			V
V_{BAT_CONN}	Battery connected threshold – rising	STBC15, V_{CHGIN} = 0 V, I_{OUT} = 0 A, PKM = 0 or 1	3.98	4.1	4.22	V
		STBC15L, V_{CHGIN} = 0 V, I_{OUT} = 0 A, PKM = 0 (peak mode disabled)		3.6		V
		STBC15L, V_{CHGIN} = 0 V, I_{OUT} = 0 A, PKM=1 (peak mode enabled)		3.9		V
$V_{BAT_CONN_H}$	Battery connected threshold hysteresis			100		mV
V_{BAT_ASD}	Battery ASD threshold	V_{CHGIN}-V_{BAT}		50		mV
V_{BAT_RECHG}	Battery recharge threshold	V_{BAT} -V_{CHGIN}		170		mV
R_{IN_BAT}	Input-to-battery on-resistance			6	10	Ω
R_{DSON_M3}	M3 transistor on-resistance			3		Ω
R_{IN_SM}	Input shelf mode pull-down resistor	SM pin vs. GND		100		kΩ
I_{IN_PKM}	PKM input current leakage				0.1	nA
I_{IN_SET}	$V_{SET0,1}$, $I_{SET0,1}$ input current leakage				0.1	nA
V_{IL}	Logic low input level ($V_{SET0,1}$, $I_{SET0,1}$)	To see threshold plot in full temperature range			0.4	V
V_{IH}	Logic high input level (VSET0,1, ISET0,1)		1.6		V_{CHGIN}	V
V_{IL2}	Logic low input level (SM, PKM)				0.4	V
V_{IH2}	Logic high input level (SM, PKM)	V_{BAT} = 3.6 V	1.8		V_{OUT}	V
		V_{BAT} = 4.2 V	2.0		V_{OUT}	
V_{OLPG}	PG output logic level	I_{OL} = 1 mA			0.4	V
I_{OHPG}	PG output current leakage	V_{OH} = 3.3 V		0.2		µA
$V_{OL\text{-}CHGIN_OK}$	$\overline{CHGIN}_{OK}$, output logic level	I_{OL} = 1 mA			0.4	V
$I_{OH\text{-}CHGIN_OK}$	$\overline{CHGIN}_{OK}$, output current leakage	V_{OH} = 3.3 V		0.2		µA

1. *Exceed maximum operative condition could damage internal device and reduce overall reliability level. In case external source could exceed this value, even during limited timing period, it is recommended to add external voltage clamp.*

5 Typical performance characteristics

V_{CHGIN} = 5 V, V_{BAT} = 3.6 V, C_1 = 10 µF, C_2 = 10 µF, $V_{SET0,1}$ = 0 V; $I_{SET0,1}$ = 0 V, SM floating, T_A = 25 °C, unless otherwise specified.

Figure 3. I_{CC} vs. temperature (V_{BAT} = 3.6 V; I_{OUT} = 1 mA)

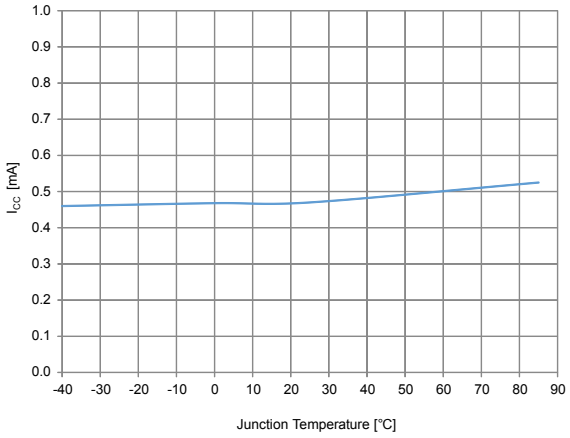


Figure 4. Floating voltage vs. temperature

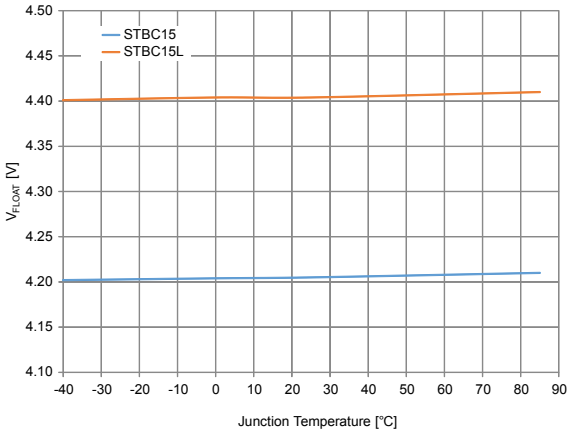


Figure 5. Charge current vs. temperature

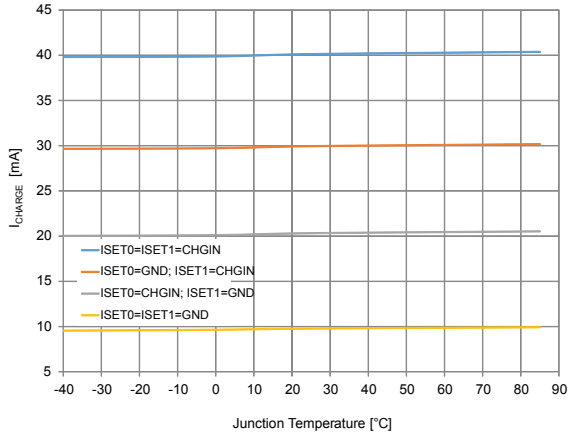


Figure 6. R_{ON} M3 vs. temperature

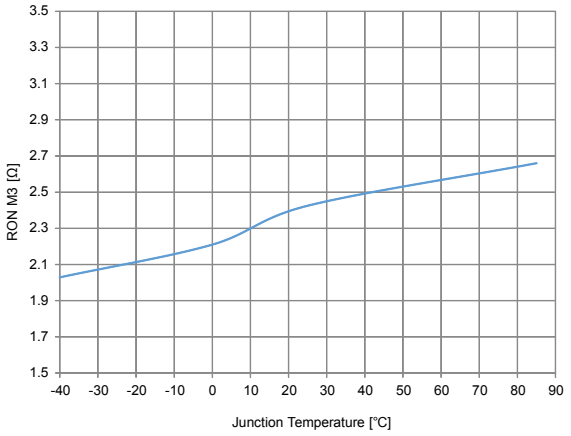


Figure 7. Battery leakage current vs. V_{BAT} (V_{CHGIN} = 0 V; V_{BAT} > V_{BAT_OVD})

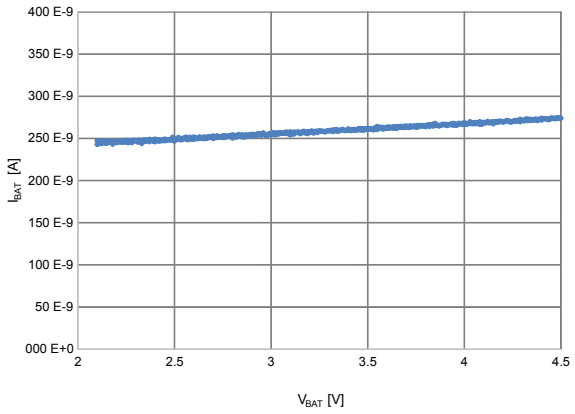
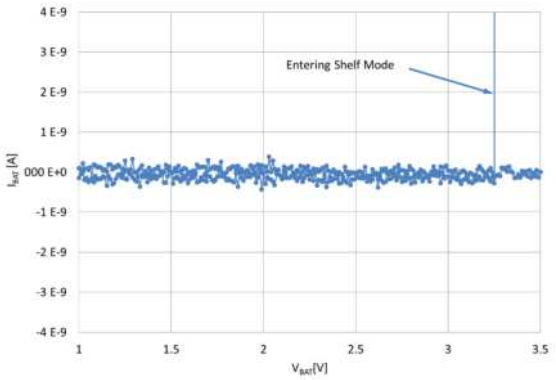


Figure 8. Battery leakage current vs. V_{BAT} (V_{CHGIN} = 0 V; V_{BAT} < V_{BAT_OVD}; shelf mode)



6 Control pin description

PG

Power-Good open-drain, active high-z output pin. It provides the status about OUT valid voltage based. If OUT voltage is higher than V_{BAT_CONN} (4.1 V) then the pin goes to high-z. It is pulled down if OUT voltage is lower V_{BAT_CONN} (4.1 V). It requires an external pull-up resistor connected to VOUT.

$\overline{CHGIN_{OK}}$

Input voltage source Power Good pin. It goes to high-z when the input voltage source is not valid. Logic negate.

$V_{SET0,1}$

Set the floating battery voltage value. They can be tied to CHGIN or GND thus determining four different settings.

$I_{SET0,1}$

Set the charging current. They can be tied to CHGIN or GND thus determining four different settings.

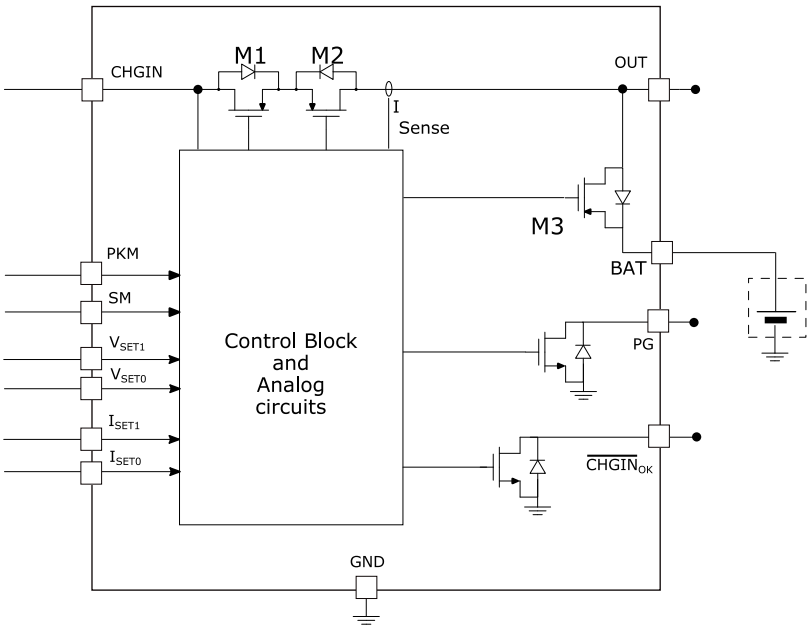
PKM

Peak mode input. It allows reducing battery shutdown threshold from normal operating mode to lower threshold level. This enables the application to temporarily support load peak current that could otherwise generate false battery shutdown detection.

SM

Shelf-mode activation pin. Active high input with internal pull-down resistor to reduce external components. When high, the device enters shelf-mode. Block diagram.

Figure 9. STBC15 block diagram



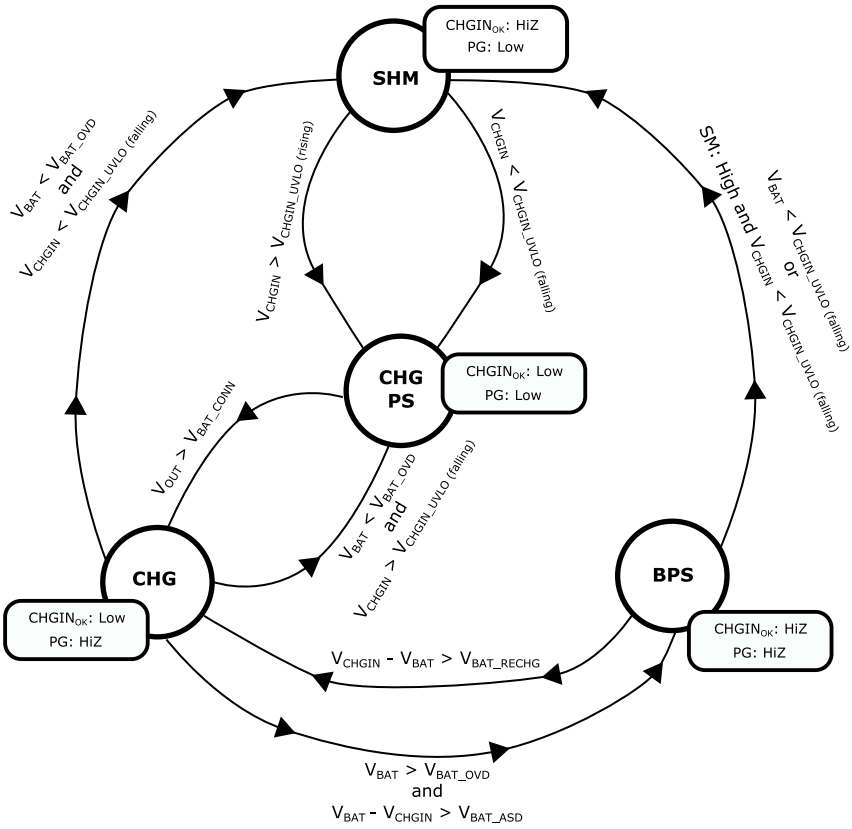
7 Operation description

7.1 Battery charger finite state machine (FSM)

The battery charger implements a CC/CV control algorithm to charge the battery connected to BAT. Since the STBC15 is dedicated to low capacity batteries pre-charge or termination phases are not necessary. Both the floating voltage and the charging current are configurable by dedicated pins, $V_{SET1,2}$ and $I_{SET1,2}$.

The device finite state machine behavior is shown in following diagram.

Figure 10. Operational simplified state machine diagram



SHM: shelf mode

BPS: system powered by battery

CHG: battery is being recharged, Vout ok

CHG PS: Vout not good, battery charged through M3 body

7.2 Floating voltage selection

The battery floating voltage can be set by $V_{SET0,1}$ pins. In order to increase the number of charging cycles, lower floating voltage values are preferred. On the other side, the reduced floating voltage leads to the decreased energy stored into the battery.

The battery floating voltage can be set by $V_{SET0,1}$ pins. In order to increase the number of charging cycles, lower floating voltage values are preferred. On the other side, the reduced floating voltage leads to the decreased energy stored into the battery. The best trade-off can be chosen according to application needs. Different range of floating voltages can be utilized by using different part numbers.

Table 6. **STBC15 floating voltage selection**

VSET1	VSET0	Floating voltage [V]
0	0	4.00
0	1	4.05
1	0	4.10
1	1	4.20

Table 7. **STBC15L floating voltage selection**

VSET1	VSET0	Floating voltage [V]
0	0	4.20
0	1	4.25
1	0	4.35
1	1	4.40

7.3 Charge current selection

The charge current is defined by external pin configuration shown in the table below.

Table 8. **Charge current selection**

ISET1	ISET0	Battery charging current [mA]
0	0	10
0	1	20
1	0	30
1	1	40

7.4 Battery recharge

When CHGIN voltage drops below the level defined by V_{BAT} - V_{BAT_ASD}, the device turns M3 on and the OUT pin is supplied by the battery (BPS state). The battery recharge restarts again when the voltage on CHGIN exceeds the level defined by V_{BAT} + V_{BAT_RECHG} voltage. The device goes to *CHG* state.

7.5 Over-discharge protection and peak mode

The STBC15 protects the battery by disconnecting it when its voltage is below a certain level defined by the V_{BAT_OVD} threshold. This function protects the battery from over-discharging. In order to maintain the over-discharge status, the battery voltage should, in any condition, stay above the V_{BAT_FF} threshold.

In some application conditions, such as during RF transmission bursts, it is requested that the battery sustains short transients below the typical V_{BAT_OVD} level. In order to support this behavior and avoid false triggering of the over-discharge mechanism, it is possible to lower the V_{BAT_OVD} threshold by using the PKM pin. When this pin is pulled low, the V_{BAT_OVD} threshold is decreased to a lower level according to the table below.

Table 9. **Battery over-discharge voltages for the STBC15**

PKM	Min. VBAT_OVD [V]	Max. VBAT_OVD [V]
0	3.2	3.3
1	2.2	2.3

Table 10. **Battery over-discharge voltages for the STBC15L**

PKM	Min. VBAT_OVD [V]	Max. VBAT_OVD [V]
x	2.65	2.75

7.6 Shelf mode

The STBC15 provides an ultra-low power mode with current consumption less than 10 nA in order to support long period of shelf storage of the final equipment with minimum battery discharge.

In this case, even if the battery is charged and its voltage is above the cut-off voltage, it can be disconnected from the system by applying a positive pulse to SM pin.

7.7 Reverse current protection

The STBC15 avoids reverse current flowing from the battery to the input voltage source when the CHGIN voltage is lower than BAT voltage. This is particularly important when a photovoltaic panel is used as an input voltage source. This function is accomplished by turning off M1 switch when CHGIN voltage drops below CHGIN UVLO threshold.

7.8 STBC15 / STBC15L difference summary

The STBC15 is dedicated to thin film batteries while the STBC15L to li-Ion batteries. Here below a summary of the main differences:

Table 11. **STBC15 / STBC15L difference summary**

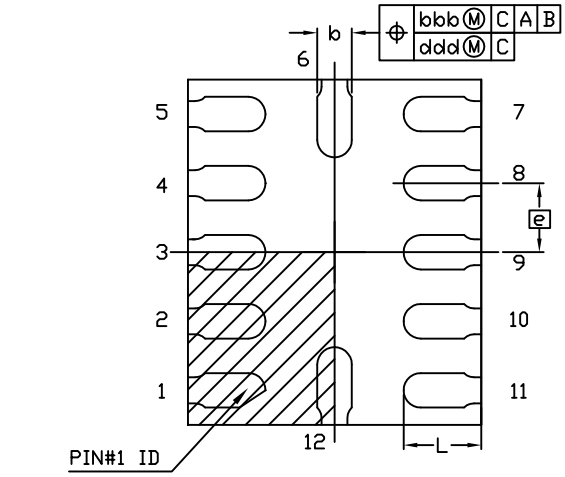
Name	PKM	STBC15	STBC15L
V_{FLOAT}	x	4.0 V to 4.2 V	4.2 V to 4.4 V
V_{BAT_OVD}	PKM=0	3.25 V	2.7 V
	PKM=1	2.25 V	2.7 V
V_{BAT_CONN}	PKM=0	4.10 V	3.6 V
	PKM=1	4.10 V	3.9 V

8 Package information

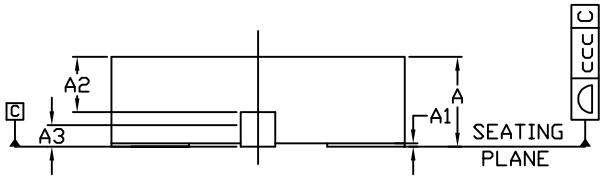
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN12 (1.7 x 2.0 mm) package information

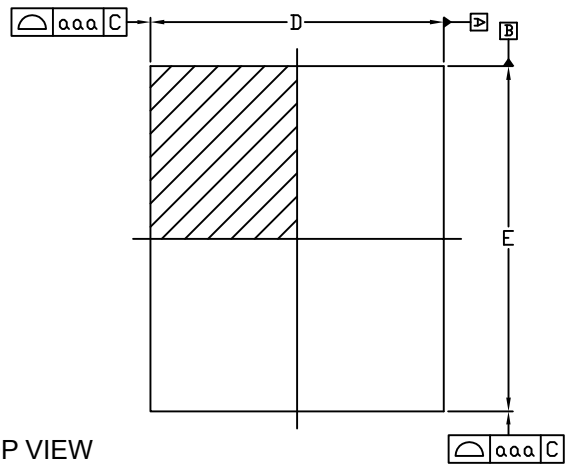
Figure 11. QFN12 (1.7 x 2.0 mm) package outline



BOTTOM VIEW



SIDE VIEW

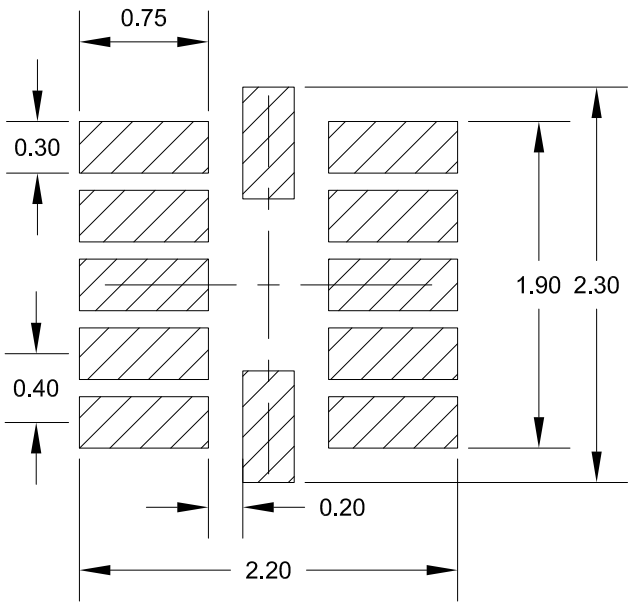


TOP VIEW

Table 12. **QFN12 (1.7 x 2.0 mm) package mechanical data**

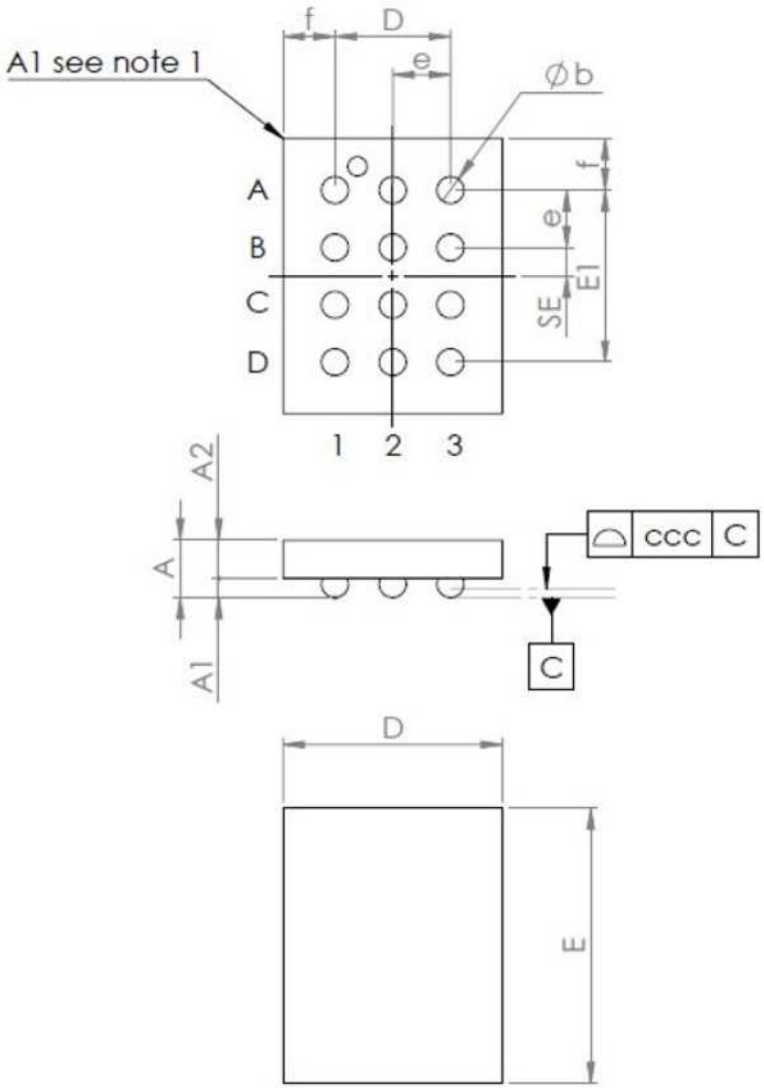
Dim.	mm		
	Min.	Typ.	Max.
A	0.4	0.50	0.55
A1	0.00	0.03	0.05
A2	0.28	0.38	0.48
A3		0.125	
b	0.15	0.20	0.25
D	1.60	1.70	1.80
E	1.95	2.00	2.05
e		0.40	
E	1.90	2.00	2.10
L	0.35	0.45	0.55
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	

Figure 12. **QFN12 (1.7 x 2.0 mm) recommended footprint**



8.2 Flip-chip12 (1.10 x 1.41 mm) package information

Figure 13. **Flip-chip12 (1.1 x 1.41 mm) package outline**



Note 1:

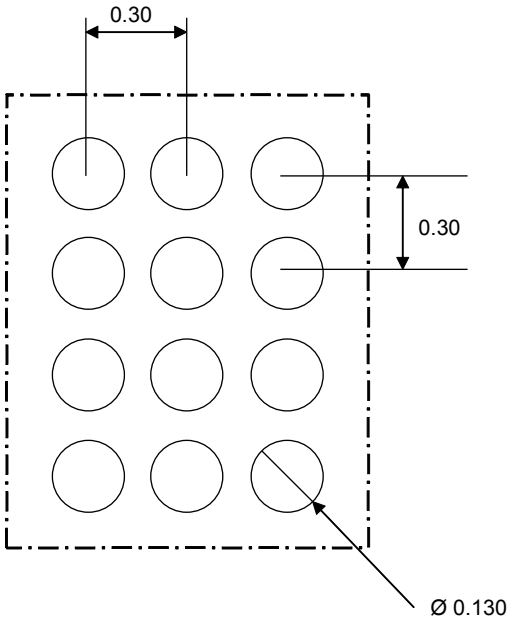
The terminal A3 on the bumps side is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.1 mm diameter -) and/or a missing bump.

The terminal A1 on the top of the product is identified by a distinguishing feature (for instance by a circular "clear area" - typically 0.5 mm diameter -)

Table 13. **Flip-chip12 (1.1 x 1.41 mm) package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.265	0.300	0.335
A1	0,085	0,100	0,115
A2	0.180	0.200	0.220
b	0,125	0,140	0,155
D	1,06	1,11	1,16
D1		0,6	
E	1,36	1,41	1,46
E1		0,9	
e		0,3	
SE		0,15	
f		0,255	
ccc			0,020

Figure 14. **Flip-chip12 (1.1 x 1.41 mm) recommended footprint**



9 Ordering information

Table 14. **Ordering information**

Order code	Battery type	Package
STBC15QTR	Thin film	QFN12
STBC15LJTR	Li-Ion	Flip-chip12

Revision history

Table 15. **Document revision history**

Date	Revision	Changes
23-May-2018	1	Initial release.
12-Jul-2021	2	Updated Table 14. Ordering information.

Contents

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