STD40P8F6AG

Automotive-grade P-channel -80 V, 18.5 mΩ typ., -40 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

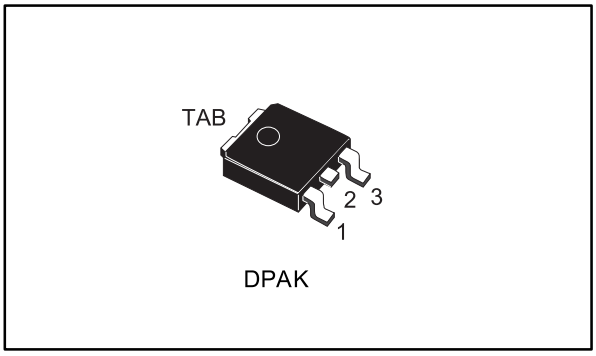
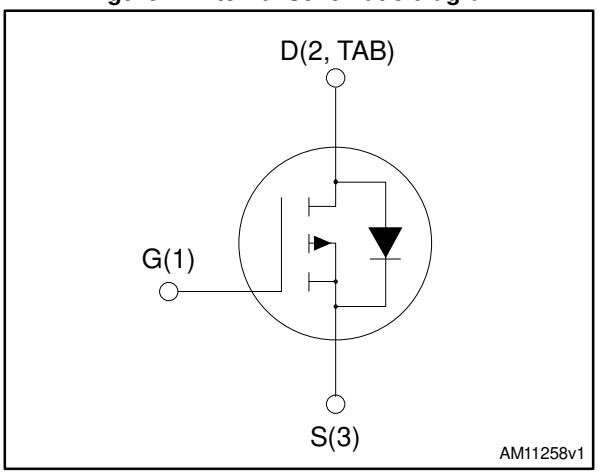


Figure 1: Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STD40P8F6AG	-80 V	28 mΩ	-40 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STD40P8F6AG	40P8F6	DPAK	Tape and reel

This is information on a product in full production.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-80	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	-40	A
I_D	Drain current (continuous) at T_C = 100 °C	-28	A
I_{DM}(1)	Drain current (pulsed)	-160	A
P_{TOT}	Total dissipation at T_C = 25 °C	100	W
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = -40 A, V_{DD} = -60 V)	240	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.5	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max(1)	50	°C/W

Notes:

(1)When mounted on 1 inch^2 FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -1 mA	-80			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = -60 V			-1	µA
		V_{GS} = 0 V, V_{DS} = -60 V, T_C = 125 °C(1)			-10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2		-4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = -10 V, I_D = -20 A		18.5	28	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0 V	-	4112	-	pF
C_{oss}	Output capacitance		-	366	-	pF
C_{rss}	Reverse transfer capacitance		-	188	-	pF
Q_g	Total gate charge	V_{DD} = -40 V, I_D = -40 A, V_{GS} = -10 V (see *Figure 14: "Gate charge test circuit"*)	-	73	-	nC
Q_{gs}	Gate-source charge		-	17.1	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -40 V, I_D = -20 A, R_G = 4.7 Ω, V_{GS} = -10 V (see *Figure 13: "Switching times test circuit for resistive load"*)	-	17.5	-	ns
t_r	Rise time		-	28.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	68.5	-	ns
t_f	Fall time		-	34.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		-40	A
I_{SDM} (1)	Source-drain current (pulsed)		-		-160	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = -40 A	-		-1.2	V
t_{rr}	Reverse recovery time	I_{SD} = -40 A, di/dt = 100 A/µs, V_{DD} = -64 V, (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	35		ns
Q_{rr}	Reverse recovery charge		-	44		nC
I_{RRM}	Reverse recovery current		-	-2.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 2: Safe operating area

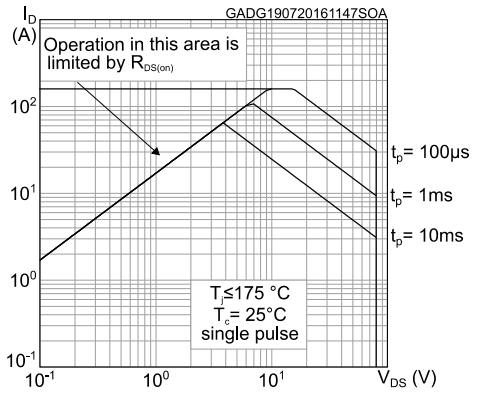


Figure 3: Thermal impedance

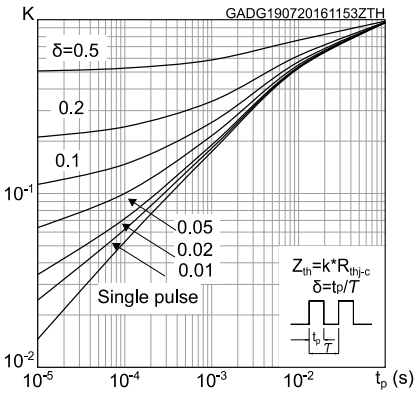


Figure 4: Output characteristics

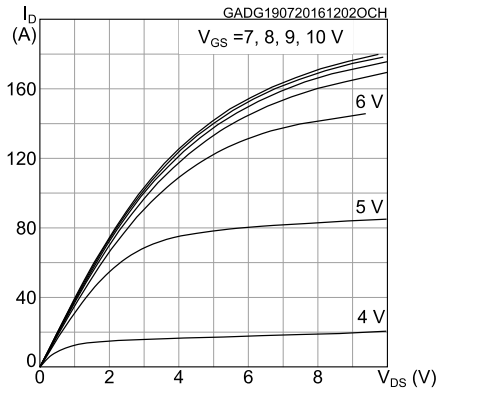


Figure 5: Transfer characteristics

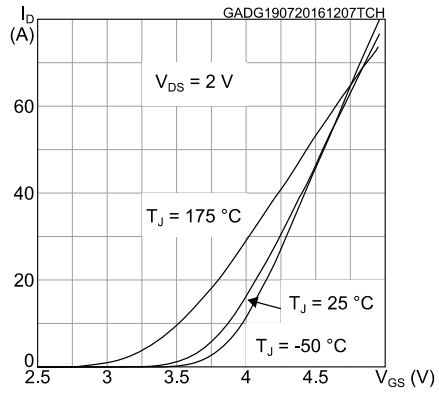


Figure 6: Gate charge vs gate-source voltage

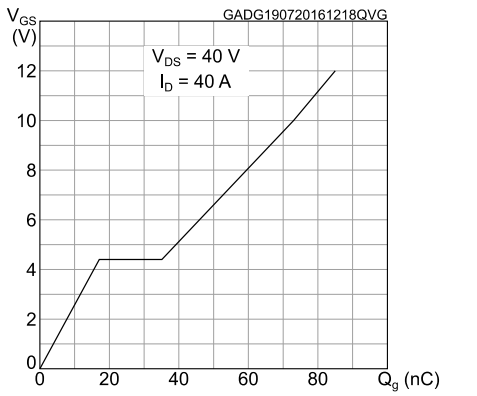


Figure 7: Static drain-source on-resistance

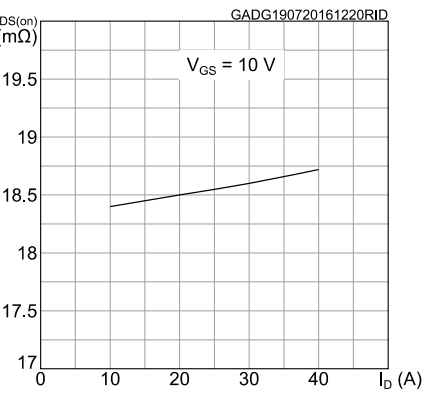


Figure 8: Capacitance variations

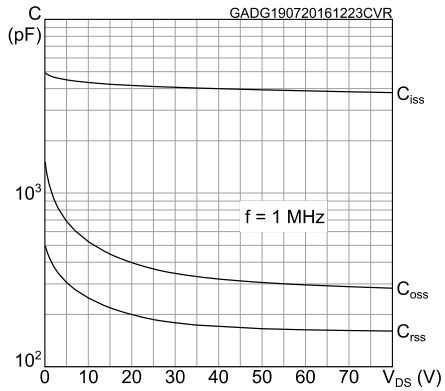


Figure 9: Normalized $V_{(BR)DSS}$ vs temperature

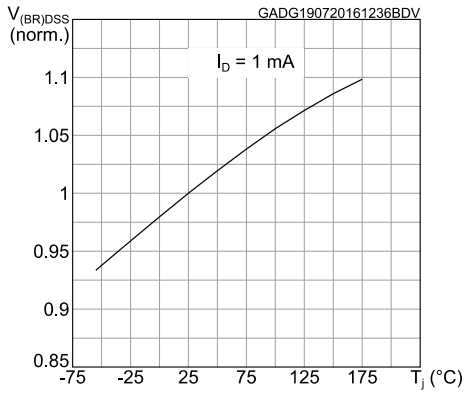


Figure 10: Normalized gate threshold voltage vs temperature

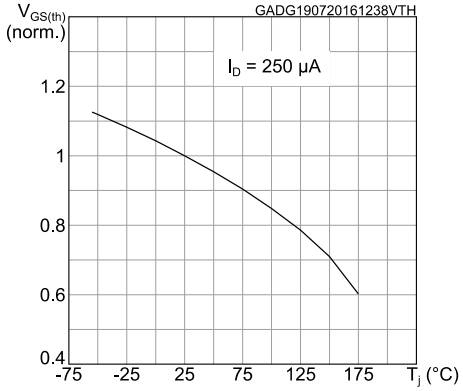


Figure 11: Normalized on-resistance vs temperature

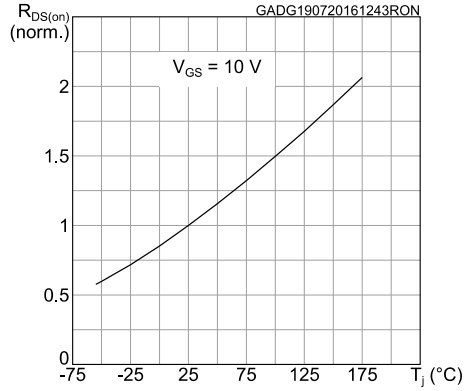
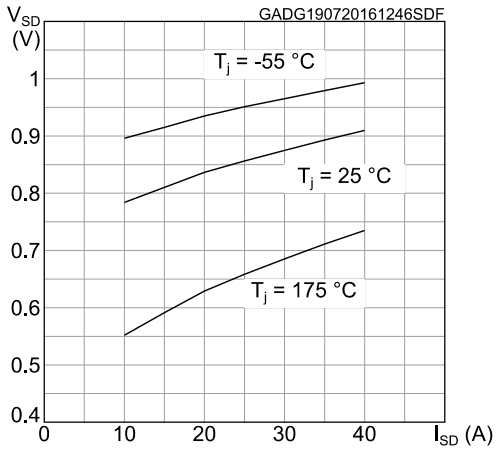


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

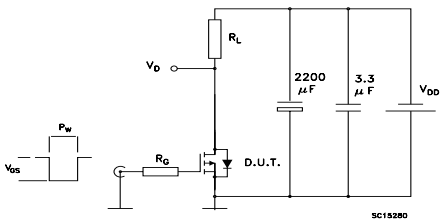


Figure 14: Gate charge test circuit

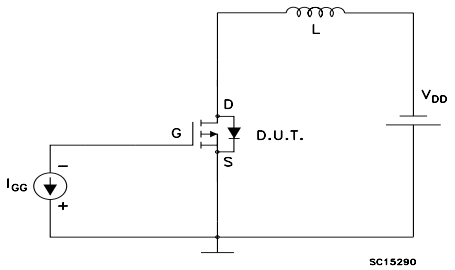
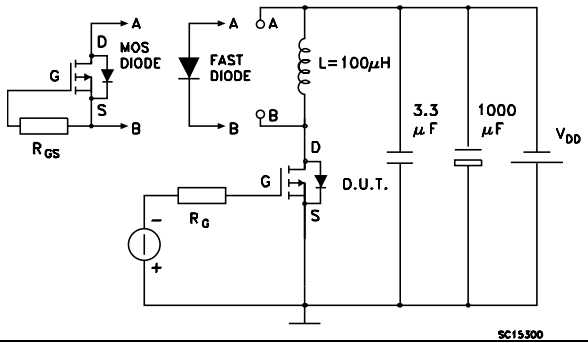


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK type A2 package information

Figure 16: DPAK (TO-252) type A2 package outline

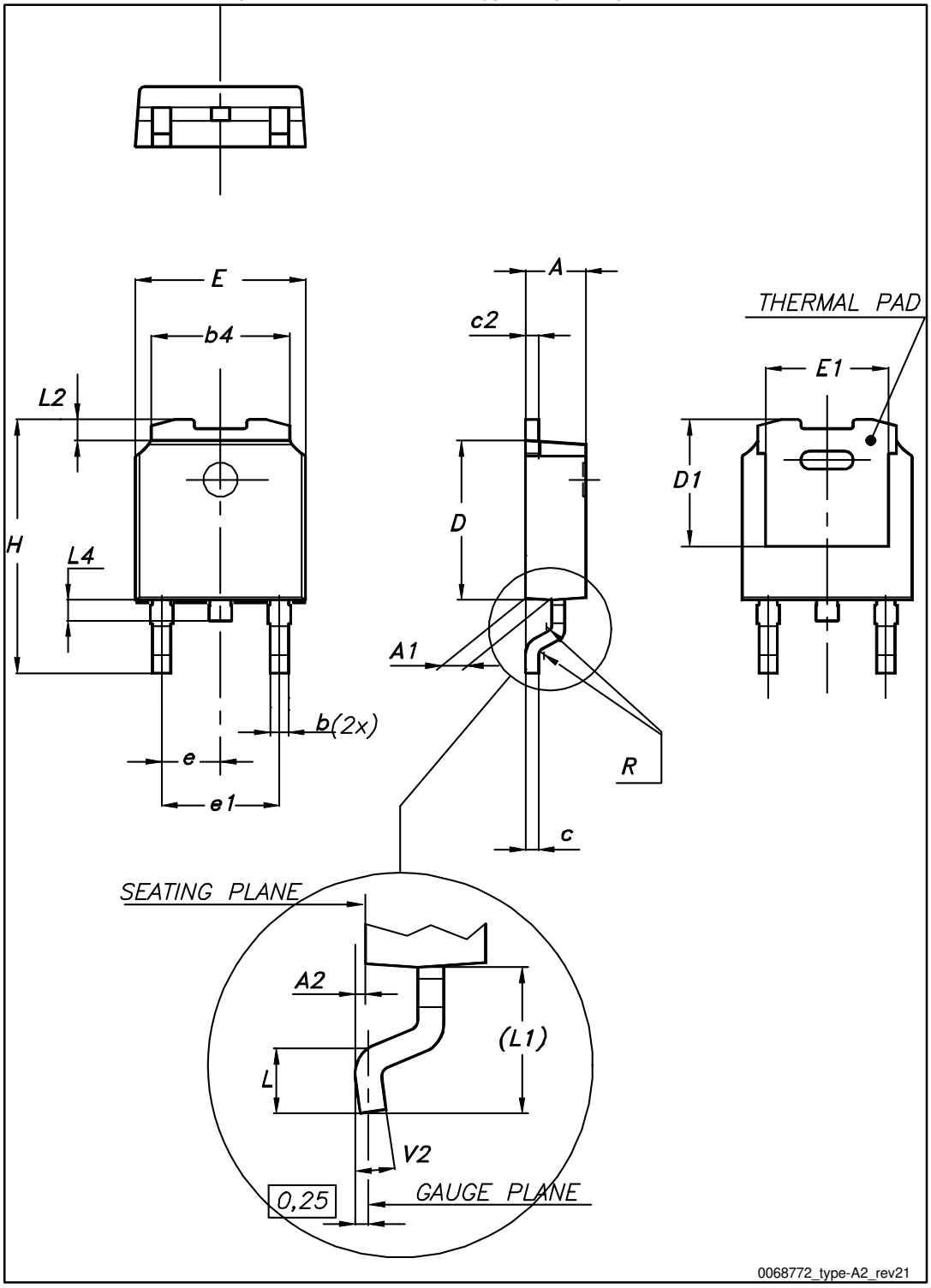
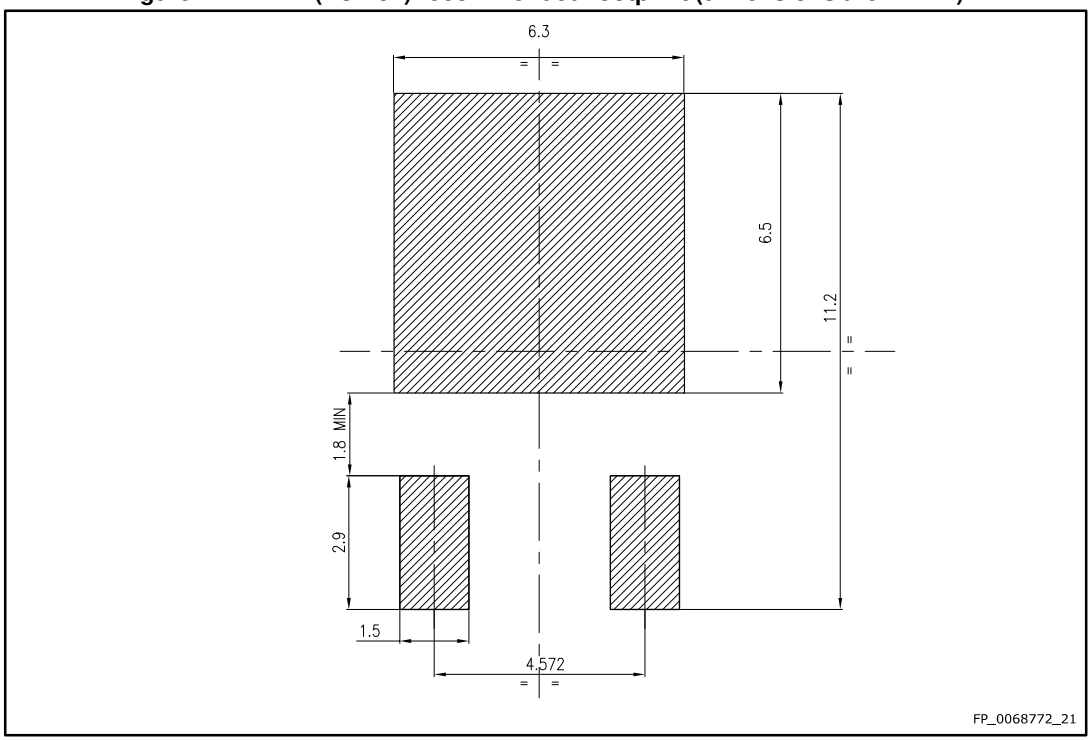


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK packing information

Figure 18: DPAK (TO-252) tape outline

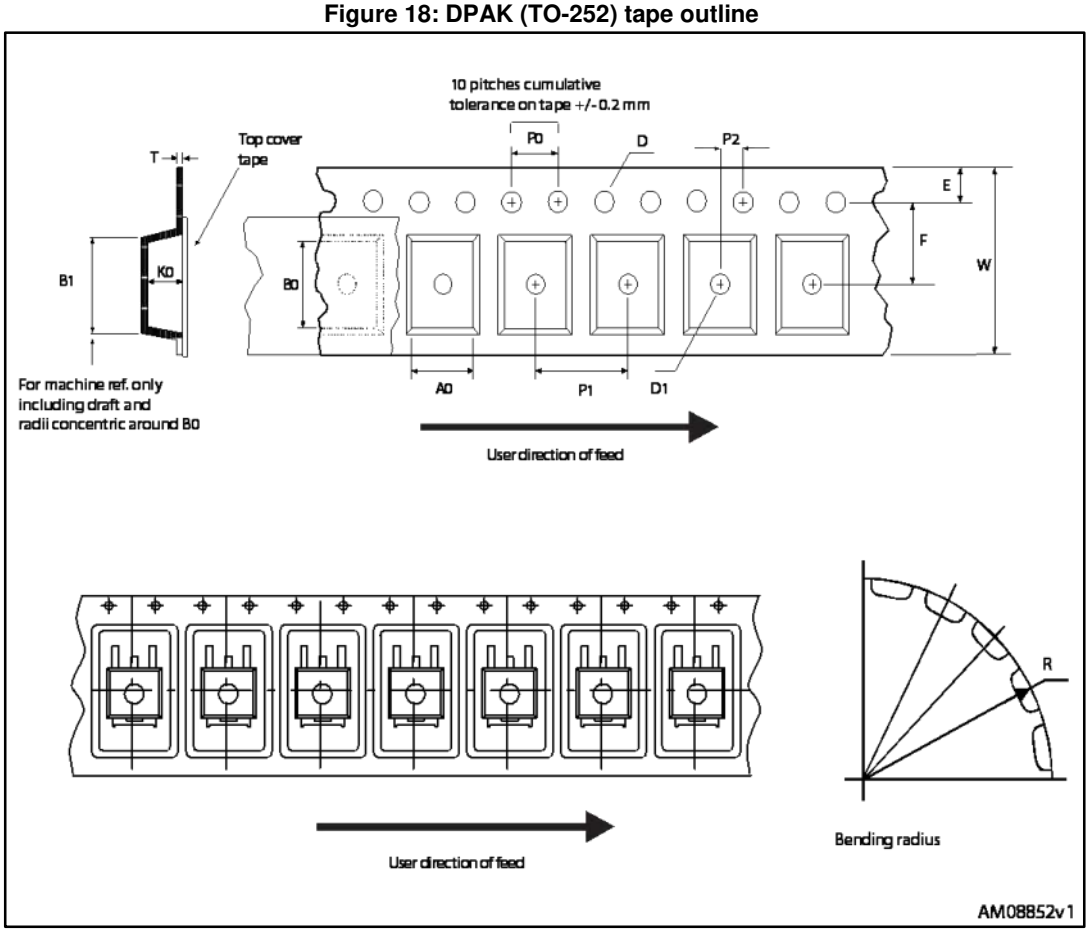


Figure 19: DPAK (TO-252) reel outline

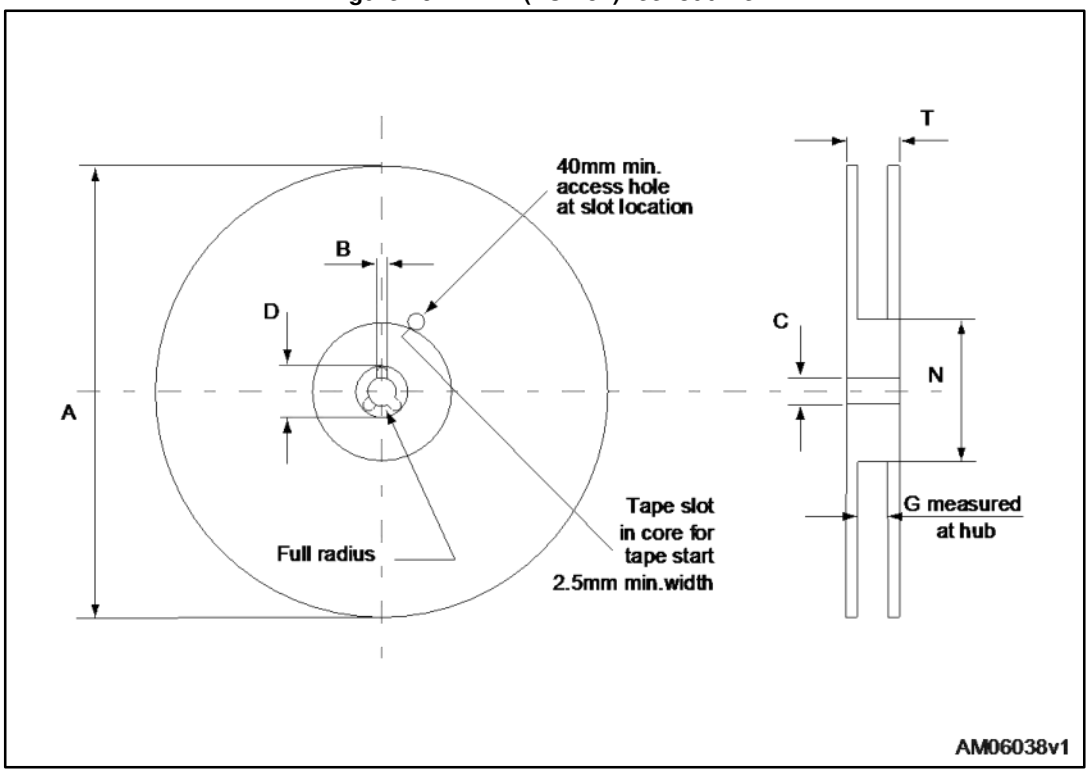


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
19-Jul-2016	1	First release.

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