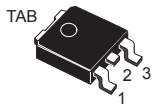
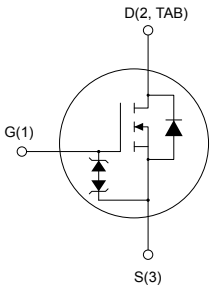
N-channel 650 V, 132 mΩ typ., 20 A MDmesh M9 Power MOSFET in a DPAK package



DPAK



AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD65N160M9	650 V	160 mΩ	20 A

- Very low FOM ($R_{DS(on)} \cdot Q_g$)
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested
- Zener-protected

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

Product status link
STD65N160M9

Product summary	
Order code	STD65N160M9
Marking	65N160M9
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D[(1)]	Drain current (continuous) at T_C = 25 °C	20	A
	Drain current (continuous) at T_C = 100 °C	12.5	
I_{DM}[(2)]	Drain current (pulsed)	60	A
P_{TOT}	Total power dissipation at T_C = 25 °C	106	W
dv/dt[(3)]	Peak diode recovery voltage slope	50	V/ns
di/dt[(3)]	Peak diode recovery current slope	900	A/µs
dv/dt[(4)]	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-220 package.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 10 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} ≤ 400 V.*
4. *V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} ≤ 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.18	°C/W
R_{thJA}[(1)]	Thermal resistance, junction-to-ambient	50	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		132	160	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	1240	-	pF
C_{oss}	Output capacitance		-	25	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	290	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 10 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	32	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	13	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	6	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		20	A
I_{SDM} (2)	Source-drain current (pulsed)		-		60	A
V_{SD} (3)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	192		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	1.8		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	17.5		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	280		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	3.6		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20.5		A

1. *Referred to TO-220 package.*
2. *Pulse width is limited by safe operating area.*
3. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

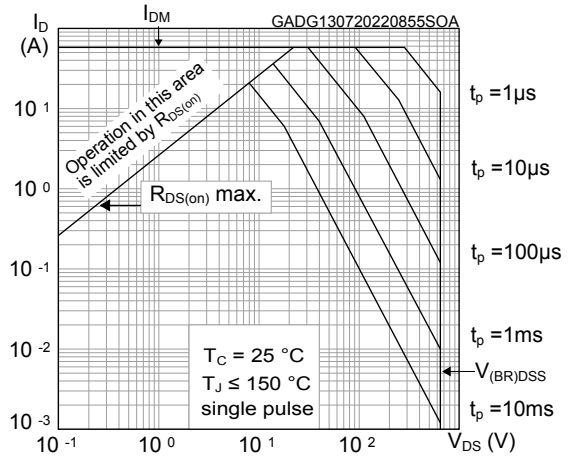


Figure 2. Maximum transient thermal impedance

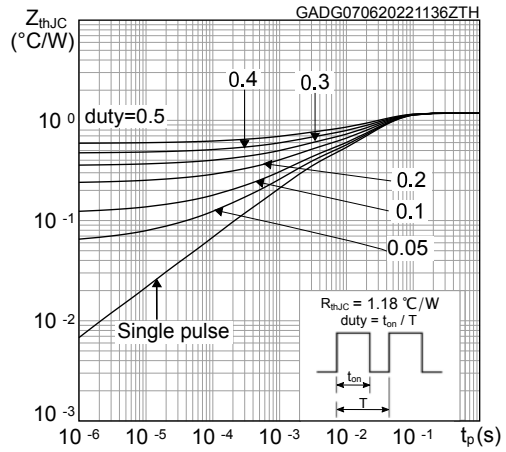


Figure 3. Typical output characteristics

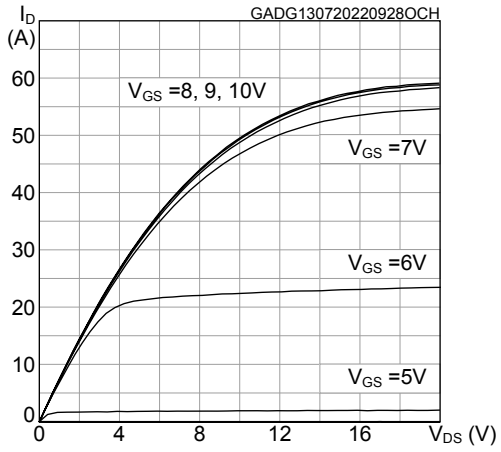


Figure 4. Typical transfer characteristics

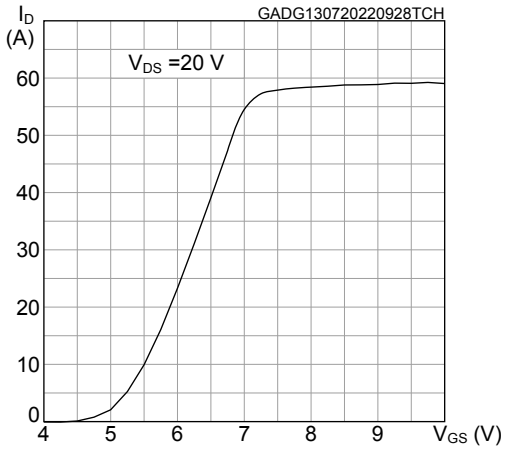


Figure 5. Typical gate charge characteristics

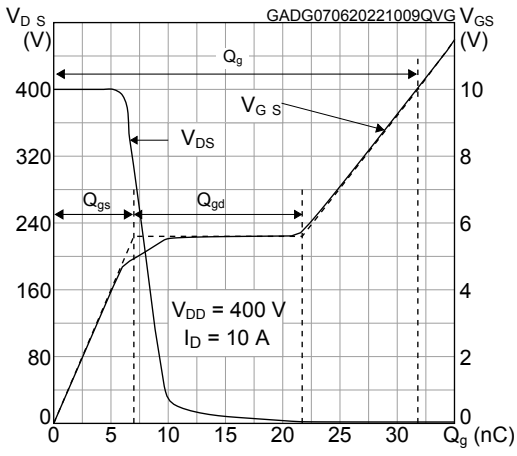


Figure 6. Typical drain-source on-resistance

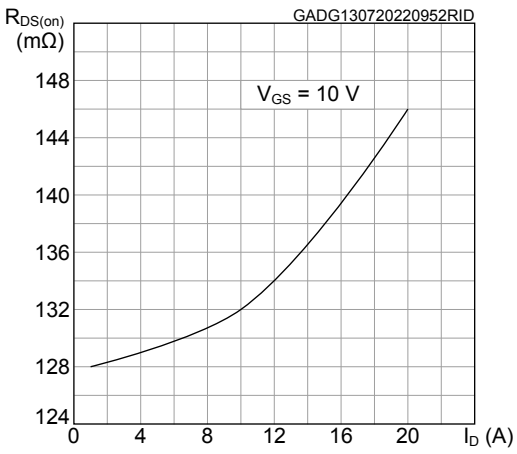


Figure 7. Typical capacitance characteristics

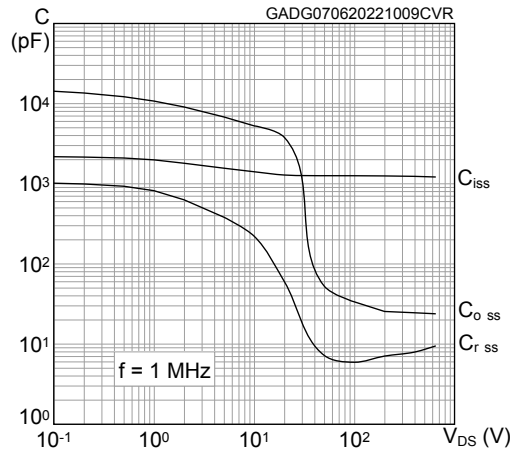


Figure 8. Typical output capacitance stored energy

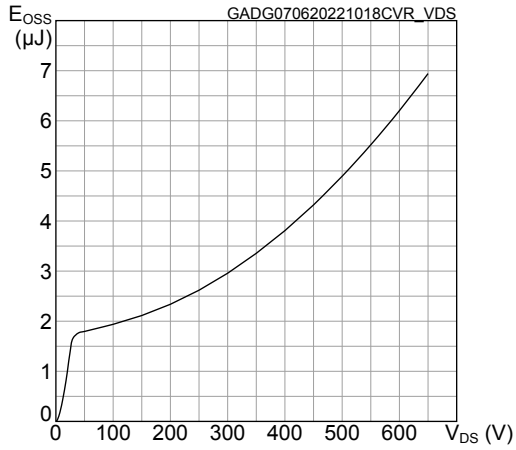


Figure 9. Normalized gate threshold vs temperature

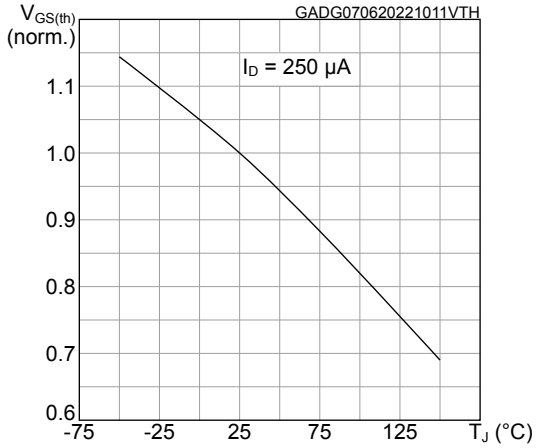


Figure 10. Normalized on-resistance vs temperature

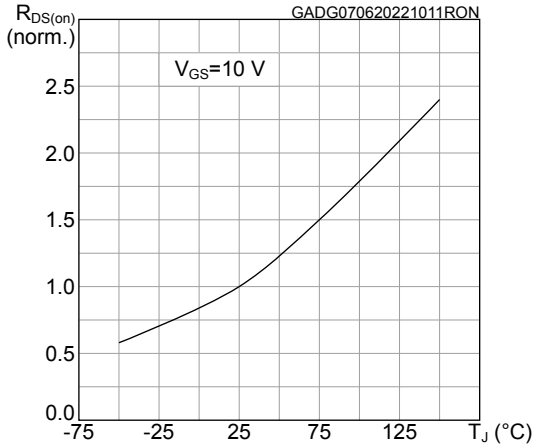


Figure 11. Normalized breakdown voltage vs temperature

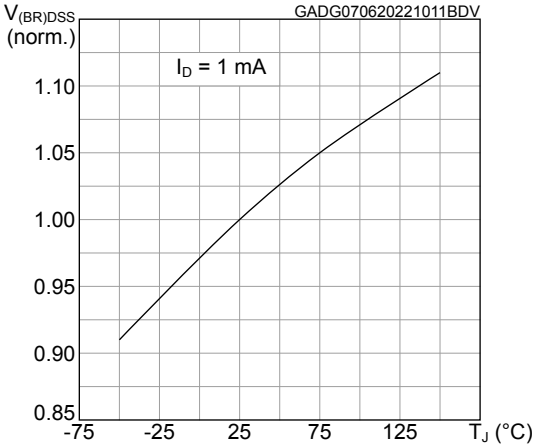
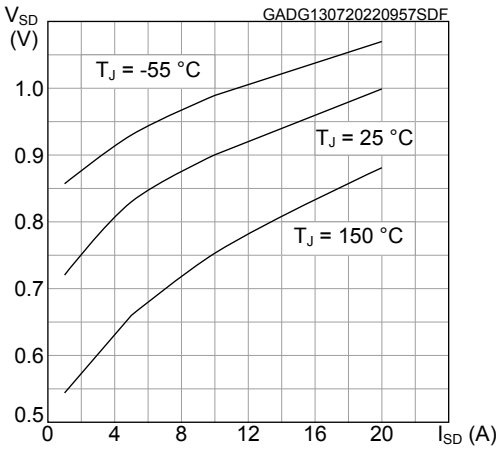
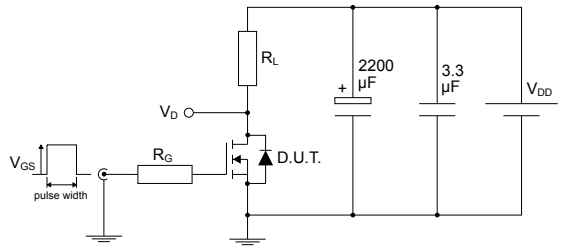


Figure 12. Typical reverse diode forward characteristics



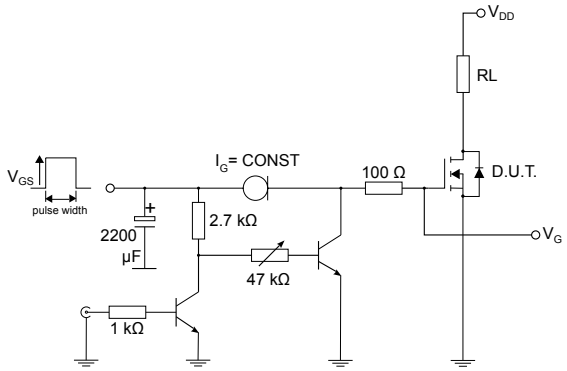
3 Test circuits

Figure 13. Test circuit for resistive load switching times



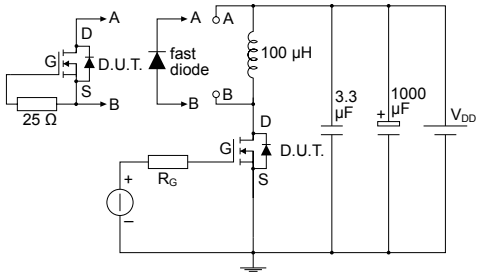
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Figure 14. Test circuit for gate charge behavior



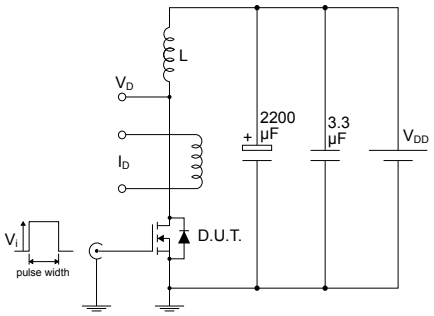
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Figure 15. Test circuit for inductive load switching and diode recovery times



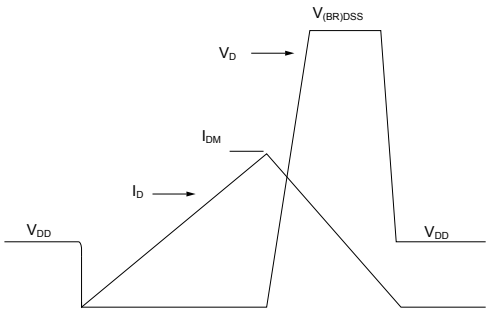
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Figure 16. Unclamped inductive load test circuit



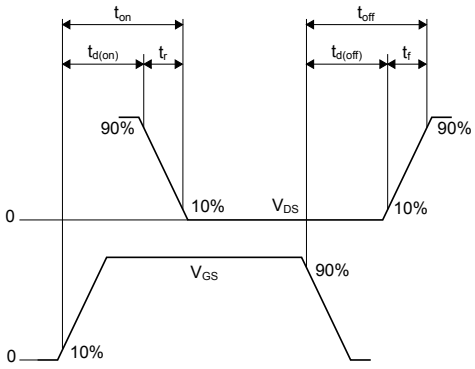
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



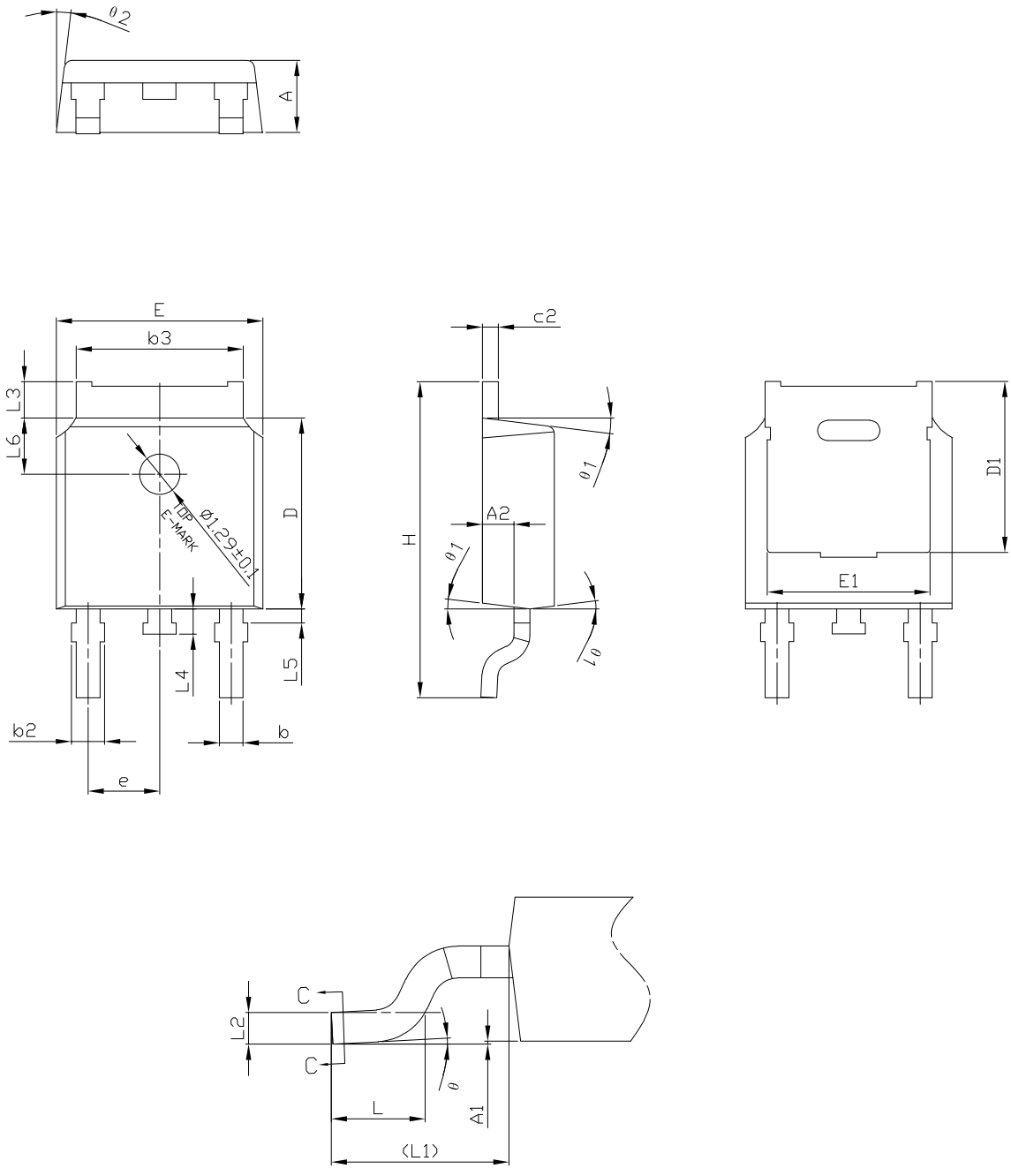
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type C3 package information

Figure 19. DPAK (TO-252) type C3 package outline

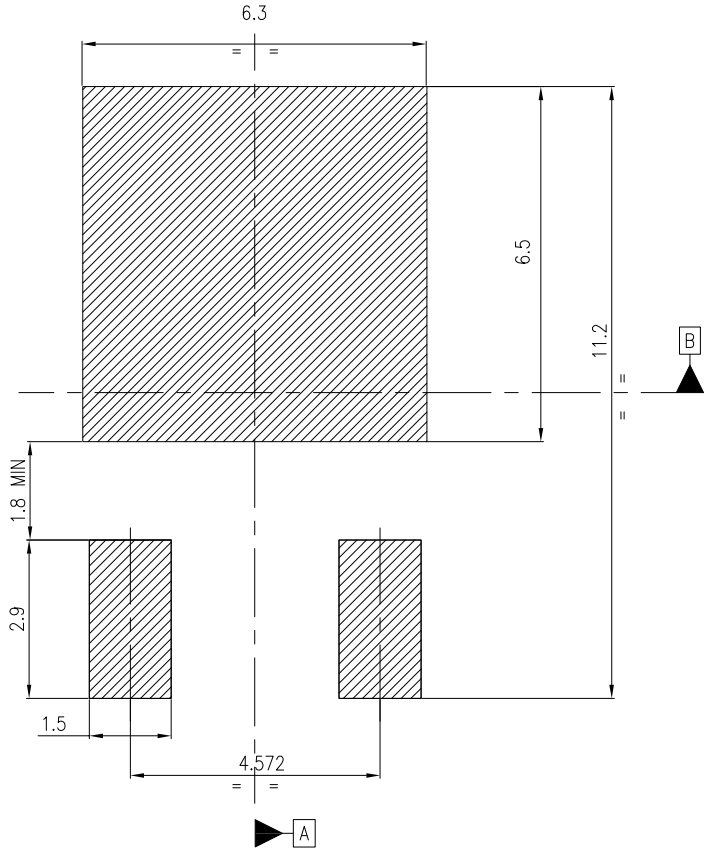


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Table 8. **DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



Notes:

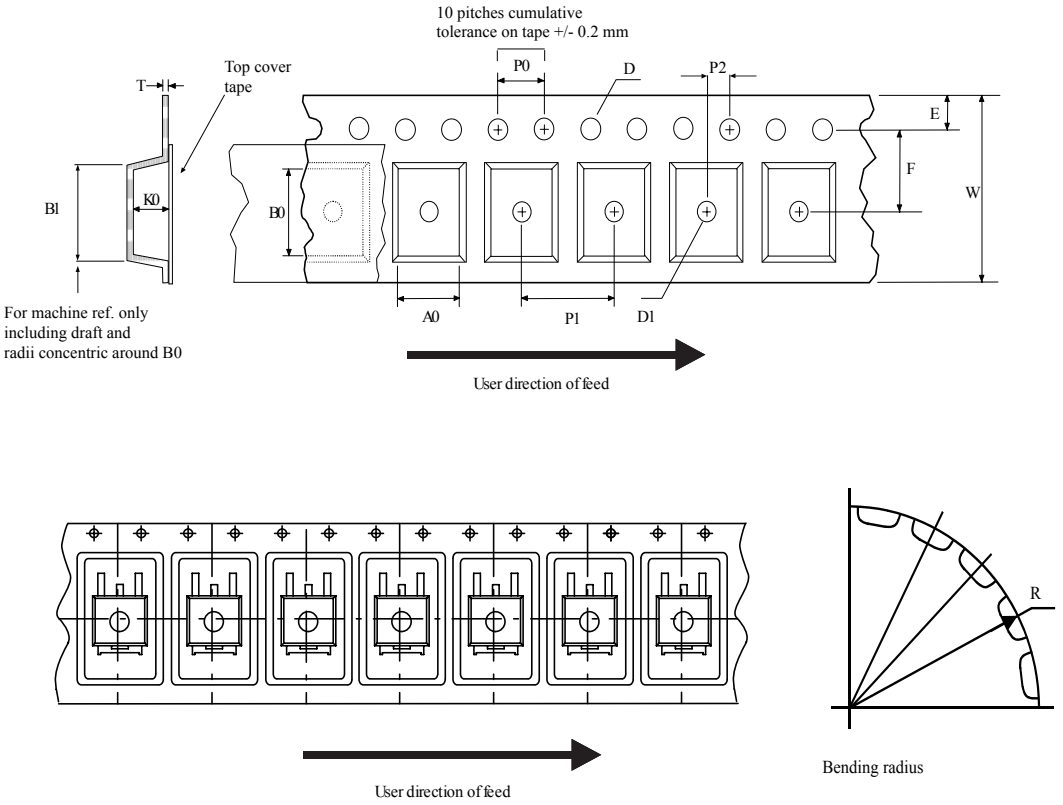
1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)

2) The device must be positioned within ⌖ 0.05 A B

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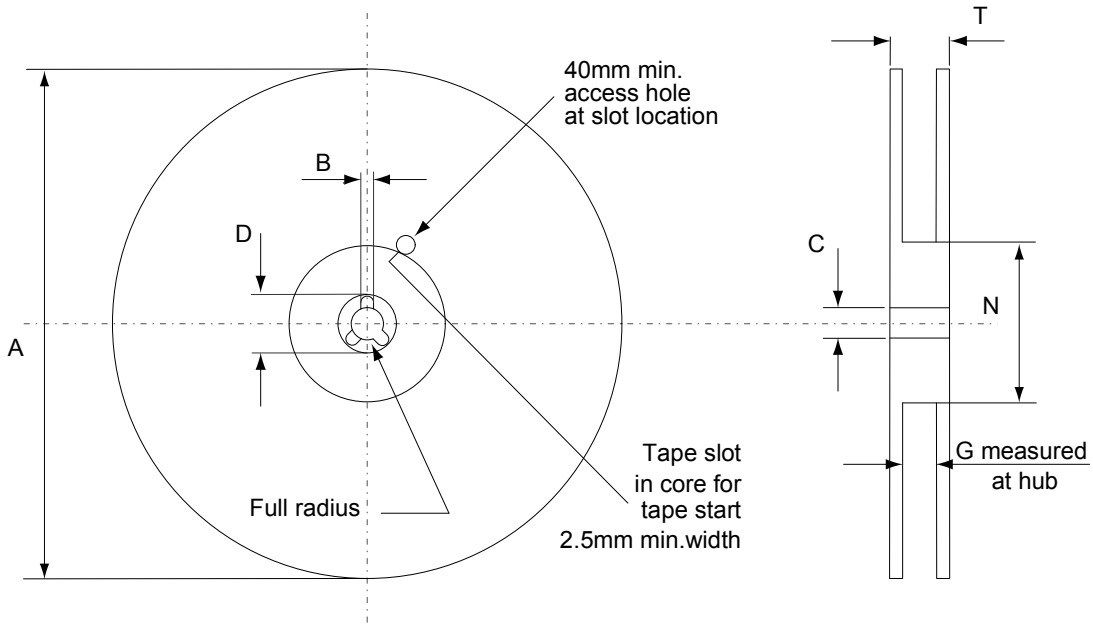
4.2 DPAK (TO-252) packing information

Figure 21. **DPAK (TO-252) tape outline**



AM08852v1

Figure 22. **DPAK (TO-252) reel outline**



AM06038v1

Table 9. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
13-Jul-2022	1	First release.
01-Dec-2022	2	Updated title in cover page. Updated *Features* in cover page. Updated *Table 1. Absolute maximum ratings.* Updated *Table 5. Dynamic.* Updated *Table 7. Source-drain diode.* Updated *Figure 3. Typical output characteristics.*
31-May-2023	3	Updated *Table 6. Switching times.* Updated *Section 3 Test circuits.* Updated *Section 4.1 DPAK (TO-252) type C3 package information.*
26-Nov-2025	4	Updated Figure 7. Typical capacitance characteristics. Minor text changes.

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