STD7N60DM2

N-channel 600 V, 0.78 Ω typ., 6 A MDmesh™ DM2 Power MOSFET in a DPAK package

Datasheet - production data

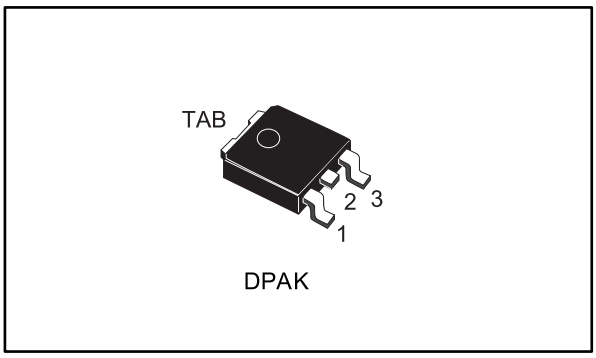
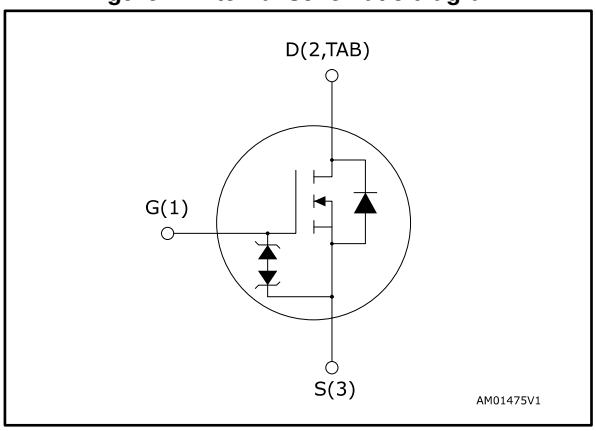


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD7N60DM2	600 V	0.90 Ω	6 A	60 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD7N60DM2	7N60DM2	DPAK	Tape and reel

This is information on a product in full production. www.st.com

Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 8
4 Package information 9
4.1 DPAK (TO-252) type A package information 9
4.2 DPAK (TO-252) packing information 12
5 Revision history 14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	6	A
	Drain current (continuous) at T_{case} = 100 °C	3.8	
I_{DM}(1)	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	60	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 6$ A, di/dt=900 A/µs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 480 V.

(3) $V_{DS} \leq 480$ V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	1.5	A
E_{AS}(2)	Single pulse avalanche energy	160	mJ

Notes:

(1) Pulse width limited by T_{jmax}.

(2) Starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		0.78	0.90	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	324	-	pF
C_{oss}	Output capacitance		-	18	-	
C_{rss}	Reverse transfer capacitance		-	2	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	25	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 6 A, V_{GS} = 0 to 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	7.5	-	nC
Q_{gs}	Gate-source charge		-	2.2	-	
Q_{gd}	Gate-drain charge		-	3.2	-	

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	10	-	ns
t_r	Rise time		-	6	-	
$t_{d(off)}$	Turn-off delay time		-	12.6	-	
t_f	Fall time		-	22.6	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}(1)	Source-drain current (pulsed)		-		24	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 6 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	69		ns
Q_{rr}	Reverse recovery charge		-	164		nC
I_{RRM}	Reverse recovery current		-	4.8		A
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	144		ns
Q_{rr}	Reverse recovery charge		-	492		nC
I_{RRM}	Reverse recovery current		-	6.8		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

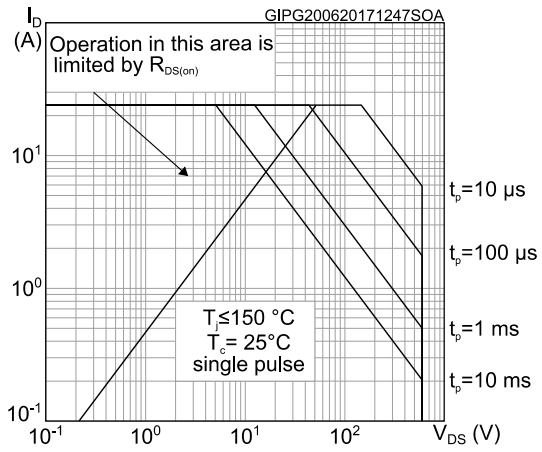


Figure 3: Thermal impedance

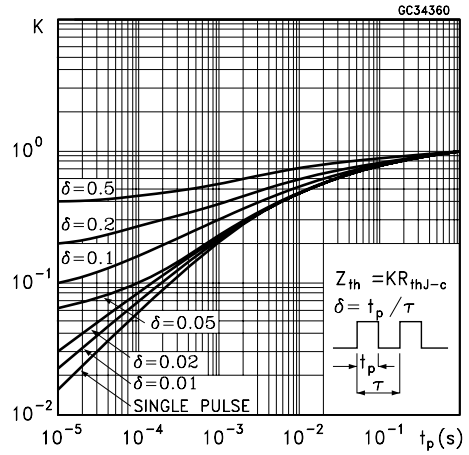


Figure 4: Output characteristics

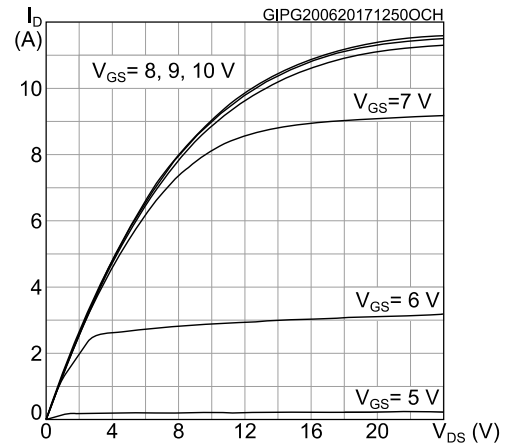


Figure 5: Transfer characteristics

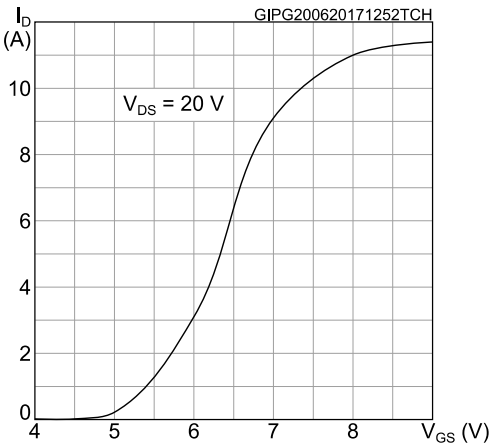


Figure 6: Gate charge vs gate-source voltage

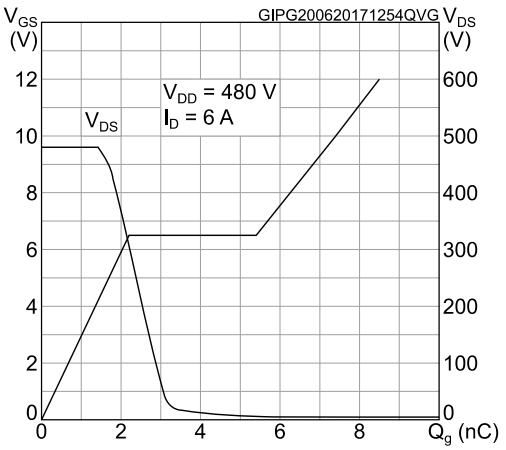


Figure 7: Static drain-source on-resistance

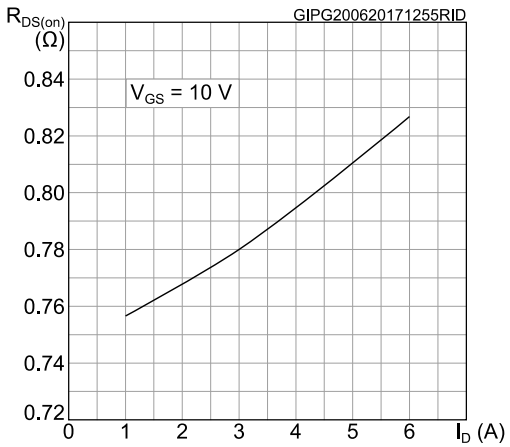


Figure 8: Capacitance variations

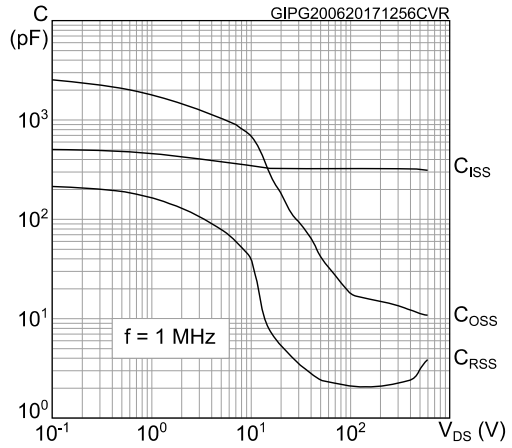


Figure 9: Output capacitance stored energy

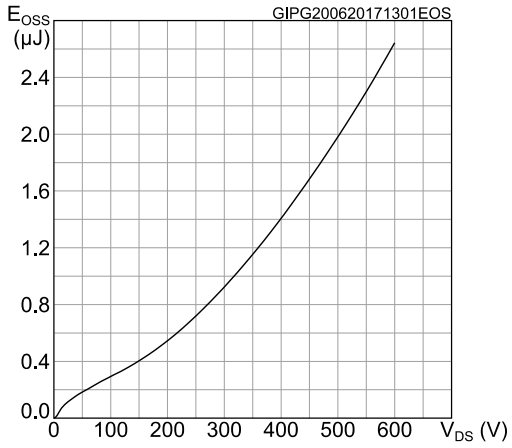


Figure 10: Normalized gate threshold voltage vs temperature

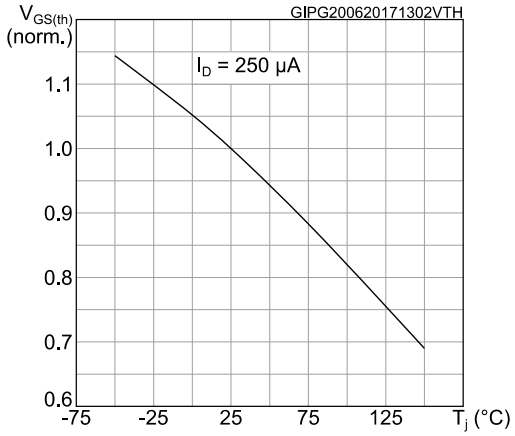


Figure 11: Normalized on-resistance vs temperature

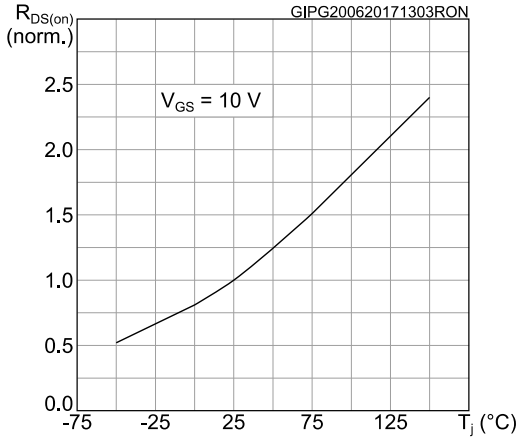


Figure 12: Source-drain diode forward characteristics

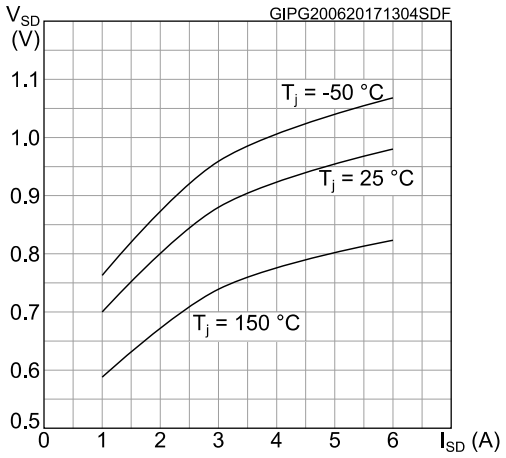
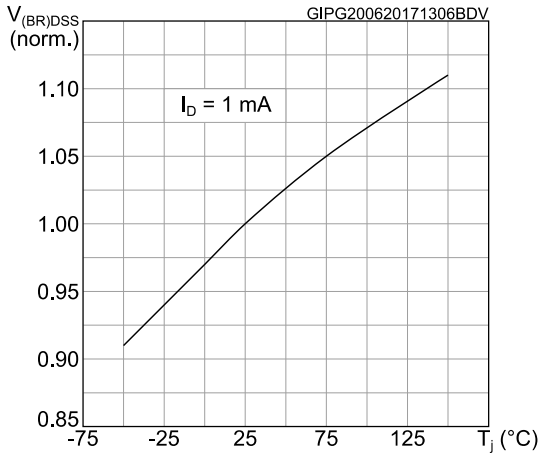


Figure 13: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 14: Test circuit for resistive load switching times

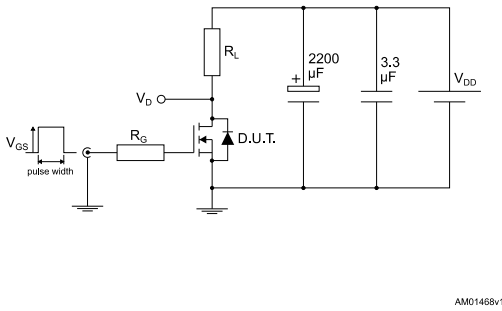


Figure 15: Test circuit for gate charge behavior

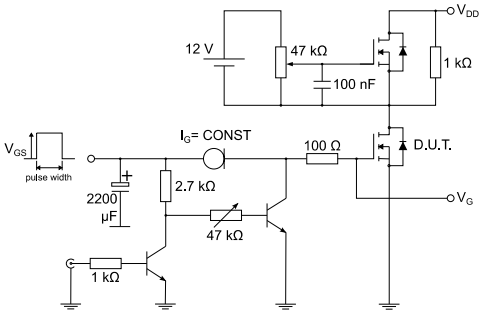


Figure 16: Test circuit for inductive load switching and diode recovery times

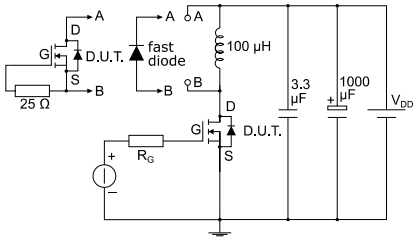


Figure 17: Unclamped inductive load test circuit

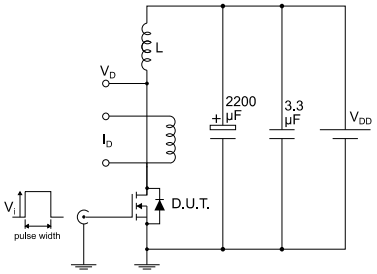


Figure 18: Unclamped inductive waveform

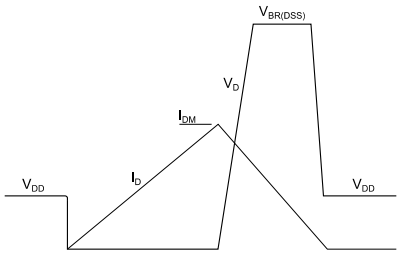
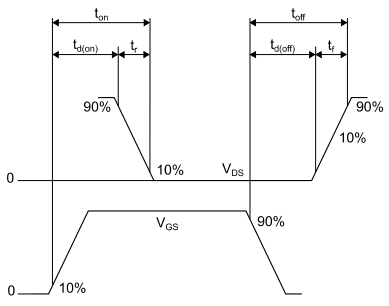


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 20: DPAK (TO-252) type A package outline

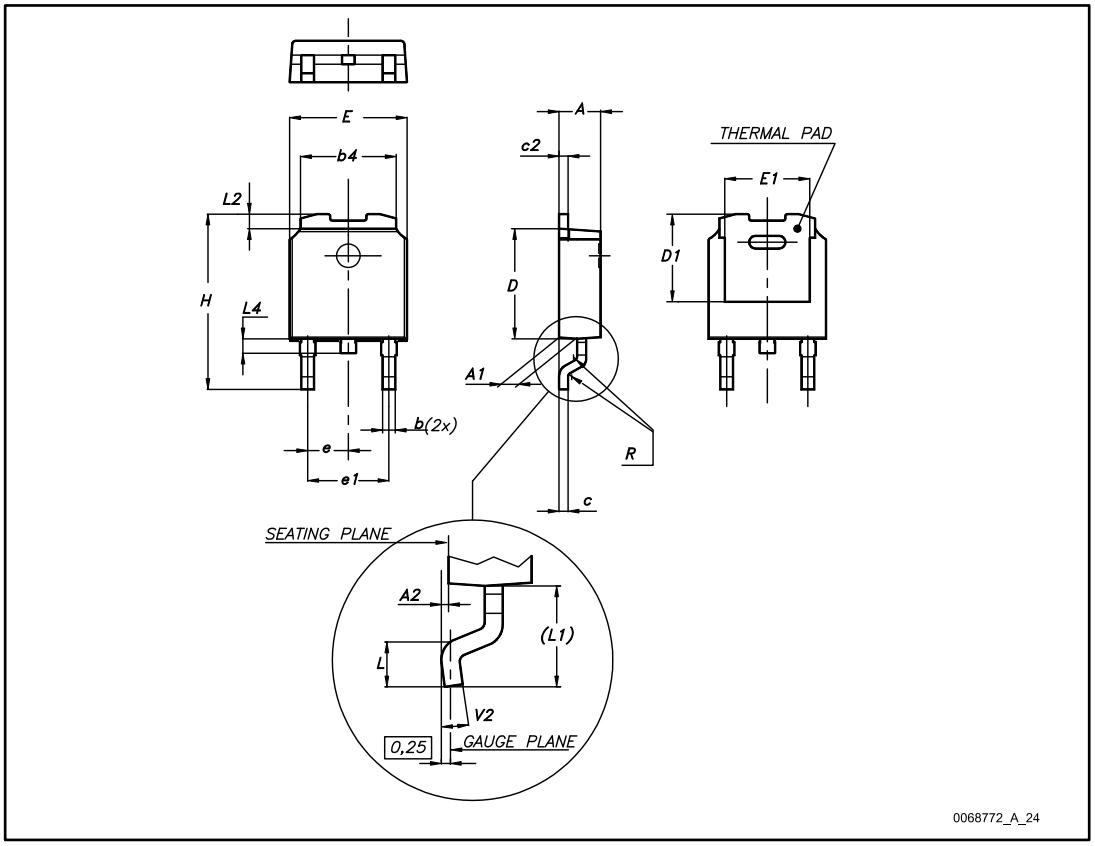
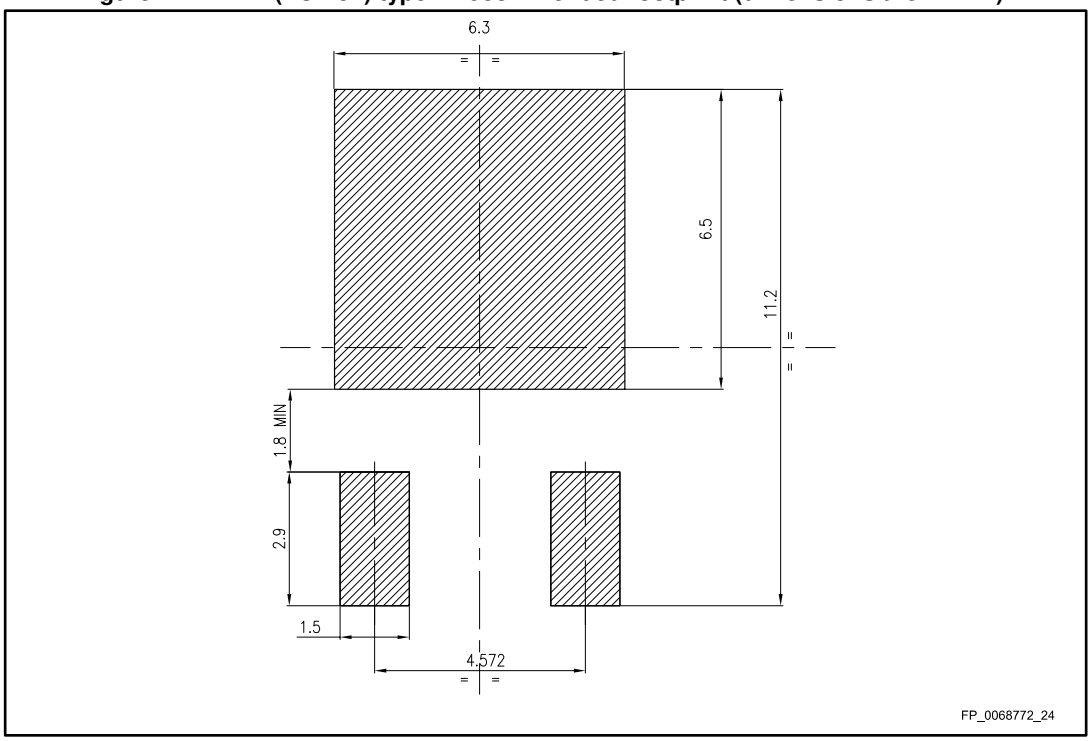


Table 9: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) type A recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 22: DPAK (TO-252) tape outline

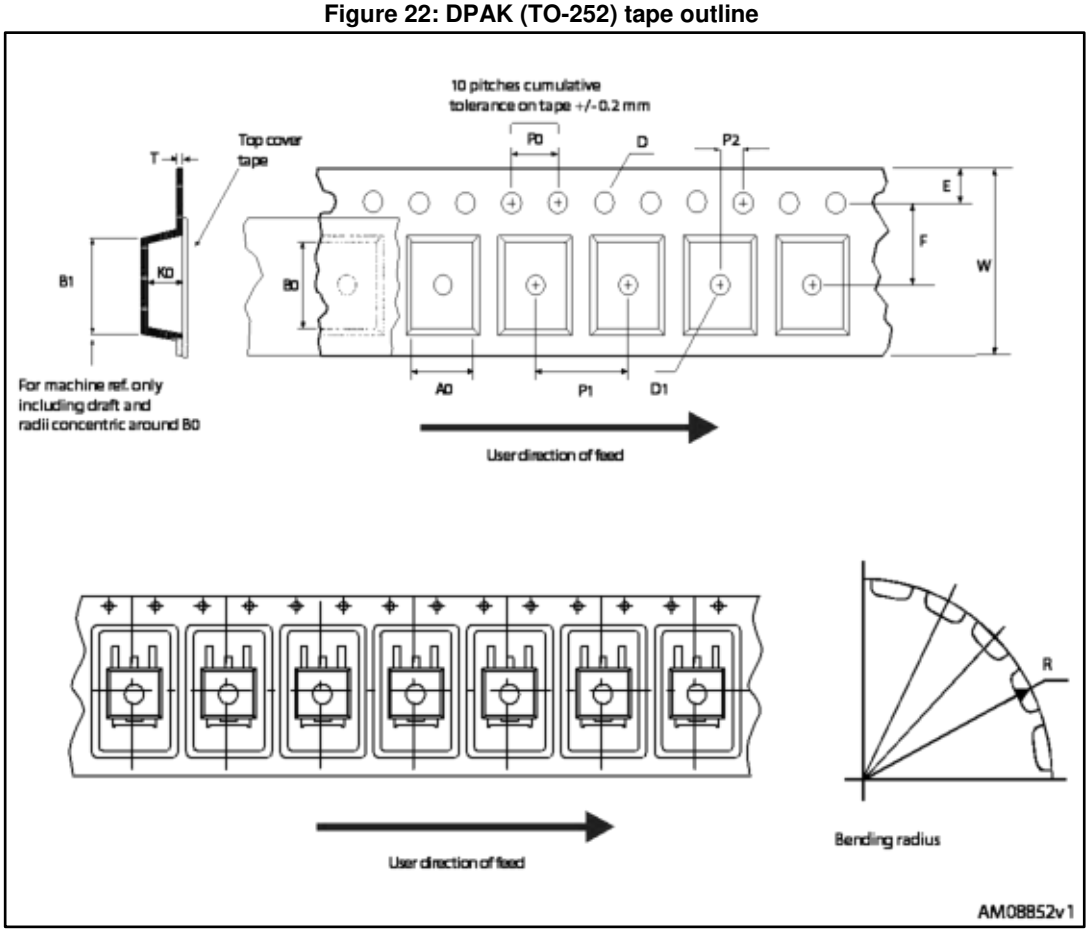


Figure 23: DPAK (TO-252) reel outline

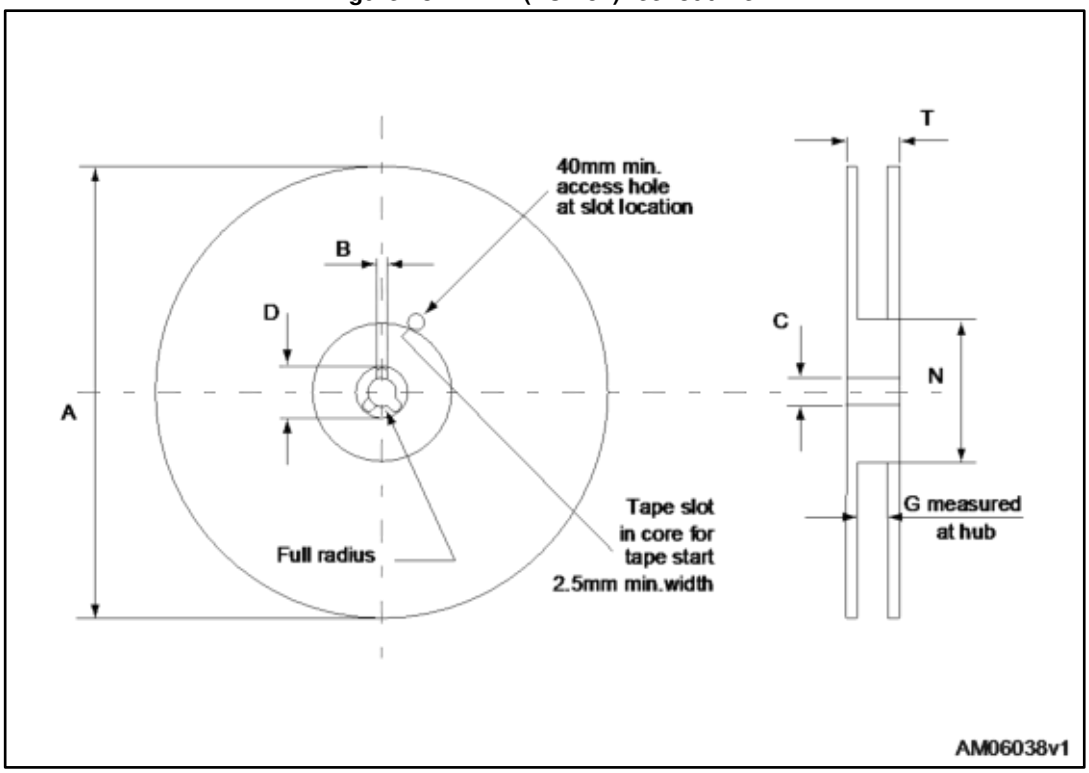


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
20-Jun-2017	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved