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STK57FU394AG-E

2-in-1 PFC and Inverter Intelligent Power Module (IPM), 600 V, 15 A

The STK57FU394AG-E is a fully-integrated PFC and inverter power stage consisting of a high-voltage driver, six motor drive IGBT's, one PFC IGBT, one PFC rectifier and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors.

The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

An internal comparator and reference connected to the over-current protection circuit allows the designer to set individual over-current protection levels for the PFC and the inverter stages. Additionally, the power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions.

Features

- Simple thermal design with PFC and inverter stage in one package.
- PFC operating frequency up to 40kHz
- Cross-conduction protection
- Adjustable over-current protection level
- Integrated bootstrap diodes and resistors

Certification

- UL1557 (File Number : E339285)

Typical Applications

- Heat Pumps
- Home Appliances
- Industrial Fans
- Industrial Pumps

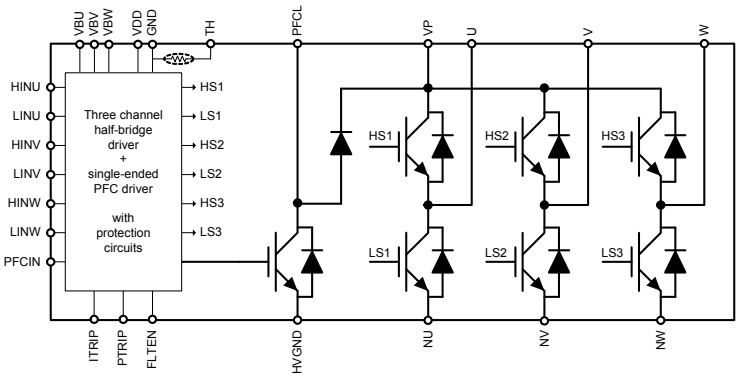
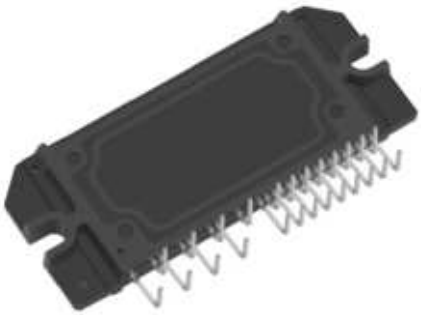


Figure 1. Functional Diagram

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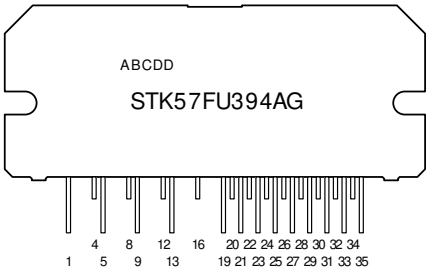
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PACKAGE PICTURE



SIP35 56x25.8 / SIP2A-3

MARKING DIAGRAM



STK57FU394AG = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot Code
Device marking is on package top side

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK57FU394AG-E	SIP35 56x25.8 / SIP2A-3 (Pb-Free)	8 / Tube

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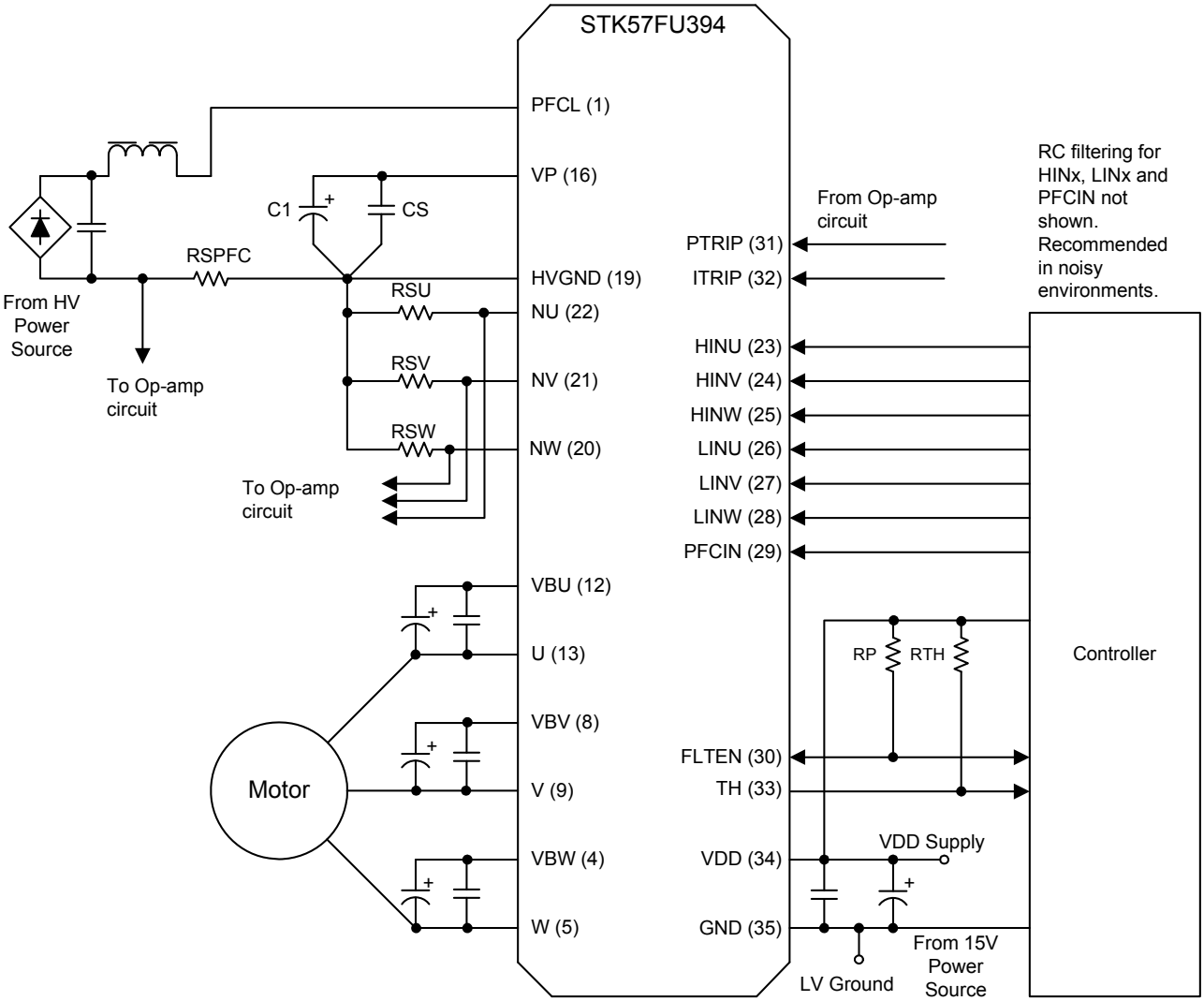


Figure 2. Application Schematic

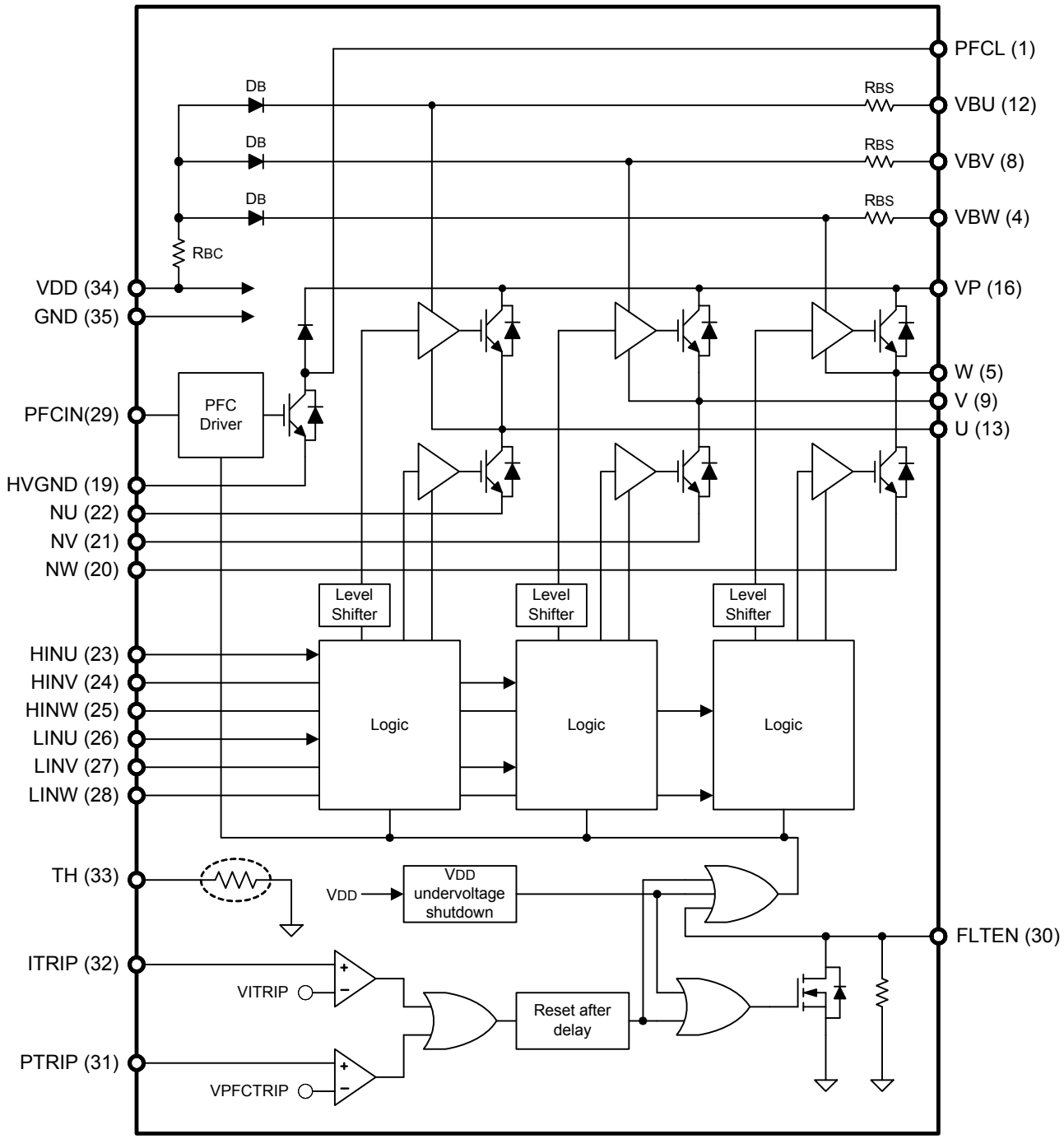


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	PFCL	PFC Inductor Connection to IGBT and Rectifier node
4	VBW	High Side Floating Supply voltage for W phase
5	W	V phase output. Internally connected to W phase high side driver ground
8	VBV	High Side Floating Supply voltage for V phase
9	V	V phase output. Internally connected to V phase high side driver ground
12	VBU	High Side Floating Supply voltage for U phase
13	U	U phase output. Internally connected to U phase high side driver ground
16	VP	Positive PFC Output Voltage
19	HVGND	Negative PFC Output Voltage
20	NW	Low Side Emitter Connection - Phase W
21	NV	Low Side Emitter Connection - Phase V
22	NU	Low Side Emitter Connection - Phase U
23	HINU	Logic Input High Side Gate Driver - Phase U
24	HINV	Logic Input High Side Gate Driver - Phase V
25	HINW	Logic Input High Side Gate Driver - Phase W
26	LINU	Logic Input Low Side Gate Driver - Phase U
27	LINV	Logic Input Low Side Gate Driver - Phase V
28	LINW	Logic Input Low Side Gate Driver – Phase W
29	PFCIN	Logic Input PFC Gate Driver
30	FLTEN	Bidirectional FAULT output and ENABLE input
31	PTRIP	Current protection pin for PFC
32	ITRIP	Current protection pin for inverter
33	TH	Thermistor output
34	VDD	+15V Main Supply
35	GND	Negative Main Supply

Note: Pins 2, 3, 6, 7, 10, 11, 14, 15, 17 and 18 are not present

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Tc=25°C unless otherwise noted.

Rating		Symbol	Conditions	Value	Unit
PFC Section					
PFC IGBT	Collector-emitter voltage	V_{CE}	PFCL to HVGND	600	V
	Repetitive peak collector current	ICP	Duty cycle 10%, pulse width 1ms	72	A
	Collector current	IC		36	A
			Tc=100°C	18	A
	Maximum power dissipation	PC		73	W
PFC Diode	Diode reverse voltage	VRM	VP to PFCL	600	V
	Repetitive peak forward current	IFP1	Duty cycle 10%, pulse width 1ms	60	A
	Diode forward current	IF1		30	A
			Tc=100°C	15	A
	Maximum power dissipation	PD1		56	W
Anti-parallel Diode	Repetitive peak forward current	IFP2	Duty cycle 10%, pulse width 1ms	11	A
	Diode forward current	IF2		5	A
	Maximum power dissipation	PD2		10	W
Maximum AC input voltage		VAC	Single-phase Full-rectified	264	V
Maximum output voltage		Vo	In the Application Circuit (VAC=200V)	450	V
Input AC current (steady state)		Iin		15	Arms
Inverter Section					
Supply voltage		V_{CC}	VP to NU, NV, NW surge < 500V (Note 3)	450	V
Collector-emitter voltage		V_{CE} max	VP to U, V, W or U to NU, V to NV, W to NW	600	V
Output current		Io	VP, U, V, W, NU, NV, NW terminal current	±15	A
			VP, U, V, W, NU, NV, NW terminal current at Tc=100°C	±8	A
Output peak current		Iop	VP, U, V, W, NU, NV, NW terminal current, pulse width 1ms	±30	A
Maximum power dissipation		Pd	IGBT per 1 channel	35	W
Gate driver section					
Gate driver supply voltage		V_{BS}, V_{DD}	VBU to U, VBV to V, VBW to W, VDD to GND (Note 4)	−0.3 to +20.0	V
Input signal voltage		VIN	HINU, HINV, HINW, LINU, LINV, LINW, PFCIN	−0.3 to V_{DD}	V
FLTEN terminal voltage		VFLTEN	FLTEN terminal	−0.3 to V_{DD}	V
ITRIP terminal voltage		VITRIP	ITRIP terminal	−0.3 to +10.0	V
PFCTRIP terminal voltage		VPTRIP	PTRIP terminal	−1.5 to +2.0	V
Intelligent Power Module					
Junction temperature		Tj	IGBT, FRD, Gate driver IC	150	°C
Storage temperature		Tstg		−45 to +125	°C
Operating case temperature		Tc	IPM case temperature	−30 to +100	°C
Tightening torque		MT	Case mounting screws	0.9	Nm
Isolation voltage		Vis	50Hz sine wave AC 1 minute (Note 5)	2000	Vrms

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between VP and NU, NV, NW terminals.
4. VBS=VBU to U, VBV to V, VBW to W
5. Test conditions : AC2500V, 1 s

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol		Min	Typ	Max	Unit
Supply voltage	V_{CC}	VP to HVGND, NU, NV, NW	0	280	400	V
Gate driver supply voltage	V_{BS}	VBU to U, VBV to V, VBW to W	12.5	15	17.5	V
	V_{DD}	V_{DD} to GND (Note 6)	13.5	15	16.5	V
ON-state input voltage	VIN(ON)	HINU, HINV, HINW, LINU, LINV, LINW, PFCIN	2.5	-	5.0	V
OFF-state input voltage	VIN(OFF)		0	-	0.3	V
PWM frequency(PFC)	fPWMp		1	-	40	kHz
PWM frequency(Inverter)	fPWMi		1	-	20	kHz
Dead time	DT	Turn-off to Turn-on (external)	1.5	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M3' type screw	0.6	-	0.9	Nm

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 7)

Tc=25°C, V_{BIAS} (V_{BS}, V_{DD})=15V unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PFC Section						
Collector-emitter cut-off current	V_{CE}=600V	I_{CE}	-	-	0.1	mA
Reverse leakage current (PFC Diode)	VR=600V	IR	-	-	0.1	mA
Collector-emitter saturation voltage	IC=30A, Tj=25°C	V_{CE}(sat)	-	1.9	2.5	V
	IC=15A, Tj=100°C		-	1.6	-	V
Diode forward voltage (PFC Diode)	IF=30A, Tj=25°C	VF1	-	2.0	2.6	V
	IF=15A, Tj=100°C		-	1.5	-	
Diode forward voltage (Anti-parallel Diode)	IF=5A, Tj=25°C	VF2	-	1.7	2.3	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	-	1.7	°C/W
	PFC Diode	θj-c(D)	-	-	2.2	°C/W
Switching characteristics						
Switching time	IC=30A, VP=300V, Tj=25°C	tON	0.1	0.3	0.8	μs
		tOFF	0.1	0.4	0.9	μs
Diode reverse recovery time		trr	-	60	-	ns
Inverter section						
Collector-emitter leakage current	V_{CE}=600V	I_{CE}	-	-	100	μA
Bootstrap diode reverse current	VR(DB)=600V	IR(BD)	-	-	100	μA
Collector to emitter saturation voltage	IC=15A, Tj=25°C	V_{CE}(SAT)	-	2.0	2.6	V
	IC=8A, Tj=100°C		-	1.7	-	V
Diode forward voltage	IF=15A, Tj=25°C	VF	-	2.1	2.7	V
	IF=8A, Tj=100°C		-	1.7	-	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	-	3.5	°C/W
Junction to case thermal resistance	FRD	θj-c(D)	-	-	7.2	°C/W
Switching time	IC = 15A, V_{CC}=300V, Tj=25°C	t_{ON}	0.1	0.5	1.0	μs
		t_{OFF}	0.2	0.7	1.2	μs
Turn-on switching loss	IC = 15A, V_{CC}=300V, Tj=25°C	E_{ON}	-	200	-	μJ
Turn-off switching loss		E_{OFF}	-	150	-	μJ
Total switching loss		E_{TOT}	-	350	-	μJ
Turn-on switching loss	IC = 15A, V_{CC}=300V, Tj=100°C	E_{ON}	-	300	-	μJ
Turn-off switching loss		E_{OFF}	-	200	-	μJ
Total switching loss		E_{TOT}	-	500	-	μJ
Diode reverse recovery energy	IC = 15A, V_{CC}=300V, Tj=100°C (di/dt set by internal driver)	E_{REC}	-	100	-	μJ
Diode reverse recovery time		trr	-	200	-	ns
Reverse bias safe operating area	Ic=30A, V_{CE}=450V	RBSOA	Full Square	-		
Short circuit safe operating area	V_{CE}=400V, Tj=100°C	SCSOA	4	-	-	μs
Allowable offset voltage slew rate	U to NU, V to NV, W to NW	dv/dt	−50	-	50	V/ns

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Driver Section						
Gate driver consumption current	V_{BS}=15V (Note 4), per driver	ID	-	0.08	0.4	mA
	V_{DD}=15V, total	ID	-	0.85	2.4	mA
High level Input voltage	HINU, HINV, HINW, LINU, LINV, LINW, PFCIN to GND	VIN H	2.5	-	-	V
Low level Input voltage		VIN L	-	-	0.8	V
Logic 1 input current	VIN=+3.3V	I_{IN+}	-	100	143	μA
Logic 0 input current	VIN=0V	I_{IN-}	-	-	2	μA
Bootstrap diode forward voltage	IF=0.1A	VF(DB)	-	0.8	-	V
Bootstrap circuit resistance	Resistor value for common boot charge line	RBC	-	22	-	Ω
	Resister values for separate boot charge lines	RBS	-	22	-	Ω
FLTEN terminal sink current	FLTEN : ON / VFAULT=0.1V	IoSD	-	2	-	mA
FLTEN clearance delay time		FLTCLR	1.3	1.65	2.0	ms
FLTEN Threshold	VEN ON-state voltage	VEN(ON)	2.5	-	-	V
	VEN OFF-state voltage	VEN(OFF)	-	-	0.8	V
ITRIP threshold voltage	ITRIP to GND	VITRIP	0.44	0.49	0.54	V
PTRIP threshold voltage	PTRIP to GND	VPTRIP	−0.37	−0.31	−0.25	V
ITRIP to shutdown propagation delay		tITRIP	490	600	850	ns
PTRIP to shutdown propagation delay		tPTRIP	440	550	800	ns
ITRIP and PTRIP blanking time		$t_{ITRIPBL}$ $t_{PFCTRIPBL}$	290	350	-	ns
V_{DD} and V_{BS} supply undervoltage positive going input threshold		V_{DDUV+} V_{BSUV+}	10.5	11.1	11.7	V
V_{DD} and V_{BS} supply undervoltage negative going input threshold		V_{DDUV-} V_{BSUV-}	10.3	10.9	11.5	V
V_{DD} and V_{BS} supply undervoltage lockout hysteresis		V_{DDUVH} V_{BSUVH}	0.14	0.2	-	V

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS PFC SECTION

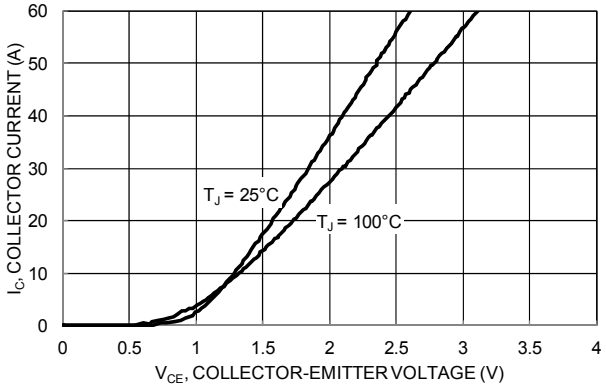


Figure 4. V_{CE} versus IC for different temperatures (V_{DD}=15V)

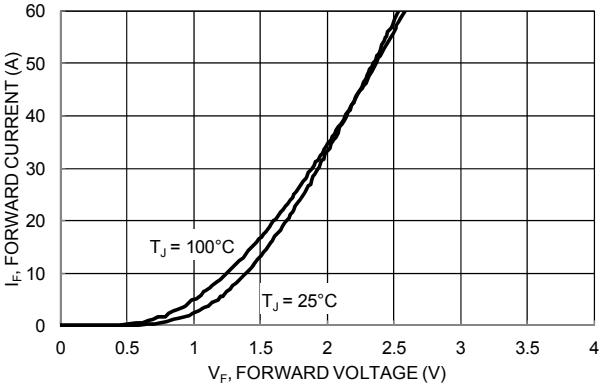


Figure 5. PFC Diode VF versus IF for different temperatures

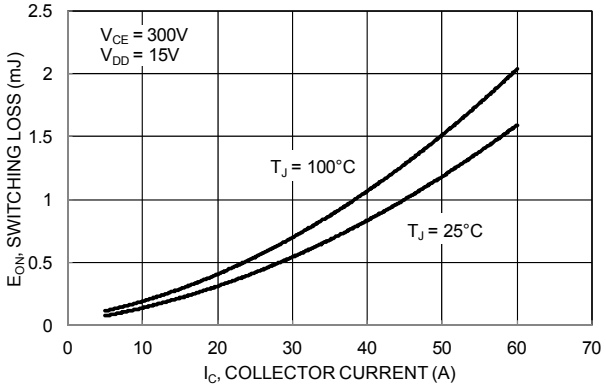


Figure 6. EON versus IC for different temperatures

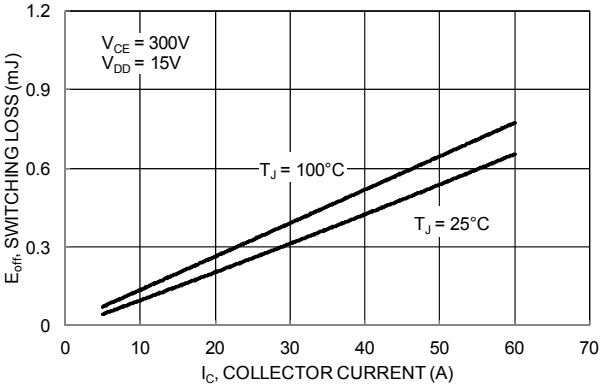


Figure 7. EOFF versus IC for different temperatures

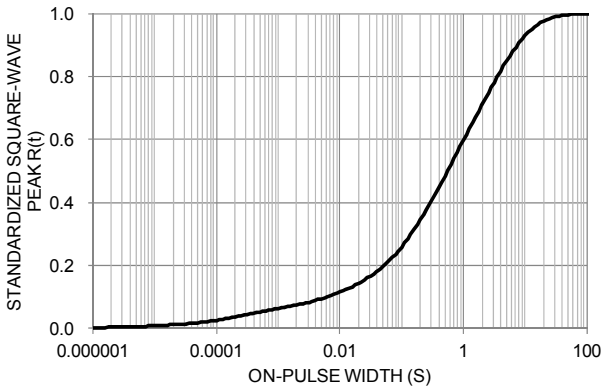


Figure 8. Thermal Impedance Plot

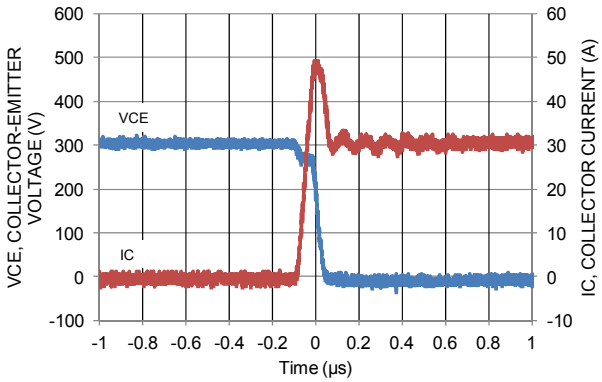


Figure 9. Turn-on waveform Tj=100°C, V_{CC}=300V

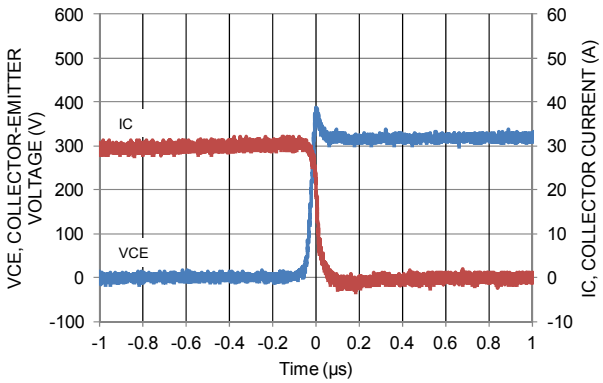


Figure 10. Turn-off waveform Tj=100°C, V_{CC}=300V

TYPICAL CHARACTERISTICS INVERTER SECTION

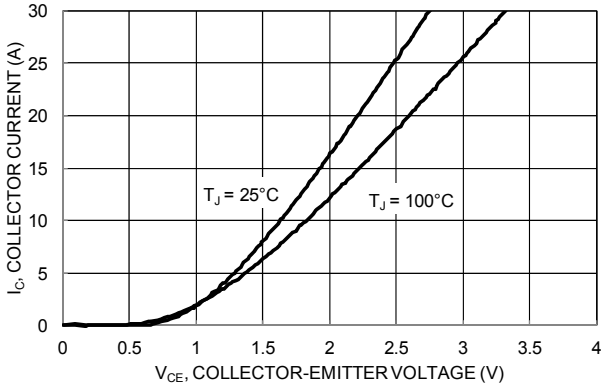


Figure 11. V_{CE} versus ID for different temperatures (V_{DD}=15V)

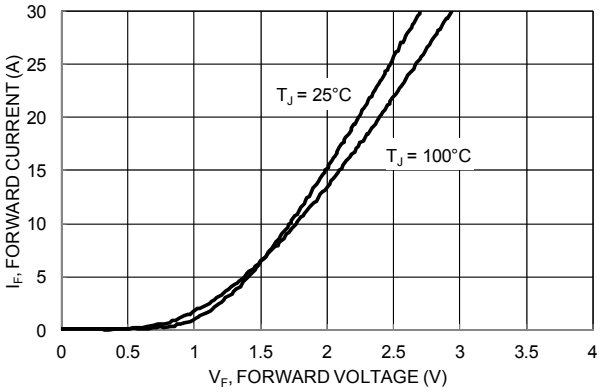


Figure 12. VF versus ID for different temperatures

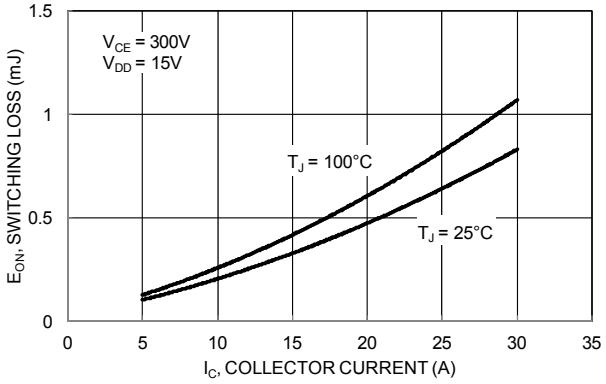


Figure 13. EON versus ID for different temperatures

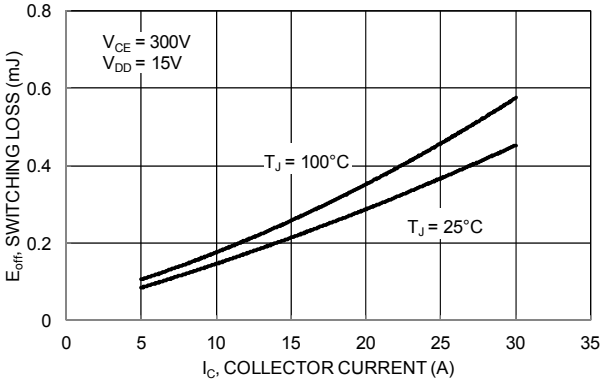


Figure 14. EOFF versus ID for different temperatures

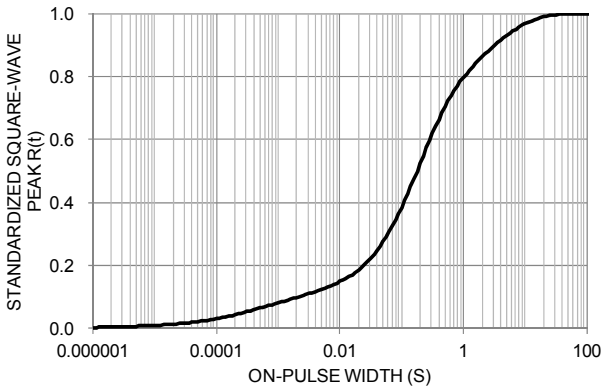


Figure 15. Thermal Impedance Plot

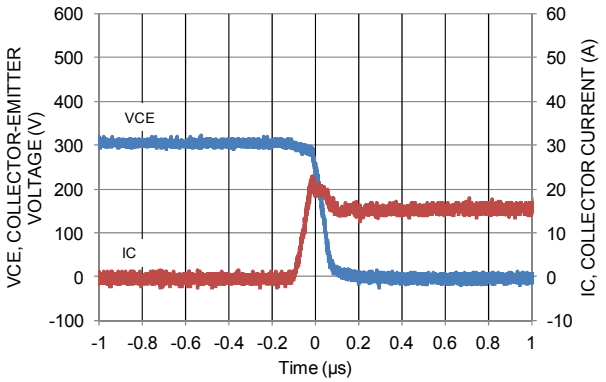


Figure 16. Turn-on waveform Tj=100°C, V_{CC}=300V

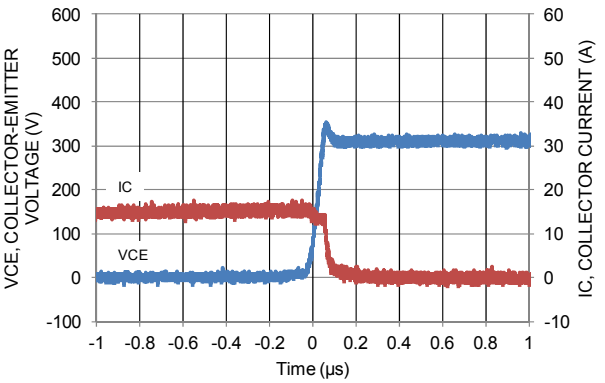


Figure 17. Turn-off waveform Tj=100°C, V_{CC}=300V

APPLICATIONS INFORMATION

Input / Output Timing Chart

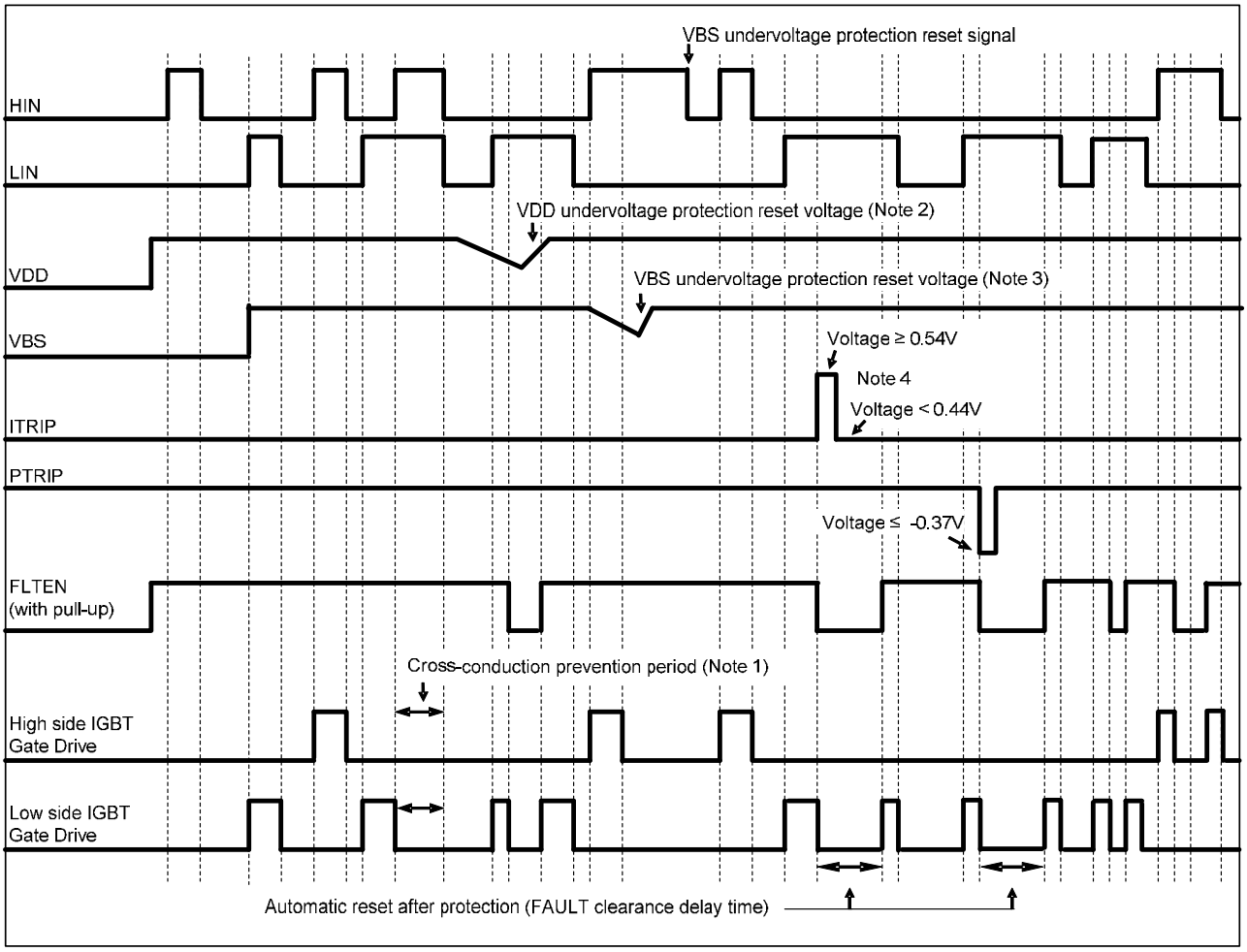


Figure 18. Input / Output Timing Chart

Notes

1. This section of the timing diagram shows the effect of cross-conduction prevention.
2. This section of the timing diagram shows that when the voltage on V_{DD} decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on V_{DD} rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage on VBU (VBV, VBW) drops, the corresponding high side output U (V, W) is switched off. When the voltage on VBU (VBV, VBW) rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed. Similarly, when the voltage on PTRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed
5. After V_{DD} has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Input / Output Logic Table

INPUT				OUTPUT			
HIN	**LIN**	**ITRIP**	**PTRIP**	**High side IGBT**	**Low side IGBT**	**U,V,W**	**FAULT**
H	L	L	L	ON (Note 5)	OFF	VP	OFF
L	H	L	L	OFF	ON	NU,NV,NW	OFF
L	L	L	L	OFF	OFF	High Impedance	OFF
H	H	L	L	OFF	OFF	High Impedance	OFF
X	X	H	X	OFF	OFF	High Impedance	ON
X	X	X	H	OFF	OFF	High Impedance	ON

Thermistor characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc=25℃	99	100	101	kΩ
	R_{100}	Tc=100℃	5.18	5.38	5.60	kΩ
B-Constant (25 to 50℃)	B		4208	4250	4293	K
Temperature Range			−40		+125	℃

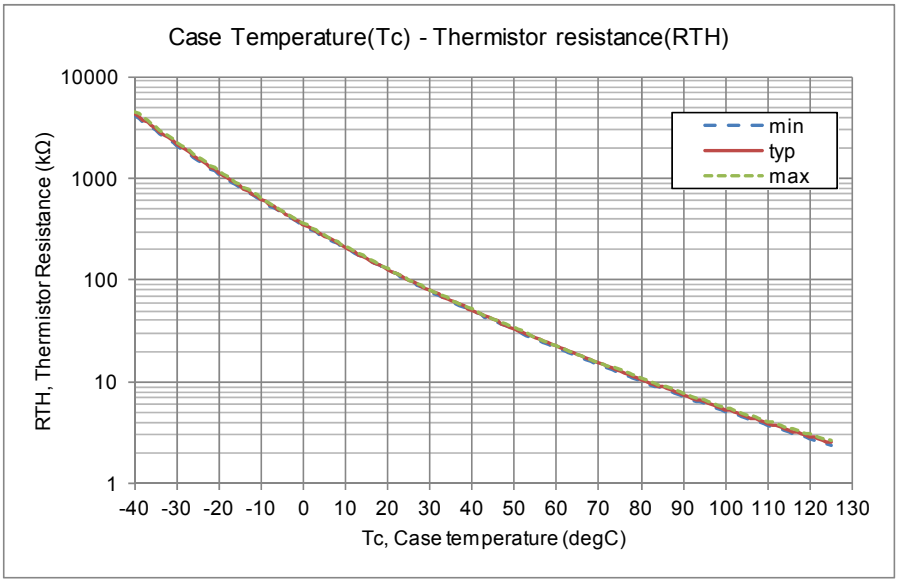


Figure 19. Thermistor Resistance versus Case Temperature

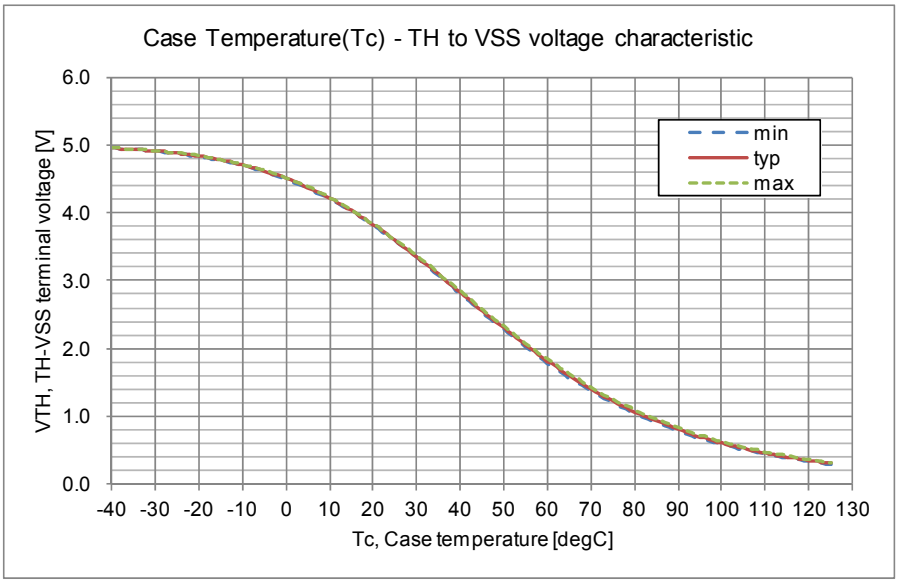


Figure 20. Thermistor Voltage versus Case Temperature
Conditions: RTH=39kΩ, pull-up voltage 5.0V (see Figure 2)

Signal inputs
Each signal input has a pull-down resistor. An additional pull-down resistor of between 2.2kΩ and 3.3kΩ is recommended on each input to improve noise immunity.

FLTEN pin
The FLTEN pin is connected to an open-drain FAULT output requiring a pull-up resistor and an ENABLE input. If the pull-up voltage is 5V, use a pull-up resistor with a value of 6.8kΩ or higher. If the pull-up voltage is 15V, use a pull-up resistor with a value of 20kΩ or higher. The pulled up voltage in normal operation for the FLTEN pin should be above 2.5V, noting that it is connected to an internal ENABLE input. The FAULT output is triggered if there is a VDD undervoltage or an overcurrent condition on either the PFC or inverter stages.
Driving the FLTEN terminal pin is used to enable or shut down the built-in driver. If the voltage on the FLTEN pin rises above the positive going FLTEN threshold, the output drivers are enabled. If the voltage on the FLTEN pin falls below the negative going FLTEN threshold, the drivers are disabled.

Undervoltage protection
If VDD goes below the VDD supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply undervoltage lockout rising threshold. The hysteresis is approximately 200mV.

Overcurrent protection
An over-current condition is detected if the voltage on the ITRIP/PTRIP pin is larger than the reference voltage. There is a blanking time of typically 350ns to improve noise immunity. After a shutdown propagation delay of typically 0.6 us, the FAULT output is switched on.

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (Io).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

Capacitors on High Voltage and VDD supplies
Both the high voltage and VDD supplies require an electrolytic capacitor and an additional high frequency capacitor. The recommended value of the high frequency capacitor is between 100nF and 10 μF.

Minimum input pulse width
When input pulse width is less than 1μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of bootstrap capacitor value
The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- V_{BS}: Bootstrap power supply.
  15V is recommended.
- QG: Total gate charge of IGBT at V_{BS}=15V.
  53nC
- UVLO: Falling threshold for UVLO.
  Specified as 12V.
- IDMAX: High side drive power dissipation.
  Specified as 0.4mA
- TONMAX: Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + IDMAX * TONMAX)/(V_{BS} - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply. If the capacitors selected are 47 μF or more, a series resistor of 20Ω should be added in series with the three capacitors to limit the current. The resistors should be inserted between VBU and U, VBV and V and VBW and W.

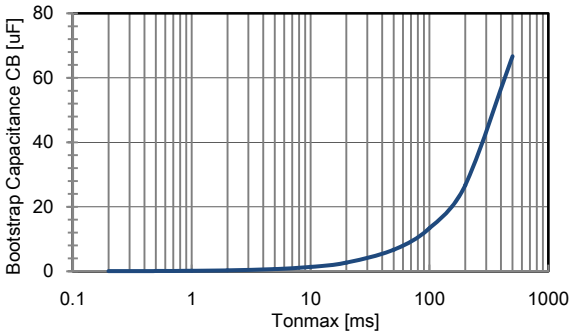


Figure 21. Bootstrap capacitance versus Tonmax

Mounting Instructions

Item	Recommended Condition
Pitch	56.0±0.1mm (Please refer to Package Outline Diagram)
Screw	diameter : M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer The size is D:7mm, d:3.2mm and t:0.5mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 20 to 30 % of final tightening on first screw Temporary tightening : 20 to 30 % of final tightening on second screw Final tightening : 0.6 to 0.9Nm on first screw Final tightening : 0.6 to 0.9Nm on second screw
Grease	Silicone grease. Thickness : 100 to 200 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

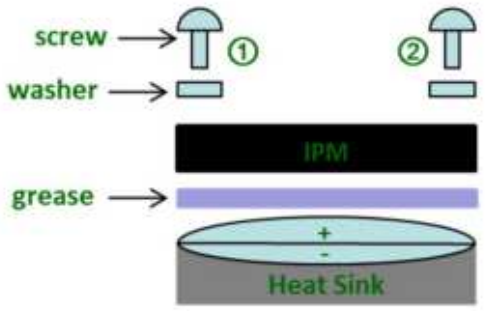


Figure 22. Mount IPM on a Heat Sink

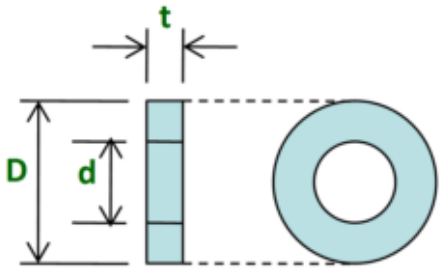


Figure23. Size of Washer

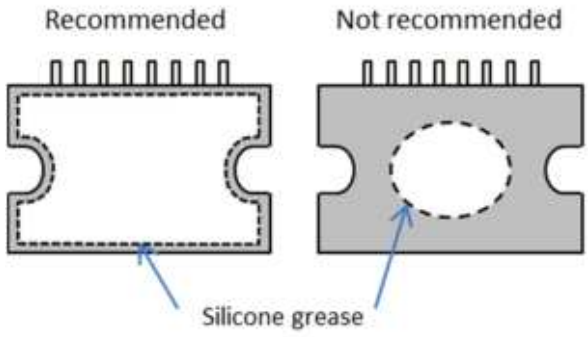


Figure24. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink
1st: Temporarily tighten maintaining a left/right balance.
2nd: Finally tighten maintaining a left/right balance.

TEST CIRCUITS

■ I_{CE}, $I_{R(DB)}$

	U+	V+	W+	U-	V-	W-	PFC IGBT
A	16	16	16	13	9	5	1
B	13	9	5	22	21	20	19

U+,V+,W+ : High side phase
U-,V-,W- : Low side phase

	U(DB)	V(DB)	W(DB)	PFC Diode
A	12	8	4	16
B	35	35	35	1

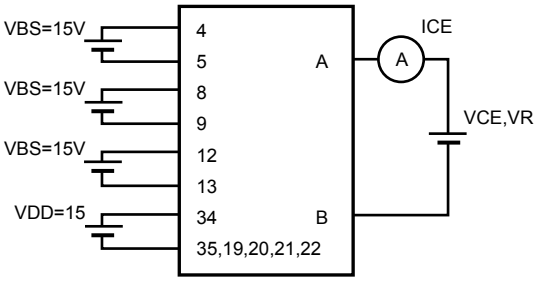


Figure 25. Test Circuit for ICE

■ $V_{CE(sat)}$ (Test by pulse)

	U+	V+	W+	U-	V-	W-	PFC IGBT
A	16	16	16	13	9	5	1
B	13	9	5	22	21	20	19
C	23	24	25	26	27	28	29

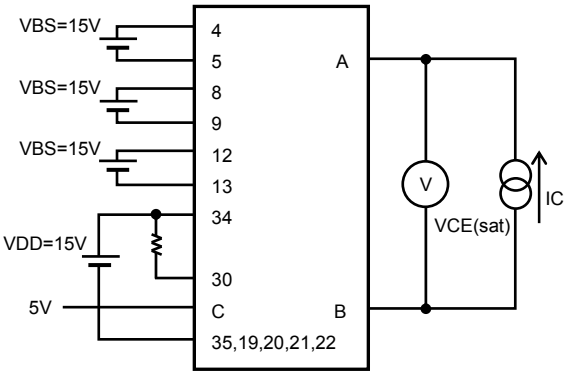


Figure 26. Test circuit for $V_{CE(SAT)}$

■ V_F (Test by pulse)

	U+	V+	W+	U-	V-	W-
A	16	16	16	13	9	5
B	13	9	5	22	21	20

	U(DB)	V(DB)	W(DB)	PFC Diode	Anti-parallel Diode
A	12	8	4	16	1
B	34	34	34	1	19

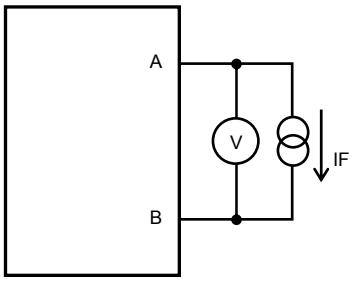


Figure 27. Test circuit for V_F

■ I_D

	VBS U+	VBS V+	VBS W+	V_{DD}
A	12	8	4	34
B	13	9	5	35

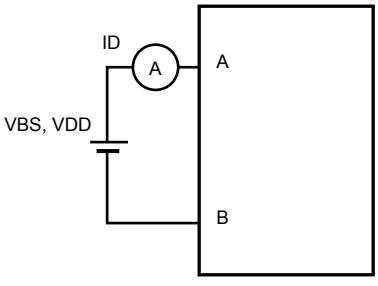
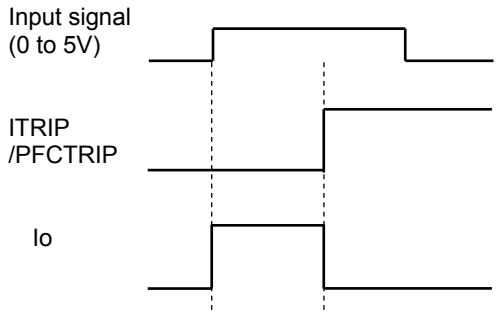


Figure 28. Test circuit for I_D

■ V_{ITRIP}, V_{PTRIP}

	VITRIP(U-)	VPTRIP
A	13	1
B	22	19
C	26	29
D	32	31



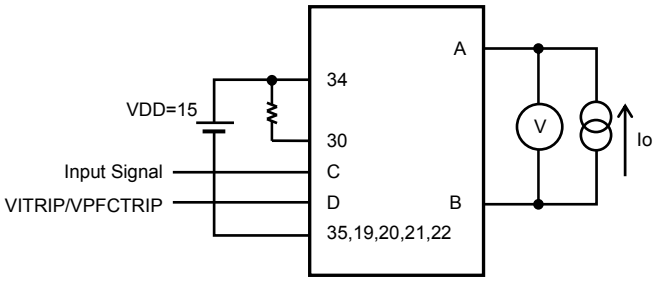
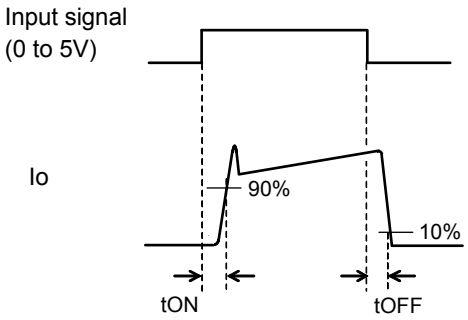


Figure 29. Test circuit for ITRIP.PTRIP

■ Switching time (The circuit is a representative example of the lower side U phase.)

	U+	V+	W+	U-	V-	W-	PFC IGBT
A	16	16	16	16	16	16	16
B	22	21	20	22	21	20	19
C	13	9	5	13	9	5	1
D	22	21	20	16	16	16	16
E	23	24	25	26	27	28	29



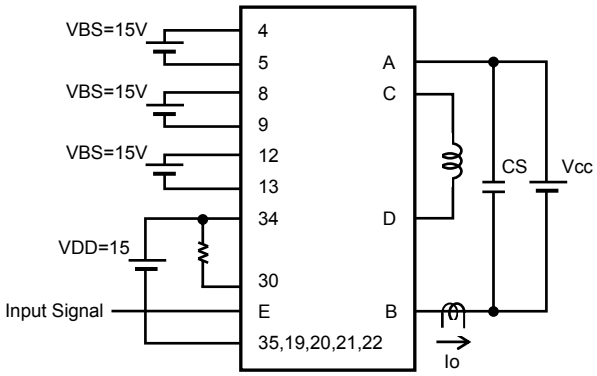
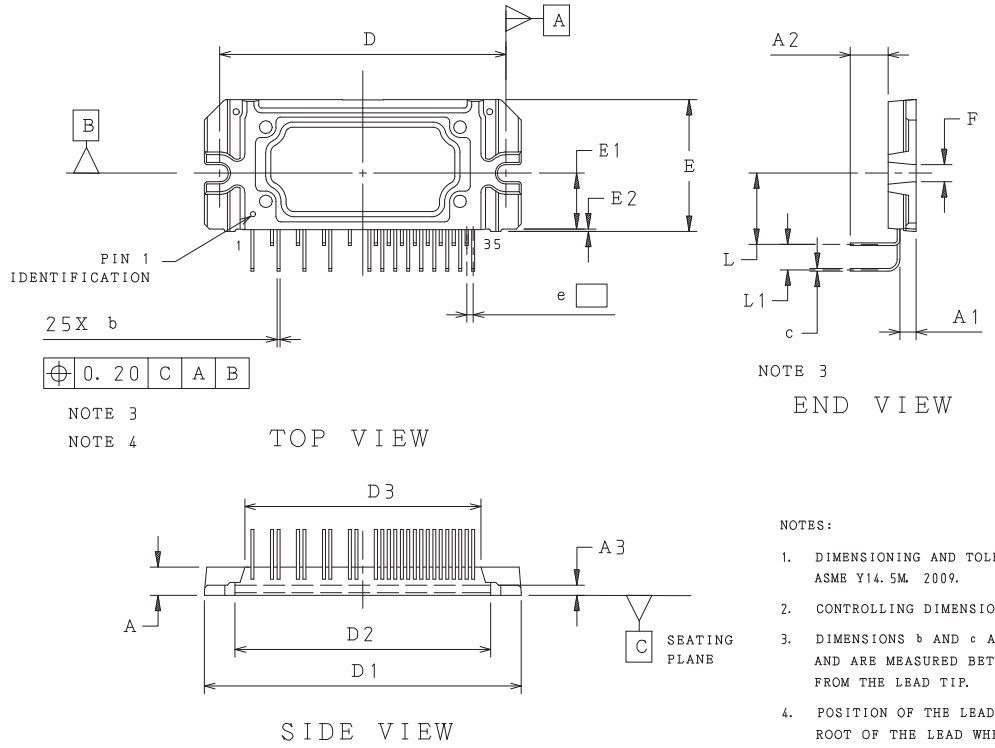


Figure 30. Test circuit for switching time

Package Dimensions

unit : mm

SIP35 56x25.8 / SIP2A-3
CASE 127DY
ISSUE O



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	5.00	5.50	6.00
A1	2.70	3.20	3.70
A2	6.90	7.40	7.90
A3	1.50	2.00	2.50
b	0.55	0.60	0.80
c	0.45	0.50	0.70
D	55.50	56.00	56.50
D1	61.50	62.00	62.50
D2	49.50	50.00	50.50
D3	45.70	46.20	46.70
E	25.30	25.80	26.30
E1	10.90 REF		
E2	0.00	0.50	1.00
e	1.27 BSC		
F	2.90	3.40	3.90
L	13.40	13.90	14.40
L1	4.50	5.00	5.50

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M. 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND c APPLY TO THE PLATED LEAD AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEADS IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. MIRROR SURFACE MARK INDICATES PIN 1 POSITION.
6. MISSING PINS ARE: 2. 3. 6. 7. 10. 11. 14. 15. 17. AND 18.

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