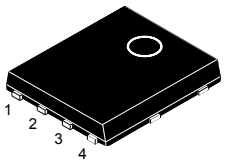
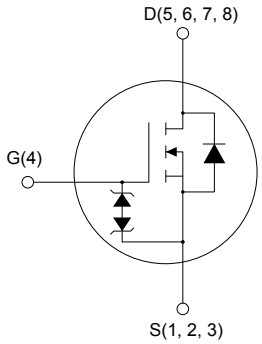
N-channel 600 V, 550 mΩ typ., 5.5 A, MDmesh™ M6 Power MOSFET in a PowerFLAT™ 5x6 HV package



PowerFLAT™ 5x6 HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL10N60M6	600 V	660 mΩ	5.5 A	48 W

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs.
STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link
STL10N60M6

Product summary	
Order code	STL10N60M6
Marking	10N60M6
Package	PowerFLAT™ 5x6 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	5.5	A
	Drain current (continuous) at T_{case} = 100 °C	3.5	
I_{DM}(1)	Drain current (pulsed)	16	A
P_{TOT}	Total power dissipation at T_{case} = 25 °C	48	W
I_{AR}(2)	Avalanche current, repetitive or not repetitive	1.4	A
E_{AS}(3)	Single pulse avalanche energy	120	mJ
dv/dt(4)	Peak diode recovery voltage slope	15	V/ns
dv/dt(5)	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *Pulse width limited by T_{jmax}.*
3. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*
4. *I_{SD} ≤ 5.5 A, di/dt = 400 A/µs, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 400 V*
5. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.6	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.75 A		550	660	mΩ

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	338	-	pF
C_{oss}	Output capacitance		-	26.2	-	
C_{rss}	Reverse transfer capacitance		-	3.8	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	59	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 6.4 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	8.8	-	nC
Q_{gs}	Gate-source charge		-	4.8	-	
Q_{gd}	Gate-drain charge		-	2.7	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 3.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	11	-	ns
t_r	Rise time		-	8.2	-	
$t_{d(off)}$	Turn-off delay time		-	23	-	
t_f	Fall time		-	10	-	

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		16	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 5.5 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 6.4 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	155		ns
Q_{rr}	Reverse recovery charge		-	0.813		µC
I_{RRM}	Reverse recovery current		-	10.5		A
t_{rr}	Reverse recovery time	I_{SD} = 6.4 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	250		ns
Q_{rr}	Reverse recovery charge		-	1.35		µC
I_{RRM}	Reverse recovery current		-	10.8		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

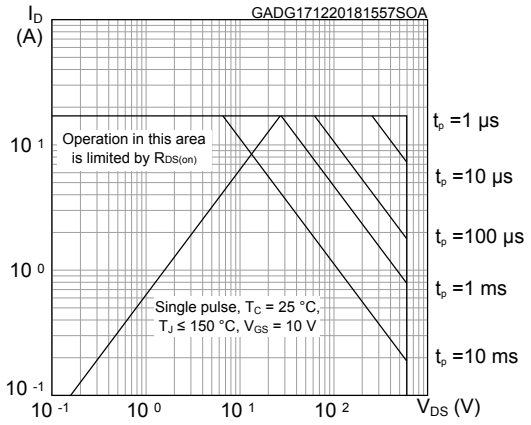


Figure 2. Thermal impedance

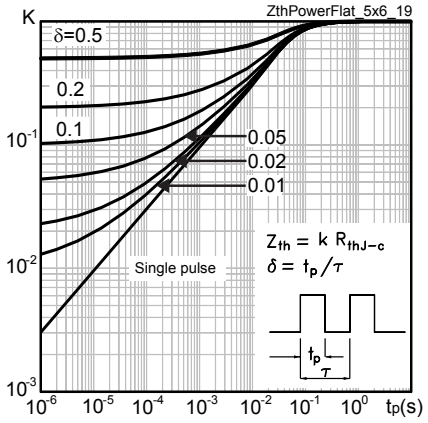


Figure 3. Output characteristics

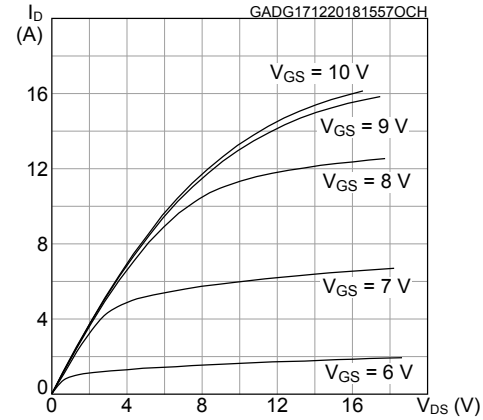


Figure 4. Transfer characteristics

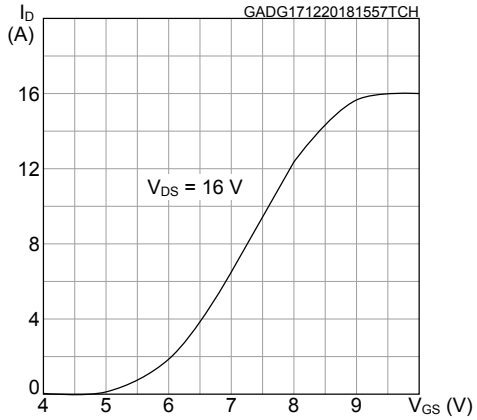


Figure 5. Gate charge vs gate-source voltage

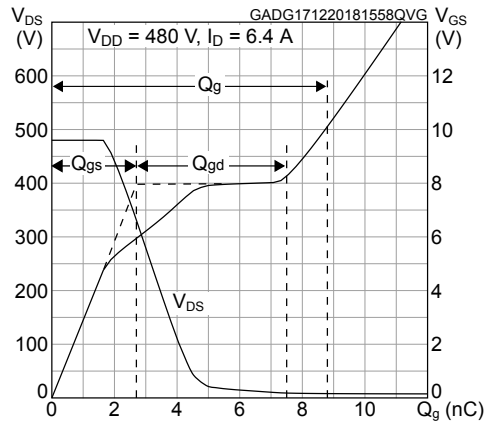


Figure 6. Static drain-source on-resistance

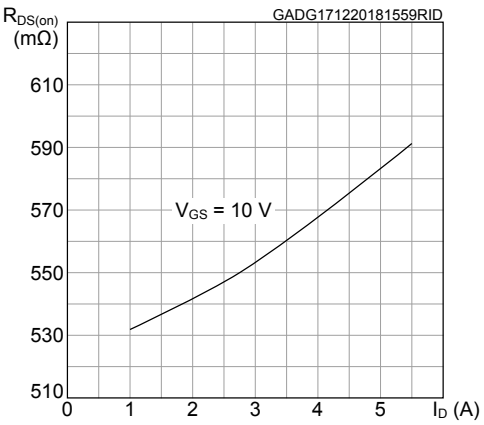


Figure 7. Capacitance variations

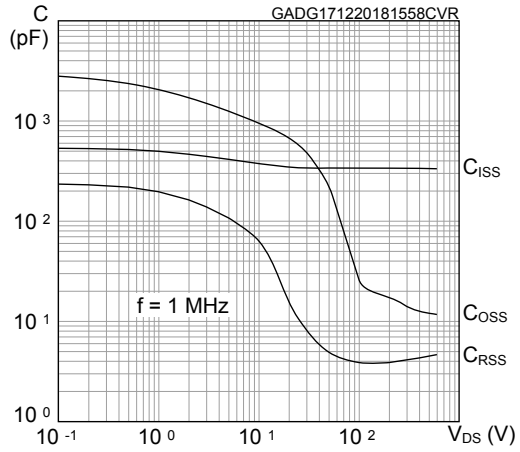


Figure 8. Output capacitance stored energy

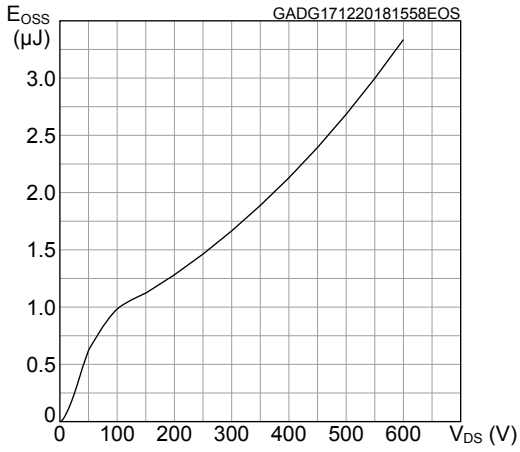


Figure 9. Normalized gate threshold voltage vs temperature

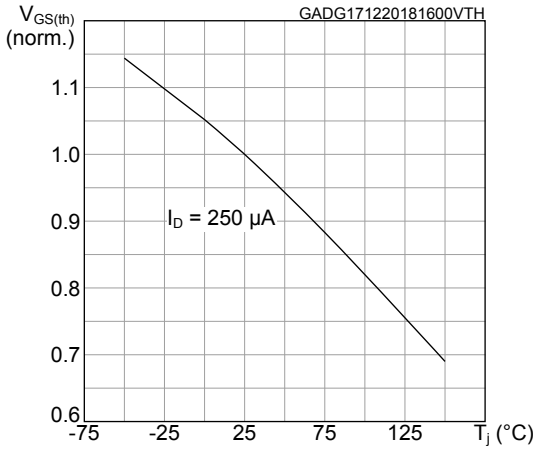


Figure 10. Normalized on-resistance vs temperature

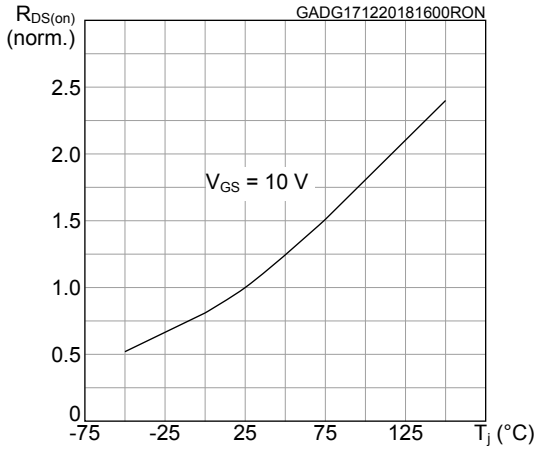


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

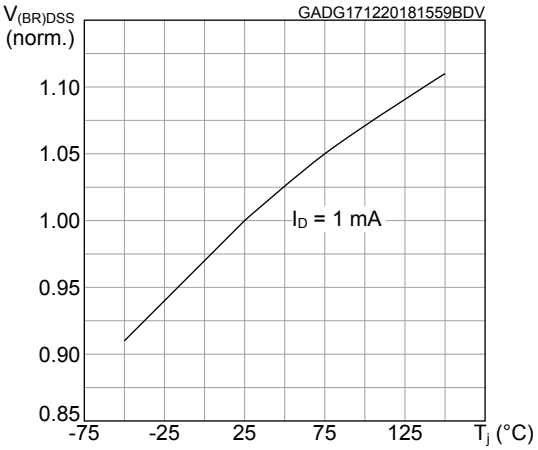
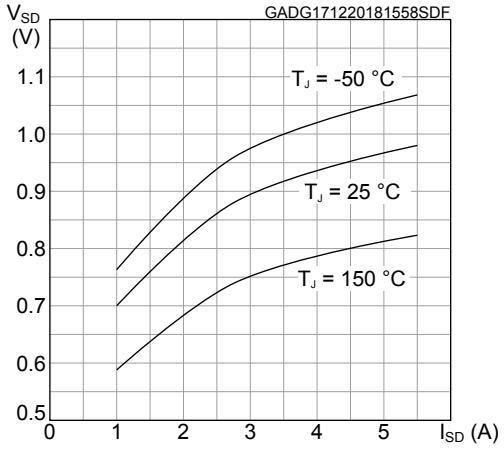


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

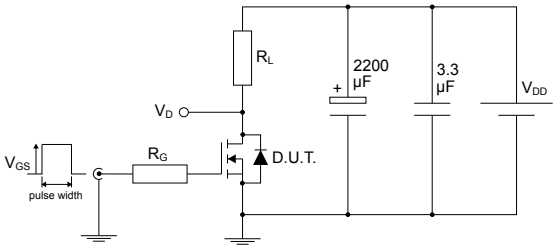


Figure 14. Test circuit for gate charge behavior

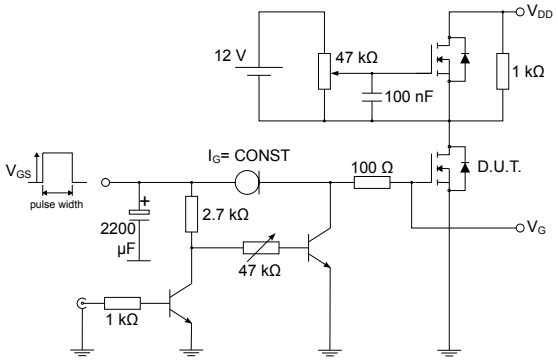


Figure 15. Test circuit for inductive load switching and diode recovery times

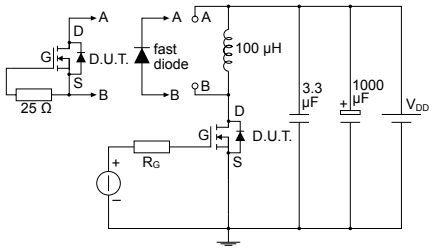


Figure 16. Unclamped inductive load test circuit

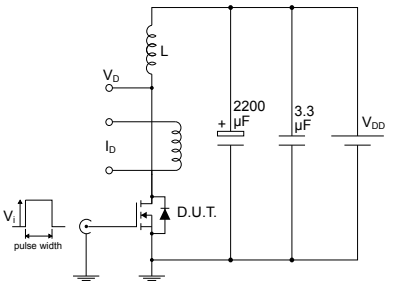


Figure 17. Unclamped inductive waveform

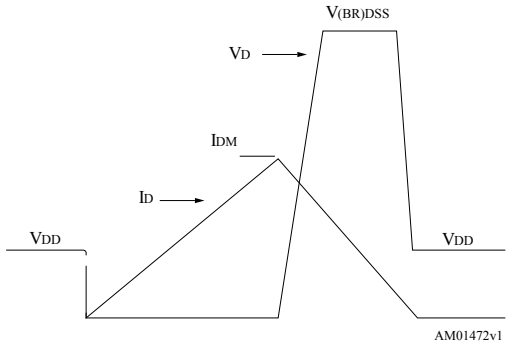
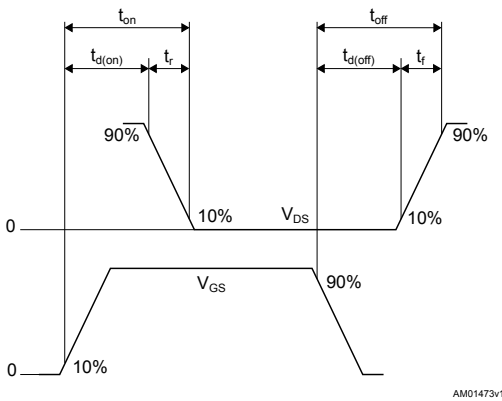


Figure 18. Switching time waveform

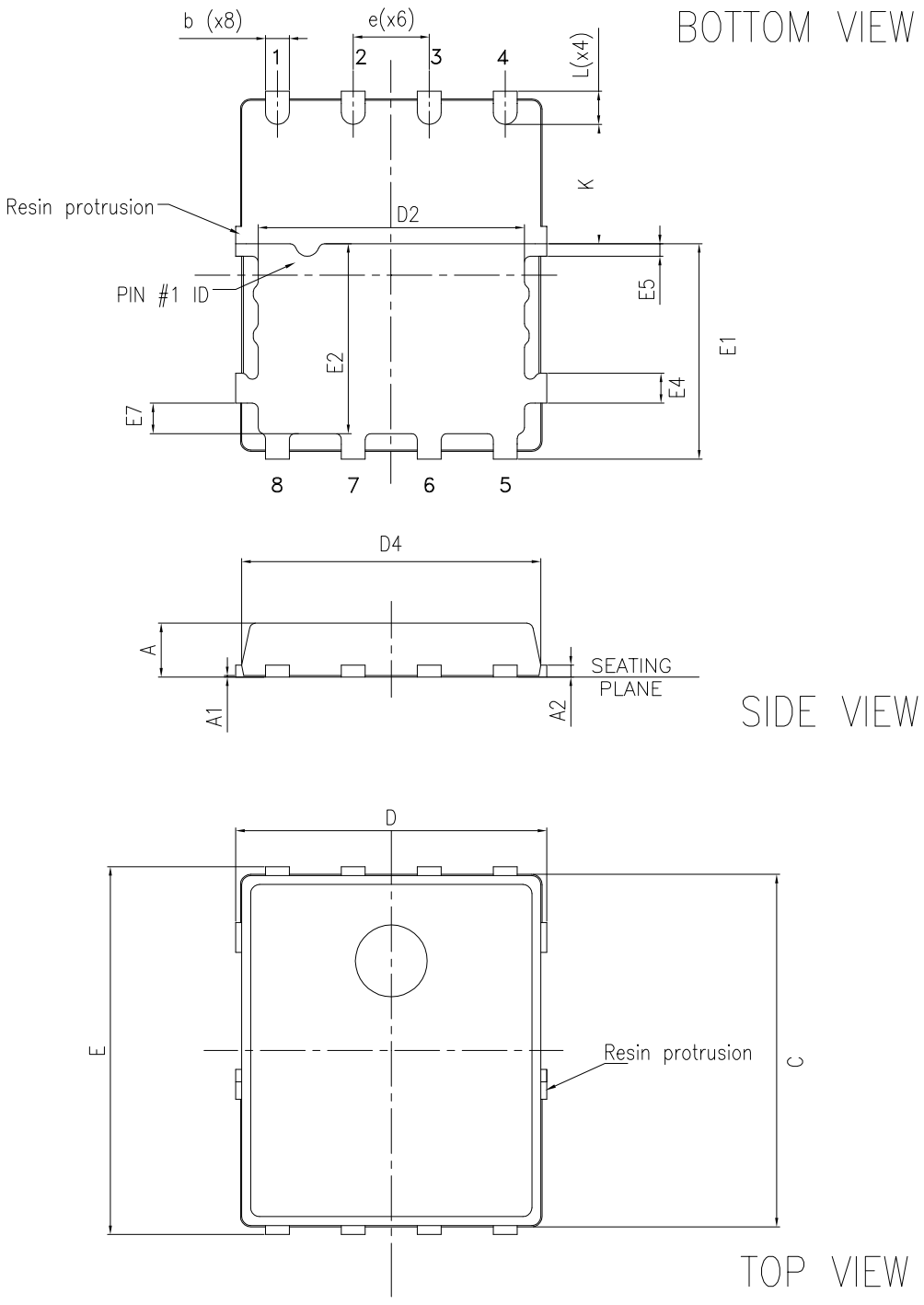


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 19. **PowerFLAT™ 5x6 HV package outline**

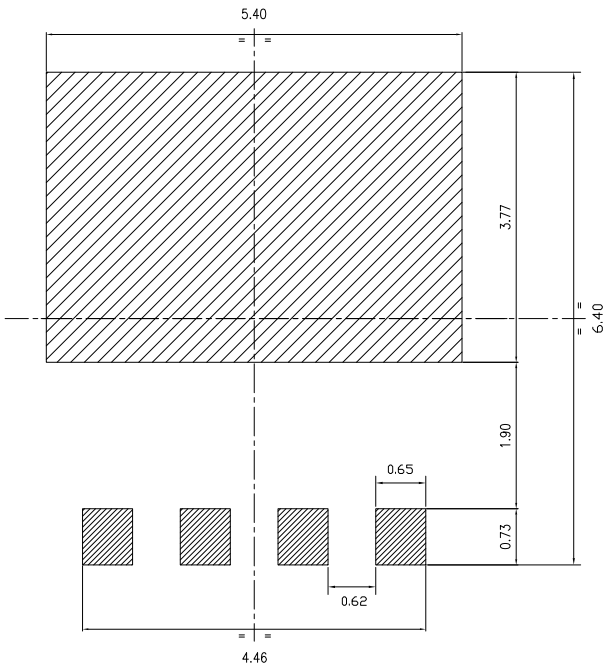


8368143_Rev_4

Table 7. **PowerFLAT™ 5x6 HV mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

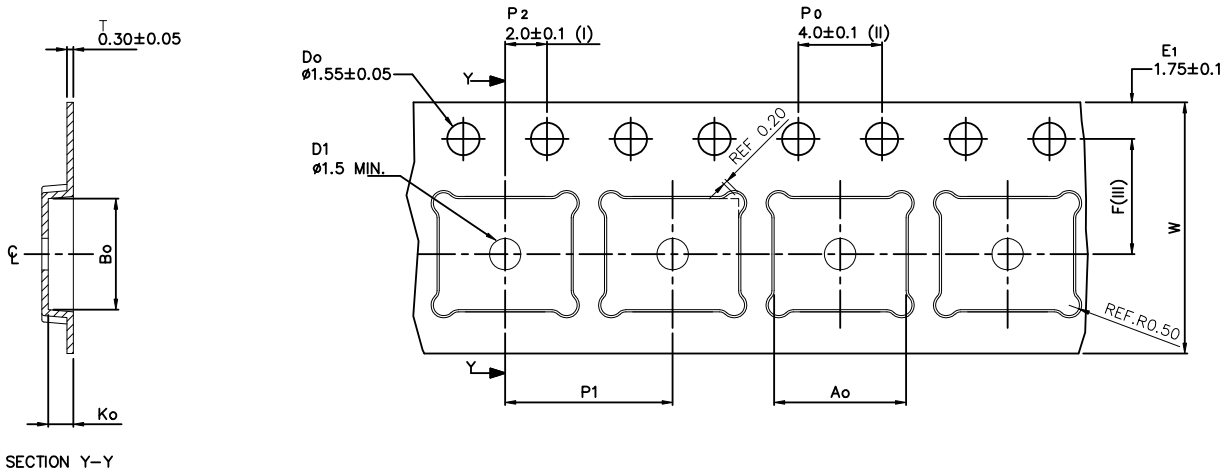
Figure 20. **PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)**



8368143_Rev_4_footprint

4.2 PowerFLAT™ 5x6 packing information

Figure 21. **PowerFLAT™ 5x6 tape (dimensions are in mm)**



Ao	6.30 +/- 0.1
Bo	5.30 +/- 0.1
Ko	1.20 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. **PowerFLAT™ 5x6 package orientation in carrier tape**

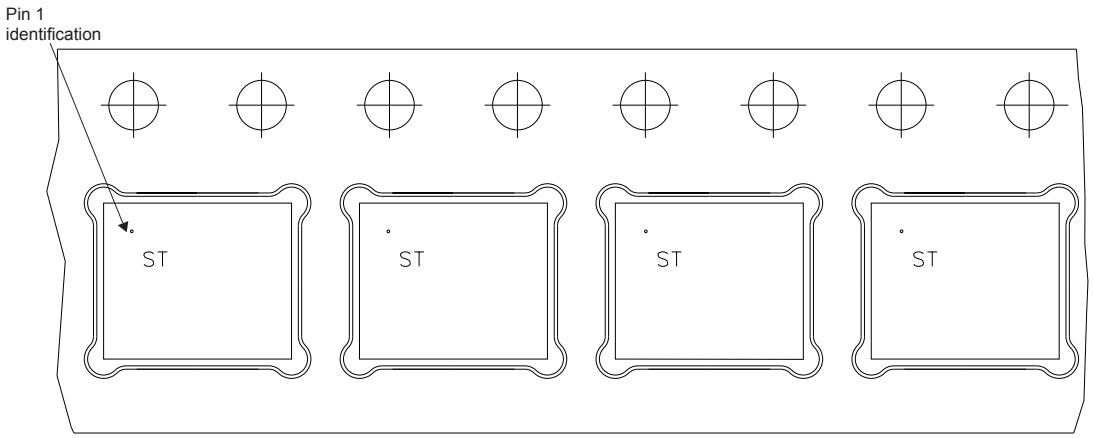
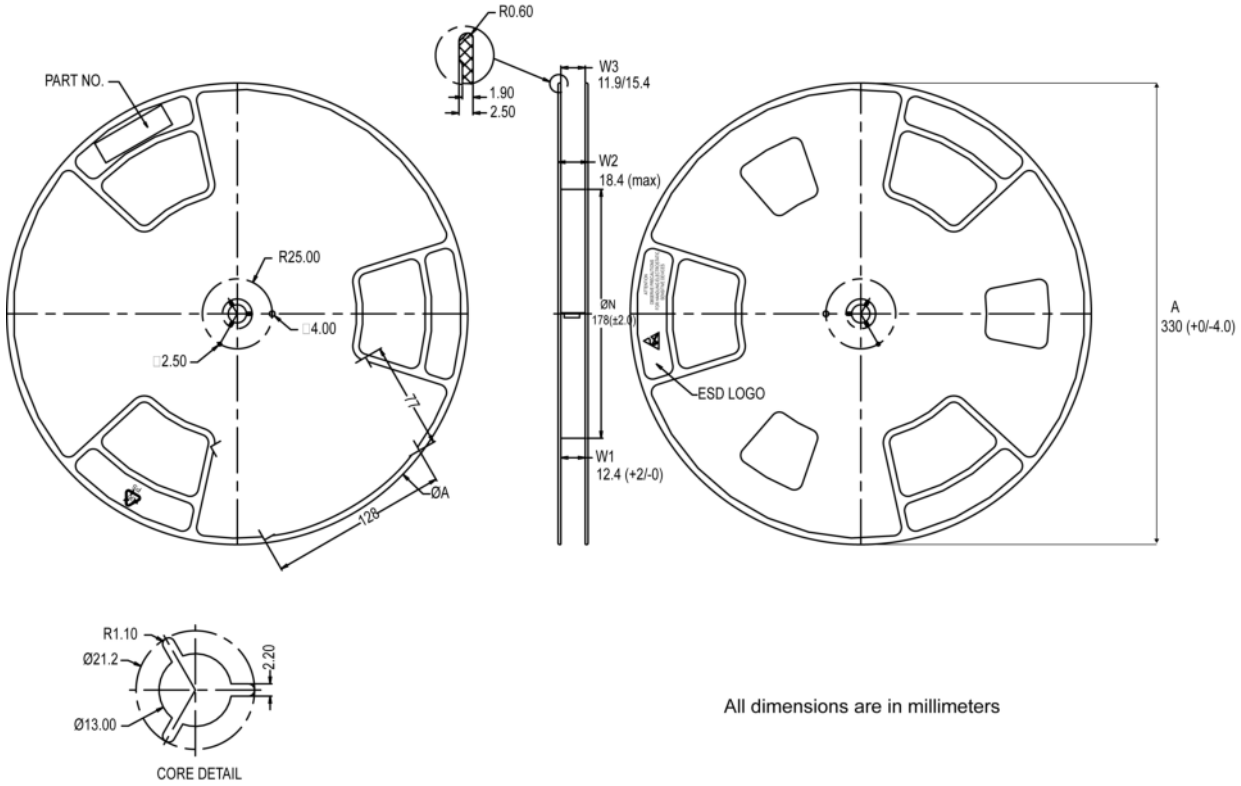


Figure 23. **PowerFLAT™ 5x6 reel**



Revision history

Table 8. **Document revision history**

Date	Version	Changes
18-Dec-2018	1	First release.

Contents

1 **Electrical ratings** 2

2 **Electrical characteristics** 3

2.1 Electrical characteristics (curves) 5

3 **Test circuits** 7

4 **Package information** 8

4.1 PowerFLAT™ 5x6 HV package information 8

4.2 PowerFLAT™ 5x6 packing information 10

Revision history 13

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved