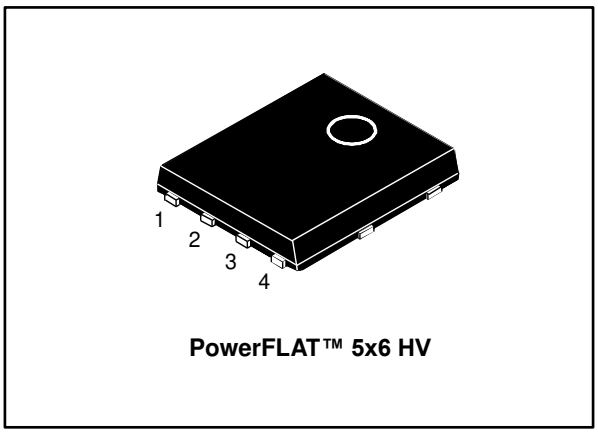
STL15N65M5

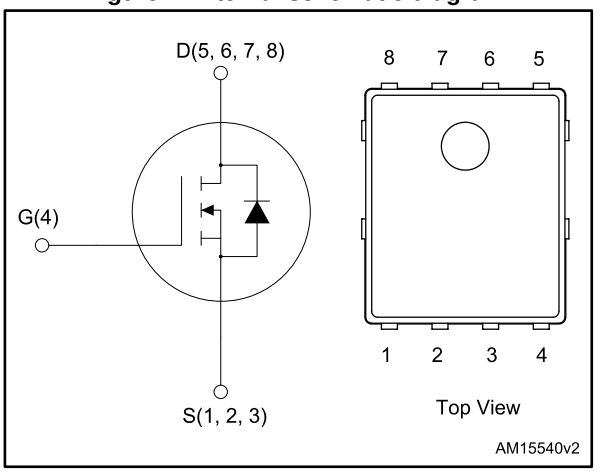
N-channel 650 V, 0.335 Ω typ., 10 A MDmesh™ M5 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data



PowerFLAT™ 5x6 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_J max.	$R_{DS(on)}$ max	I_D
STL15N65M5	710 V	0.375 Ω	10 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL15N65M5	15N65M5	PowerFLAT™ 5x6 HV	Tape and reel

This is information on a product in full production.

www.st.com

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2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 9
4 Package information 10
4.1 Power Flat™ 5x6 HV package information 11
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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	10	A
I_D	Drain current (continuous) at T_C = 100 °C	5	A
I_{DM} (1)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C	52	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	160	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		°C

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 10 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} = 400 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.4	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	59	°C/W

Notes:

(1)When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 650 V			1	µA
		V_{DS} = 650 V, T_C=125 °C (1), V_{GS} = 0 V			100	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 25 V, V_{DS} = 0			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 5 A		0.335	0.375	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	816	-	pF
C_{oss}	Output capacitance		-	23	-	pF
C_{rss}	Reverse transfer capacitance		-	2.6	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	70	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	21	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5.5 A, V_{GS} = 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	22	-	nC
Q_{gs}	Gate-source charge		-	5.5	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC

Notes:

(1)$C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS}.

(2)$C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 7 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"* and *Figure 20: "Switching time waveform"*)	-	30	-	ns
$t_{r(V)}$	Voltage rise time		-	8	-	ns
$t_{f(I)}$	Current fall time		-	11	-	ns
$t_{c(off)}$	Crossing time		-	12.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM}(1)	Source-drain current (pulsed)		-		40	A
V_{SD}(2)	Forward on voltage	I_{SD} = 10 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	244		ns
Q_{rr}	Reverse recovery charge		-	2.35		µC
I_{RRM}	Reverse recovery current		-	19.2		A
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	308		ns
Q_{rr}	Reverse recovery charge		-	2.93		µC
I_{RRM}	Reverse recovery current		-	19		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

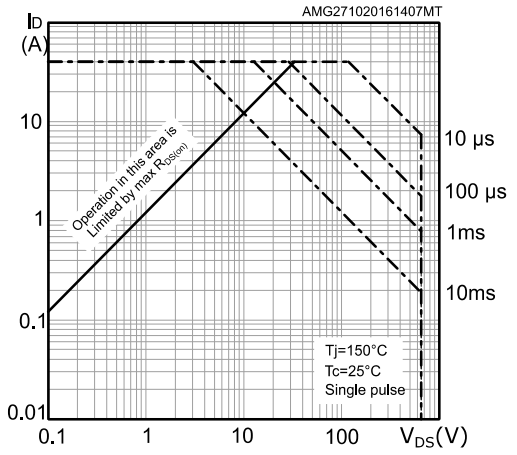


Figure 3: Thermal impedance

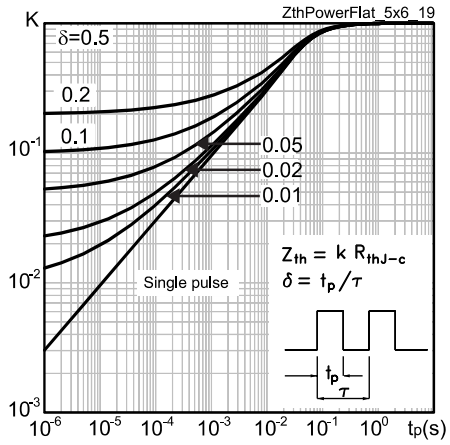


Figure 4: Output characteristics

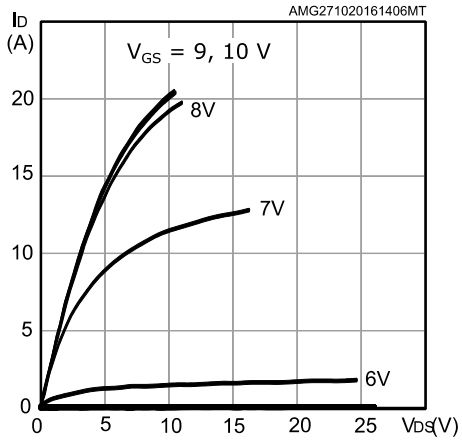


Figure 5: Transfer characteristics

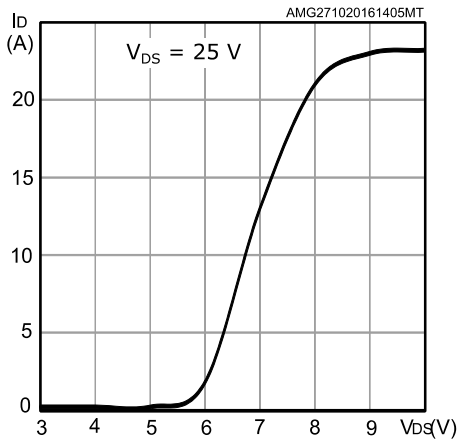


Figure 6: Static drain-source on-resistance

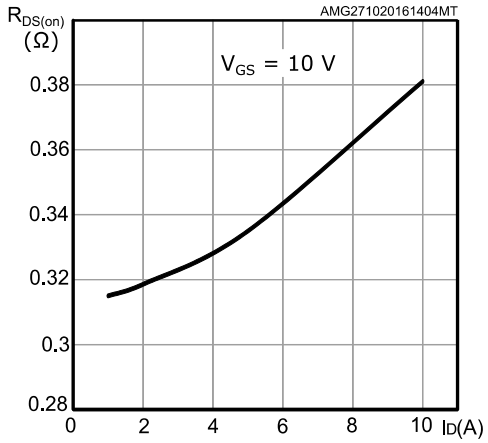


Figure 7: Gate charge vs gate-source voltage

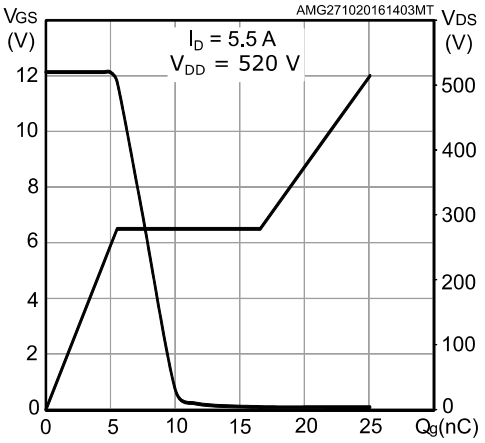


Figure 8: Capacitance variations

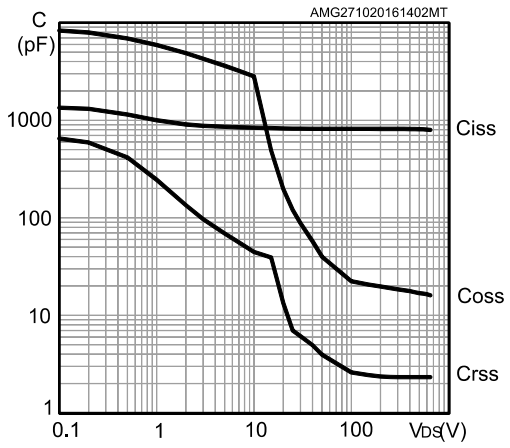


Figure 9: Output capacitance stored energy

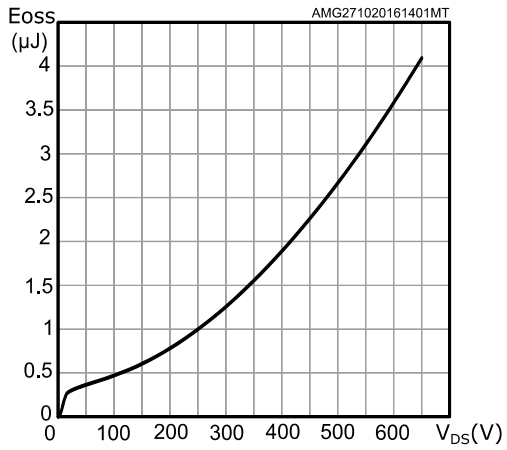


Figure 10: Normalized gate threshold voltage vs temperature

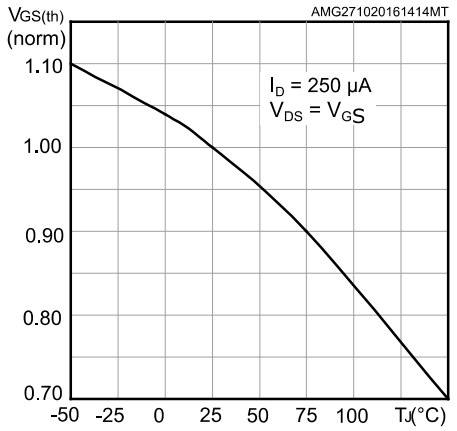


Figure 11: Normalized on-resistance vs temperature

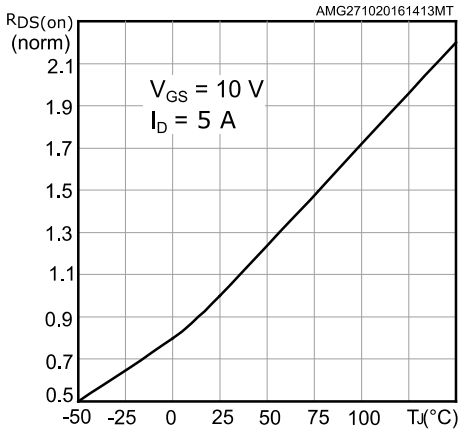


Figure 12: Source-drain diode forward characteristics

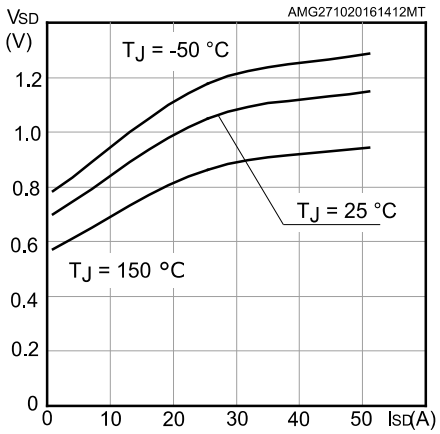


Figure 13: Normalized $V_{(BR)DSS}$ vs temperature

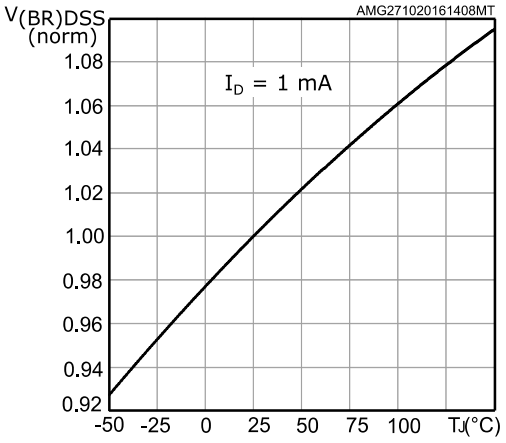
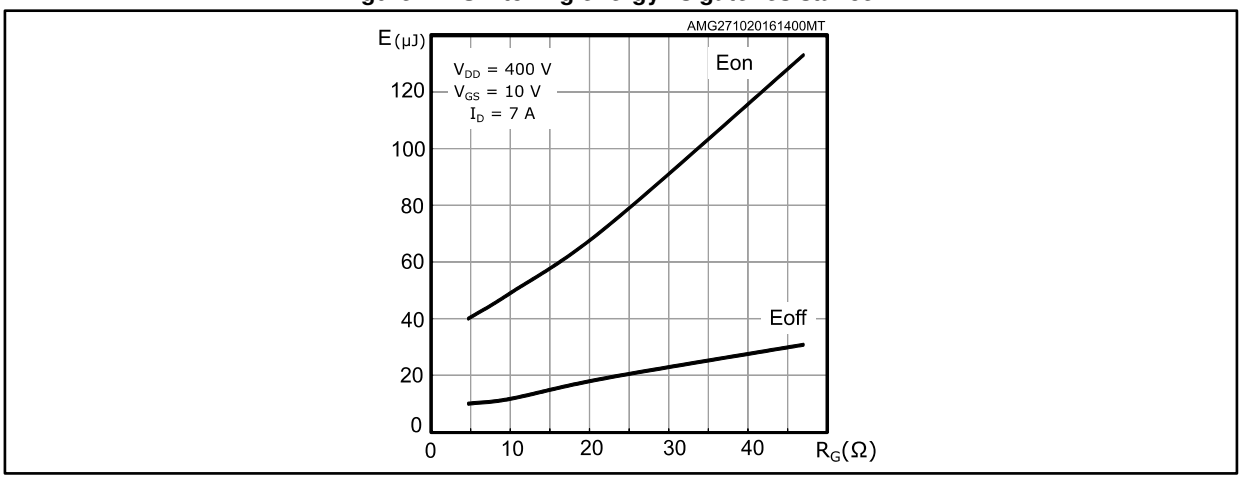


Figure 14: Switching energy vs gate resistance(1)



Notes:

(1)Eon including reverse recovery of a SiC diode.

3 Test circuits

Figure 15: Test circuit for resistive load switching times

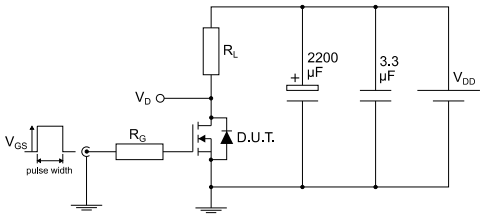


Figure 16: Test circuit for gate charge behavior

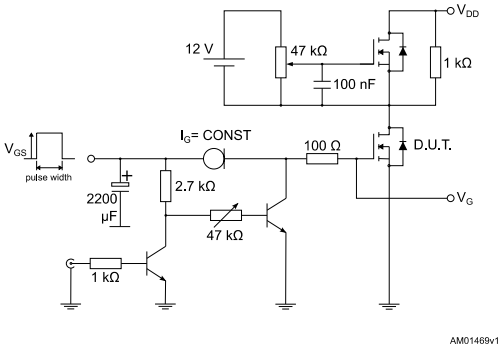


Figure 17: Test circuit for inductive load switching and diode recovery times

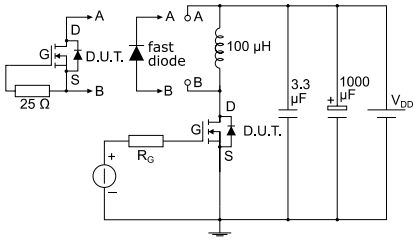


Figure 18: Unclamped inductive load test circuit

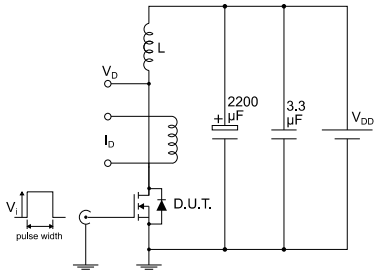


Figure 19: Unclamped inductive waveform

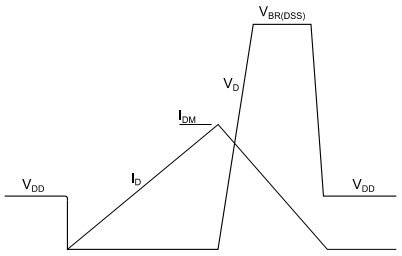
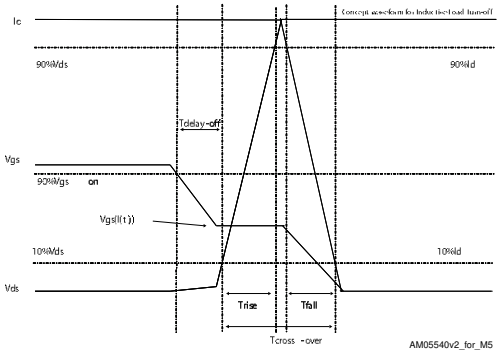


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 Power Flat™ 5x6 HV package information

Figure 21: PowerFLAT™ 5x6 HV package outline

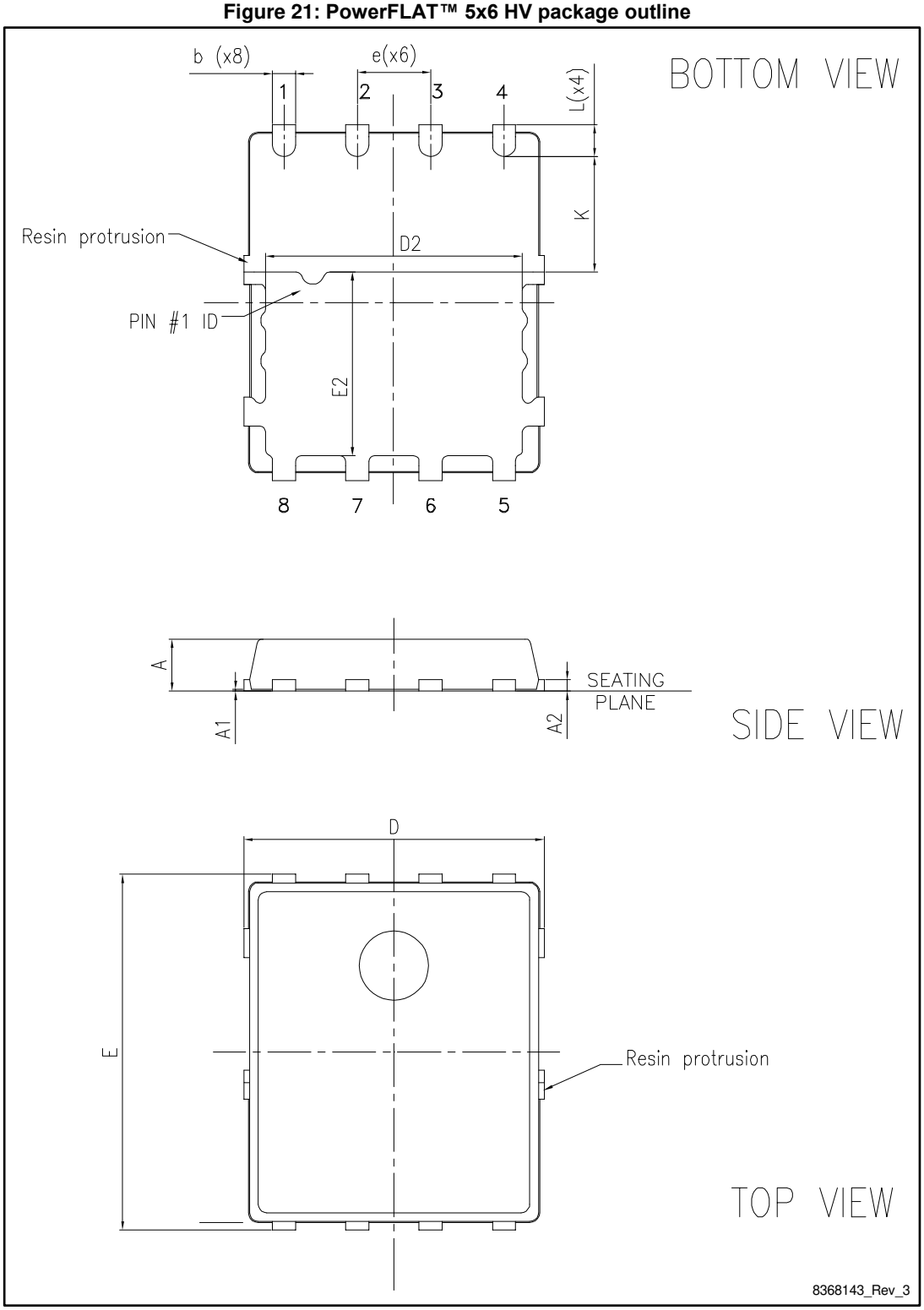
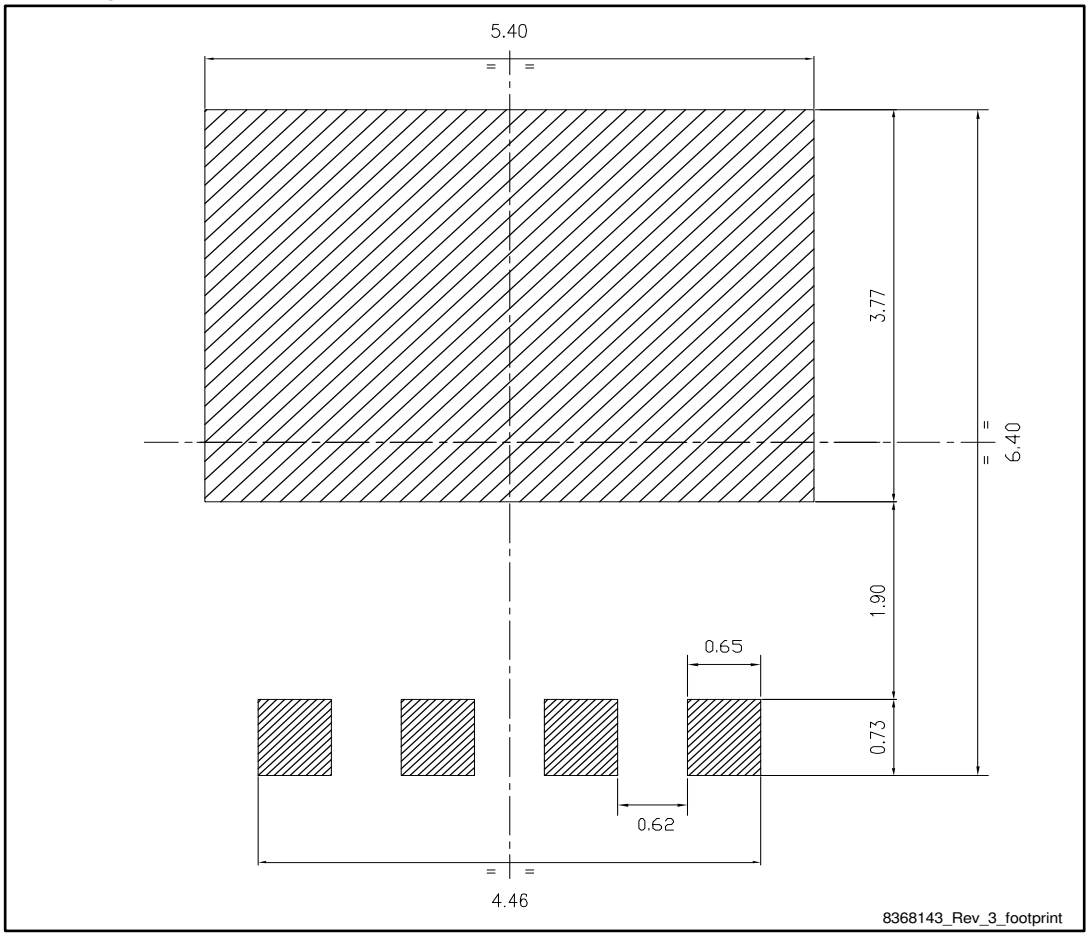


Table 8: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 22: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 Power Flat™ 5x6 HV packing information

Figure 23: PowerFLAT™ 5x6 tape (dimensions are in mm)

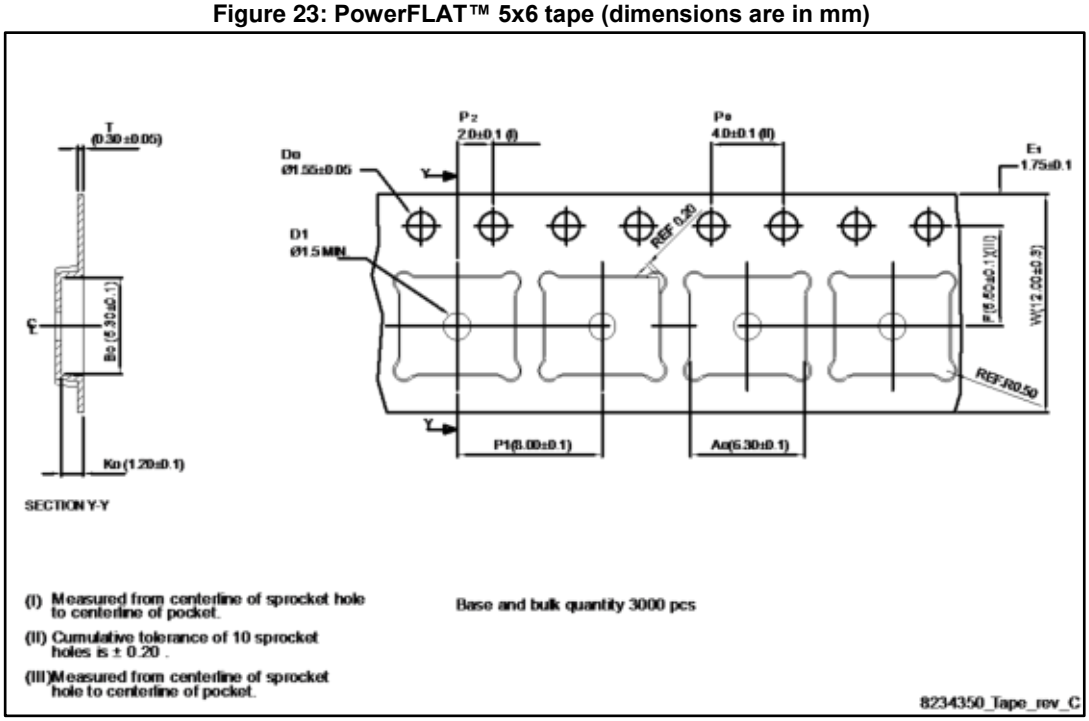


Figure 24: PowerFLAT™ 5x6 package orientation in carrier tape

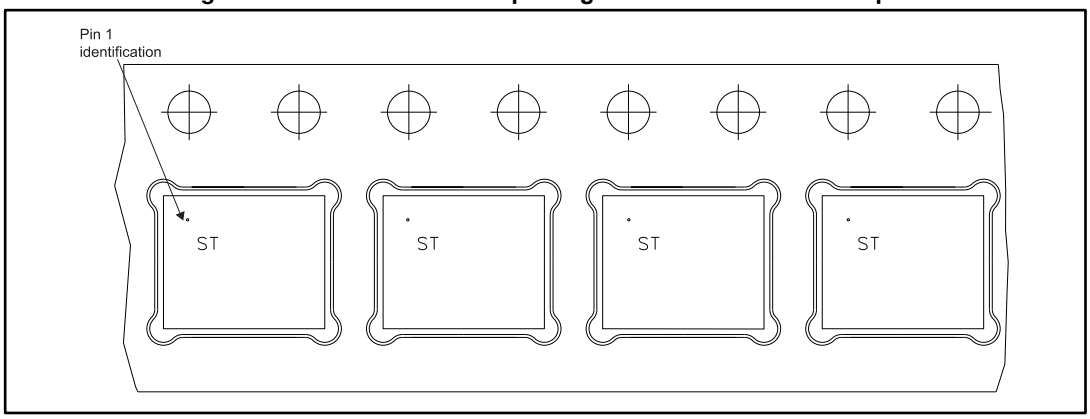
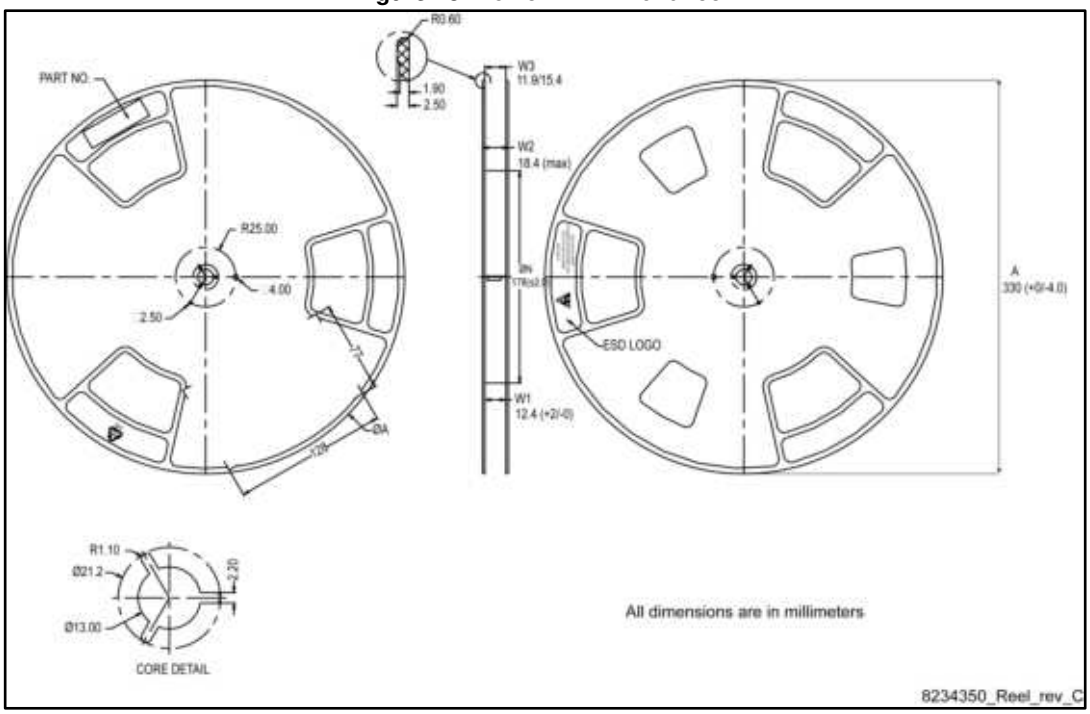


Figure 25: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
26-Jun-2013	1	First release
05-Dec-2016	2	Updated title, features and description in cover page. Updated *Figure 1: "Internal schematic diagram"*, *Table 2: "Absolute maximum ratings"* and *Section 4: "Package information"*. Minor text changes.

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