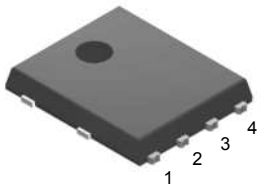
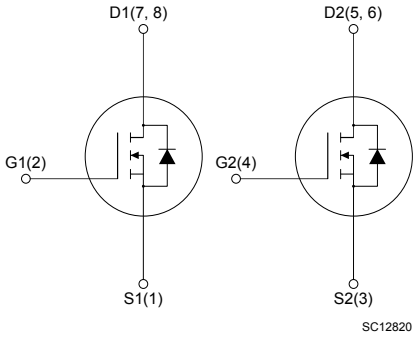
STL40DN3LLH5

Datasheet

Automotive-grade dual N-channel 30 V, 16 mΩ typ., 40 A STripFET H5 Power MOSFET in a PowerFLAT 5x6 double island WF package



PowerFLAT 5x6 double island WF



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL40DN3LLH5	30 V	18 mΩ	40 A

- AEC-Q101 qualified
- High avalanche ruggedness
- Logic level
- Low gate drive power loss
- Low on-resistance $R_{DS(on)}$
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Product status link
STL40DN3LLH5

Product summary	
Order code	STL40DN3LLH5
Marking	40DN3LH5
Package	PowerFLAT 5x6 double island WF
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±22	V
I_D	Drain current (continuous) at T_C = 25 °C	40	A
	Drain current (continuous) at T_C = 25 °C	28	
I_D(1)	Drain current (continuous) at T_A = 25 °C	11	A
	Drain current (continuous) at T_A = 100 °C	7	
I_{DM}(1)(2)	Drain current (pulsed)	44	A
I_{DM}(2)	Drain current (pulsed)	160	A
P_{TOT}	Total dissipation at T_C = 25 °C (one channel active)	50	W
	Total dissipation at T_A = 25 °C (one channel active)(1)	4.7	
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*
2. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thjC}	Thermal resistance, junction-to-case	3.0	°C/W
R_{thjA}(1)	Thermal resistance, junction-to-ambient	32	°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

2 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	30	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 125 °C(1)	-	-	10	
I_{GSS}	Gate-body leakage current	V_{GS} = ±22 V, V_{DS} = 0 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	-	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.5 A	-	16	18	mΩ
		V_{GS} = 4.5 V, I_D = 5.5 A	-	20	25	

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}(1)	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	475	-	pF
C_{oss}(1)	Output capacitance		-	97	-	pF
C_{rss}(1)	Reverse transfer capacitance		-	19	-	pF
Q_g(1)	Total gate charge	V_{DD} = 15 V, I_D = 11 A, V_{GS} = 0 to 4.5 V (see the Figure 12. Test circuit for gate charge behavior)	-	4.5	-	nC
Q_{gs}(1)	Gate-source charge		-	1.7	-	nC
Q_{gd}(1)	Gate-drain charge		-	1.9	-	nC

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(1)	Turn-on delay time	V_{DD} = 15 V, I_D = 11 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	4	-	ns
t_r(1)	Rise time		-	22	-	ns
$t_{d(off)}$(1)	Turn-off delay time		-	13	-	ns
t_f(1)	Fall time		-	2.8	-	ns

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 11 A, V_{GS} = 0 V	-	-	1.1	V
t_{rr}	Reverse recovery time	I_D = 11 A, di/dt = 100 A/µs, V_{DD} = 25 V, T_J = 150 °C (see the Figure 13. Test circuit for inductive load switching and diode recovery times)	-	16.2	-	ns
Q_{rr}	Reverse recovery charge		-	1	-	nC
I_{RRM}	Reverse recovery current		-	8.1	-	A

1. *Pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

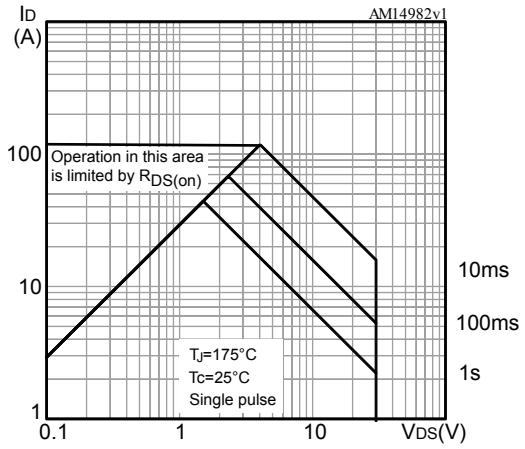


Figure 2. Normalized transient thermal impedance

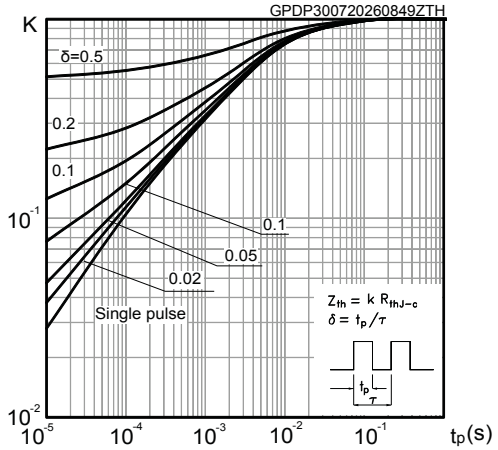


Figure 3. Typical output characteristics

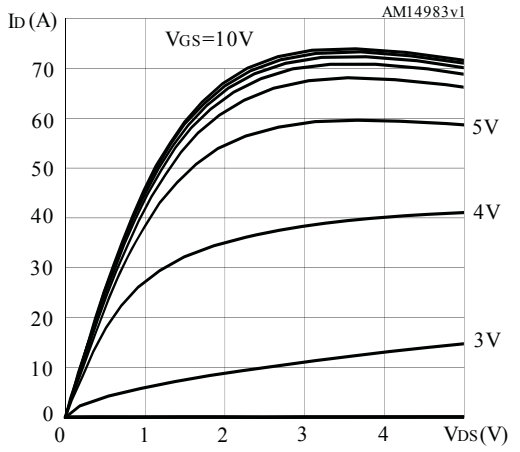


Figure 4. Typical tranfer characteristics

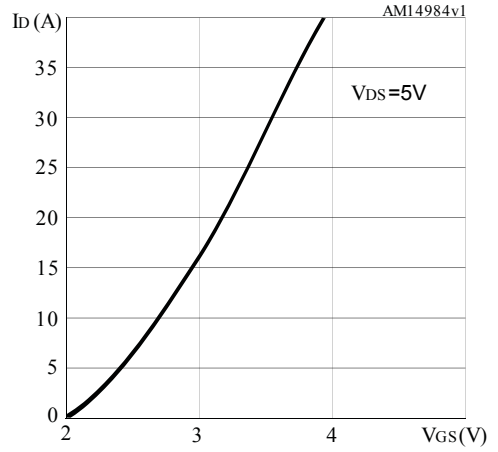


Figure 5. Typical gate charge characteristics

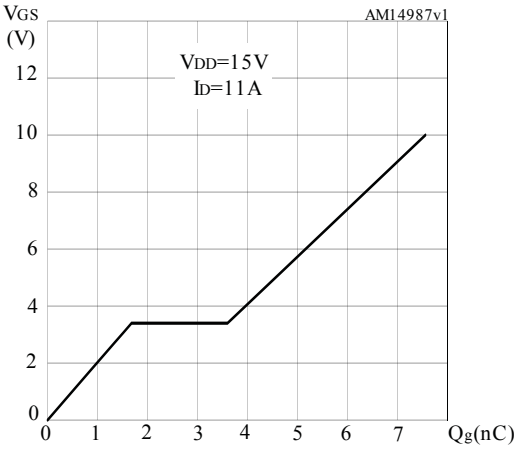


Figure 6. Typical capacitance characteristics

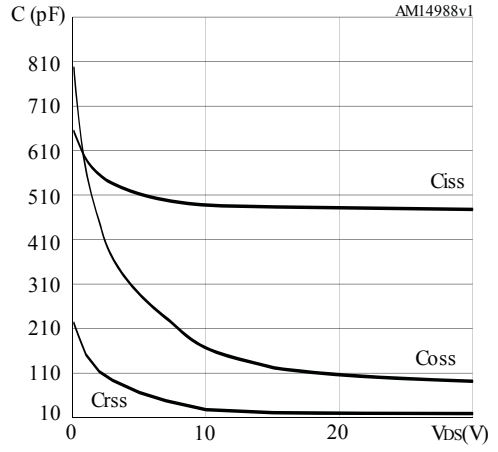


Figure 7. Typical drain-source on-resistance

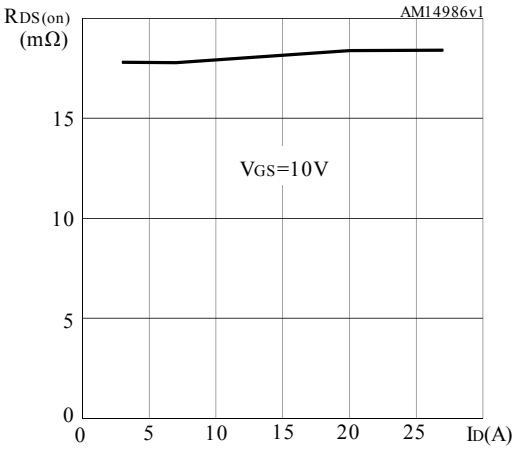


Figure 8. Normalized $V_{(BR)DSS}$ vs temperature

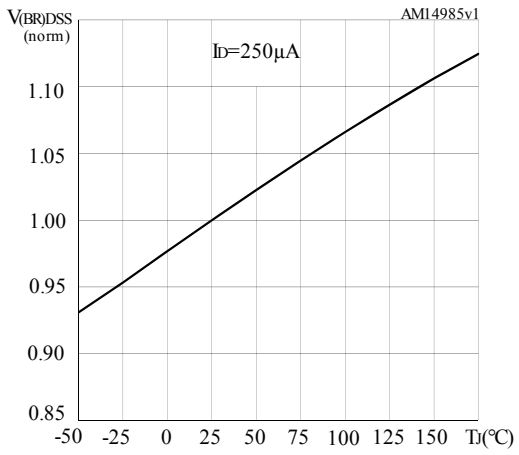


Figure 9. Normalized gate threshold voltage vs temperature

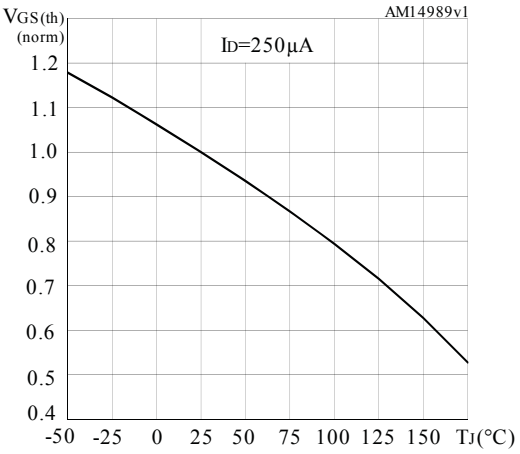
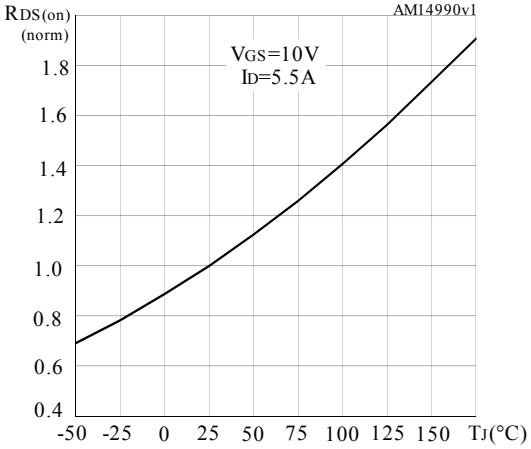
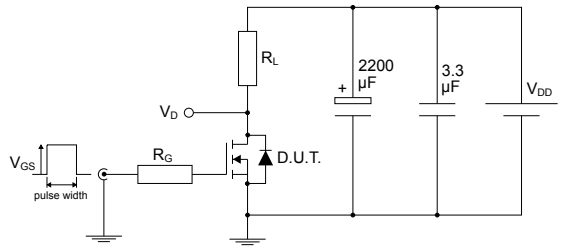


Figure 10. Normalized on-resistance vs temperature



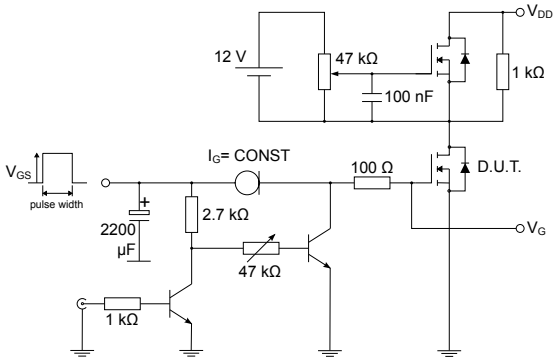
3 Test circuits

Figure 11. Test circuit for resistive load switching times



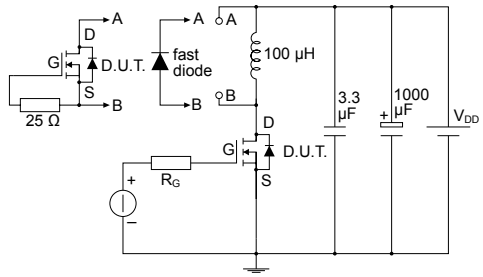
AM01468v1

Figure 12. Test circuit for gate charge behavior



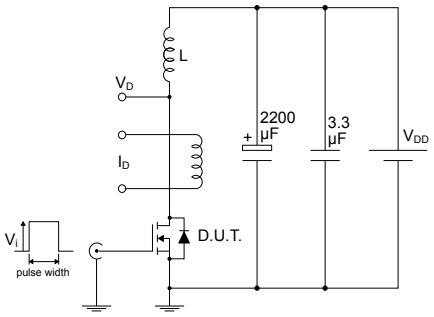
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Figure 13. Test circuit for inductive load switching and diode recovery times



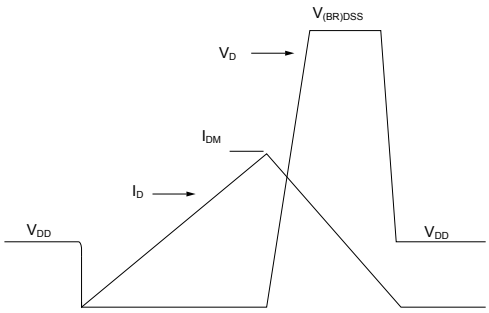
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Figure 14. Unclamped inductive load test circuit



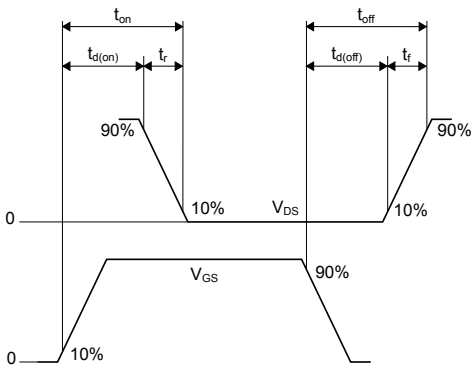
AM01471v1

Figure 15. Unclamped inductive waveform



AM01472v1

Figure 16. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 double island WF type R package information

Figure 17. PowerFLAT 5x6 double island WF type R package outline

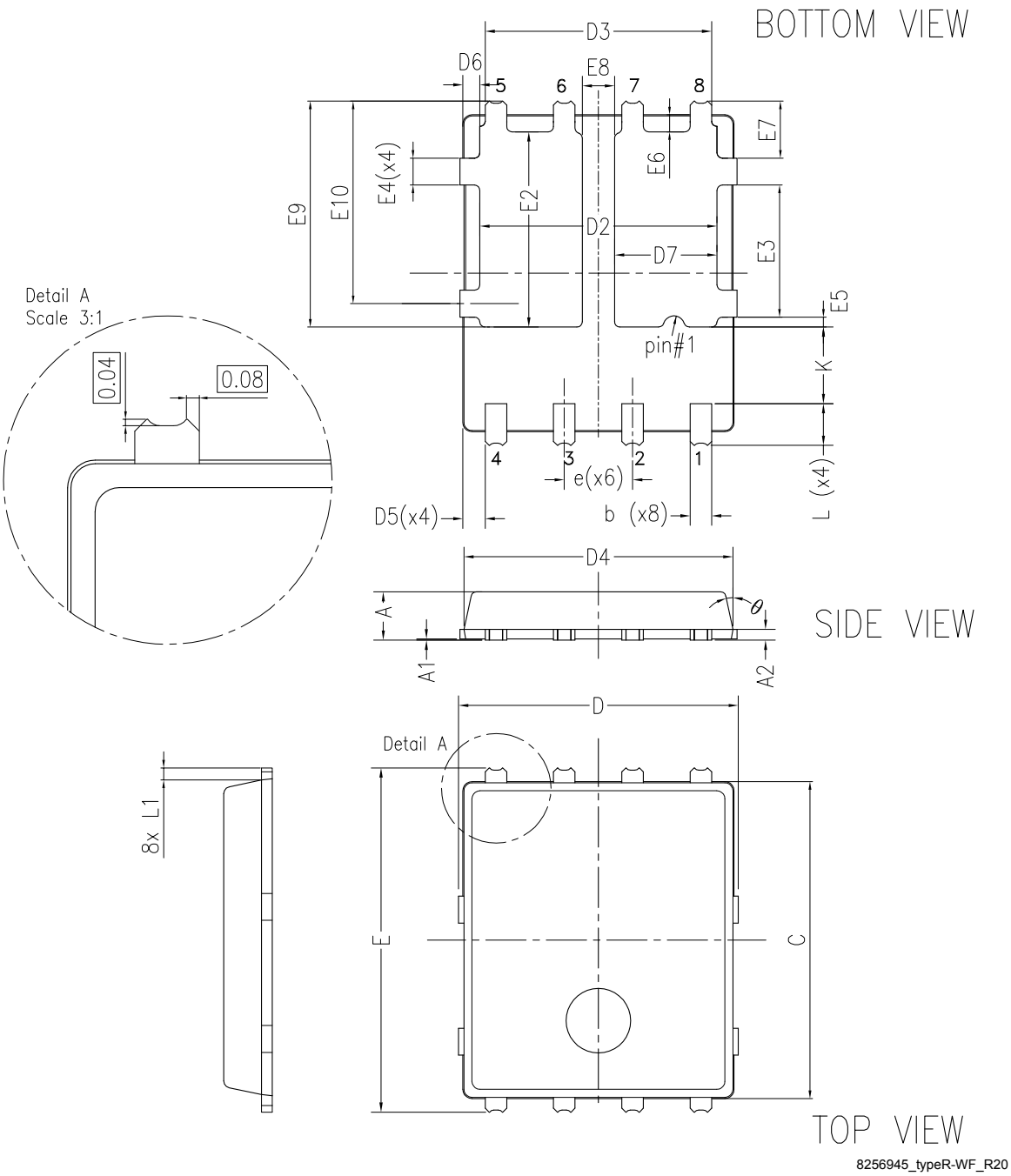
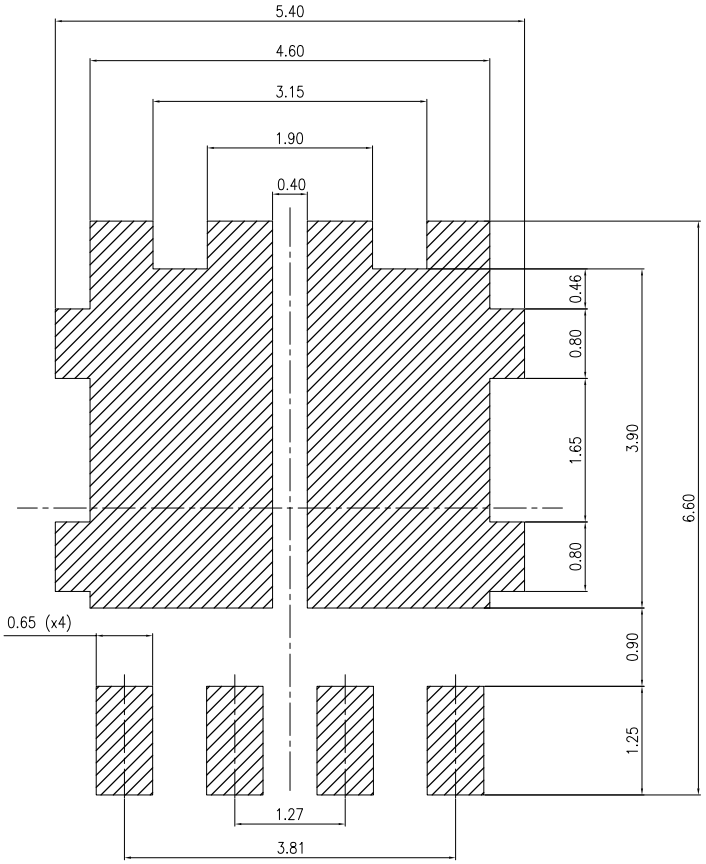


Table 7. **PowerFLAT 5x6 double island WF type R mechanical data**

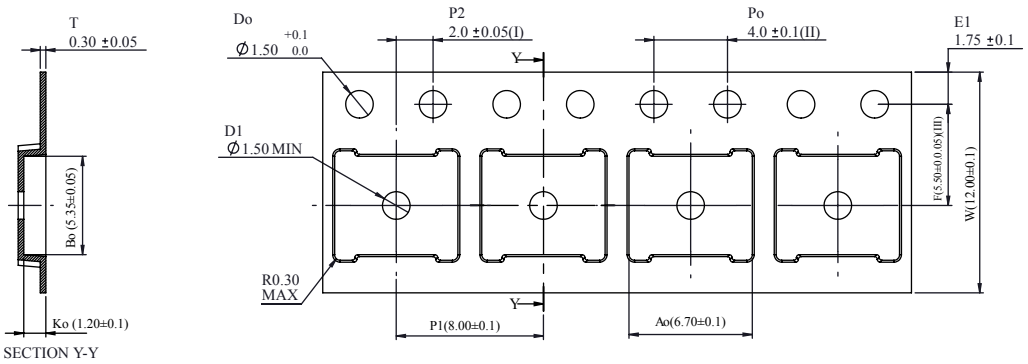
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.00		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 18. **PowerFLAT 5x6 double island recommended footprint (dimensions are in mm)**



4.2 PowerFLAT 5x6 WF packing information

Figure 19. PowerFLAT 5x6 WF tape (dimensions are in mm)



(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

Figure 20. PowerFLAT 5x6 package orientation in carrier tape

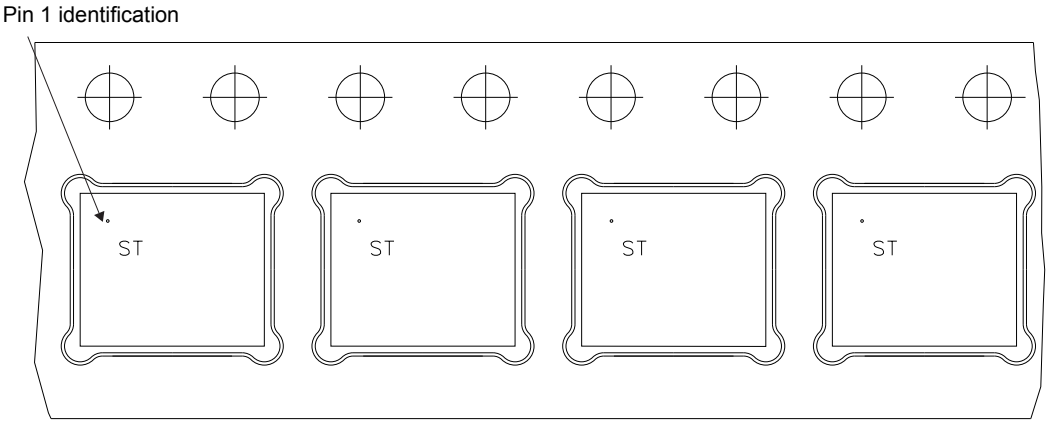
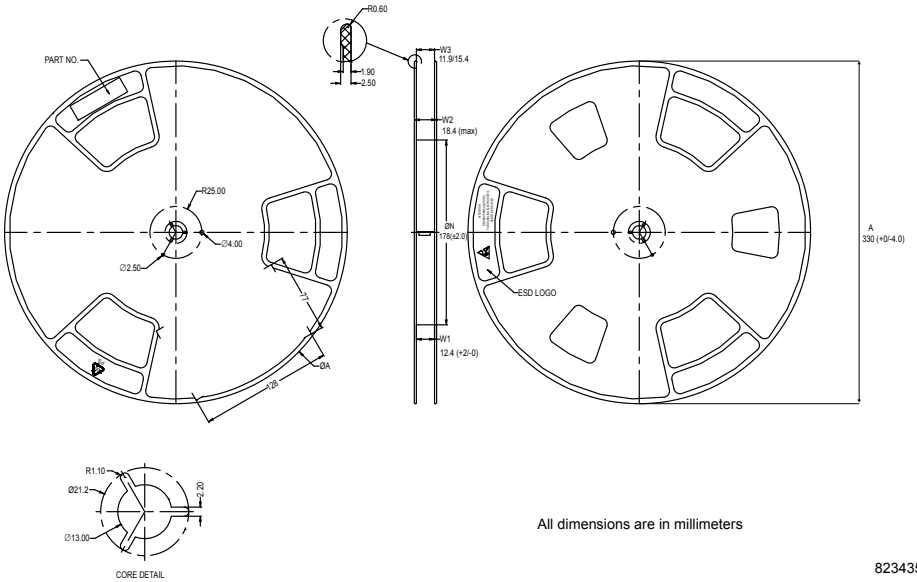


Figure 21. **PowerFLAT 5x6 reel (dimensions are in mm)**



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
24-Jan-2011	1	First release.
03-Oct-2012	2	*Section 2.1: Electrical characteristics (curves)* has been added. Document status promoted from preliminary data to datasheet. Minor text changes.
14-Dec-2012	3	Modified the *Applications* section on the cover page to *"Automotive switching applications"*.
23-Feb-2015	4	Updated *Section 4: Package mechanical data* and added *Section 5: Packing information*. Updated title and features in cover page. Minor text changes.
27-Oct-2015	5	Updated title and features in cover page. Updated *Table 2*, *Table 3*, *Table 4* and *Table 7*. Updated *Section 4: Package information*. Minor text changes.
11-Mar-2016	6	Updated silhoette in cover page. Updated *Table 1: Device summary*, *Table 2: Absolute maximum ratings*, *Table 3: Thermal resistance* and *Table 4: On/off states*. Updated *Figure 2: Safe operating area*. Updated *Section 4.1: PowerFLAT 5x6 double island WF type R*. Updated *Section 5: Packing information*. Minor text changes.
7-Oct-2016	7	Updated marking and *Section 4.1: PowerFLAT 5x6 double island WF type R*. Minor text changes.
30-Jul-2026	8	Updated Section 4: Package information. Minor text changes.

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