STM32L496xx

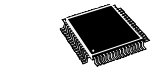
Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 100 DMIPS, up to 1 MB flash, 320 KB SRAM, USB OTG FS, audio, HASH, external SMPS

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

- Ultra-low-power with FlexPowerControl
  - 1.71 V to 3.6 V power supply
  - -40 °C to 85/125 °C temperature range
  - 320 nA in V_{BAT} mode: supply for RTC and 32 x 32-bit backup registers
  - 25 nA Shutdown mode (5 wakeup pins)
  - 108 nA Standby mode (5 wakeup pins)
  - 426 nA Standby mode with RTC
  - 2.57 µA Stop 2 mode, 2.86 µA Stop 2 with RTC
  - 91 µA/MHz run mode (LDO mode)
  - 37 µA/MHz run mode (at 3.3 V SMPS mode)
  - Batch acquisition mode (BAM)
  - 5 µs wakeup from Stop mode
  - Brownout reset (BOR) in all modes except shutdown
  - Interconnect matrix
- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from flash memory, frequency up to 80 MHz, MPU, 100 DMIPS, and DSP instructions
- Performance benchmark
  - 1.25 DMIPS/MHz (Drystone 2.1)
  - 273.55 Coremark® (3.42 Coremark/MHz at 80 MHz)
- Energy benchmark
  - 279 ULPMark™ CP score
  - 80.2 ULPMark™ PP score
- 16 timers: 2x 16-bit advanced motor-control, 2x 32-bit and 5x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer



LQFP64 (10 x 10)
LQFP100 (14 x 14)
LQFP144 (20 × 20)



WLCSP100L
(4.618 x 4.142)



WLCSP115 (4.63 x 4.15)



UFBGA169 (7 x 7)
UFBGA132 (7 × 7)

- RTC with hardware calendar, alarms, and calibration
- Up to 136 fast I/Os, most 5 V-tolerant, up to 14 I/Os with independent supply down to 1.08 V
- Dedicated Chrom-ART Accelerator for enhanced graphic content creation (DMA2D)
- 8- to 14-bit camera interface up to 32 MHz (black & white) or 10 MHz (color)
- Encryption hardware accelerator: HASH (SHA-256)
- Memories
  - Up to 1 MB flash, 2 banks read-while-write, proprietary code readout protection
  - 320 KB of SRAM including 64 KB with hardware parity check
  - External memory interface for static memories supporting SRAM, PSRAM, NOR, and NAND memories
  - Dual-flash QUADSPI memory interface
- Clock sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)

Product label



This is information on a product in full production. www.st.com

  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25% accuracy)
  - Internal 48 MHz with clock recovery
  - 3 PLLs for system clock, USB, audio, ADC
- LCD 8× 40 or 4× 44 with step-up converter
- Up to 24 capacitive sensing channels: support touchkey, linear and rotary touch sensors
- 4x digital filters for sigma delta modulator
- Rich analog peripherals (independent supply)
  - 3× 12-bit ADCs 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
  - 2x 12-bit DAC output channels, low-power sample and hold
  - 2x operational amplifiers with built-in PGA
  - 2x ultra-low-power comparators
- 20x communication interfaces
  - USB OTG 2.0 full-speed, LPM, and BCD
  - 2x SAIs (serial audio interface)
  - 4x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 6 USART, UART, and LPUART (SPI, ISO 7816, LIN, IrDA, and modem)
  - 3 SPI (plus 1 with quad-SPI, plus 3 with USART)
  - 2x CANs (2.0B Active) and SDMMC
  - SWPMI single wire protocol controller I/F
  - IRTIM (Infrared interface)
- 14-channel DMA controller
- True random number generator
- CRC calculation unit, 96-bit unique ID
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part numbers
STM32L496xx	STM32L496AG, STM32L496QG, STM32L496RG, STM32L496VG, STM32L496WG, STM32L496ZG, STM32L496AE, STM32L496QE, STM32L496RE, STM32L496VE, STM32L496ZE

Contents

1 Introduction 13

2 Description 14

3 Functional overview 18

3.1 Arm® Cortex®-M4 core with FPU 18

3.2 Adaptive real-time memory accelerator (ART Accelerator™) 18

3.3 Memory protection unit 18

3.4 Embedded flash memory 19

3.5 Embedded SRAM 20

3.6 Multi-AHB bus matrix 21

3.7 Firewall 21

3.8 Boot modes 22

3.9 Cyclic redundancy check calculation unit (CRC) 22

3.10 Power supply management 23

3.10.1 Power supply schemes 23

3.10.2 Power supply supervisor 25

3.10.3 Voltage regulator 26

3.10.4 Low-power modes 26

3.10.5 Reset mode 34

3.10.6 VBAT operation 34

3.11 Interconnect matrix 35

3.12 Clocks and startup 37

3.13 General-purpose inputs/outputs (GPIOs) 40

3.14 Direct memory access controller (DMA) 40

3.15 Chrom-ART Accelerator™ (DMA2D) 41

3.16 Interrupts and events 41

3.16.1 Nested vectored interrupt controller (NVIC) 41

3.16.2 Extended interrupt/event controller (EXTI) 41

3.17 Analog to digital converter (ADC) 42

3.17.1 Temperature sensor 42

3.17.2 Internal voltage reference (VREFINT) 43

3.17.3 VBAT battery voltage monitoring . . . 43
3.18 Digital to analog converter (DAC) . . . 43
3.19 Voltage reference buffer (VREFBUF) . . . 44
3.20 Comparators (COMP) . . . 45
3.21 Operational amplifier (OPAMP) . . . 45
3.22 Touch sensing controller (TSC) . . . 45
3.23 Liquid crystal display controller (LCD) . . . 46
3.24 Digital filter for Sigma-Delta modulators (DFSDM) . . . 46
3.25 True random number generator (RNG) . . . 48
3.26 Digital camera interface (DCMI) . . . 48
3.27 HASH hardware accelerator (HASH) . . . 48
3.28 Timers and watchdogs . . . 48
3.28.1 Advanced-control timer (TIM1, TIM8) . . . 49
3.28.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17) . . . 50
3.28.3 Basic timers (TIM6 and TIM7) . . . 50
3.28.4 Low-power timer (LPTIM1 and LPTIM2) . . . 50
3.28.5 Infrared interface (IRTIM) . . . 51
3.28.6 Independent watchdog (IWDG) . . . 51
3.28.7 System window watchdog (WWDG) . . . 51
3.28.8 SysTick timer . . . 51
3.29 Real-time clock (RTC) and backup registers . . . 52
3.30 Inter-integrated circuit interface (I^2C) . . . 53
3.31 Universal synchronous/asynchronous receiver transmitter (USART) . . . 54
3.32 Low-power universal asynchronous receiver transmitter (LPUART) . . . 55
3.33 Serial peripheral interface (SPI) . . . 56
3.34 Serial audio interfaces (SAI) . . . 56
3.35 Single wire protocol master interface (SWPMI) . . . 57
3.36 Controller area network (CAN) . . . 57
3.37 Secure digital input/output and MultiMediaCards interface (SDMMC) . . . 58
3.38 Universal serial bus on-the-go full-speed (OTG_FS) . . . 58
3.39 Clock recovery system (CRS) . . . 59
3.40 Flexible static memory controller (FSMC) . . . 59
3.41 Dual-flash Quad SPI memory interface (QUADSPI) . . . 60

3.42 Development support 61
3.42.1 Serial wire JTAG debug port (SWJ-DP) 61
3.42.2 Embedded Trace Macrocell™ 61

4 Pinouts and pin description 62

5 Memory mapping 116

6 Electrical characteristics 122

6.1 Parameter conditions 122
6.1.1 Minimum and maximum values 122
6.1.2 Typical values 122
6.1.3 Typical curves 122
6.1.4 Loading capacitor 122
6.1.5 Pin input voltage 122
6.1.6 Power supply scheme 123
6.1.7 Current consumption measurement 124
6.2 Absolute maximum ratings 124
6.3 Operating conditions 126
6.3.1 General operating conditions 126
6.3.2 Operating conditions at power-up / power-down 127
6.3.3 Embedded reset and power control block characteristics 128
6.3.4 Embedded voltage reference 130
6.3.5 Supply current characteristics 131
6.3.6 Wakeup time from low-power modes and voltage scaling transition times 158
6.3.7 External clock source characteristics 160
6.3.8 Internal clock source characteristics 164
6.3.9 PLL characteristics 170
6.3.10 Flash memory characteristics 171
6.3.11 EMC characteristics 172
6.3.12 +Electrical sensitivity characteristics 174
6.3.13 I/O current injection characteristics 175
6.3.14 I/O port characteristics 175
6.3.15 NRST pin characteristics 182
6.3.16 Extended interrupt and event controller input (EXTI) characteristics . . 183
6.3.17 Analog switches booster 183

6.3.18 Analog-to-Digital converter characteristics 184
6.3.19 Digital-to-Analog converter characteristics 197
6.3.20 Voltage reference buffer characteristics 202
6.3.21 Comparator characteristics 204
6.3.22 Operational amplifiers characteristics 205
6.3.23 Temperature sensor characteristics 208
6.3.24 V_{BAT} monitoring characteristics 209
6.3.25 LCD controller characteristics 209
6.3.26 DFSDM characteristics 210
6.3.27 Timer characteristics 212
6.3.28 Communication interfaces characteristics 214
6.3.29 FSMC characteristics 226
6.3.30 Camera interface (DCMI) timing specifications 243
6.3.31 SWPMI characteristics 244
6.3.32 SD/SDIO MMC card host interface (SDIO) characteristics 244

7 Package information 248
7.1 Device marking 248
7.2 UFBGA169 package information (A0YV) 249
7.3 LQFP144 package information (1A) 251
7.4 UFBGA132 package information (A0G8) 255
7.5 WLCSP115 package information (B0E8) 257
7.6 LQFP100 package information (1L) 261
7.7 WLCSP100L package information (A07D) 264
7.8 LQFP64 package information (5W) 268
7.9 Thermal characteristics 271
7.9.1 Reference document 271
7.9.2 Selecting the product temperature range 271

8 Ordering information 274

9 Important security notice 276

10 Revision history 277

List of tables

Table 1. Device summary . . . 2
Table 2. STM32L496xx features and peripherals . . . 15
Table 3. Access status versus readout protection level and execution modes . . . 19
Table 4. STM32L496xx modes overview . . . 27
Table 5. Functionalities depending on the working mode . . . 32
Table 6. STM32L496xx peripherals interconnect matrix . . . 35
Table 7. DMA implementation . . . 40
Table 8. Temperature sensor calibration values . . . 43
Table 9. Internal voltage reference calibration values . . . 43
Table 10. Timer feature comparison . . . 49
Table 11. I2C implementation . . . 53
Table 12. STM32L496xx USART/UART/LPUART features . . . 54
Table 13. SAI implementation . . . 57
Table 14. Legend/abbreviations used in the pinout table . . . 72
Table 15. STM32L496xx pin definitions . . . 73
Table 16. Alternate function AF0 to AF7 . . . 98
Table 17. Alternate function AF8 to AF15 . . . 107
Table 18. STM32L496xx memory map and peripheral register boundary addresses . . . 117
Table 19. Voltage characteristics . . . 124
Table 20. Current characteristics . . . 125
Table 21. Thermal characteristics . . . 126
Table 22. General operating conditions . . . 126
Table 23. Operating conditions at power-up / power-down . . . 127
Table 24. Embedded reset and power control block characteristics . . . 128
Table 25. Embedded internal voltage reference . . . 130
Table 26. Current consumption in Run and Low-power run modes, code with data processing running from flash, ART enable (Cache ON Prefetch OFF) . . . 132
Table 27. Current consumption in Run modes, code with data processing running from flash, (ART enable Cache ON Prefetch OFF) and power supplied (by external SMPS (VDD12 = 1.10 V) . . . 133
Table 28. Current consumption in Run and Low-power run modes, code with data processing running from flash, ART disable . . . 134
Table 29. Current consumption in Run modes, code with data processing running from flash, ART disable and power supplied by external SMPS (VDD12 = 1.10 V) . . . 135
Table 30. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 . . . 136
Table 31. Current consumption in Run, code with data processing running from SRAM1 and power supplied by external SMPS (VDD12 = 1.10 V) . . . 137
Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from flash, ART enable (Cache ON Prefetch OFF) . . . 138
Table 33. Typical current consumption in Run, with different codes running from flash, ART enable (Cache ON Prefetch OFF) and power supplied (by external SMPS (VDD12 = 1.10 V) . . . 138
Table 34. Typical current consumption in Run, with different codes running from flash, ART enable (Cache ON Prefetch OFF) and power supplied (by external SMPS (VDD12 = 1.05 V) . . . 139
Table 35. Typical current consumption in Run and Low-power run modes, with different codes running from flash, ART disable . . . 139

Table 36. Typical current consumption in Run modes, with different codes running from flash, ART disable and power supplied by external SMPS (VDD12 = 1.10 V) 140
Table 37. Typical current consumption in Run modes, with different codes running from flash, ART disable and power supplied by external SMPS (VDD12 = 1.05 V) 140
Table 38. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1 141
Table 39. Typical current consumption in Run, with different codes running from SRAM1 and power supplied by external SMPS (VDD12 = 1.10 V) 141
Table 40. Typical current consumption in Run, with different codes running from SRAM1 and power supplied by external SMPS (VDD12 = 1.05 V) 142
Table 41. Current consumption in Sleep and Low-power sleep modes, flash ON 143
Table 42. Current consumption in Sleep, flash ON and power supplied by external SMPS (VDD12 = 1.10 V) 144
Table 43. Current consumption in Low-power sleep modes, flash in power-down 145
Table 44. Current consumption in Stop 2 mode 145
Table 45. Current consumption in Stop 1 mode 148
Table 46. Current consumption in Stop 0 mode 149
Table 47. Current consumption in Standby mode 150
Table 48. Current consumption in Shutdown mode 152
Table 49. Current consumption in VBAT mode 153
Table 50. Peripheral current consumption 155
Table 51. Low-power mode wakeup timings 158
Table 52. Regulator modes transition times 160
Table 53. Wakeup time using USART/LPUART 160
Table 54. High-speed external user clock characteristics 160
Table 55. Low-speed external user clock characteristics 161
Table 56. HSE oscillator characteristics 162
Table 57. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) 163
Table 58. HSI16 oscillator characteristics 164
Table 59. MSI oscillator characteristics 166
Table 60. HSI48 oscillator characteristics 169
Table 61. LSI oscillator characteristics 170
Table 62. PLL, PLLSAI1, PLLSAI2 characteristics 170
Table 63. Flash memory characteristics 171
Table 64. Flash memory endurance and data retention 172
Table 65. EMS characteristics 173
Table 66. EMI characteristics for fHSE = 8 MHz and fHCLK = 80 MHz 174
Table 67. ESD absolute maximum ratings 174
Table 68. Electrical sensitivities 174
Table 69. I/O current injection susceptibility 175
Table 70. I/O static characteristics 176
Table 71. Output voltage characteristics 179
Table 72. I/O AC characteristics 180
Table 73. NRST pin characteristics 182
Table 74. EXTI Input Characteristics 183
Table 75. Analog switches booster characteristics 183
Table 76. ADC characteristics 184
Table 77. Maximum ADC RAIN 186
Table 78. ADC accuracy - limited test conditions 1 188
Table 79. ADC accuracy - limited test conditions 2 190
Table 80. ADC accuracy - limited test conditions 3 192
Table 81. ADC accuracy - limited test conditions 4 194

Table 82. DAC characteristics . . . 197
Table 83. DAC accuracy . . . 200
Table 84. VREFBUF characteristics . . . 202
Table 85. COMP characteristics . . . 204
Table 86. OPAMP characteristics . . . 205
Table 87. TS characteristics . . . 208
Table 88. V_{BAT} monitoring characteristics . . . 209
Table 89. V_{BAT} charging characteristics . . . 209
Table 90. LCD controller characteristics . . . 209
Table 91. DFSDM characteristics . . . 210
Table 92. TIMx characteristics . . . 213
Table 93. IWDG min/max timeout period at 32 kHz (LSI) . . . 213
Table 94. WWDG min/max timeout value at 80 MHz (PCLK) . . . 213
Table 95. I2C analog filter characteristics . . . 214
Table 96. SPI characteristics . . . 215
Table 97. Quad SPI characteristics in SDR mode . . . 217
Table 98. QUADSPI characteristics in DDR mode . . . 218
Table 99. SAI characteristics . . . 220
Table 100. SD / MMC dynamic characteristics, VDD=2.7 V to 3.6 V . . . 223
Table 101. eMMC dynamic characteristics, VDD = 1.71 V to 1.9 V . . . 223
Table 102. USB OTG DC electrical characteristics . . . 224
Table 103. USB OTG electrical characteristics . . . 225
Table 104. USB BCD DC electrical characteristics . . . 226
Table 105. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 228
Table 106. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings . . . 228
Table 107. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 229
Table 108. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings . . . 230
Table 109. Asynchronous multiplexed PSRAM/NOR read timings . . . 231
Table 110. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . 231
Table 111. Asynchronous multiplexed PSRAM/NOR write timings . . . 232
Table 112. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . 233
Table 113. Synchronous multiplexed NOR/PSRAM read timings . . . 235
Table 114. Synchronous multiplexed PSRAM write timings . . . 237
Table 115. Synchronous non-multiplexed NOR/PSRAM read timings . . . 238
Table 116. Synchronous non-multiplexed PSRAM write timings . . . 240
Table 117. Switching characteristics for NAND flash read cycles . . . 242
Table 118. Switching characteristics for NAND flash write cycles . . . 243
Table 119. DCMI characteristics . . . 243
Table 120. SWPMI electrical characteristics . . . 244
Table 121. SD / MMC dynamic characteristics, VDD=2.7 V to 3.6 V . . . 245
Table 122. SD / MMC dynamic characteristics, VDD=1.71 V to 1.9 V . . . 247
Table 123. UFBGA169 - Mechanical data . . . 249
Table 124. UFBGA169 - Recommended PCB design rules (0.5 mm pitch BGA) . . . 250
Table 125. LQFP144 - Mechanical data . . . 252
Table 126. UFBGA132 - Mechanical data . . . 255
Table 127. UFBGA132 - Recommended PCB design rules (0.5 mm pitch BGA) . . . 256
Table 128. WLCSP115 - Mechanical data . . . 258
Table 129. WLCSP115 - recommended PCB design rules . . . 259
Table 130. LQFP100 - Mechanical data . . . 262
Table 131. WLCSP100L - Mechanical data . . . 265
Table 132. WLCSP100L - Recommended PCB design rules (0.4 mm pitch) . . . 266
Table 133. LQFP64 - Mechanical data . . . 269

Table 134. Package thermal characteristics 271
Table 135. STM32L496xx ordering information scheme 274
Table 136. Document revision history 277

List of figures

Figure 1. STM32L496xx block diagram . . . 17
Figure 2. Multi-AHB bus matrix . . . 21
Figure 3. Power supply overview . . . 24
Figure 4. Power-up/down sequence . . . 25
Figure 5. Clock tree . . . 39
Figure 6. Voltage reference buffer . . . 44
Figure 7. STM32L496Ax UFBGA169 pinout(1) (2) . . . 62
Figure 8. STM32L496Ax, external SMPS device, UFBGA169 pinout(1) (2) . . . 63
Figure 9. STM32L496Zx LQFP144 pinout(1) (2) . . . 64
Figure 10. STM32L496Zx, external SMPS device, LQFP144 pinout(1) (2) . . . 65
Figure 11. STM32L496Qx UFBGA132 ballout(1) (2) . . . 66
Figure 12. STM32L496Qx, external SMPS device, UFBGA132 ballout(1) (2) . . . 66
Figure 13. STM32L496Wx, external SMPS device, WLCSP115 ballout(1) (2) . . . 67
Figure 14. STM32L496Vx LQFP100 pinout(1) . . . 68
Figure 15. STM32L496Vx, external SMPS device, LQFP100 pinout(1) . . . 69
Figure 16. STM32L496Vx WLCSP100L pinout(1) (2) . . . 70
Figure 17. STM32L496Vx, external SMPS device, WLCSP100L pinout(1) (2) . . . 70
Figure 18. STM32L496Rx LQFP64 pinout(1) . . . 71
Figure 19. STM32L496Rx, external SMPS, LQFP64 pinout(1) . . . 71
Figure 20. STM32L496xx memory map . . . 116
Figure 21. Pin loading conditions . . . 122
Figure 22. Pin input voltage . . . 122
Figure 23. Power supply scheme . . . 123
Figure 24. Current consumption measurement scheme with and without external SMPS power supply . . . 124
Figure 25. VREFINT versus temperature . . . 131
Figure 26. High-speed external clock source AC timing diagram . . . 161
Figure 27. Low-speed external clock source AC timing diagram . . . 161
Figure 28. Typical application with an 8 MHz crystal . . . 163
Figure 29. Typical application with a 32.768 kHz crystal . . . 164
Figure 30. HSI16 frequency versus temperature . . . 165
Figure 31. Typical current consumption versus MSI frequency . . . 168
Figure 32. HSI48 frequency versus temperature . . . 170
Figure 33. I/O input characteristics . . . 178
Figure 34. I/O AC characteristics definition(1) . . . 182
Figure 35. Recommended NRST pin protection . . . 183
Figure 36. ADC accuracy characteristics . . . 196
Figure 37. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function . . . 196
Figure 38. 12-bit buffered / non-buffered DAC . . . 199
Figure 39. SPI timing diagram - slave mode and CPHA = 0 . . . 216
Figure 40. SPI timing diagram - slave mode and CPHA = 1 . . . 216
Figure 41. SPI timing diagram - master mode . . . 217
Figure 42. Quad SPI timing diagram - SDR mode . . . 219
Figure 43. Quad SPI timing diagram - DDR mode . . . 220
Figure 44. SAI master timing waveforms . . . 222
Figure 45. SAI slave timing waveforms . . . 222
Figure 46. SDIO high-speed mode . . . 224

Figure 47. SD default mode . . . 224
Figure 48. USB OTG timings – Definition of data signal rise and fall time . . . 225
Figure 49. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 227
Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 229
Figure 51. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 230
Figure 52. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 232
Figure 53. Synchronous multiplexed NOR/PSRAM read timings . . . 234
Figure 54. Synchronous multiplexed PSRAM write timings . . . 236
Figure 55. Synchronous non-multiplexed NOR/PSRAM read timings . . . 238
Figure 56. Synchronous non-multiplexed PSRAM write timings . . . 239
Figure 57. NAND controller waveforms for read access . . . 241
Figure 58. NAND controller waveforms for write access(a) . . . 241
Figure 59. NAND controller waveforms for common memory read access . . . 242
Figure 60. NAND controller waveforms for common memory write access . . . 242
Figure 61. DCMI timing diagram . . . 243
Figure 62. SDIO high-speed mode . . . 245
Figure 63. SD default mode . . . 245
Figure 64. UFBGA169 - Outline . . . 249
Figure 65. UFBGA169 - Recommended footprint . . . 250
Figure 66. LQFP144 - Outline(15) . . . 251
Figure 67. LQFP144 - Recommended footprint . . . 254
Figure 68. UFBGA132 - Outline . . . 255
Figure 69. UFBGA132 - Recommended footprint . . . 256
Figure 70. WLCSP115 - Outline . . . 257
Figure 71. WLCSP115 - Recommended footprint . . . 259
Figure 72. WLCSP115 (external SMPS device) marking (package top view) . . . 260
Figure 73. LQFP100 - Outline(15) . . . 261
Figure 74. LQFP100 - Recommended footprint . . . 263
Figure 75. WLCSP100L - Outline . . . 264
Figure 76. WLCSP100L - Recommended footprint . . . 265
Figure 77. WLCSP100L marking (package top view) . . . 266
Figure 78. WLCSP100L (external SMPS device) marking (package top view) . . . 267
Figure 79. LQFP64 - Outline(15) . . . 268
Figure 80. LQFP64 - Recommended footprint . . . 270

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L496xx microcontrollers.

This document must be read in conjunction with the STM32L47x, STM32L48x, STM32L49x and STM32L4Ax reference manual (RM0351), available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, refer to the Cortex®-M4 Technical Reference Manual, available from the www.arm.com website.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32L496xx errata sheet (ES0335), available on the STMicroelectronics website www.st.com.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32L496xx devices are ultra-low-power microcontrollers based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision that supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L496xx devices embed high-speed memories (up to 1 Mbyte of flash memory, 320 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L496xx devices embed several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 24 capacitive sensing channels are available. The devices also embed an integrated LCD driver 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces, namely four I2Cs, three SPIs, three USARTs, two UARTs and one Low-Power UART, two SAIs, one SDMMC, two CANs, one USB OTG full-speed, one SWPMI (single wire protocol master interface), a camera interface and a DMA2D controller.

The STM32L496xx devices embed HASH hardware accelerators.

The STM32L496xx operates in the -40 to +85 °C (+105 °C junction), -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V V_{DD} power supply when using internal LDO regulator and a 1.05 to 1.32V V_{DD12} power supply when using external SMPS supply. A comprehensive set of power-saving modes makes possible the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, 3.3 V dedicated supply input for USB and up to 14 I/Os can be supplied independently down to 1.08 V. A VBAT input makes it possible to backup the RTC and backup registers. Dedicated V_{DD12} power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

The STM32L496xx family offers seven packages from 64-pin to 169-pin packages.

Table 2. STM32L496xx features and peripherals

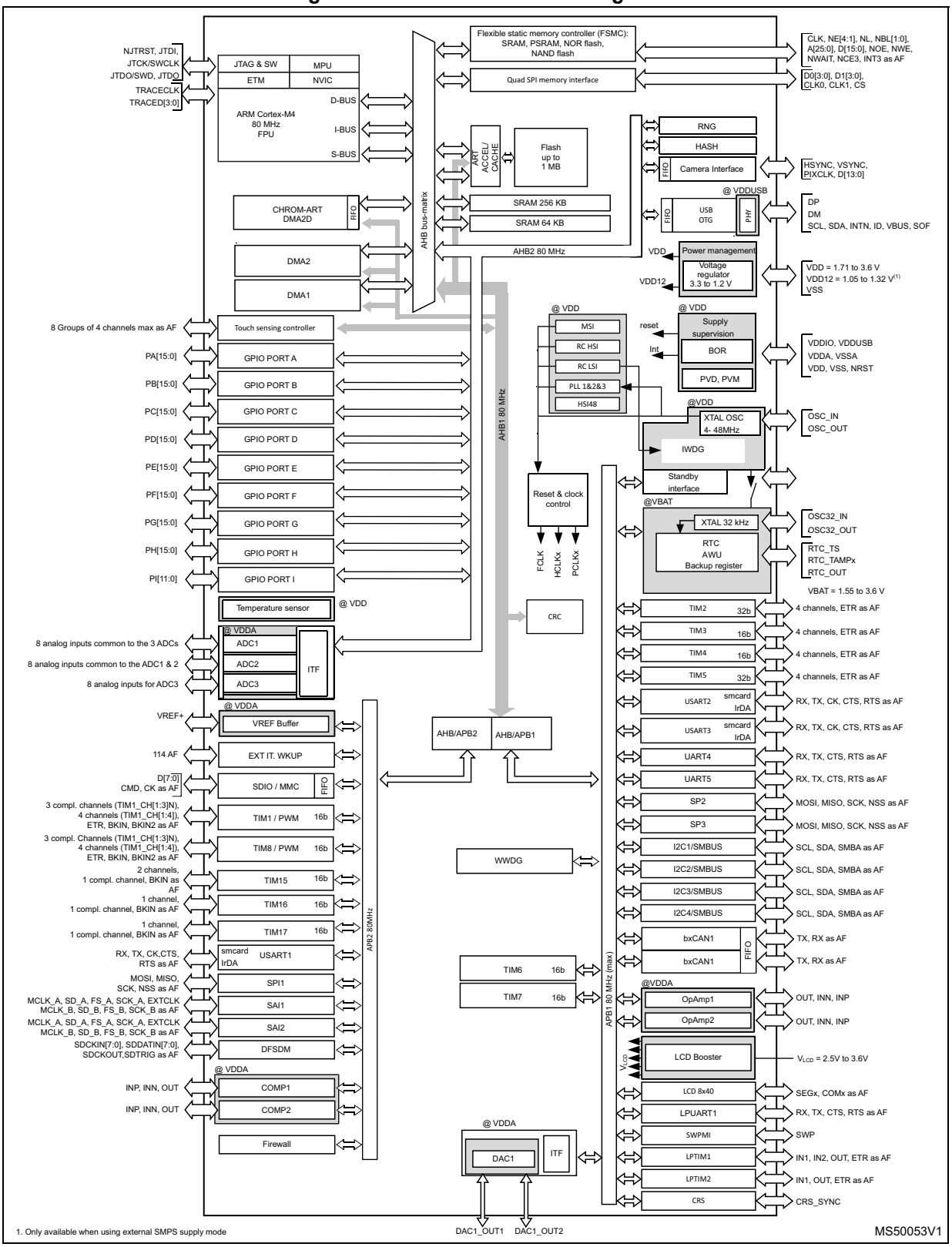
Peripheral		STM32 L496Ax		STM32 L496Zx		STM32 L496Qx		STM32 L496Wx		STM32 L496Vx		STM32 L496Rx	
Flash memory (bytes)		512 K	1 M	512 K	1 M	512 K	1 M	512 K	1 M	512 K	1 M	512 K	1 M
SRAM (bytes)		320 K											
External controller for static memories		Yes		Yes		Yes		Yes(1)		Yes(1)		No	
Quad SPI		Yes											
Timers	Advanced control	2 (16-bit)											
	General purpose	5 (16-bit) 2 (32-bit)											
	Basic	2 (16-bit)											
	Low power	2 (16-bit)											
	SysTick timer	1											
	Watchdog timers (independent window)	2											
Comm. interfaces	SPI	3											
	I^2C	4											
	USART UART LPUART	3 2 1											
	SAI	2											
	CAN	2											
	USB OTG FS	Yes											
	SDMMC	Yes											
	SWPMI	Yes											
Digital filters for sigma-delta modulators		Yes (4 filters)											
Number of channels		8											
RTC		Yes											
Tamper pins		3											
Camera interface		Yes						Yes(2)		Yes		Yes(2)	
Chrom-ART Accelerator™		Yes											
LCD COM x SEG		Yes 8x40 or 4x44											
Random generator		Yes											
HASH		Yes											

Table 2. STM32L496xx features and peripherals (continued)

Peripheral	STM32 L496Ax	STM32 L496Zx	STM32 L496Qx	STM32 L496Wx	STM32 L496Vx	STM32 L496Rx
GPIOs(3)	136	115	110	86	83	52
Wakeup pins	5	5	5	5	5	4
Nb of I/Os down to 1.08 V(4)	14	14	14	13	0	0
Capacitive sensing Number of channels	24	24	24	18	21	21
12-bit ADCs	3	3	3	3	3	3
Number of channels	24	24	19	16	16	16
12-bit DAC channels	2					
Internal voltage reference buffer	Yes					
Analog comparators	2					
Operational amplifiers	2					
Maximum CPU frequency	80 MHz					
Operating voltage (V_{DD})	1.71 to 3.6 V					
Operating voltage (V_{DD12})	1.05 to 1.32 V					
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 130 °C					
Packages	UFBGA169	LQFP144	UFBGA132	WLCSP115	LQFP100 WLCSP100L	LQFP64

1. For LQFP100, WLCSP100L and WLCSP115 packages, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip select.
2. Only up to 13 data bits.
3. If an external SMPS package type is used, two GPIOs are replaced by VDD12 pins to connect the SMPS power supplies, reducing the number of available GPIOs by two.
4. These GPIOs are supplied by V_{DDIO2}.

Figure 1. STM32L496xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm® processors for embedded systems, developed to provide a low-cost platform that meets the needs of MCU implementation with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an Arm® core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions enabling efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded Arm® core, the STM32L496xx family is compatible with all Arm® tools and software.

Figure 1 shows the general block diagram of the STM32L496xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator optimized for STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over flash memory technologies, which normally requires the processor to wait for the flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80 MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 Gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded flash memory

STM32L496xx devices feature up to 1 Mbyte of embedded flash memory available for storing programs and data. The flash memory is divided into two banks allowing read-while-write operations. This feature permits to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP_RDP) allows the user to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- single error detection and correction
- double error detection.

The address of the ECC fail can be read in the ECC register.

3.5 Embedded SRAM

STM32L496xx devices feature 320 Kbyte of embedded SRAM, split into two blocks:

- 256 Kbyte mapped at address 0x2000 0000 (SRAM1)
- 64 Kbyte located at address 0x1000 0000 with hardware parity check (SRAM2).

  This memory is also mapped at address 0x2004 0000, offering a contiguous address space with the SRAM1.

  This block is accessed through the ICode/DCode buses for maximum performance. These 64 Kbyte SRAM can also be retained in Standby mode.

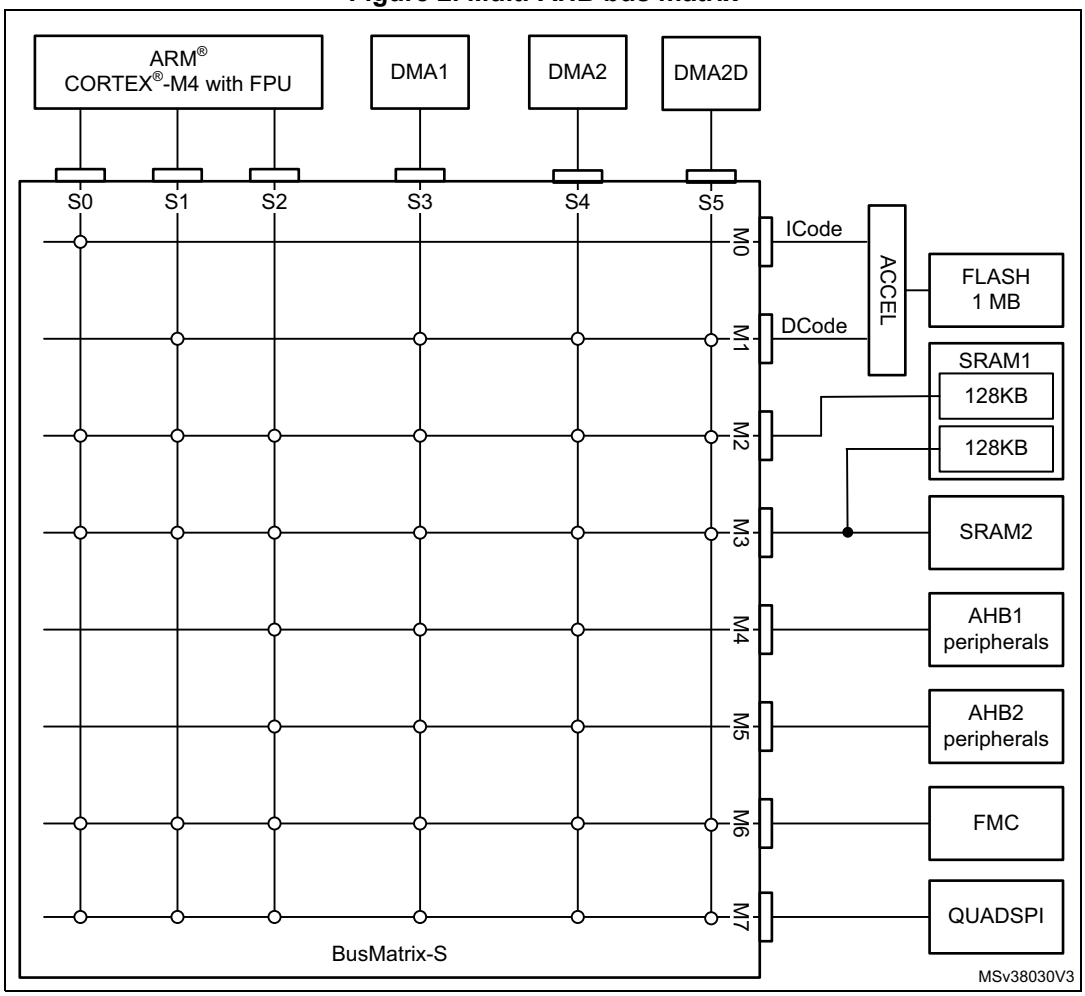
  The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs and the DMA2D) and the slaves (flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

The Firewall main features are the following:

- Three segments can be protected and defined thanks to the Firewall registers:
  - Code segment (located in flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segments are configurable:
  - Code segment: up to 1024 Kbyte with granularity of 256 bytes
  - Non-volatile data segment: up to 1024 Kbyte with granularity of 256 bytes
  - Volatile data segment: up to 256 Kbyte of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the Firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the Firewall configuration

The flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.8 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from user flash memory
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the flash memory by using USART, I2C, SPI, CAN or USB OTG FS in Device mode through DFU (device firmware upgrade).

BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

An empty check mechanism is implemented to force the boot from system flash if the first memory location is not programmed and if the boot selection is configured to boot from main flash. If the boot selection uses BOOT0 pin to boot from the main flash memory, but the first flash memory location is found empty, the flash empty check mechanism forces boot from the system memory (containing embedded bootloader). Then due to bootloader activation, some of the GPIOs are reconfigured from the High-Z state. Please refer to AN2606 for more details concerning the bootloader and GPIOs configuration in system memory boot mode.

It is possible to disable this feature by configuring the option bytes (instead of BOOT0 pin) to force boot from the main flash memory (nSWBOOT0 = 0, nBOOT0 = 1).

3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of

the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.10 Power supply management

3.10.1 Power supply schemes

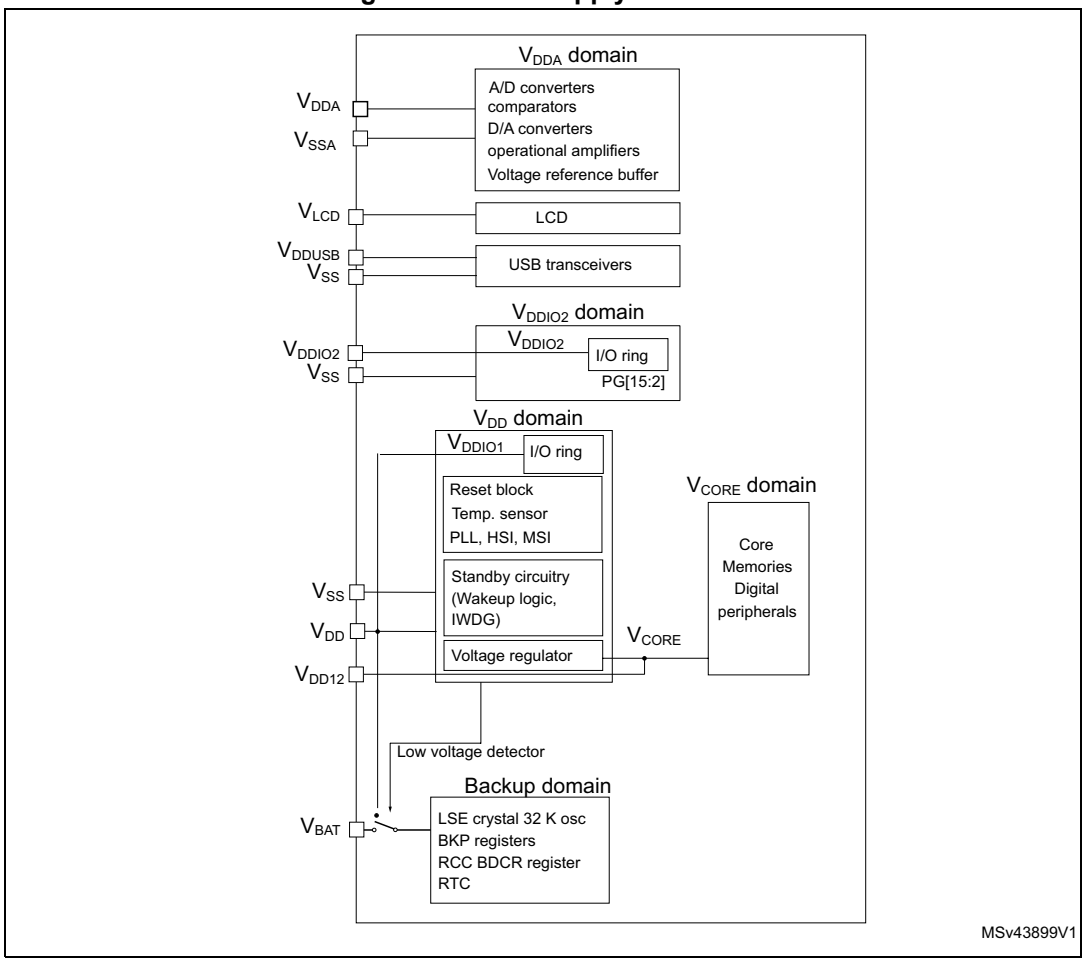
- V_{DD} = 1.71 to 3.6 V: external power supply for I/Os (V_{DDIO1}), the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- V_{DD12} = 1.05 to 1.32 V: external power supply bypassing internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.
- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 (DAC/OPAMPs) to 3.6 V: external analog power supply for ADCs, DAC, OPAMPs, Comparators and Voltage reference buffer. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- V_{DDIO2} = 1.08 to 3.6 V: external power supply for 14 I/Os (PG[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage.
- V_{LCD} = 2.5 to 3.6 V: the LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
- V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: When the functions supplied by V_{DDA}, V_{DDUSB} or V_{DDIO2} are not used, these supplies should preferably be shorted to V_{DD}.

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant (refer to Table 19: Voltage characteristics).

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1} or V_{DDIO2}, with V_{DDIO1} = V_{DD}. V_{DDIO2} supply voltage level is independent from V_{DDIO1}.

Figure 3. Power supply overview

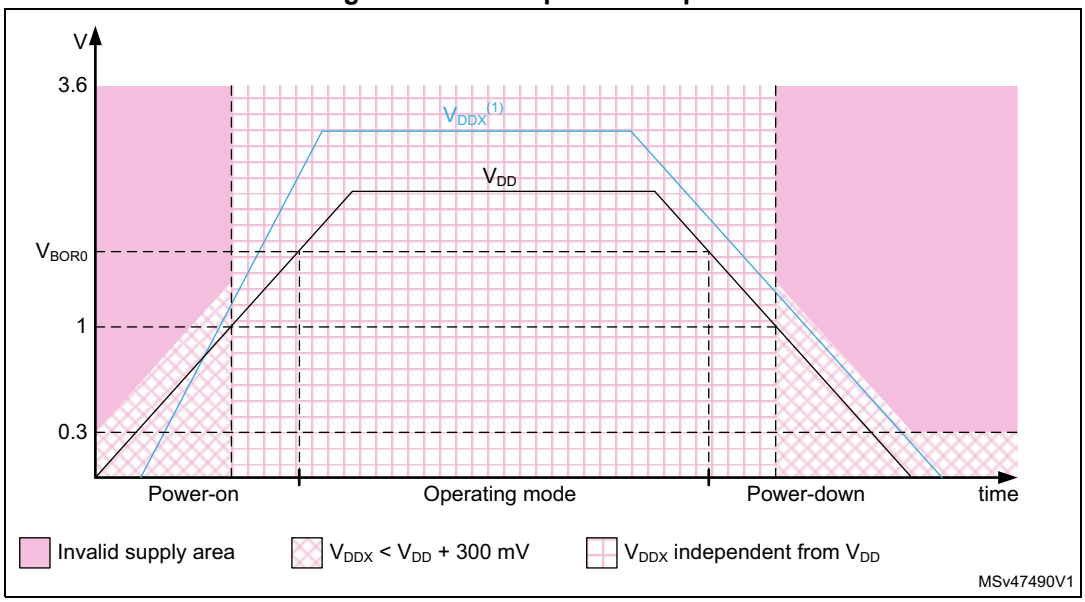


During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{LCD}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 4. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{LCD}.

3.10.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.10.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbyte SRAM2 in Standby with SRAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L496xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The V_{CORE} can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

When the MR is in use, the STM32L496xx with the external SMPS option permits to force an external V_{CORE} supply on the VDD12 supply pins.

When V_{DD12} is forced by an external source and is higher than the output of the internal LDO, the current is taken from this external supply and the overall power efficiency is significantly improved if using an external step down DC/DC converter.

3.10.4 Low-power modes

The ultra-low-power STM32L496xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources.

Table 4. STM32L496xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA and peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Run	MR range 1	Yes	ON[4]	ON	Any	All	N/A	108 µA/MHz	N/A
	SMPS range 2 High							40 µA/MHz[5]	
	MR range 2					All except OTG_FS, RNG		93 µA/MHz	
	SMPS range 2 Low							39 µA/MHz[6]	
LPRun	LPR	Yes	ON[4]	ON	Any except PLL	All except OTG_FS, RNG	N/A	129 µA/MHz	to Range 1: 4 µs to Range 2: 64 µs
Sleep	MR range 1	No	ON[4]	ON[7]	Any	All	Any interrupt or event	32 µA/MHz	6 cycles
	SMPS range 2 High							11.5 µA/MHz[5]	
	MR range 2					All except OTG_FS, RNG		30 µA/MHz	
	SMPS range 2 Low							13 µA/MHz[6]	
LPSleep	LPR	No	ON[4]	ON[7]	Any except PLL	All except OTG_FS, RNG	Any interrupt or event	51 µA/MHz	6 cycles
Stop 0	MR Range 1[8]	No	OFF	ON	LSE LSI	BOR, PVD, PVM RTC,LCD, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1,2) USARTx (x=1...5)[9] LPUART1[9] I2Cx (x=1...4)[10] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) USARTx (x=1...5)[9] LPUART1[9] I2Cx (x=1...4)[10] LPTIMx (x=1,2) OTG_FS[11] SWPMI1[12]	TBD	2.7 µs in SRAM 6.2 µs in flash
	MR Range 2[8]							127 µA	

Table 4. STM32L496xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA and peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1,2) DAC1 OPAMPx (x=1,2) USARTx (x=1...5)[9] LPUART1[9] I2Cx (x=1...4)[10] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) USARTx (x=1...5)[9] LPUART1[9] I2Cx (x=1...4)[10] LPTIMx (x=1,2) OTG_FS[11] SWPMI1[12]	11.2 µA w/o RTC 11.8 µA w RTC	6.6 µs in SRAM 7.8 µs in flash
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) I2C3[10] LPUART1[9] LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, LCD, IWDG COMPx (x=1..2) I2C3[10] LPUART1[9] LPTIM1	2.57 µA w/o RTC 2.86 µA w/RTC	6.8 µs in SRAM 8.2 µs in flash

Table 4. STM32L496xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA and peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Standby	LPR	Powered Off	Off	SRAM 2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[13] BOR, RTC, IWDG	0.48 µA w/o RTC 0.78 µA w/ RTC	15.3 µs
	OFF			Powered Off				0.11 µA w/o RTC 0.42 µA w/ RTC	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down[14]	Reset pin 5 I/Os (WKUPx)[14] RTC	0.03 µA w/o RTC 0.23 µA w/ RTC	306 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. Theoretical value based on V_{DD} = 3.3 V, DC/DC Efficiency of 85%, V_{CORE} = 1.10 V
6. Theoretical value based on V_{DD} = 3.3 V, DC/DC Efficiency of 85%, V_{CORE} = 1.05 V
7. The SRAM1 and SRAM2 clocks can be gated on or off independently.
8. SMPS mode can be used in STOP0 Mode, but no significant power gain can be expected.
9. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
10. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
11. OTG_FS wakeup by resume from suspend and attach detection protocol event.
12. SWPMI1 wakeup by resume from suspend.
13. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
14. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with V_{CORE} supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the V_{CORE} domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in Standby mode, supplied by the low-power Regulator (Standby with SRAM2 retention mode).

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

  The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode permits to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 5. Functionalities depending on the working mode(1)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (up to 1 MB)	O(2)	O(2)	O(2)	O(2)	-	-	-	-	-	-	-	-	-
SRAM1 (256 KB)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 KB)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	O(4)	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
Quad SPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
DMA2D	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed Internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi-Speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O

Table 5. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Number of RTC Tamper pins	3	3	3	3	3	O	3	O	3	O	3	O	3
Camera interface	O	O	O	O	-	-	-	-	-	-	-	-	-
LCD	O	O	O	O	O	O	O	O	-	-	-	-	-
USB OTG FS	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3,4,5)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
CAN(x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SWPMI1	O	O	O	O	-	O	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
DAC1	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1 (LPTIM1)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-

Table 5. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
HASH hardware accelerator	O	O	O	O	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.10.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.10.6 VBAT operation

The VBAT pin permits to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.11 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, low-power run and sleep, Stop 0, Stop 1 and Stop 2 modes.

Table 6. STM32L496xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADCx DAC1 DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
TIM16/TIM17	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-

Table 6. STM32L496xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADCx DAC1 DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 only.

3.12 Clocks and startup

The clock controller (see *Figure 5*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

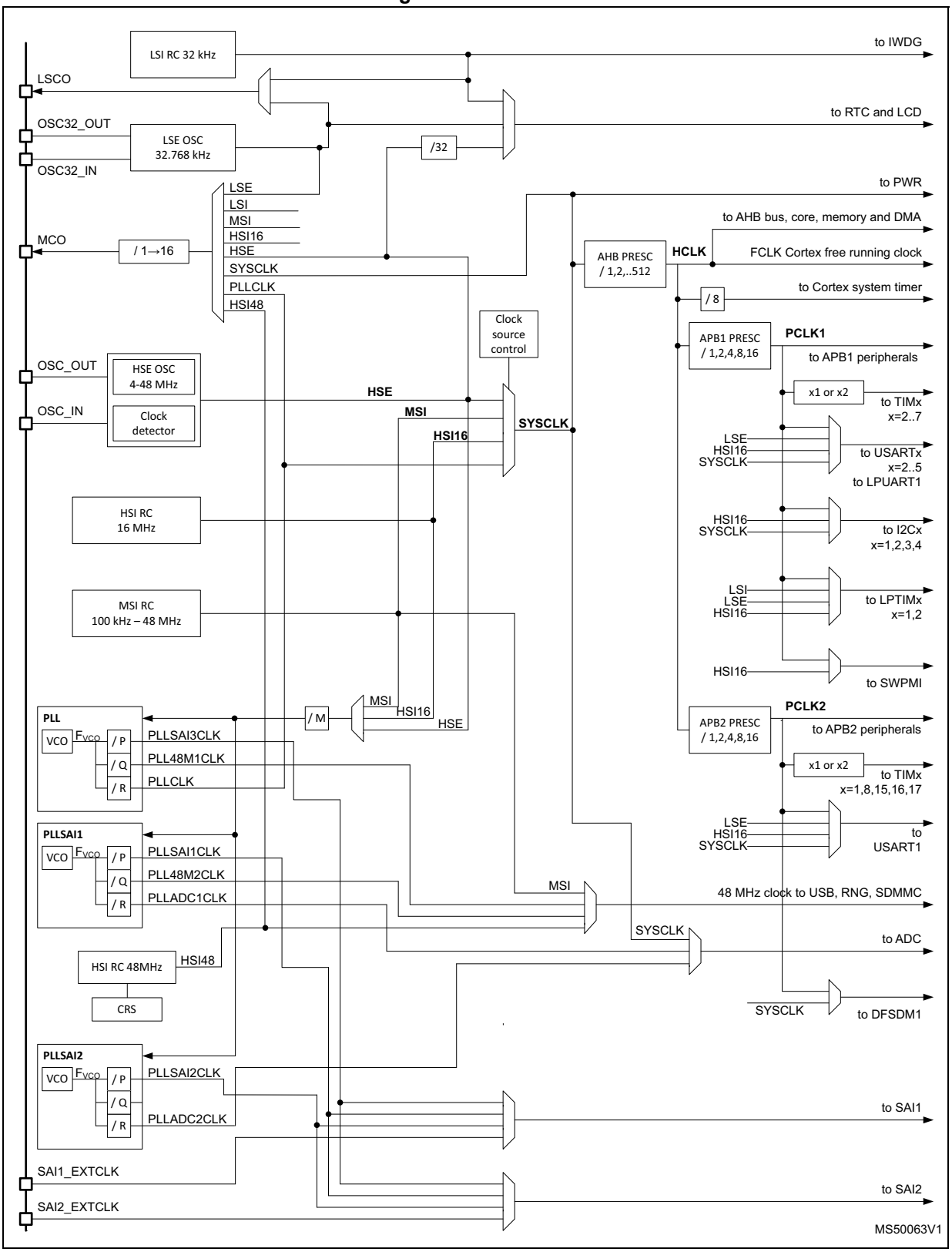
- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- RC48 with clock recovery system (HSI48): internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO: microcontroller clock output:** it outputs one of the internal clocks for external use by the application. Low frequency clocks (LSI, LSE) are available down to Stop 1 low power state.
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes down to Standby mode. LSE can also be output on LSCO in Shutdown mode. LSCO is not available in VBAT mode.

Several prescalers permit to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 80 MHz.

Figure 5. Clock tree



3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (example: request 1 has priority over request 2)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.15 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.16 Interrupts and events

3.16.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 90 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.16.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 41 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 136 GPIOs can be connected to the 16 external interrupt lines.

3.17 Analog to digital converter (ADC)

The device embeds 3 successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 24 external channels, some of them shared between ADC1 and ADC2, or ADC1, ADC2 and ADC3.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1_OUT1 and DAC1_OUT2.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Handles two ADC converters for dual mode operation (simultaneous or interleaved sampling modes)
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into 3 data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.17.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 and ADC3_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 8. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.17.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 9. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.17.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18 or ADC3_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.18 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.19 Voltage reference buffer (VREFBUF)

The STM32L496xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DAC and also as voltage reference for external components through the VREF+ pin.

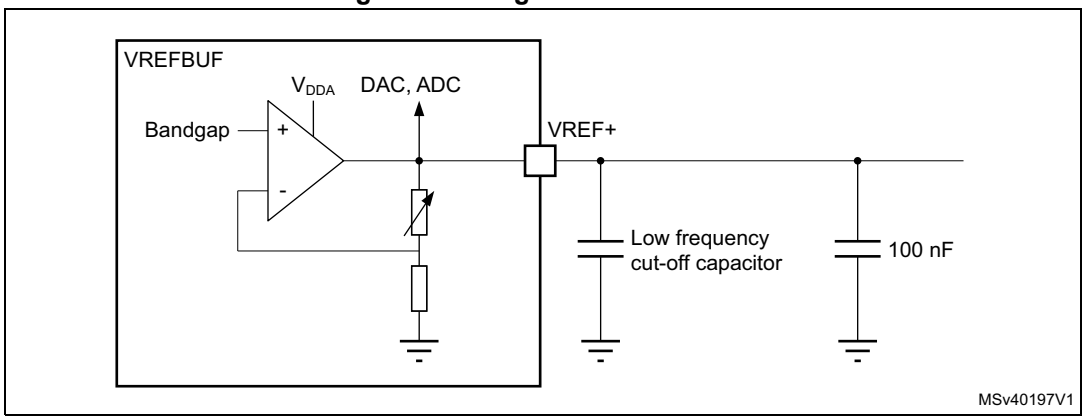
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 6. Voltage reference buffer



3.20 Comparators (COMP)

The STM32L496xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.21 Operational amplifier (OPAMP)

The STM32L496xx embeds two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.22 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 24 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.23 Liquid crystal display controller (LCD)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the VLCD pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Integrated voltage output buffers for higher LCD driving capability
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.24 Digital filter for Sigma-Delta modulators (DFSDM)

The device embeds one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in

hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM or from internal ADCs).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADCs data or device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM1_FLT0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion
- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode

without having any impact on the timing of “injected” conversions

– “injected” conversions for precise timing and with high conversion priority

3.25 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.26 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.27 HASH hardware accelerator (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the HMAC (keyed-hash message authentication code) algorithm suitable for a variety of applications.

It computes a message digest (160 bits for the SHA-1 algorithm, 256 bits for the SHA-256 algorithm and 224 bits for the SHA-224 algorithm,128 bits for the MD5 algorithm) for messages of up to (2^{64} - 1) bits, while HMAC algorithms provide a way of authenticating messages by means of hash functions. HMAC algorithms consist in calling the SHA-1, SHA-224, SHA-256 or MD5 hash function twice.

3.28 Timers and watchdogs

The STM32L496xx includes two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.28.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.28.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.28.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L496xx (see *Table 10* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.28.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.28.4 Low-power timer (LPTIM1 and LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 is active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only)

3.28.5 Infrared interface (IRTIM)

The STM32L496xx includes one infrared interface (IRTIM), which can be used with an infrared LED to perform remote control functions. It uses TIM16 and TIM17 output channels to generate output signal waveforms on IR_OUT pin.

3.28.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.28.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.28.8 SysTick timer

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.29 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

3.30 Inter-integrated circuit interface (I^2C)

The device embeds four I2C. Refer to *Table 11* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 3.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 5: Clock tree*.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 11. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

3.31 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L496xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable, and are able to communicate at speeds of up to 10 Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 204 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 12. STM32L496xx USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

3.32 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.33 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to 40 Mbits/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.34 Serial audio interfaces (SAI)

The device embeds 2 SAI. Refer to *Table 13* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility permitting to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 13. SAI implementation

SAI features(1)	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO size	X (8 words)	X (8 words)
SPDIF	X	X

1. X: supported

3.35 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.36 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

Dual CAN peripheral configuration is available. The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - Scalable filter banks: 28 filter banks shared between CAN1 and CAN2
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.37 Secure digital input/output and MultiMediaCards interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.38 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that can be provided by the internal multispeed oscillator (MSI) automatically trimmed by 32.768 kHz external oscillator (LSE).This permits to use the USB device without external high speed crystal (HSE).

The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

The major features are:

- Combined Rx and Tx FIFO size of 1.25 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

3.39 Clock recovery system (CRS)

The STM32L496xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.40 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (4 memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbyte of data
- 8-,16- bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

For WLCSP100L package, address lines [A18:A16] are missing versus other 100 pin packages, thus FMC provides only 2MB of addressable space, split into 64K blocks. The main usage of the FMC in this case is to drive external LCD interface.

3.41 Dual-flash Quad SPI memory interface (QUADSPI)

The Dual-flash Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external flash is memory mapped and is seen by the system as if it were an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

The Dual-flash Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- Dual-flash mode, where 8 bits can be sent/received simultaneously by accessing two flash memories in parallel.
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.42 Development support

3.42.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using only two pins instead of the five required by the JTAG (JTAG pins can be reused as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.42.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell™ provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L496xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell™ operates with third party debugger software tools.

4 Pinouts and pin description

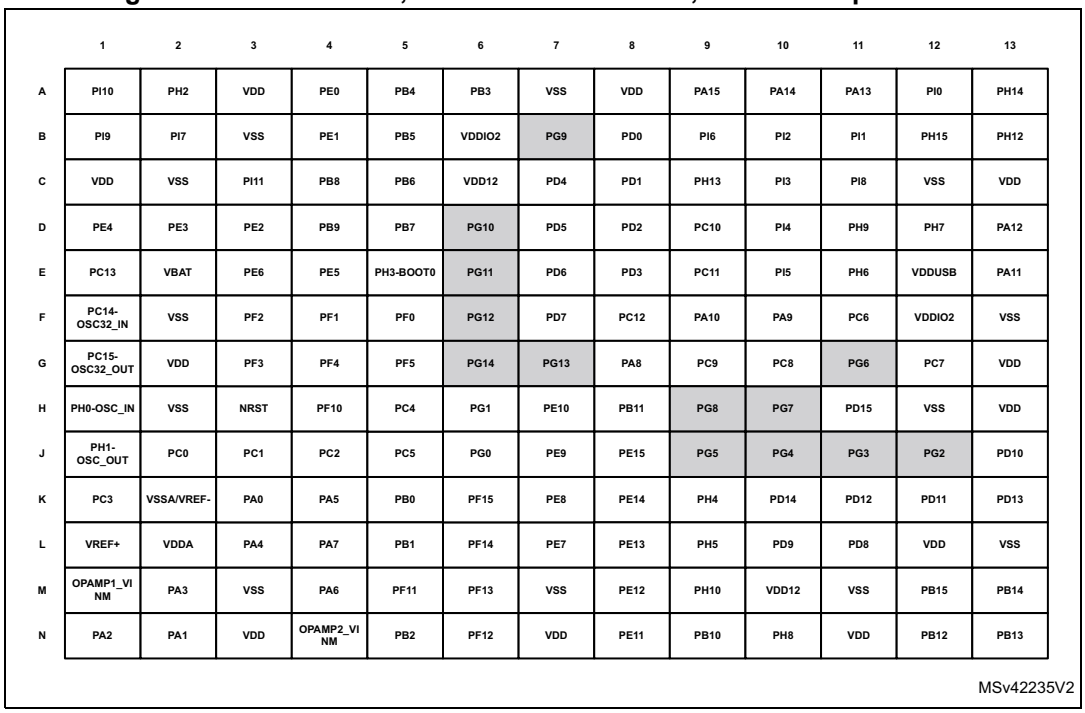
Figure 7. STM32L496Ax UFBGA169 pinout(1)(2)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv38036V5

1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 8. STM32L496Ax, external SMPS device, UFBGA169 pinout(1)(2)

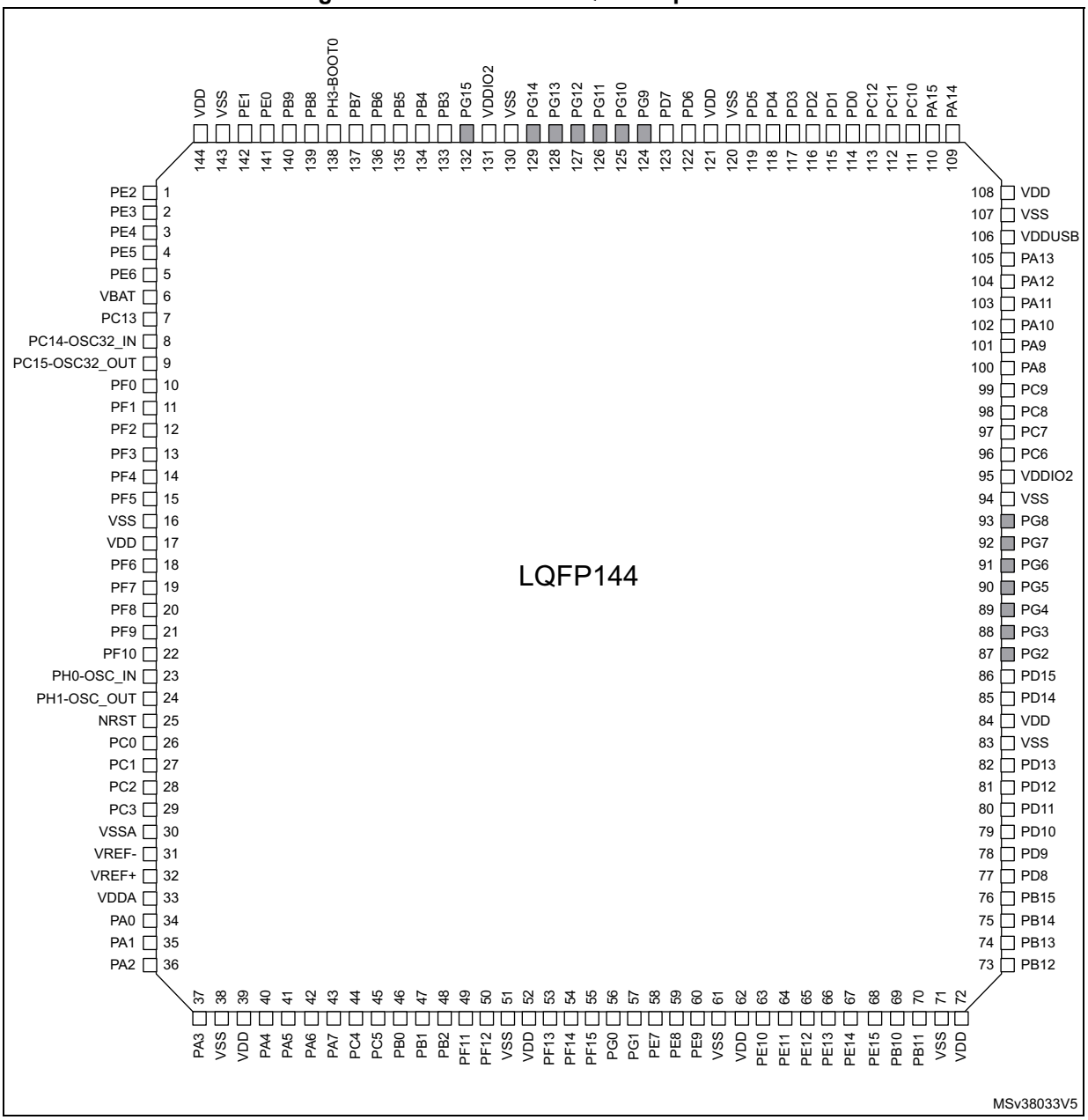


	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	VDD12	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	VDD12	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

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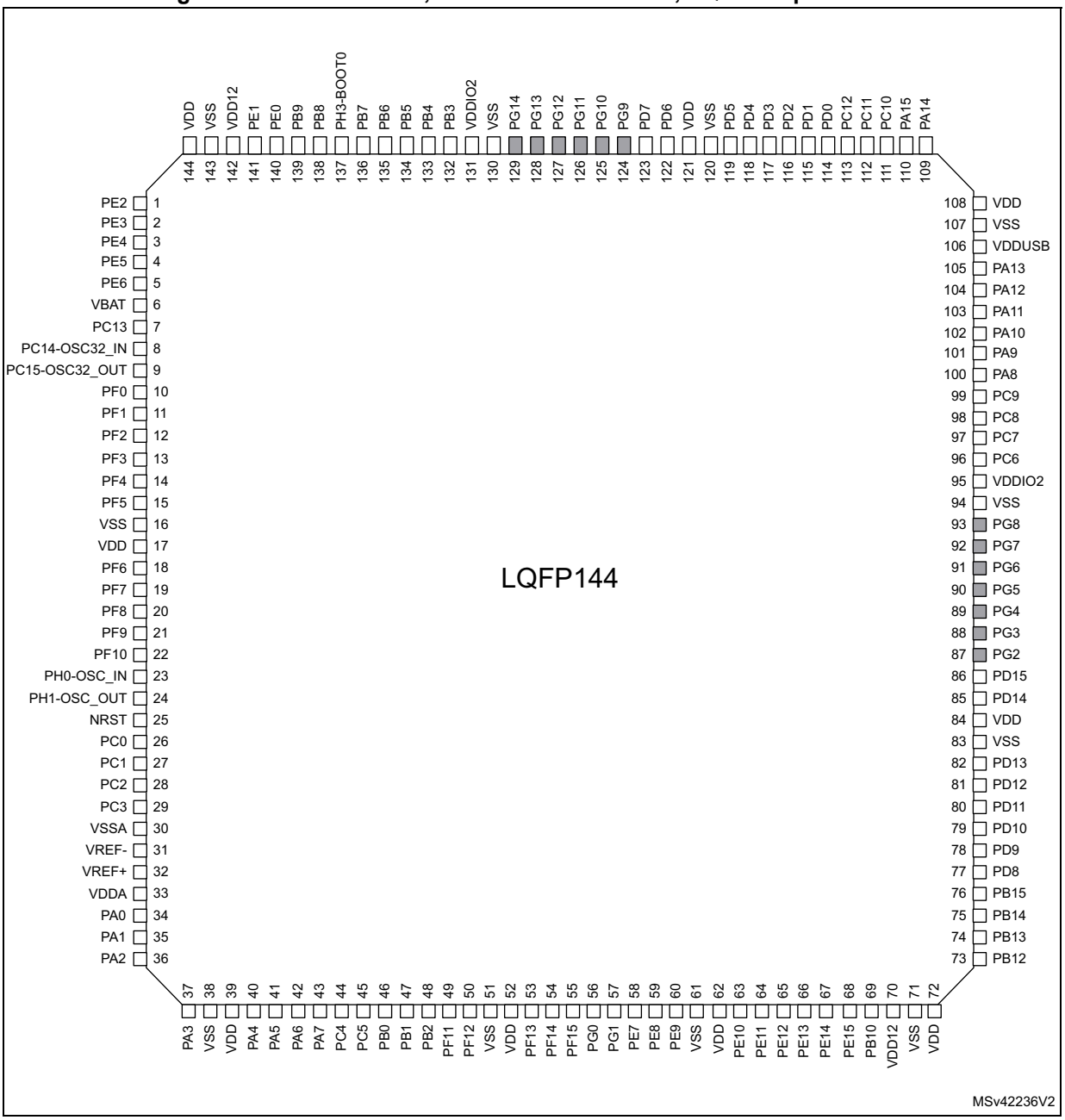
1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 9. STM32L496Zx LQFP144 pinout(1)(2)



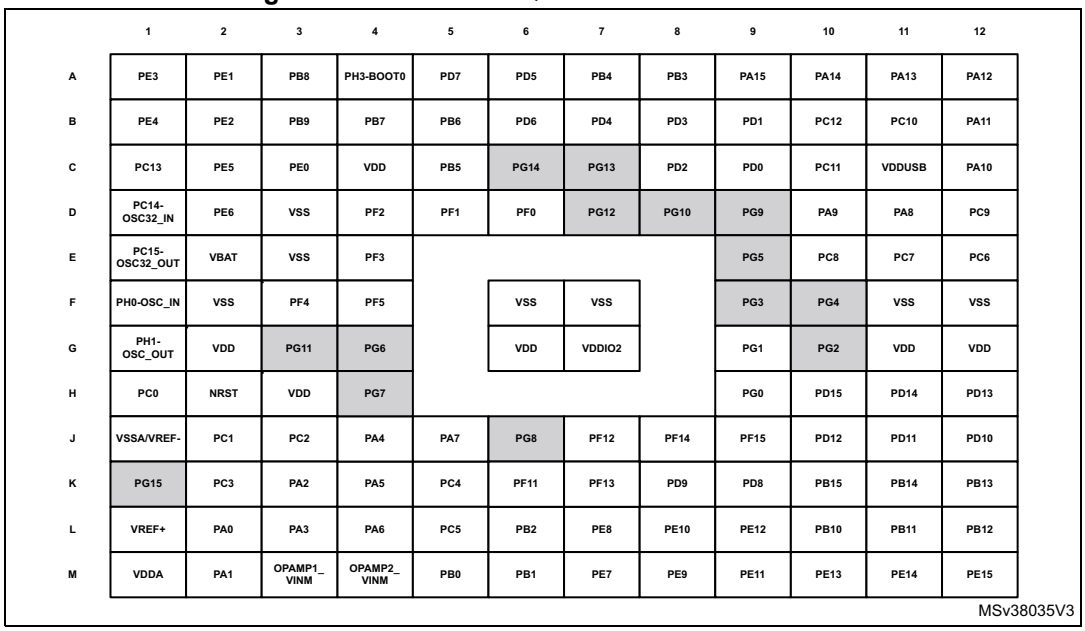
1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 10. STM32L496Zx, external SMPS device, LQFP144 pinout(1)(2)



1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 11. STM32L496Qx UFBGA132 ballout(1)(2)

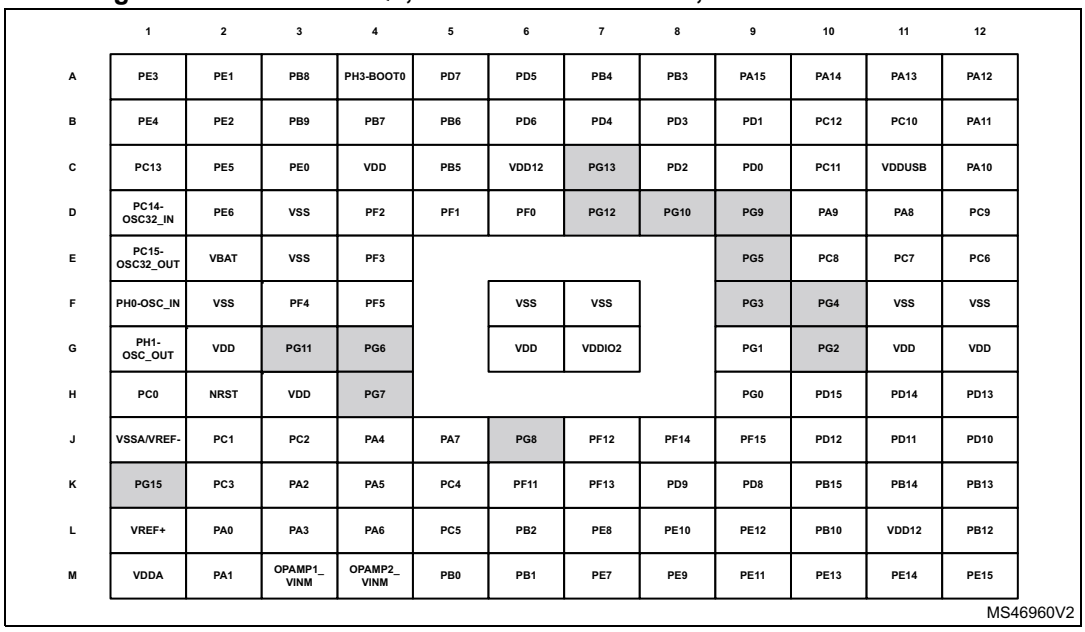


	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

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1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 12. STM32L496Qx, external SMPS device, UFBGA132 ballout(1)(2)

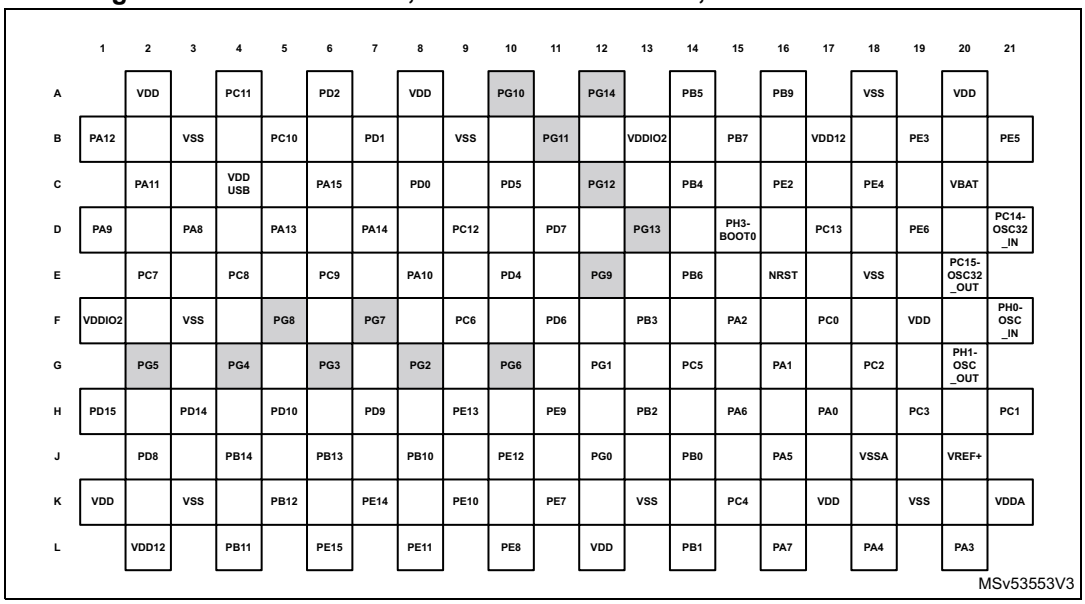


	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	VDD12	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	VDD12	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

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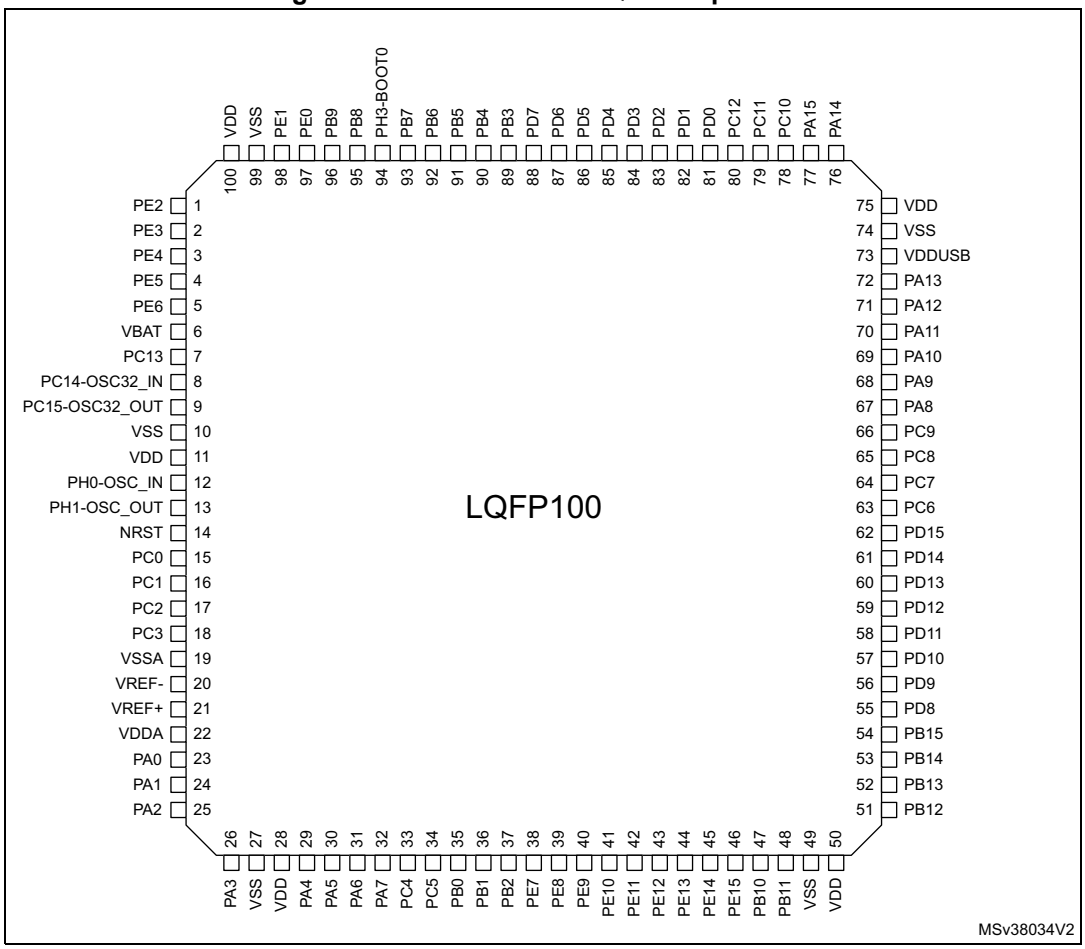
1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 13. STM32L496Wx, external SMPS device, WLCSP115 ballout(1)(2)



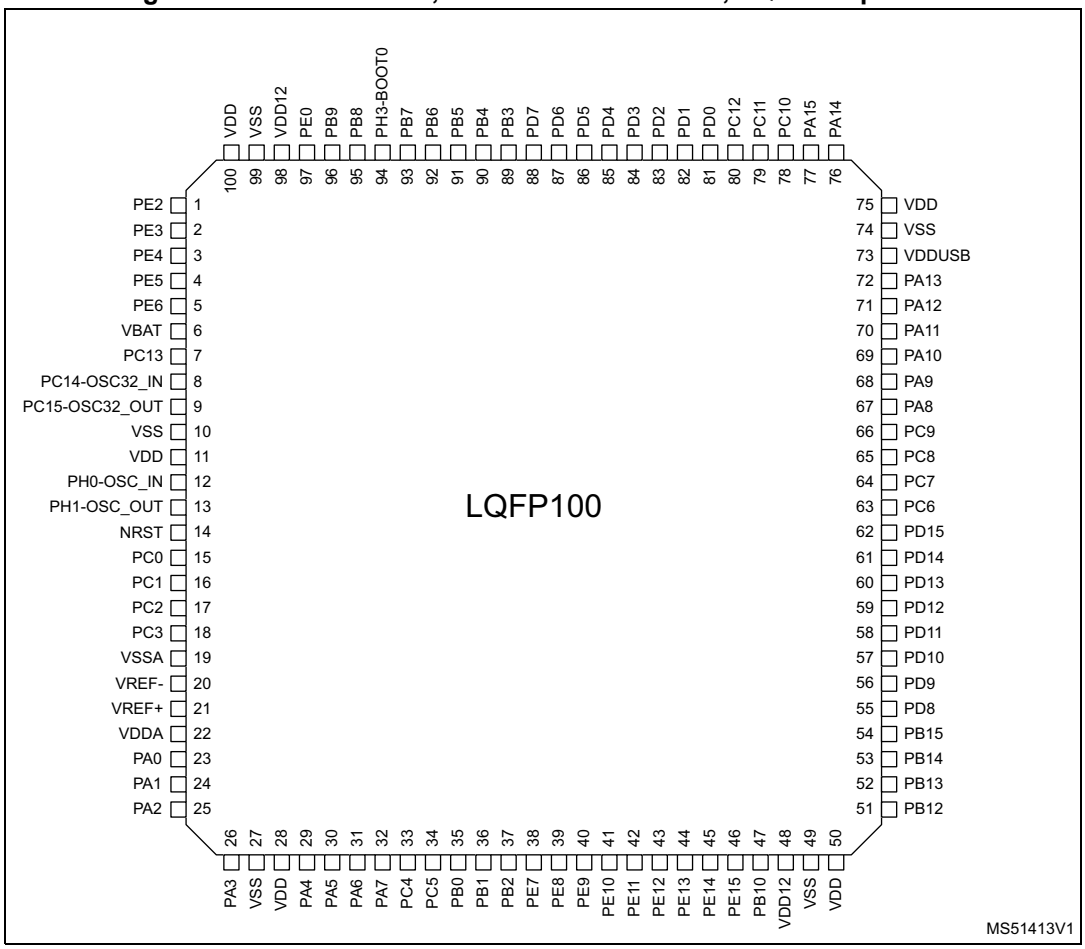
1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 14. STM32L496Vx LQFP100 pinout(1)



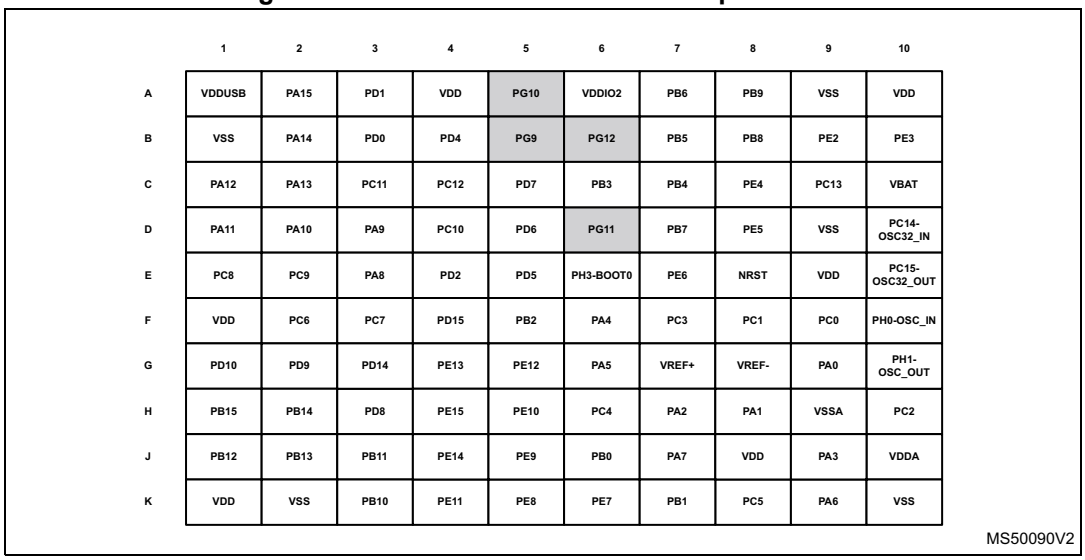
1. The above figure shows the package top view.

Figure 15. STM32L496Vx, external SMPS device, LQFP100 pinout(1)



1. The above figure shows the package top view.

Figure 16. STM32L496Vx WLCSP100L pinout(1)(2)

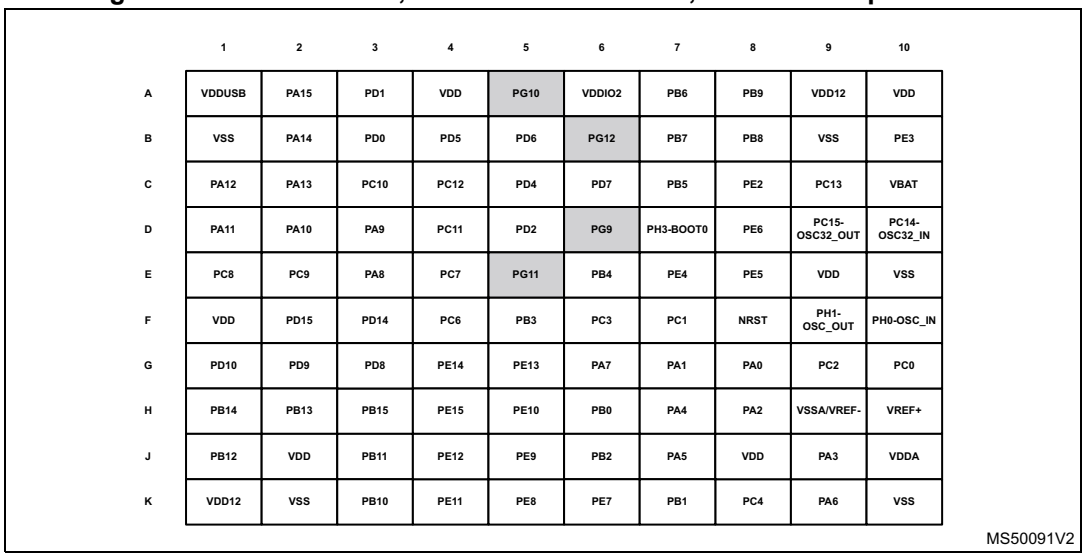


	1	2	3	4	5	6	7	8	9	10
A	VDDUSB	PA15	PD1	VDD	PG10	VDDIO2	PB6	PB9	VSS	VDD
B	VSS	PA14	PD0	PD4	PG9	PG12	PB5	PB8	PE2	PE3
C	PA12	PA13	PC11	PC12	PD7	PB3	PB4	PE4	PC13	VBAT
D	PA11	PA10	PA9	PC10	PD6	PG11	PB7	PE5	VSS	PC14-OSC32_IN
E	PC8	PC9	PA8	PD2	PD5	PH3-BOOT0	PE6	NRST	VDD	PC15-OSC32_OUT
F	VDD	PC6	PC7	PD15	PB2	PA4	PC3	PC1	PC0	PH0-OSC_IN
G	PD10	PD9	PD14	PE13	PE12	PA5	VREF+	VREF-	PA0	PH1-OSC_OUT
H	PB15	PB14	PD8	PE15	PE10	PC4	PA2	PA1	VSSA	PC2
J	PB12	PB13	PB11	PE14	PE9	PB0	PA7	VDD	PA3	VDDA
K	VDD	VSS	PB10	PE11	PE8	PE7	PB1	PC5	PA6	VSS

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1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 17. STM32L496Vx, external SMPS device, WLCSP100L pinout(1)(2)

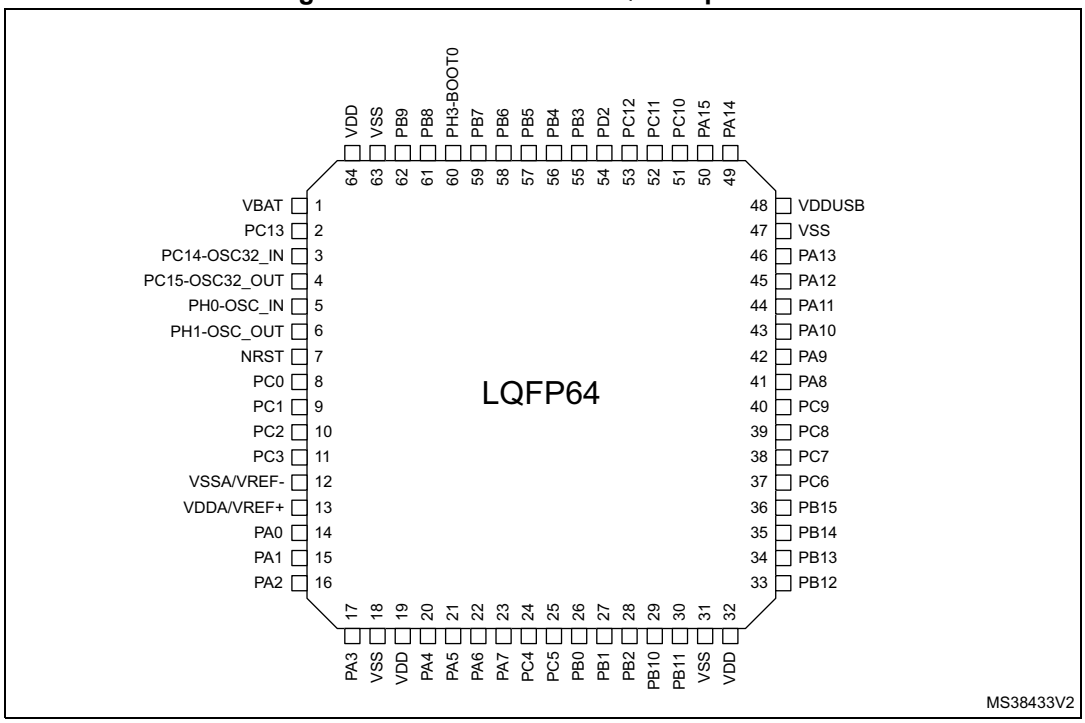


	1	2	3	4	5	6	7	8	9	10
A	VDDUSB	PA15	PD1	VDD	PG10	VDDIO2	PB6	PB9	VDD12	VDD
B	VSS	PA14	PD0	PD5	PD6	PG12	PB7	PB8	VSS	PE3
C	PA12	PA13	PC10	PC12	PD4	PD7	PB5	PE2	PC13	VBAT
D	PA11	PA10	PA9	PC11	PD2	PG9	PH3-BOOT0	PE6	PC15-OSC32_OUT	PC14-OSC32_IN
E	PC8	PC9	PA8	PC7	PG11	PB4	PE4	PE5	VDD	VSS
F	VDD	PD15	PD14	PC6	PB3	PC3	PC1	NRST	PH1-OSC_OUT	PH0-OSC_IN
G	PD10	PD9	PD8	PE14	PE13	PA7	PA1	PA0	PC2	PC0
H	PB14	PB13	PB15	PE15	PE10	PB0	PA4	PA2	VSSA/VREF-	VREF+
J	PB12	VDD	PB11	PE12	PE9	PB2	PA5	VDD	PA3	VDDA
K	VDD12	VSS	PB10	PE11	PE8	PE7	PB1	PC4	PA6	VSS

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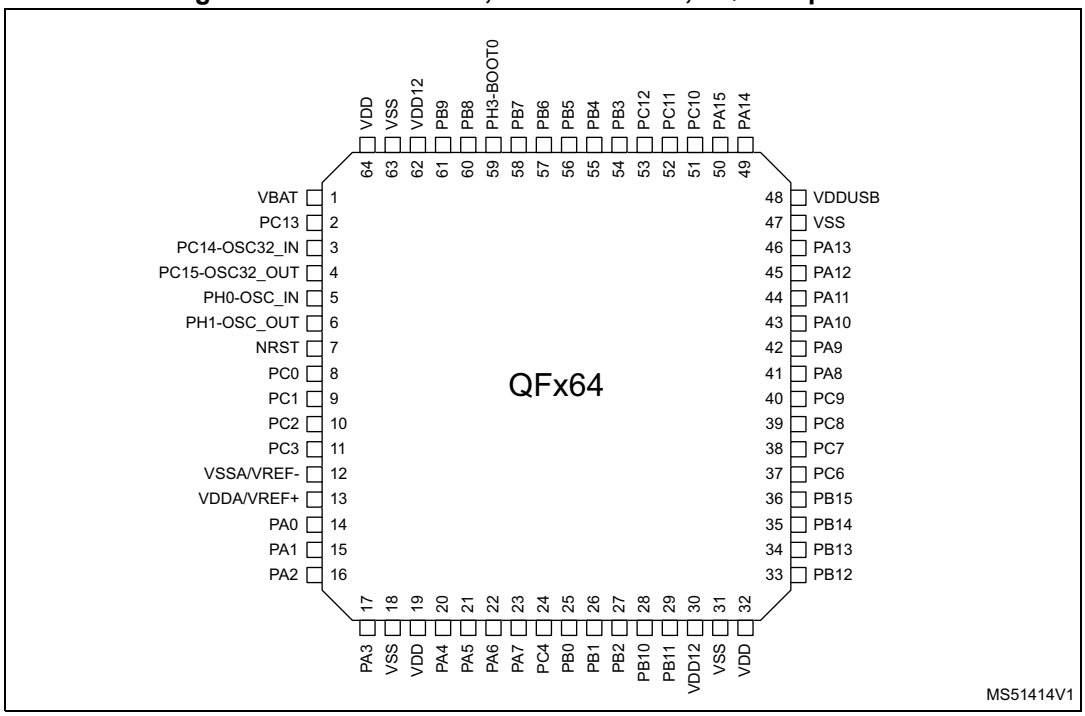
1. The above figure shows the package top view.
2. The I/O pins supplied by V_{DDIO2} are shown in gray.

Figure 18. STM32L496Rx LQFP64 pinout(1)



1. The above figure shows the package top view.

Figure 19. STM32L496Rx, external SMPS, LQFP64 pinout(1)



1. The above figure shows the package top view.

Table 14. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_l (2)	I/O, with LCD function supplied by V_{LCD}
		_u (3)	I/O, with USB function supplied by V_{DDUSB}
		_a (4)	I/O, with Analog switch function supplied by V_{DDA}
		_s (5)	I/O supplied only by V_{DDIO2}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 15* are: FT_f, FT_fa, FT_fl, FT_fla.
2. The related I/O structures in *Table 15* are: FT_l, FT_fl, FT_lu.
3. The related I/O structures in *Table 15* are: FT_u, FT_lu.
4. The related I/O structures in *Table 15* are: FT_a, FT_la, FT_fa, FT_fla, TT_a, TT_la.
5. The related I/O structures in *Table 15* are: FT_s, FT_fs.

Note: FT_a and FT_fa pins can be connected to analog peripherals inputs. When analog peripheral is not connected to this FT_a or FT_fa pins (analog switch from GPIO to peripheral is not closed, for example ADC not uses given pin as ADC input), then GPIO can accept V_{DD} + 3.6 V (5 V tolerant I/O). However, once the I/O input is connected to the analog peripheral (for example ADC selects as input channel from this pin), the parasitic diode from this I/O pin to V_{DDA} and/or V_{REF+} does not allow to use higher voltage on given I/O pin than V_{DDA} or V_{REF+} and pin is no more 5 V-tolerant I/O.

Table 15. STM32L496xx pin definitions

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	-	-	-	-	-	C3	C3	PI11	I/O	FT	-	EVENTOUT	-
-	-	B9	C8	1	1	C16	B2	B2	1	1	D3	D3	PE2	I/O	FT_l	-	TRACECK, TIM3_ETR, TSC_G7_IO1, LCD_SEG38, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	B10	B10	2	2	B19	A1	A1	2	2	D2	D2	PE3	I/O	FT_l	-	TRACED0, TIM3_CH1, TSC_G7_IO2, LCD_SEG39, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	-	C8	E7	3	3	C18	B1	B1	3	3	D1	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	-	D8	E8	4	4	B21	C2	C2	4	4	E4	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	-	E7	D8	5	5	D19	D2	D2	5	5	E3	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, DCMI_D7, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3/WKUP3
1	1	C10	C10	6	6	C20	E2	E2	6	6	E2	E2	VBAT	S	-	-	-	-
2	2	C9	C9	7	7	D17	C1	C1	7	7	E1	E1	PC13	I/O	FT	(1) (2)	EVENTOUT	RTC_TAMP1/RTC_TS/RTC_OUT/WKUP2

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
3	3	D10	D10	8	8	D21	D1	D1	8	8	F1	F1	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	4	E10	D9	9	9	E20	E1	E1	9	9	G1	G1	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	D6	D6	10	10	F5	F5	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	-	-	-	-	-	D5	D5	11	11	F4	F4	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	-	-	-	-		D4	D4	12	12	F3	F3	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	-	E4	E4	13	13	G3	G3	PF3	I/O	FT_a	-	FMC_A3, EVENTOUT	ADC3_INP6, ADC3_INN5
-	-	-	-	-	-	-	F3	F3	14	14	G4	G4	PF4	I/O	FT_a	-	FMC_A4, EVENTOUT	ADC3_INP7, ADC3_INN6
-	-	-	-	-	-	-	F4	F4	15	15	G5	G5	PF5	I/O	FT_a	-	FMC_A5, EVENTOUT	ADC3_INP8, ADC3_INN7
-	-	D9	E10	10	10	-	F2	F2	16	16	F2	F2	VSS	S	-	-	-	-
-	-	E9	E9	11	11	F19	G2	G2	17	17	G2	G2	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	18	18	-	-	PF6	I/O	FT_a	-	TIM5_ETR, TIM5_CH1, QUADSPI_BK1_IO3, SAI1_SD_B, EVENTOUT	ADC3_INP9,ADC3_INN8

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	-	-	-	19	19	-	-	PF7	I/O	FT_a	-	TIM5_CH2, QUADSPI_BK1_IO2, SAI1_MCLK_B, EVENTOUT	ADC3_INP10, ADC3_INN9
-	-	-	-	-	-	-	-	-	20	20	-	-	PF8	I/O	FT_a	-	TIM5_CH3, QUADSPI_BK1_IO0, SAI1_SCK_B, EVENTOUT	ADC3_INP11, ADC3_INN10
-	-	-	-	-	-	-	-	-	21	21	-	-	PF9	I/O	FT_a	-	TIM5_CH4, QUADSPI_BK1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	ADC3_INP12, ADC3_INN11
-	-	-	-	-	-	-	-	-	22	22	H4	H4	PF10	I/O	FT_a	-	QUADSPI_CLK, DCMI_D11, TIM15_CH2, EVENTOUT	ADC3_INP13, ADC3_INN12
5	5	F10	F10	12	12	F21	F1	F1	23	23	H1	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	6	G10	F9	13	13	G20	G1	G1	24	24	J1	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	7	E8	F8	14	14	E16	H2	H2	25	25	H3	H3	NRST	I/O	RST	-	-	-
8	8	F9	G10	15	15	F17	H1	H1	26	26	J2	J2	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C4_SCL, I2C3_SCL, DFSDM1_DATIN4, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, EVENTOUT	ADC123_INP1

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
9	9	F8	F7	16	16	H21	J2	J2	27	27	J3	J3	PC1	I/O	FT_fla	-	TRACED0, LPTIM1_OUT, I2C4_SDA, SPI2_MOSI, I2C3_SDA, DFSDM1_CKIN4, LPUART1_TX, QUADSPI_BK2_IO0, LCD_SEG19, SAI1_SD_A, EVENTOUT	ADC123_INP2, ADC123_INN1
10	10	H10	G9	17	17	G18	J3	J3	28	28	J4	J4	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, QUADSPI_BK2_IO1, LCD_SEG20, EVENTOUT	ADC123_INP3, ADC123_INN2
11	11	F7	F6	18	18	H19	K2	K2	29	29	K1	K1	PC3	I/O	FT_la	-	LPTIM1_ETR, SPI2_MOSI, QUADSPI_BK2_IO2, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC123_INP4, ADC123_INN3
-	-	H9	-	19	19	J18	-	-	30	30	-	-	VSSA	S	-	-	-	-
-	-	G8	-	20	20	-	-	-	31	31	-	-	VREF-	S	-	-	-	-
12	12	-	H9	-	-	-	J1	J1	-	-	K2	K2	VSSA/VREF-	S	-	-	-	-
-	-	G7	H10	21	21	J20	L1	L1	32	32	L1	L1	VREF+	S	-	-	-	VREFBUF_OUT
-	-	J10	J10	22	22	K21	M1	M1	33	33	L2	L2	VDDA	S	-	-	-	-
13	13	-	-	-	-	-	-	-	-	-	-	-	VDDA/VREF+	-	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
14	14	G9	G8	23	23	H17	L2	L2	34	34	K3	K3	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINPP, ADC12_INP5, ADC12_INN4, RTC_TAMP2/WKUP1
-	-	-	-	-	-	-	M3	M3	-	-	M1	M1	OPAMP1_ VINM	I	TT	-	-	-
15	15	H8	G7	24	24	G16	M2	M2	35	35	N2	N2	PA1	I/O	FT_la	(3)	TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS_DE, UART4_RX, LCD_SEG0, TIM15_CH1N, EVENTOUT	OPAMP1_VINPM, ADC12_INP6, ADC12_INN5
16	16	H7	H8	25	25	F15	K3	K3	36	36	N1	N1	PA2	I/O	FT_la	-	TIM2_CH3, TIM5_CH3, USART2_TX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG1, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_INP7, ADC12_INN6, WKUP4/LSCO
17	17	J9	J9	26	26	L20	L3	L3	37	37	M2	M2	PA3	I/O	TT_la	-	TIM2_CH4, TIM5_CH4, USART2_RX, LPUART1_RX, QUADSPI_CLK, LCD_SEG2, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC12_INP8, ADC12_INN7
18	18	K10	K10	27	27	-	E3	E3	38	38	H2	H2	VSS	S	-	-	-	-
19	19	J8	J8	28	28	K17	H3	H3	39	39	G13	G13	VDD	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
20	20	F6	H7	29	29	L18	J4	J4	40	40	L3	L3	PA4	I/O	TT_a	-	SPI1_NSS, SPI3_NSS, USART2_CK, DCMI_HSYNC, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC12_INP9, ADC12_INN8, DAC1_OUT1
21	21	G6	J7	30	30	J16	K4	K4	41	41	K4	K4	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC12_INP10, DAC1_OUT2, ADC12_INN9
22	22	K9	K9	31	31	H15	L4	L4	42	42	M4	M4	PA6	I/O	FT_la	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK, SPI1_MISO, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT	OPAMP2_VINPP, ADC12_INP11, ADC12_INN10
-	-	-	-	-	-	-	M4	M4	-	-	N4	N4	OPAMP2_ VINM	I	TT	-	-	-
23	23	J7	G6	32	32	L16	J5	J5	43	43	L4	L4	PA7	I/O	FT_fla	(3)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, TIM17_CH1, EVENTOUT	OPAMP2_VINPM, ADC12_INP12, ADC12_INN11
24	24	H6	K8	33	33	K15	K5	K5	44	44	H5	H5	PC4	I/O	FT_la	-	USART3_TX, QUADSPI_BK2_IO3, LCD_SEG22, EVENTOUT	COMP1_INPM, ADC12_INP13, ADC12_INN12

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
25	-	K8	-	34	34	G14	L5	L5	45	45	J5	J5	PC5	I/O	FT_la	-	USART3_RX, LCD_SEG23, EVENTOUT	COMP1_INPP, ADC12_INP14, ADC12_INN13, WKUP5
26	25	J6	H6	35	35	J14	M5	M5	46	46	K5	K5	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, LCD_SEG5, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC12_INP15, ADC12_INN14
27	26	K7	K7	36	36	L14	M6	M6	47	47	L5	L5	PB1	I/O	FT_la	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INPM, ADC12_INP16, ADC12_INN15
28	27	F5	J6	37	37	H13	L6	L6	48	48	N5	N5	PB2	I/O	FT_la	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, LCD_VLCD, EVENTOUT	COMP1_INP
-	-	-	-	-	-	-	K6	K6	49	49	M5	M5	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	-	-	-	-	J7	J7	50	50	N6	N6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	-	-	-	-	K13	-	-	51	51	-	-	VSS	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	K1	-	-	52	52	A8	A8	VDD	S	-	-	-	-
-	-	-	-	-	-	-	K7	K7	53	53	M6	M6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, FMC_A7, EVENTOUT	-
-	-	-	-	-	-	-	J8	J8	54	54	L6	L6	PF14	I/O	FT_fa	-	I2C4_SCL, DFSDM1_CKIN6, TSC_G8_IO1, FMC_A8, EVENTOUT	-
-	-	-	-	-	-	-	J9	J9	55	55	K6	K6	PF15	I/O	FT_fa	-	I2C4_SDA, TSC_G8_IO2, FMC_A9, EVENTOUT	-
-	-	-	-	-	-	J12	H9	H9	56	56	J6	J6	PG0	I/O	FT	-	TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	-	-	-	-	G12	G9	G9	57	57	H6	H6	PG1	I/O	FT	-	TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	-	K6	K6	38	38	K11	M7	M7	58	58	L7	L7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	-	K5	K5	39	39	L10	L7	L7	59	59	K7	K7	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	-	J5	J5	40	40	H11	M8	M8	60	60	J7	J7	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	-	F6	F6	61	61	M7	M7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	G6	G6	62	62	N7	N7	VDD	S	-	-	-	-
-	-	H5	H5	41	41	K9	L8	L8	63	63	H7	H7	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	-	K4	K4	42	42	L8	M9	M9	64	64	N8	N8	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, QUADSPI_BK1_NCS, FMC_D8, EVENTOUT	-
-	-	G5	J4	43	43	J10	L9	L9	65	65	M8	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	-	G4	G5	44	44	H9	M10	M10	66	66	L8	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-
-	-	J4	G4	45	45	K7	M11	M11	67	67	K8	K8	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	H4	H4	46	46	L6	M12	M12	68	68	J8	J8	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-
29	28	K3	K3	47	47	J8	L10	L10	69	69	N9	N9	PB10	I/O	FT_fl	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
30	29	J3	J3	48	-	L4	L11	-	70	-	H8	H8	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
-	30	-	K1	-	48	-	-	L11	-	70	-	M10	VDD12	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	K9	K9	PH4	I/O	FT_f	-	I2C2_SCL, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	L9	L9	PH5	I/O	FT_f	-	I2C2_SDA, DCMI_PIXCLK, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	-	-	-	-	-	N10	N10	PH8	I/O	FT_f	-	I2C3_SDA, DCMI_HSYNC, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	M9	M9	PH10	I/O	FT	-	TIM5_CH1, DCMI_D1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	M10	-	PH11	I/O	FT	-	TIM5_CH2, DCMI_D2, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	M3	M3	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	N3	N3	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	M11	M11	VSS	S	-	-	-	-
31	31	K2	K2	49	49	-	F12	F12	71	71	L13	L13	VSS	S	-	-	-	-
32	32	K1	J2	50	50	-	G12	G12	72	72	L12	L12	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	N11	N11	VDD	S	-	-	-	-
33	33	J1	J1	51	51	K5	L12	L12	73	73	N12	N12	PB12	I/O	FT_l	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, DFSDM1_DATIN1, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, CAN2_RX, LCD_SEG12, SWPMI1_IO, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

| Pin number | | |

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	G2	G2	56	56	H7	K8	K8	78	78	L10	L10	PD9	I/O	FT_l	-	USART3_RX, DCMI_PIXCLK, LCD_SEG29, FMC_D14, SAI2_MCLK_A, EVENTOUT	-
-	-	G1	G1	57	57	H5	J12	J12	79	79	J13	J13	PD10	I/O	FT_l	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	-	58	58	-	J11	J11	80	80	K12	K12	PD11	I/O	FT_l	-	I2C4_SMBA, USART3_CTS, TSC_G6_IO2, LCD_SEG31, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	59	59	-	J10	J10	81	81	K11	K11	PD12	I/O	FT_fl	-	TIM4_CH1, I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	60	60	-	H12	H12	82	82	K13	K13	PD13	I/O	FT_fl	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, LCD_SEG33, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	-	-	-	-	83	83	H12	H12	VSS	S	-	-	-	-
-	-	F1	F1	-	-	-	-	-	84	84	H13	H13	VDD	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	G3	F3	61	61	H3	H11	H11	85	85	K10	K10	PD14	I/O	FT_l	-	TIM4_CH3, LCD_SEG34, FMC_D0, EVENTOUT	-
-	-	F4	F2	62	62	H1	H10	H10	86	86	H11	H11	PD15	I/O	FT_l	-	TIM4_CH4, LCD_SEG35, FMC_D1, EVENTOUT	-
-	-	-	-	-	-	G8	G10	G10	87	87	J12	J12	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	-	-	G6	F9	F9	88	88	J11	J11	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	-	-	-	-	G4	F10	F10	89	89	J10	J10	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	G2	E9	E9	90	90	J9	J9	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	-	-	-	-	G10	G4	G4	91	91	G11	G11	PG6	I/O	FT_s	-	I2C3_SMBA, LPUART1_RTS_DE, EVENTOUT	-
-	-	-	-	-	-	F7	H4	H4	92	92	H10	H10	PG7	I/O	FT_fs	-	I2C3_SCL, LPUART1_TX, FMC_INT, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	F5	J6	J6	93	93	H9	H9	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	-	F3	-	-	94	94	F13	F13	VSS	S	-	-	-	-
-	-	-	-	-	-	F1	-	-	95	95	F12	F12	VDDIO2	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
						Alternate functions	Additional functions
UFBGA169_SMPS	F11	PC6	I/O	FT_l	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, TSC_G4_IO1, DCMI_D0, LCD_SEG24, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
UFBGA169	F11						
LQFP144_SMPS	96						
LQFP144	96						
UFBGA132_SMPS	E12						
UFBGA132	E12						
WLCSP115_SMPS	F9						
LQFP100_SMPS	63						
LQFP100	63						
WLCSP100L_SMPS	F4						
WLCSP100L	F2						
LQFP64_SMPS	37						
LQFP64	37						
UFBGA169_SMPS	G12	PC7	I/O	FT_l	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, TSC_G4_IO2, DCMI_D1, LCD_SEG25, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
UFBGA169	G12						
LQFP144_SMPS	97						
LQFP144	97						
UFBGA132_SMPS	E11						
UFBGA132	E11						
WLCSP115_SMPS	E2						
LQFP100_SMPS	64						
LQFP100	64						
WLCSP100L_SMPS	E4						
WLCSP100L	F3						
LQFP64_SMPS	38						
LQFP64	38						
UFBGA169_SMPS	G10	PC8	I/O	FT_l	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, DCMI_D2, LCD_SEG26, SDMMC1_D0, EVENTOUT	-
UFBGA169	G10						
LQFP144_SMPS	98						
LQFP144	98						
UFBGA132_SMPS	E10						
UFBGA132	E10						
WLCSP115_SMPS	E4						
LQFP100_SMPS	65						
LQFP100	65						
WLCSP100L_SMPS	E1						
WLCSP100L	E1						
LQFP64_SMPS	39						
LQFP64	39						
UFBGA169_SMPS	G9	PC9	I/O	FT_fl	-	TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, LCD_SEG27, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT	-
UFBGA169	G9						
LQFP144_SMPS	99						
LQFP144	99						
UFBGA132_SMPS	D12						
UFBGA132	D12						
WLCSP115_SMPS	E6						
LQFP100_SMPS	66						
LQFP100	66						
WLCSP100L_SMPS	E2						
WLCSP100L	E2						
LQFP64_SMPS	40						
LQFP64	40						

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
41	41	E3	E3	67	67	D3	D11	D11	100	100	G8	G8	PA8	I/O	FT_l	-	MCO, TIM1_CH1, USART1_CK, OTG_FS_SOF, LCD_COM0, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
42	42	D3	D3	68	68	D1	D10	D10	101	101	F10	F10	PA9	I/O	FT_lu	-	TIM1_CH2, SPI2_SCK, DCMI_D0, USART1_TX, LCD_COM1, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
43	43	D2	D2	69	69	E8	C12	C12	102	102	F9	F9	PA10	I/O	FT_lu	-	TIM1_CH3, DCMI_D1, USART1_RX, OTG_FS_ID, LCD_COM2, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
44	44	D1	D1	70	70	C2	B12	B12	103	103	E13	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, CAN1_RX, OTG_FS_DM, TIM1_BKIN2_COMP1, EVENTOUT	-
45	45	C1	C1	71	71	B1	A12	A12	104	104	D13	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	46	C2	C2	72	72	D5	A11	A11	105	105	A11	A11	PA13 (JTMS/ SWDIO)	I/O	FT	(4)	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
47	47	B1	B1	-	-	B3	-	-	-	-	-	-	VSS	S	-	-	-	-
48	48	A1	A1	73	73	C4	C11	C11	106	106	E12	E12	VDDUSB	S	-	-	-	-
-	-	-	-	74	74	E18	F11	F11	107	107	C12	C12	VSS	S	-	-	-	-
-	-	-	-	75	75	A2	G11	G11	108	108	C13	C13	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	E11	E11	PH6	I/O	FT	-	I2C2_SMBA, DCMI_D8, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	D12	D12	PH7	I/O	FT_f	-	I2C3_SCL, DCMI_D9, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	D11	D11	PH9	I/O	FT	-	I2C3_SMBA, DCMI_D0, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	B13	B13	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	A13	A13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	B12	B12	PH15	I/O	FT	-	TIM8_CH3N, DCMI_D11, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	A12	A12	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS, DCMI_D13, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	C11	C11	PI8	I/O	FT	-	DCMI_D12, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	B11	B11	PI1	I/O	FT	-	SPI2_SCK, DCMI_D8, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	-	-	-	-	-	B10	B10	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, DCMI_D9, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	C10	C10	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI, DCMI_D10, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	D10	D10	PI4	I/O	FT	-	TIM8_BKIN, DCMI_D5, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	E10	E10	PI5	I/O	FT	-	TIM8_CH1, DCMI_VSYNC, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	C9	C9	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	B9	B9	PI6	I/O	FT	-	TIM8_CH2, DCMI_D6, EVENTOUT	-
49	49	B2	B2	76	76	D7	A10	A10	109	109	A10	A10	PA14 (JTCK/ SWCLK)	I/O	FT	(4)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, OTG_FS_SOF, SWPMI1_RX, SAI1_FS_B, EVENTOUT	-
50	50	A2	A2	77	77	C6	A9	A9	110	110	A9	A9	PA15 (JTDI)	I/O	FT_l	(4)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS_DE, UART4_RTS_DE, TSC_G3_IO1, LCD_SEG17, SWPMI1_SUSPEND, SAI2_FS_B, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
51	51	D4	C3	78	78	B5	B11	B11	111	111	D9	D9	PC10	I/O	FT_l	-	TRACED1, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, DCMI_D8, LCD_COM4/LCD_SEG28/ LCD_SEG40, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-
52	52	C3	D4	79	79	A4	C10	C10	112	112	E9	E9	PC11	I/O	FT_l	-	QUADSPI_BK2_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, DCMI_D4, LCD_COM5/LCD_SEG29/ LCD_SEG41, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
53	53	C4	C4	80	80	D9	B10	B10	113	113	F8	F8	PC12	I/O	FT_l	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9, LCD_COM6/LCD_SEG30/ LCD_SEG42, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	-	B3	B3	81	81	C8	C9	C9	114	114	B8	B8	PD0	I/O	FT	-	SPI2_NSS, DFSDM1_DATIN7, CAN1_RX, FMC_D2, EVENTOUT	-
-	-	A3	A3	82	82	B7	B9	B9	115	115	C8	C8	PD1	I/O	FT	-	SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, FMC_D3, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
54	-	E4	D5	83	83	A6	C8	C8	116	116	D8	D8	PD2	I/O	FT_l	-	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11, LCD_COM7/LCD_SEG31/ LCD_SEG43, SDMMC1_CMD, EVENTOUT	-
-	-	-	-	84	84	-	B8	B8	117	117	E8	E8	PD3	I/O	FT	-	SPI2_SCK, DCMI_D5, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS, QUADSPI_BK2_NCS, FMC_CLK, EVENTOUT	-
-	-	B4	C5	85	85	E10	B7	B7	118	118	C7	C7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, QUADSPI_BK2_IO0, FMC_NOE, EVENTOUT	-
-	-	E5	B4	86	86	C10	A6	A6	119	119	D7	D7	PD5	I/O	FT	-	USART2_TX, QUADSPI_BK2_IO1, FMC_NWE, EVENTOUT	-
-	-	-	-	-	-	A18	-	-	120	120	-	-	VSS	S	-	-	-	-
-	-	A4	A4	-	-	A8	-	-	121	121	-	-	VDD	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	D5	B5	87	87	F11	B6	B6	122	122	E7	E7	PD6	I/O	FT	-	DCMI_D10, QUADSPI_BK2_IO1, DFSDM1_DATIN1, USART2_RX, QUADSPI_BK2_IO2, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	-	C5	C6	88	88	D11	A5	A5	123	123	F7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, QUADSPI_BK2_IO3, FMC_NE1, EVENTOUT	-
-	-	B5	D6	-	-	E12	D9	D9	124	124	B7	B7	PG9	I/O	FT_s	-	SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	-	A5	A5	-	-	A10	D8	D8	125	125	D6	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	-	D6	E5	-	-	B11	G3	G3	126	126	E6	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, SPI3_MOSI, USART1_CTS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	-	B6	B6	-	-	C12	D7	D7	127	127	F6	F6	PG12	I/O	FT_s	-	LPTIM1_ETR, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	-	-	-	-	-	D13	C7	C7	128	128	G7	G7	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, FMC_A24, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	A12	C6	-	129	129	G6	G6	PG14	I/O	FT_fs	-	I2C1_SCL, FMC_A25, EVENTOUT	-
-	-	-	-	-	-	B9	F7	F7	130	130	A7	A7	VSS	S	-	-	-	-
-	-	A6	A6	-	-	B13	G7	G7	131	131	B6	B6	VDDIO2	S	-	-	-	-
-	-	-	-	-	-	-	K1	K1	132	-	C6	-	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, DCMI_D13, EVENTOUT	-
55	54	C6	F5	89	89	F13	A8	A8	133	132	A6	A6	PB3 (JTDO/TRACESWO)	I/O	FT_la	(4)	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS_DE, OTG_FS_CRS_SYNC, LCD_SEG7, SAI1_SCK_B, EVENTOUT	COMP2_INM
56	55	C7	E6	90	90	C14	A7	A7	134	133	A5	A5	PB4 (NJTRST)	I/O	FT_fla	(4)	NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS, UART5_RTS_DE, TSC_G2_IO1, DCMI_D12, LCD_SEG8, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
57	56	B7	C7	91	91	A14	C5	C5	135	134	B5	B5	PB5	I/O	FT_la	-	LPTIM1_IN1, TIM3_CH2, CAN2_RX, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS, TSC_G2_IO2, DCMI_D10, LCD_SEG9, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	-
58	57	A7	A7	92	92	E14	B5	B5	136	135	C5	C5	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, I2C4_SCL, DFSDM1_DATIN5, USART1_TX, CAN2_TX, TSC_G2_IO3, DCMI_D5, TIM8_BKIN2_COMP2, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP
59	58	D7	B7	93	93	B15	B4	B4	137	136	D5	D5	PB7	I/O	FT_fla	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, I2C4_SDA, DFSDM1_CKIN5, USART1_RX, UART4_CTS, TSC_G2_IO4, DCMI_VSYNC, LCD_SEG21, FMC_NL, TIM8_BKIN_COMP1, TIM17_CH1N, EVENTOUT	COMP2_INM, PVD_IN
60	59	E6	D7	94	94	D15	A4	A4	138	137	E5	E5	PH3-BOOT0	I/O	FT	-	EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin number												Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
61	60	B8	B8	95	95	-	A3	A3	139	138	C4	C4	PB8	I/O	FT_fl	-	TIM4_CH3, I2C1_SCL, DFSDM1_DATIN6, CAN1_RX, DCMI_D6, LCD_SEG16, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
62	61	A8	A8	96	96	A16	B3	B3	140	139	D4	D4	PB9	I/O	FT_fl	-	IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM1_CKIN6, CAN1_TX, DCMI_D7, LCD_COM3, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	62	-	-	-	-	B17	-	C6	-	-	-	C6	VDD12	S	-	-	-	-
-	-	-	-	97	97	-	C3	C3	141	140	A4	A4	PE0	I/O	FT_l	-	TIM4_ETR, DCMI_D2, LCD_SEG36, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	-	-	-	98	-	-	A2	A2	142	141	B4	B4	PE1	I/O	FT_l	-	DCMI_D3, LCD_SEG37, FMC_NBL1, TIM17_CH1, EVENTOUT	-
-	-	-	A9	-	98	L2	-	-	-	142	-	-	VDD12	S	-	-	-	-
63	63	A9	B9	99	99	K19	D3	D3	143	143	B3	B3	VSS	S	-	-	-	-
64	64	A10	A10	100	100	L12	C4	C4	144	144	A3	A3	VDD	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin number													Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP64_SMPS	WLCSP100L	WLCSP100L_SMPS	LQFP100	LQFP100_SMPS	WLCSP115_SMPS	UFBGA132	UFBGA132_SMPS	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	-	K3	-	-	-	-	C2	C2	VSS	S	-	-	-	-
-	-	-	-	-	-	A20	-	-	-	-	C1	C1	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	A2	A2	PH2	I/O	FT	-	QUADSPI_BK2_IO0, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	B2	B2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	B1	B1	PI9	I/O	FT	-	CAN1_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	A1	A1	PI10	I/O	FT	-	EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current(3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0351 reference manual.
3. OPAMPx_VINM pins are not available as additional functions on pins PA1 and PA7 on UFBGA packages. On UFBGA packages, use the OPAMPx_VINM dedicated pins available on M3 and M4 balls.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCLK	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	-	DCMI_D0	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	-	DCMI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_ DATIN0	USART3_RTS_ DE
	PB2	RTC_OUT	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_ DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS
	PB5	-	LPTIM1_IN1	TIM3_CH2	CAN2_RX	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	DFSDM1_ DATIN5	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	DFSDM1_CKIN5	USART1_RX
	PB8	-	-	TIM4_CH3	-	I2C1_SCL	-	DFSDM1_ DATIN6	-
	PB9	-	IR_OUT	TIM4_CH4	-	I2C1_SDA	SPI2_NSS	DFSDM1_CKIN6	-
	PB10	-	TIM2_CH3	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	DFSDM1_ DATIN7	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	DFSDM1_CKIN7	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN_ COMP2	I2C2_SMBA	SPI2_NSS	DFSDM1_ DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	-	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_ DATIN2	USART3_RTS_ DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	I2C4_SCL	-	I2C3_SCL	-	DFSDM1_ DATIN4	-
	PC1	TRACED0	LPTIM1_OUT	I2C4_SDA	SPI2_MOSI	I2C3_SDA	-	DFSDM1_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_ CKOUT	-
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	-	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_ DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	-	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3	-	I2C3_SDA	-
	PC10	TRACED1	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	-	QUADSPI_ BK2_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port D	PD0	-	-	-	-	-	SPI2_NSS	DFSDM1_ DATIN7	-
	PD1	-	-	-	-	-	SPI2_SCK	DFSDM1_CKIN7	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS_ DE
	PD3	-	-	-	SPI2_SCK	DCMI_D5	SPI2_MISO	DFSDM1_ DATIN0	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM1_CKIN0	USART2_RTS_ DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	-	DCMI_D10	QUADSPI_ BK2_IO1	DFSDM1_ DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM1_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-	-	USART3_RTS_ DE
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM1_ DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_ DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM1_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM1_ DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM1_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	QUADSPI_CLK	-	-	-	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_ DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	-	-	-
	PG7	-	-	-	-	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_ DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH2	-	-	-	QUADSPI_ BK2_IO0	-	-	-	-
	PH3	-	-	-	-	-	-	-	-
	PH4	-	-	-	-	I2C2_SCL	-	-	-
	PH5	-	-	-	-	I2C2_SDA	-	-	-
	PH6	-	-	-	-	I2C2_SMBA	-	-	-
	PH7	-	-	-	-	I2C3_SCL	-	-	-
	PH8	-	-	-	-	I2C3_SDA	-	-	-
	PH9	-	-	-	-	I2C3_SMBA	-	-	-
	PH10	-	-	TIM5_CH1	-	-	-	-	-
	PH11	-	-	TIM5_CH2	-	-	-	-	-
	PH12	-	-	TIM5_CH3	-	-	-	-	-
	PH13	-	-	-	TIM8_CH1N	-	-	-	-
	PH14	-	-	-	TIM8_CH2N	-	-	-	-
	PH15	-	-	-	TIM8_CH3N	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS	-	-
	PI1	-	-	-	-	-	SPI2_SCK	-	-
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI	-	-
	PI4	-	-	-	TIM8_BKIN	-	-	-	-
	PI5	-	-	-	TIM8_CH1	-	-	-	-
	PI6	-	-	-	TIM8_CH2	-	-	-	-
	PI7	-	-	-	TIM8_CH3	-	-	-	-
	PI8	-	-	-	-	-	-	-	-
	PI9	-	-	-	-	-	-	-	-
	PI10	-	-	-	-	-	-	-	-
	PI11	-	-	-	-	-	-	-	-

1. Refer to *Table 17* for AF8 to AF15.

Table 17. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	LCD_SEG0	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG1	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG2	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	DCMI_HSYNC	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_ CTS	-	QUADSPI_BK1_IO3	LCD_SEG3	TIM1_BKIN_ COMP2	TIM8_BKIN_C OMP2	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_BK1_IO2	LCD_SEG4	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	LCD_COM0	SWPMI1_IO	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	LCD_COM1	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	LCD_COM2	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	OTG_FS_DM	-	TIM1_BKIN2_ COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	SWPMI1_TX	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	OTG_FS_SOF	-	SWPMI1_RX	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_ DE	TSC_G3_IO1	-	LCD_SEG17	SWPMI1_ SUSPEND	SAI2_FS_B	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port B	PB0	-	-	QUADSPI_BK1_IO1	LCD_SEG5	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_ RTS_DE	-	QUADSPI_BK1_IO0	LCD_SEG6	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	-	LCD_VLCD	-	-	-	EVENTOUT
	PB3	-	-	OTG_FS_CRS_SYNC	LCD_SEG7	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_ RTS_DE	TSC_G2_IO1	DCMI_D12	LCD_SEG8	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS	TSC_G2_IO2	DCMI_D10	LCD_SEG9	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	CAN2_TX	TSC_G2_IO3	DCMI_D5	-	TIM8_BKIN2_ COMP2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS	TSC_G2_IO4	DCMI_VSYNC	LCD_SEG21	FMC_NL	TIM8_BKIN_C OMP1	TIM17_CH1N	EVENTOUT
	PB8	-	CAN1_RX	DCMI_D6	LCD_SEG16	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	-	CAN1_TX	DCMI_D7	LCD_COM3	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	QUADSPI_CLK	LCD_SEG10	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG11	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_ RTS_DE	TSC_G1_IO1	CAN2_RX	LCD_SEG12	SWPMI1_IO	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_ CTS	TSC_G1_IO2	CAN2_TX	LCD_SEG13	SWPMI1_TX	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	LCD_SEG14	SWPMI1_RX	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	TSC_G1_IO4	-	LCD_SEG15	SWPMI1_ SUSPEND	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port C	PC0	LPUART1_RX	-	-	LCD_SEG18	-	-	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	QUADSPI_BK2_IO0	LCD_SEG19	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	QUADSPI_BK2_IO1	LCD_SEG20	-	-	-	EVENTOUT
	PC3	-	-	QUADSPI_BK2_IO2	LCD_VLCD	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	QUADSPI_BK2_IO3	LCD_SEG22	-	-	-	EVENTOUT
	PC5	-	-	-	LCD_SEG23	-	-	-	EVENTOUT
	PC6	-	TSC_G4_IO1	DCMI_D0	LCD_SEG24	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	-	TSC_G4_IO2	DCMI_D1	LCD_SEG25	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	DCMI_D2	LCD_SEG26	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	OTG_FS_NOE	LCD_SEG27	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2_ COMP1	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	DCMI_D8	LCD_COM4/ LCD_SEG28/ LCD_SEG40	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	DCMI_D4	LCD_COM5/ LCD_SEG29/ LCD_SEG41	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	DCMI_D9	LCD_COM6/ LCD_SEG30/ LCD_SEG42	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port D	PD0	-	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	DCMI_D11	LCD_COM7/ LCD_SEG31/ LCD_SEG43	SDMMC1_ CMD	-	-	EVENTOUT
	PD3	-	-	QUADSPI_BK2_NCS	-	FMC_CLK	-	-	EVENTOUT
	PD4	-	-	QUADSPI_BK2_IO0	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	QUADSPI_BK2_IO1	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	QUADSPI_BK2_IO2	-	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	QUADSPI_BK2_IO3	-	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	DCMI_HSYNC	LCD_SEG28	FMC_D13	-	-	EVENTOUT
	PD9	-	-	DCMI_PIXCLK	LCD_SEG29	FMC_D14	SAI2_MCLK_A	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	LCD_SEG30	FMC_D15	SAI2_SCK_A	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	LCD_SEG31	FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	LCD_SEG32	FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	LCD_SEG33	FMC_A18	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	LCD_SEG34	FMC_D0	-	-	EVENTOUT
	PD15	-	-	-	LCD_SEG35	FMC_D1	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port E	PE0	-	-	DCMI_D2	LCD_SEG36	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	DCMI_D3	LCD_SEG37	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	LCD_SEG38	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	LCD_SEG39	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	DCMI_D4	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	DCMI_D6	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	DCMI_D7	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	QUADSPI_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	QUADSPI_BK1_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	QUADSPI_BK1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	QUADSPI_BK1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	QUADSPI_BK1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	QUADSPI_BK1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	QUADSPI_BK1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	QUADSPI_BK1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	QUADSPI_BK1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	QUADSPI_BK1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	DCMI_D11	-	-	-	TIM15_CH2	EVENTOUT
	PF11	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_ CTS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_ RTS_DE	-	-	-	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	-	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE/ FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	-	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	FMC_A25	-	-	EVENTOUT
	PG15	-	-	DCMI_D13	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	-	-	-	-	-	EVENTOUT
	PH5	-	-	DCMI_PIXCLK	-	-	-	-	EVENTOUT
	PH6	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PH7	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PH8	-	-	DCMI_HSYNC	-	-	-	-	EVENTOUT
	PH9	-	-	DCMI_D0	-	-	-	-	EVENTOUT
	PH10	-	-	DCMI_D1	-	-	-	-	EVENTOUT
	PH11	-	-	DCMI_D2	-	-	-	-	EVENTOUT
	PH12	-	-	DCMI_D3	-	-	-	-	EVENTOUT
	PH13	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PH14	-	-	DCMI_D4	-	-	-	-	EVENTOUT
	PH15	-	-	DCMI_D11	-	-	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/ FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENTOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

1. Refer to *Table 16* for AF0 to AF7.

5 Memory mapping

Figure 20. STM32L496xx memory map

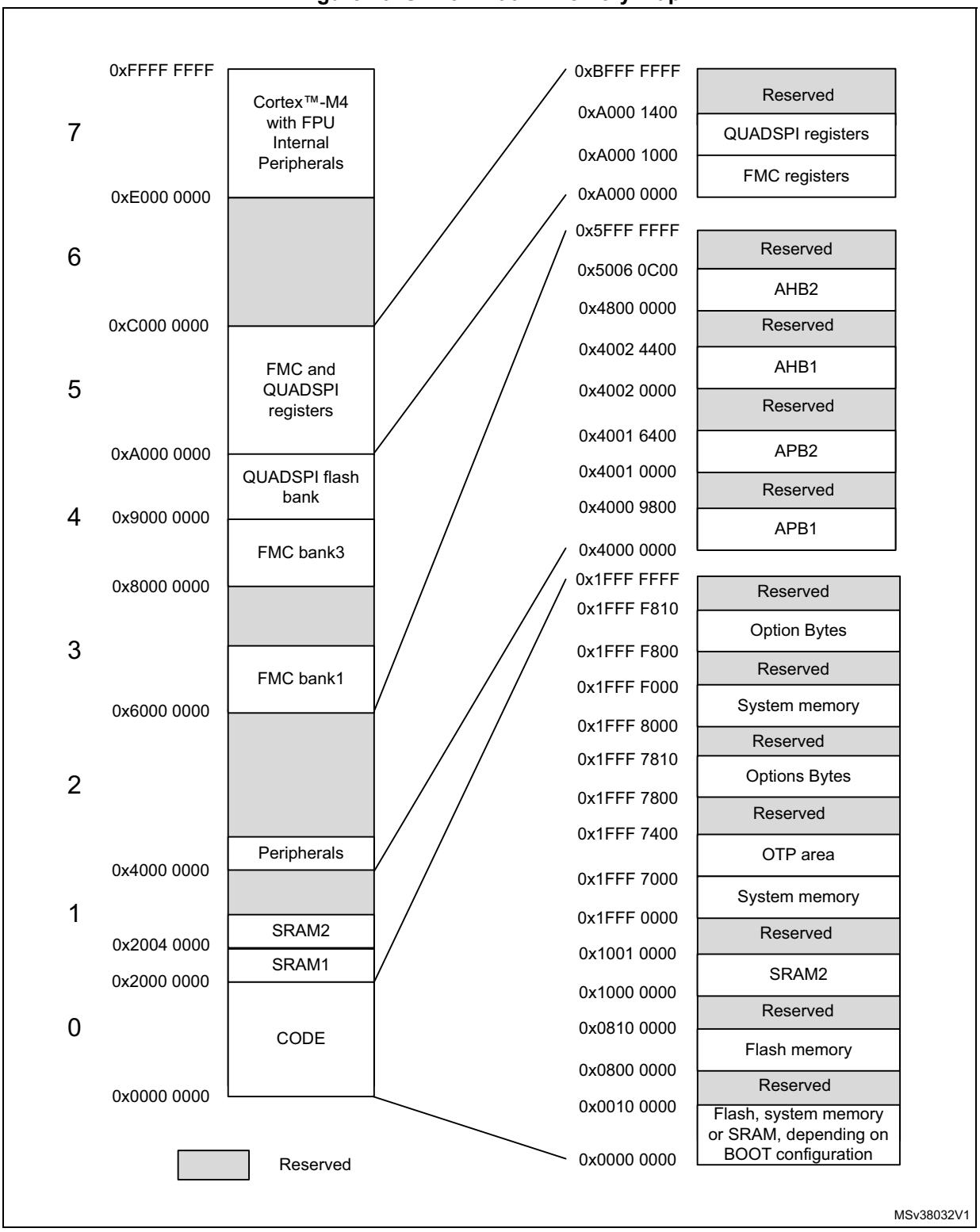


Table 18. STM32L496xx memory map and peripheral register boundary addresses(1)

Bus	Boundary address	Size (bytes)	Peripheral
AHB4	0xA000 1000 - 0xA000 13FF	1 K	QUADSPI
AHB3	0xA000 0400 - 0xA000 0FFF	3 K	Reserved
	0xA000 0000 - 0xA000 03FF	1 K	FMC
-	0x5006 0C00 - 0x5FFF FFFF	~260 M	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	1 K	RNG
	0x5006 0400 - 0x5006 07FF	1 K	HASH
	0x5005 0400 - 0x5006 03FF	63 K	Reserved
	0x5005 0000 - 0x5005 03FF	1 K	DCMI
	0x5004 0400 - 0x5004 FFFF	62 K	Reserved
	0x5004 0000 - 0x5004 03FF	1 K	ADC
	0x5000 0000 - 0x5003 FFFF	16 K	OTG_FS
	0x4800 2400 - 0x4FFF FFFF	~127 M	Reserved
	0x4800 2000 - 0x4800 23FF	1 K	GPIOI
	0x4800 1C00 - 0x4800 1FFF	1 K	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 K	GPIOG
	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
-	0x4002 BC00 - 0x47FF FFFF	~127 M	Reserved

Table 18. STM32L496xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
AHB1	0x4002 B000 - 0x4002 BBFF	3 K	DMA2D
	0x4002 4400 - 0x4002 AFFF	26 K	Reserved
	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	1 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1

Table 18. STM32L496xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 6400 - 0x4001 FFFF	39 K	Reserved
	0x4001 6000 - 0x4001 63FF	1 K	DFSDM1
	0x4001 5C00 - 0x4001 5FFF	1 K	Reserved
	0x4001 5800 - 0x4001 5BFF	1 K	SAI2
	0x4001 5400 - 0x4001 57FF	1 K	SAI1
	0x4001 4C00 - 0x4001 53FF	2 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	Reserved
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 2800 - 0x4001 2BFF	1 K	SDMMC1
	0x4001 2000 - 0x4001 27FF	2 K	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 K	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0200 - 0x4001 03FF	1 K	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG

Table 18. STM32L496xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 K	Reserved
	0x4000 9400 - 0x4000 97FF	1 K	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 K	Reserved
	0x4000 8800 - 0x4000 8BFF	1 K	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 K	I2C4
	0x4000 8000 - 0x4000 83FF	1 K	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 K	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 K	OPAMP
	0x4000 7400 - 0x4000 77FF	1 K	DAC1
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	1 K	Reserved
	0x4000 6800 - 0x4000 6BFF	1 K	CAN2
	0x4000 6400 - 0x4000 67FF	1 K	CAN1
	0x4000 6000 - 0x4000 63FF	1 K	CRS
	0x4000 5C00- 0x4000 5FFF	1 K	I2C3
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4

Table 18. STM32L496xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2
	0x4000 3400 - 0x4000 37FF	1 K	Reserved
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 2400 - 0x4000 27FF	1 K	LCD
	0x4000 1800 - 0x4000 23FF	3 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00- 0x4000 0FFF	1 K	TIM5
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

1. The gray color is used for reserved boundary addresses.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 21*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 22*.

Figure 21. Pin loading conditions

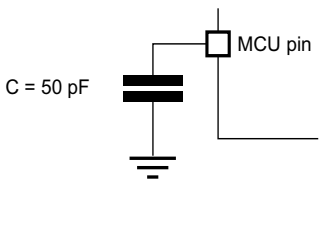
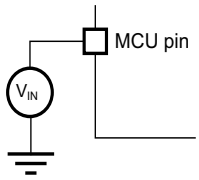
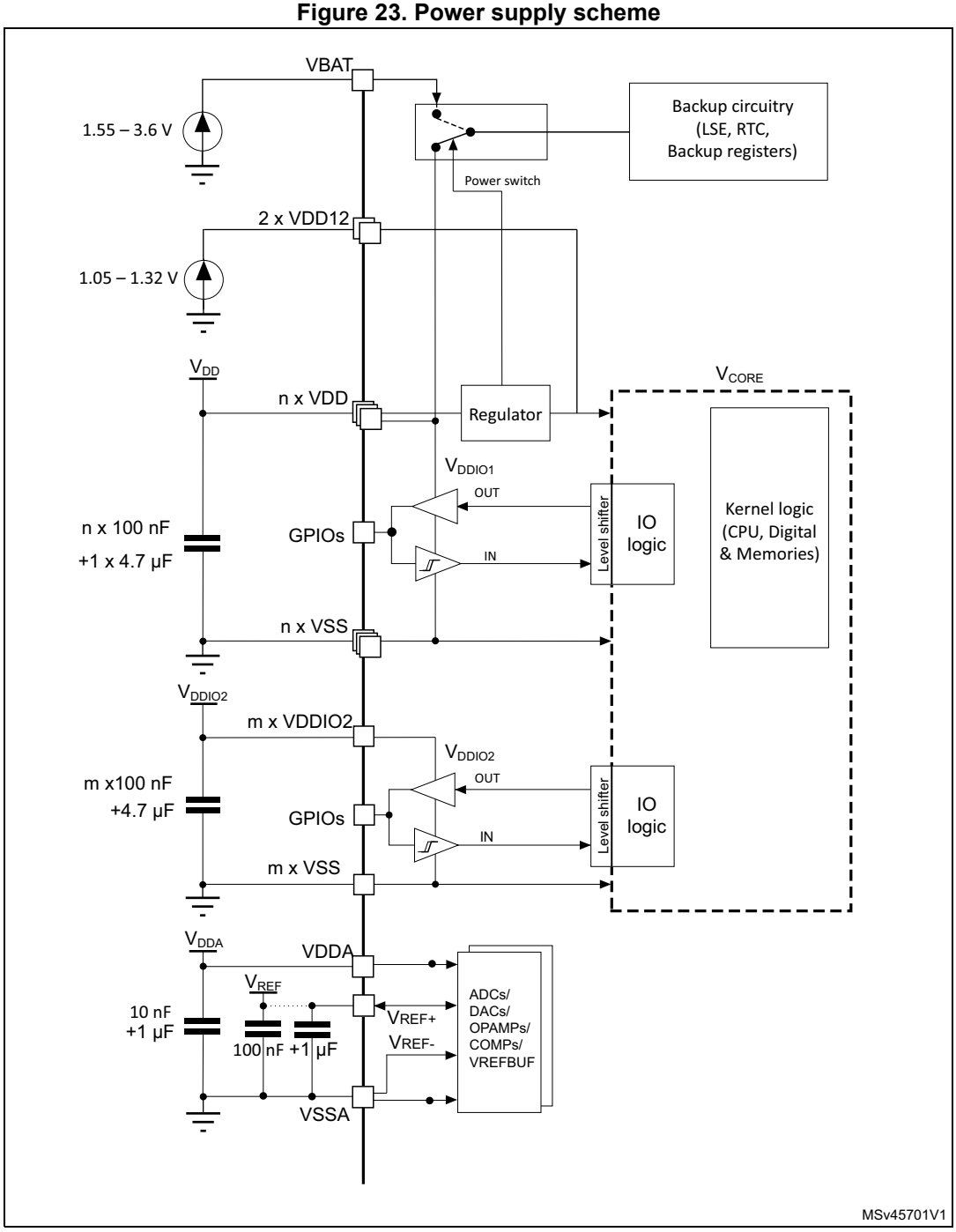


Figure 22. Pin input voltage



6.1.6 Power supply scheme

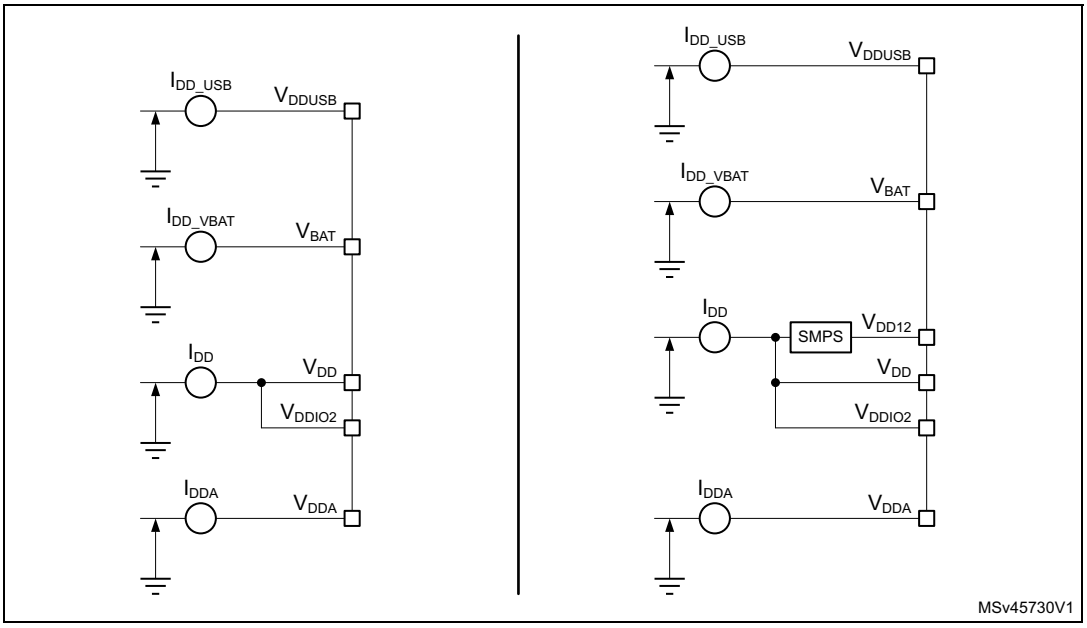
Figure 23. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 24. Current consumption measurement scheme with and without external SMPS power supply



The I_{DD_ALL} parameters given in *Table 26* to *Table 48* represent the total MCU consumption including the current supplying V_{DD}, V_{DDIO2}, V_{DDA}, V_{DDUSB} and V_{BAT}.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19*, *Table 20* and *Table 21* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 19. Voltage characteristics(1)

Symbol	Ratings		Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}, V_{REF+})		-0.3	4.0	V
V_{DD12} - V_{SS}	External SMPS supply voltage	Range 1	-0.3	1.4	
		Range 2	-0.3		
V_{IN}(2)	Input voltage on FT_xxx pins		V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) + 4.0(3)(4)	
	Input voltage on TT_xx pins		V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin		V_{SS}	9.0	
	Input voltage on any other pins		V_{SS}-0.3	4.0	

Table 19. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)	-	50	mV
$V_{DDX}-V_{SS}$	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT}, V_{REF+})	-0.3	4.0	V
$V_{REF+} - V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 20. Current characteristics

Symbol	Ratings	Max	Unit
$\sum I_{VDD}$	Total current into sum of all V_{DD} power lines (source)(1) (2)	150	mA
$\sum I_{VSS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)(2)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(3)	100	
	Total output current sourced by sum of all I/Os and control pins(3)	100	
$I_{INJ(PIN)}$(4)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(5)	
	Injected current on PA4, PA5	-5/0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(6)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. Valid also for V_{DD12} on SMPS package
3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DD12}	Standard operating voltage	Full frequency range	1.08	1.32	
		Up to 26 MHz	1.05		
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	
V_{DDUSB}	USB supply voltage	USB used	3.0	3.6	
		USB not used	0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O	-0.3	V_{DDIOx}+0.3(2)	
		BOOT0	0	9	
		All I/O except BOOT0 and TT_xx	-0.3	Min(Min(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V, 5.5 V)(3)(4)	

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6(5)	LQFP144	-	-	625	mW
		LQFP100	-	-	476	
		LQFP64	-	-	444	
		UFBGA169		-	385	
		UFBGA132	-	-	364	
		WLCSP100L	-	-	559	
P_D	Power dissipation at T_A = 125 °C for suffix 3(5)	LQFP144	-	-	156	mW
		LQFP100	-	-	119	
		LQFP64	-	-	111	
		UFBGA169		-	96	
		UFBGA132	-	-	91	
		WLCSP100L	-	-	140	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(6)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(6)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	105	°C
		Suffix 3 version		–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. A GPIO with analog input function enabled cannot exceed min(V_{DDA}, V_{REF+}) + 0.3 V.
3. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between Min(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V and 5.5V.
4. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
5. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.9: Thermal characteristics*).
6. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.9: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	

Table 23. Operating conditions at power-up / power-down(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	µs/V
	V_{DDUSB} fall time rate		10	∞	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	0	∞	µs/V
	V_{DDIO2} fall time rate		10	∞	

1. At Power up, the V_{DD12} voltage should not be forced externally

The requirements for power-up/down sequence specified in *Section 3.10.1: Power supply schemes* must be respected.

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	

Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

6.3.4 Embedded voltage reference

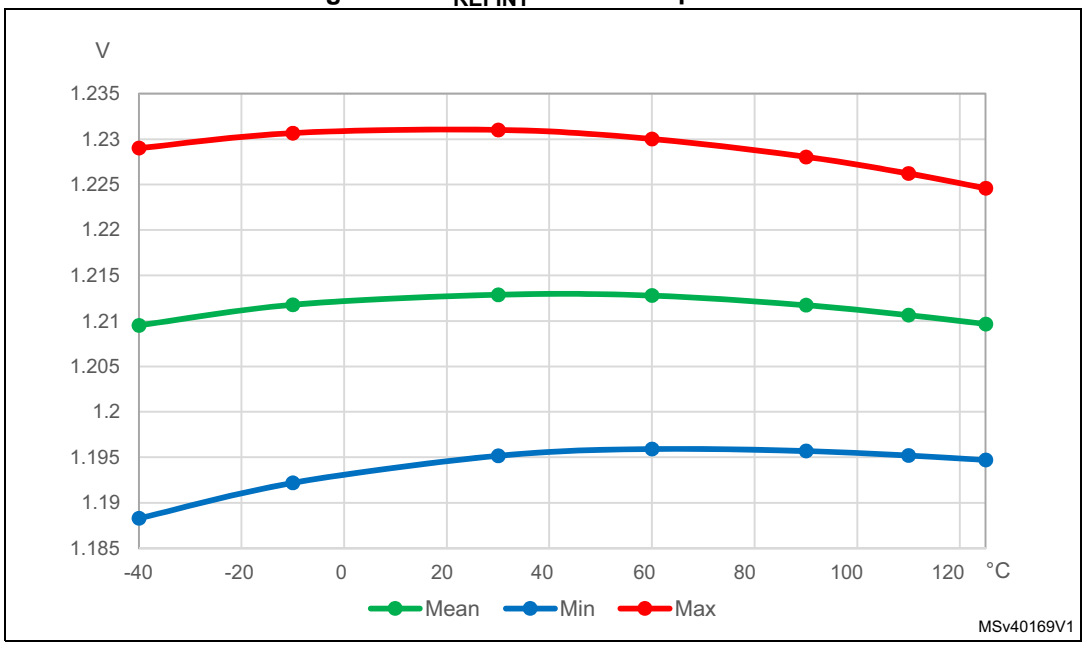
The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 25. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 25. V_{REFINT} versus temperature



6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 24*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0351 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 26* to *Table 49* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.65	2.69	2.82	3.05	3.51	2.9	3.0	3.3	3.8	4.7	mA
				16 MHz	1.68	1.72	1.85	2.07	2.53	1.9	2.0	2.2	2.7	3.7	
				8 MHz	0.91	0.94	1.07	1.29	1.74	1.0	1.1	1.4	1.8	2.8	
				4 MHz	0.52	0.55	0.68	0.9	1.35	0.6	0.7	0.9	1.4	2.4	
				2 MHz	0.33	0.36	0.48	0.7	1.15	0.4	0.5	0.7	1.2	2.2	
				1 MHz	0.23	0.26	0.38	0.6	1.06	0.3	0.4	0.6	1.1	2.0	
				100 kHz	0.14	0.17	0.3	0.52	0.97	0.2	0.3	0.5	1.0	2.0	
			Range 1	80 MHz	9.44	9.5	9.67	9.93	10.4	10.3	10.4	10.7	11.3	12.4	
				72 MHz	8.52	8.59	8.75	9.01	9.53	9.3	9.4	9.7	10.3	11.4	
				64 MHz	7.61	7.67	7.83	8.09	8.61	8.3	8.4	8.7	9.3	10.4	
				48 MHz	5.72	5.78	5.94	6.2	6.72	6.3	6.4	6.7	7.3	8.4	
				32 MHz	3.87	3.92	4.07	4.33	4.84	4.2	4.4	4.7	5.2	6.3	
				24 MHz	2.94	2.99	3.14	3.39	3.9	3.2	3.4	3.6	4.2	5.3	
				16 MHz	2.01	2.06	2.2	2.45	2.95	2.2	2.3	2.6	3.2	4.2	
I_{DD_ALL} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	274	307	444	678	1150	318	425	656	1167	2197	µA
				1 MHz	158	195	328	564	1040	195	309	558	1047	2084	
				400 kHz	88.2	123	256	490	969	116	232	485	973	2012	
				100 kHz	63	90.6	223	457	934	79	195	447	942	1975	

1. Guaranteed by characterization results, unless otherwise specified.

Table 27. Current consumption in Run modes, code with data processing running from flash, (ART enable Cache ON Prefetch OFF) and power supplied (by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	80 MHz	3.39	3.42	3.48	3.57	3.74	mA
			72 MHz	3.06	3.09	3.15	3.24	3.43	
			64 MHz	2.74	2.76	2.81	2.91	3.10	
			48 MHz	2.06	2.08	2.14	2.23	2.42	
			32 MHz	1.39	1.41	1.46	1.56	1.74	
			24 MHz	1.06	1.07	1.13	1.22	1.40	
			16 MHz	0.72	0.74	0.79	0.88	1.06	
			8 MHz	0.39	0.41	0.46	0.56	0.75	
			4 MHz	0.22	0.24	0.29	0.39	0.58	
			2 MHz	0.14	0.16	0.21	0.30	0.50	
			1 MHz	0.10	0.11	0.16	0.26	0.46	
			100 kHz	0.06	0.07	0.13	0.22	0.42	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 28. Current consumption in Run and Low-power run modes, code with data processing running from flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.1	3.14	3.28	3.51	3.98	3.5	3.6	3.8	4.3	5.3	mA
				16 MHz	2.19	2.23	2.36	2.59	3.05	2.5	2.6	2.8	3.3	4.3	
				8 MHz	1.22	1.26	1.39	1.61	2.07	1.4	1.5	1.7	2.2	3.2	
				4 MHz	0.69	0.73	0.85	1.08	1.53	0.8	0.9	1.1	1.6	2.6	
				2 MHz	0.41	0.44	0.57	0.79	1.24	0.5	0.6	0.8	1.3	2.3	
				1 MHz	0.27	0.3	0.43	0.65	1.1	0.3	0.4	0.6	1.1	2.1	
				100 kHz	0.14	0.18	0.3	0.52	0.97	0.2	0.3	0.5	1.0	2.0	
			Range 1	80 MHz	10	10.1	10.3	10.5	11.1	11.1	11.2	11.6	12.2	13.31	
				72 MHz	9.02	9.1	9.29	9.59	10.1	10	10.1	10.5	11.0	12.2	
				64 MHz	8.94	9.02	9.2	9.48	10	9.9	10.1	10.4	11.0	12.1	
				48 MHz	7.51	7.59	7.77	8.05	8.59	8.4	8.6	8.9	9.5	10.6	
				32 MHz	5.38	5.45	5.62	5.88	6.41	6.0	6.2	6.5	7.0	8.2	
				24 MHz	4.07	4.12	4.28	4.54	5.06	4.5	4.7	5.0	5.5	6.6	
				16 MHz	2.86	2.92	3.07	3.33	3.84	3.2	3.3	3.6	4.2	5.3	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	378	412	549	782	1260	436	538	761	1287	2317	µA
				1 MHz	213	246	381	618	1100	255	367	609.	1105	2138	
				400 kHz	101	144	277	514	989	141	256	507	995	2033	
				100 kHz	62	95.8	228	463	939	85	201	454	947	1982	

1. Guaranteed by characterization results, unless otherwise specified.

Table 29. Current consumption in Run modes, code with data processing running from flash, ART disable and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	80 MHz	3.59	3.63	3.70	3.77	3.99	mA
			72 MHz	3.24	3.27	3.34	3.45	3.63	
			64 MHz	3.21	3.24	3.31	3.41	3.59	
			48 MHz	2.70	2.73	2.79	2.89	3.09	
			32 MHz	1.93	1.96	2.02	2.11	2.30	
			24 MHz	1.46	1.48	1.54	1.63	1.82	
			16 MHz	1.03	1.05	1.10	1.20	1.38	
			8 MHz	0.53	0.54	0.60	0.69	0.89	
			4 MHz	0.30	0.31	0.37	0.47	0.66	
			2 MHz	0.18	0.19	0.25	0.34	0.53	
			1 MHz	0.12	0.13	0.19	0.28	0.47	
			100 kHz	0.06	0.08	0.13	0.22	0.42	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 30. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.72	2.76	2.89	3.12	3.58	3.0	3.1	3.4	3.8	4.8	mA
				16 MHz	1.73	1.76	1.89	2.12	2.58	1.9	2.0	2.3	2.7	3.7	
				8 MHz	0.93	0.96	1.09	1.31	1.77	1.0	1.1	1.42	1.8	2.8	
				4 MHz	0.53	0.57	0.69	0.91	1.36	0.6	0.7	0.9	1.4	2.4	
				2 MHz	0.33	0.36	0.49	0.71	1.16	0.4	0.5	0.7	1.2	2.2	
				1 MHz	0.23	0.26	0.39	0.61	1.06	0.2	0.4	0.6	1.1	2.1	
				100 kHz	0.14	0.17	0.3	0.52	0.97	0.2	0.3	0.5	1.0	2.0	
			Range 1	80 MHz	9.71	9.78	9.95	10.2	10.8	10.6	10.7	11.1	11.6	12.7	
				72 MHz	8.77	8.84	9	9.27	9.8	9.6	9.7	10.0	10.6	11.7	
				64 MHz	7.82	7.89	8.05	8.32	8.84	8.5	8.7	9.0	9.5	10.6	
				48 MHz	5.87	5.93	6.1	6.36	6.88	6.4	6.6	6.9	7.4	8.5	
				32 MHz	3.97	4.03	4.18	4.44	4.95	4.4	4.5	4.8	5.3	6.4	
				24 MHz	3.02	3.07	3.22	3.47	3.99	3.3	3.5	3.7	4.3	5.4	
				16 MHz	2.07	2.11	2.26	2.51	3.02	2.3	2.4	2.7	3.2	4.3	
I_{DD_ALL} (LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	258	296	430	665	1140	295	402	634	1154	2180	µA
				1 MHz	136	180	314	550	1020	170	283	530	1034	2065	
				400 kHz	78.5	109	241	475	951	90	206	458	958	1991	
				100 kHz	37.4	78.1	208	440	918	53	171	429	925	1957	

1. Guaranteed by characterization results, unless otherwise specified.

Table 31. Current consumption in Run, code with data processing running from SRAM1 and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	80 MHz	3.49	3.52	3.58	3.67	3.88	mA
			72 MHz	3.15	3.18	3.24	3.33	3.52	
			64 MHz	2.81	2.84	2.89	2.99	3.18	
			48 MHz	2.11	2.13	2.19	2.29	2.47	
			32 MHz	1.43	1.45	1.50	1.60	1.78	
			24 MHz	1.09	1.10	1.16	1.25	1.43	
			16 MHz	0.74	0.76	0.81	0.90	1.09	
			8 MHz	0.40	0.41	0.47	0.57	0.76	
			4 MHz	0.23	0.25	0.30	0.39	0.59	
			2 MHz	0.14	0.16	0.21	0.31	0.50	
			1 MHz	0.10	0.11	0.17	0.26	0.46	
			100 kHz	0.06	0.07	0.13	0.22	0.42	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 32. Typical current consumption in Run and Low-power run modes, with different codes running from flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.65	mA	102	µA/MHz
				Coremark	2.97		114	
				Dhrystone 2.1	3.1		119	
				Fibonacci	2.9		112	
				While(1)	2.43		93	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	9.44	mA	118	µA/MHz
				Coremark	10.6		133	
				Dhrystone 2.1	10.9		136	
				Fibonacci	10.3		129	
				While(1)	8.66		108	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	274	µA	137	µA/MHz
				Coremark	307		154	
				Dhrystone 2.1	308		154	
				Fibonacci	273		137	
				While(1)	258		129	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 33. Typical current consumption in Run, with different codes running from flash, ART enable (Cache ON Prefetch OFF) and power supplied (by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.14	mA	44	µA/MHz
				Coremark	1.28		49	
				Dhrystone 2.1	1.34		51	
				Fibonacci	1.25		48	
				While(1)	1.05		40	
			f_{HCLK} = 80 MHz	Reduced code(2)	3.39		42	
				Coremark	3.81		48	
				Dhrystone 2.1	3.92		49	
				Fibonacci	3.70		46	
				While(1)	3.11		39	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 34. Typical current consumption in Run, with different codes running from flash, ART enable (Cache ON Prefetch OFF) and power supplied (by external SMPS (V_{DD12} = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.04	mA	40	µA/MHz
				Coremark	1.17		45	
				Dhrystone 2.1	1.22		47	
				Fibonacci	1.14		44	
				While(1)	0.96		37	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 35. Typical current consumption in Run and Low-power run modes, with different codes running from flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	3.1	mA	119	µA/MHz
				Coremark	2.85		110	
				Dhrystone 2.1	2.86		110	
				Fibonacci	2.63		101	
				While(1)	2.42		93.1	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	10	mA	125	µA/MHz
				Coremark	9.33		117	
				Dhrystone 2.1	9.4		118	
				Fibonacci	8.66		108	
				While(1)	8.61		108	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code(1)	378	µA	189	µA/MHz
				Coremark	412		206	
				Dhrystone 2.1	418		209	
				Fibonacci	392		196	
				While(1)	266		133	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 36. Typical current consumption in Run modes, with different codes running from flash, ART disable and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.34	mA	51	µA/MHz
				Coremark	1.23		47	
				Dhrystone 2.1	1.23		47	
				Fibonacci	1.13		44	
				While(1)	1.04		40	
			f_{HCLK} = 80 MHz	Reduced code(1)	3.59		45	
				Coremark	3.35		42	
				Dhrystone 2.1	3.38		42	
				Fibonacci	3.11		39	
				While(1)	3.10		39	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 37. Typical current consumption in Run modes, with different codes running from flash, ART disable and power supplied by external SMPS (V_{DD12} = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals	f_{HCLK} = 26 MHz	Reduced code(2)	1.22	mA	47	µA/MHz
				Coremark	1.12		43	
				Dhrystone 2.1	1.12		43	
				Fibonacci	1.03		40	
				While(1)	0.95		37	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 38. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code(1)	2.72	mA	105	µA/MHz
				Coremark	2.72		105	
				Dhrystone 2.1	2.65		102	
				Fibonacci	2.47		95	
				While(1)	2.37		91	
			Range 1 f_{HCLK} = 80 MHz	Reduced code(1)	9.71	mA	121	µA/MHz
				Coremark	9.7		121	
				Dhrystone 2.1	9.48		119	
				Fibonacci	8.79		110	
				While(1)	8.45		106	
I_{DD_ALL} (LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ = 2 MHz all peripherals disable		Reduced code(1)	258	µA	129	µA/MHz
				Coremark	268		134	
				Dhrystone 2.1	240		120	
				Fibonacci	230		115	
				While(1)	255		128	

1. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 39. Typical current consumption in Run, with different codes running from SRAM1 and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.17	mA	45	µA/MHz
				Coremark	1.17		45	
				Dhrystone 2.1	1.14		44	
				Fibonacci	1.07		41	
				While(1)	1.02		39	
			f_{HCLK} = 80 MHz	Reduced code(1)	3.49		44	
				Coremark	3.49		44	
				Dhrystone 2.1	3.41		43	
				Fibonacci	3.16		39	
				While(1)	3.04		38	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 40. Typical current consumption in Run, with different codes running from SRAM1 and power supplied by external SMPS (V_{DD12} = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.07	mA	41	µA/MHz
				Coremark	1.07		41	
				Dhrystone 2.1	1.04		40	
				Fibonacci	0.97		37	
				While(1)	0.93		36	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 41. Current consumption in Sleep and Low-power sleep modes, flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.79	0.82	0.95	1.17	1.63	0.9	1.0	1.2	1.7	2.7	mA
				16 MHz	0.54	0.57	0.7	0.92	1.38	0.6	0.7	1.0	1.4	2.4	
				8 MHz	0.33	0.37	0.49	0.71	1.17	0.4	0.5	0.7	1.2	2.2	
				4 MHz	0.23	0.26	0.39	0.61	1.06	0.3	0.4	0.6	1.1	2.1	
				2 MHz	0.18	0.21	0.34	0.56	1.01	0.2	0.3	0.5	1.0	1.0	
				1 MHz	0.16	0.19	0.31	0.53	0.99	0.2	0.3	0.5	1.0	1.0	
				100 kHz	0.13	0.17	0.29	0.51	0.96	0.1	0.3	0.5	1.0	1.9	
			Range 1	80 MHz	2.57	2.62	2.76	3.01	3.53	2.8	2.9	3.2	3.8	4.9	
				72 MHz	2.34	2.38	2.53	2.78	3.29	2.6	2.7	3.0	3.5	4.6	
				64 MHz	2.1	2.15	2.29	2.54	3.05	2.3	2.4	2.7	3.3	4.4	
				48 MHz	1.58	1.63	1.78	2.03	2.54	1.8	1.9	2.2	2.7	3.8	
				32 MHz	1.11	1.15	1.3	1.54	2.05	1.2	1.4	1.7	2.2	3.3	
				24 MHz	0.87	0.91	1.06	1.3	1.81	1.0	1.1	1.4	1.9	3.0	
				16 MHz	0.63	0.67	0.82	1.06	1.56	0.7	0.8	1.1	1.6	2.7	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	103	140	270	506	985	130	247	500	990	2025	µA
				1 MHz	74.2	111	245	476	955	100	215	467	963	1999	
				400 kHz	60	89.8	224	457	937	79	194	444	941	1975	
				100 kHz	53.7	84.1	216	448	928	70	185	434	933	1967	

1. Guaranteed by characterization results, unless otherwise specified.

Table 42. Current consumption in Sleep, flash ON and power supplied by external SMPS (V_{DD12} = 1.10 V)

Symbol	Parameter	Conditions(1)		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Sleep)	Supply current in sleep mode,	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	80 MHz	0.92	0.94	0.99	1.08	1.27	mA
			72 MHz	0.84	0.86	0.91	1.00	1.18	
			64 MHz	0.75	0.77	0.82	0.91	1.10	
			48 MHz	0.57	0.59	0.64	0.73	0.91	
			32 MHz	0.40	0.41	0.47	0.55	0.74	
			24 MHz	0.31	0.33	0.38	0.47	0.65	
			16 MHz	0.23	0.24	0.29	0.38	0.56	
			8 MHz	0.14	0.16	0.21	0.31	0.50	
			4 MHz	0.10	0.11	0.17	0.26	0.46	
			2 MHz	0.08	0.09	0.15	0.24	0.44	
			1 MHz	0.07	0.08	0.13	0.23	0.43	
			100 kHz	0.06	0.07	0.13	0.22	0.41	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, V_{DD12} = 1.10 V

Table 43. Current consumption in Low-power sleep modes, flash in power-down

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	92.7	124	258	487	968	105	224	474	969	2006	µA
				1 MHz	63.5	97.5	223	460	951	75	193	446	942	1975	
				400 kHz	42.6	75.6	207	443	947	54	171	426	923	1955	
				100 kHz	31.2	67.6	199	437	905	44	162	420	916	1947	

1. Guaranteed by characterization results, unless otherwise specified.

Table 44. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled	1.8 V	2.57	6.86	25.2	60.1	135	5.3	16.4	64	154.6	353	µA
			2.4 V	2.62	6.91	25.5	60.6	137	5.3	16.6	64.9	156.7	359	
			3 V	2.69	6.93	25.7	61.5	140	5.4	16.9	66.3	159.7	366	
			3.6 V	2.7	7.08	26.3	62.9	143	5.4	17.4	67.8	163.8	375	
		LCD enabled(2) clocked by LSI	1.8 V	2.92	7.19	25.3	59.5	135	5.3	16.6	64.8	155.6	355	
			2.4 V	2.99	7.3	25.6	60.3	136	5.5	16.8	65.9	157.9	360	
			3 V	3.04	7.41	26.1	61.7	140	5.9	17.3	67.1	160.8	367	
			3.6 V	3.31	7.7	26.8	63.2	143	6.2	17.9	69.1	165.0	376	

Table 44. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI, LCD disabled	1.8 V	2.97	7.46	26.2	61.4	139	6.1	17.2	64.8	155.4	354	µA
			2.4 V	3.09	7.61	26.5	62.3	140	6.2	17.5	65.7	157.6	360	
			3 V	3.15	7.81	27	63.5	144	6.5	17.9	67.2	160.6	367	
			3.6 V	3.4	8.05	27.7	65.2	147	7.1	18.7	69.0	164.9	376	
		RTC clocked by LSI, LCD enabled(3)	1.8 V	2.98	7.31	25.5	60	135	5.5	16.8	65.1	155.8	355	
			2.4 V	3.10	7.46	25.8	60.7	137	5.8	17.1	66.3	158.2	360	
			3 V	3.23	7.63	26.4	62.1	141	6.2	17.5	67.6	161.4	367	
			3.6 V	3.47	7.95	27.1	63.6	144	6.58	18.3	69.5	165.5	376	
		RTC clocked by LSE bypassed at 32768Hz,LCD disabled	1.8 V	2.93	7.52	26.2	61.4	139	-	-	-	-	-	
			2.4 V	3.1	7.68	26.6	62.1	140	-	-	-	-	-	
			3 V	3.3	7.81	26.9	63.4	143	-	-	-	-	-	
			3.6 V	3.48	8.07	27.6	65.0	146	-	-	-	-	-	
		RTC clocked by LSE quartz(3) in low drive mode, LCD disabled	1.8 V	2.86	7.48	26.2	61.4	-	-	-	-	-	-	
			2.4 V	3.01	7.56	26.5	62.2	-	-	-	-	-	-	
			3 V	3.18	7.65	26.8	63.5	-	-	-	-	-	-	
			3.6 V	3.31	7.94	27.5	65.1	-	-	-	-	-	-	

Table 44. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(wake up from Stop 2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See (4).	3 V	1.69	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (4).	3 V	1.35	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See (4).	3 V	1.7	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 45. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 1)	Supply current in Stop 1 mode, RTC disabled	-	LCD disabled	1.8 V	11.2	30.7	107	243	523	25.4	79.6	287	651	1395	µA
				2.4 V	11.3	30.8	108	244	526	25.5	79.8	288	655	1403	
				3 V	11.6	31	108	245	530	25.9	80.5	290	659	1413	
				3.6 V	11.9	31.5	109	248	536	28.6	81.4	293	665	1428	
		-	LCD enabled(2) clocked by LSI	1.8 V	11.7	29.7	102	234	504	27.1	81.1	288.5	653	1397	
				2.4 V	11.7	29.9	102	234	506	27.2	81.0	289	656	1405	
				3 V	12.1	29.9	103	234	508	27.4	81.6	291	660	1415	
				3.6 V	12.2	30.1	103	235	510	28.8	82.4	294	667	1429	
I_{DD_ALL} (Stop 1 with RTC)	Supply current in stop 1 mode, RTC enabled	RTC clocked by LSI	LCD disabled	1.8 V	11.9	31.1	108	244	524	26.6	80.5	288	652	1396	µA
				2.4 V	12.1	31.4	109	245	528	26.7	80.9	289	656	1404	
				3 V	12.4	31.7	109	246	531	27.7	81.6	291	660	1415	
				3.6 V	12.6	32.3	110	249	537	28.9	82.8	295	667	1429	
			LCD enabled(2)	1.8 V	11.7	30.1	104	235	510	26.7	80.6	288	653	1397	
				2.4 V	11.8	30.2	104	238	511	26.7	81.1	290	657	1406	
				3 V	11.8	30.5	104	238	515	28.3	81.8	2912	661	1416	
				3.6 V	12.3	31	105	239	519	30.9	83.0	295	668	1430	
		RTC clocked by LSE bypassed at 32768 Hz	LCD disabled	1.8 V	11.6	31.3	108	244	524	-	-	-	-	-	
				2.4 V	11.8	31.6	109	245	527	-	-	-	-	-	
				3 V	12.3	31.9	109	246	531	-	-	-	-	-	
				3.6 V	12.7	32.5	111	249	537	-	-	-	-	-	
		RTC clocked by LSE quartz(3) in low drive mode	LCD disabled	1.8 V	11.5	31.1	108	244	-	-	-	-	-	-	
				2.4 V	11.5	31.4	109	246	-	-	-	-	-	-	
				3 V	12	31.7	109	247	-	-	-	-	-	-	
				3.6 V	12.4	32.3	110	250	-	-	-	-	-	-	

Table 45. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See (4).		3 V	0.99	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).		3 V	1.1	-	-	-	-	-	-	-	-	-	
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See (4).		3 V	0.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 46. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions	TYP					MAX(1)					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	127	153	244	404	734	148	218	471	905	1795	µA
		2.4 V	129	155	247	407	737	151	221	474	910	1803	
		3 V	131	156	249	409	741	154	224	478	915	1813	
		3.6 V	133	158	251	412	744	157	228	482	921	1822(2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 47. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	108	299	1343	3822	10353	227	899	4159	13059	36572	nA
			2.4 V	118	348	1562	4447	12012	252	1009	4846	15026	41366	
			3 V	133	404	1777	5071	13589	318	1211	6082	17245	46714	
			3.6 V	171	501	2115	5898	15539	435	1508	7230	19850	52888(2)	
		With independent watchdog	1.8 V	296	-	-	-	-	-	-	-	-	-	
			2.4 V	349	-	-	-	-	-	-	-	-	-	
			3 V	411	-	-	-	-	-	-	-	-	-	
			3.6 V	506	-	-	-	-	-	-	-	-	-	
I_{DD_ALL} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	377	581	1700	4270	11100	763	1422	5182	13585	36564	nA
			2.4 V	461	700	2020	5030	12900	942	1704	5992	15473	41383	
			3 V	559	843	2390	5990	15500	1166	2032	6938	17889	46728	
			3.6 V	689	1050	2920	7130	18100	1454	2511	7754	20714	53018	
		RTC clocked by LSI, with independent watchdog	1.8 V	422	-	-	-	-	-	-	-	-	-	
			2.4 V	518	-	-	-	-	-	-	-	-	-	
			3 V	560	-	-	-	-	-	-	-	-	-	
			3.6 V	780	-	-	-	-	-	-	-	-	-	

Table 47. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSE bypassed at 32768Hz	1.8 V	308	504	1683	4193	10783	-	-	-	-	-	nA
			2.4 V	400	633	1963	4957	12583	-	-	-	-	-	
			3 V	508	779	2319	5925	15130	-	-	-	-	-	
			3.6 V	661	1009	2825	7027	17540	-	-	-	-	-	
		RTC clocked by LSE quartz (3) in low drive mode	1.8 V	426	624	1679	4244	10884	-	-	-	-	-	
			2.4 V	521	751	1985	4952	12619	-	-	-	-	-	
			3 V	643	914	2371	5931	15121	-	-	-	-	-	
			3.6 V	819	1162	2914	7019	17551	-	-	-	-	-	
I_{DD_ALL} (SRAM2)(4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	371	1111	4297	10153	22747	806	2640	10537	24695	54376	nA
			2.4 V	372	1112	4328	10154	22888	809	2661	10545	24767	54505	
			3 V	374	1116	4403	10429	23711	811	2683	10553	24840	54634	
			3.6 V	378	1149	4545	10702	24361	814	2704	10561	24913	54763	
I_{DD_ALL} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See (5).	3 V	1.4	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: II_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
5. Wakeup with code execution from flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 48. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	24	161	983	3020	8970	85	556	3314	10498	31391	nA
			2.4 V	31	193	1150	3530	10300	111	648	3844	11897	35017	
			3 V	44	242	1400	4260	12500	154	780	4447	13473	39297	
			3.6 V	76	338	1790	5220	14700	236	1009	5354	15679	44571	
I_{DD_ALL} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	225	363	1190	3230	9180	-	-	-	-	-	nA
			2.4 V	314	478	1440	3820	10700	-	-	-	-	-	
			3 V	421	621	1790	4660	12900	-	-	-	-	-	
			3.6 V	561	831	2280	5730	15300	-	-	-	-	-	
		RTC clocked by LSE quartz (2) in low drive mode	1.8 V	341	472	1303	3459	-	-	-	-	-	-	
			2.4 V	435	586	1572	4041	-	-	-	-	-	-	
			3 V	553	732	1982	5145	-	-	-	-	-	-	
			3.6 V	716	948	2520	6325	-	-	-	-	-	-	
I_{DD_ALL} (wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is MSI = 4 MHz. See (3).	3 V	0.6	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 49. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
$I_{VDD_VBAT}(V_{BAT})$	Backup domain supply current	RTC disabled	1.8 V	2	18	110	329	908	-	-	-	-	-	nA
			2.4 V	2	20	125	371	1016	-	-	-	-	-	
			3 V	3	25	154	546	1965	-	-	-	-	-	
			3.6 V	10	57	324	963	2688	-	-	-	-	-	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	198	216	312	535	-	-	-	-	-	-	
			2.4 V	280	300	411	664	-	-	-	-	-	-	
			3 V	375	402	544	943	-	-	-	-	-	-	
			3.6 V	488	529	791	1459	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	320	347	448	856	1432	-	-	-	-	-	
			2.4 V	405	436	550	921	1567	-	-	-	-	-	
			3 V	512	545	686	1128	2529	-	-	-	-	-	
			3.6 V	648	705	976	1588	3293	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull resistors generate a current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 70: I/O static characteristics*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 50*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load internal and external connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 50*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 19: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 50*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 50. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	4.44	3.75	4.00	µA/MHz
	ADC independent clock domain	0.40	0.08	0.30	
	ADC AHB clock domain	5.55	4.63	5.00	
	CRC	0.48	0.42	0.50	
	DMA1	2.00	1.60	2.00	
	DMA2	1.76	1.50	1.50	
	DMA2D	24.33	20.21	24.50	
	FLASH	8.50	7.10	8.00	
	FMC	7.58	6.29	7.00	
	GPIOA(2)	1.59	1.25	1.50	
	GPIOB(2)	1.56	1.25	1.50	
	GPIOC(2)	1.58	1.29	1.50	
	GPIOD(2)	1.40	1.17	1.40	
	GPIOE(2)	1.36	1.13	1.40	
	GPIOF(2)	1.70	1.40	1.50	
	GPIOG(2)	1.80	1.50	1.80	
	GPIOH(2)	1.50	1.30	1.50	
	GPIOI(2)	1.18	0.96	1.00	
	HASH	2.18	1.79	2.00	
	DCMI	1.6	1.3	1.2	
	OTG_FS independent clock domain	23.20	NA	NA	
	OTG_FS AHB clock domain	14.30	NA	NA	
	QUADSPI	6.84	5.67	6.50	

Table 50. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	RNG independent clock domain	2.20	NA	NA	µA/MHz
	RNG AHB clock domain	0.51	NA	NA	
	SRAM1	2.80	2.29	2.50	
	SRAM2	1.20	1.00	1.00	
	TSC	1.50	1.17	1.00	
	All AHB peripherals	121.00	79.10	87.20	
APB1	AHB to APB1 bridge(3)	0.90	0.70	0.90	µA/MHz
	CAN1	3.68	3.04	3.50	
	DAC1	3.20	2.70	3.00	
	I2C1 independent clock domain	3.80	3.20	3.30	
	I2C1 APB clock domain	1.00	0.79	1.00	
	I2C2 independent clock domain	3.41	2.83	3.00	
	I2C2 APB clock domain	0.98	0.79	1.00	
	I2C3 independent clock domain	2.89	2.38	2.50	
	I2C3 APB clock domain	0.98	0.83	1.00	
	I2C4 independent clock domain	3.41	2.83	3.00	
	I2C4 APB clock domain	0.98	0.79	1.00	
	LCD	1.03	0.80	1.03	
	LPUART1 independent clock domain	2.40	2.00	2.20	
	LPUART1 APB clock domain	0.98	0.83	0.80	
	LPTIM1 independent clock domain	3.10	2.54	2.54	
	LPTIM1 APB clock domain	0.88	0.75	0.90	
	LPTIM2 independent clock domain	2.86	2.42	2.25	
	LPTIM2 APB clock domain	0.90	0.67	0.75	
	OPAMP	0.29	0.20	0.30	
	PWR	0.80	0.63	0.60	
	SPI2	1.78	1.50	1.50	
	SPI3	1.76	1.50	1.50	
	SWPMI1 independent clock domain	2.10	1.50	2.00	
	SWPMI1 APB clock domain	1.00	0.79	0.75	

Table 50. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	TIM2	5.85	4.88	5.70	µA/MHz
	TIM3	5.20	4.25	5.00	
	TIM4	4.50	3.67	4.20	
	TIM5	5.60	4.58	5.10	
	TIM6	0.85	0.70	0.90	
	TIM7	0.86	0.71	0.90	
	USART2 independent clock domain	4.06	3.40	4.00	
	USART2 APB clock domain	1.38	1.17	1.40	
	USART3 independent clock domain	4.80	3.92	4.60	
	USART3 APB clock domain	1.80	1.50	1.80	
	UART4 independent clock domain	3.80	3.10	3.00	
	UART4 APB clock domain	1.30	1.13	1.30	
	UART5 independent clock domain	3.83	3.17	3.50	
	UART5 APB clock domain	1.60	1.25	1.50	
	WWDG	0.39	0.33	0.40	
	All APB1 on	84.20	74.96	82.70	
APB2	AHB to APB2 bridge(4)	1.00	0.90	0.90	µA/MHz
	DFSDM1	6.00	5.00	5.50	
	FW	0.28	0.30	0.30	
	SAI1 independent clock domain	2.60	2.10	2.30	
	SAI1 APB clock domain	2.09	1.80	2.00	
	SAI2 independent clock domain	3.30	2.70	3.00	
	SAI2 APB clock domain	2.50	2.00	2.50	
	SDMMC1 independent clock domain	4.20	3.90	4.20	
	SDMMC1 APB clock domain	2.10	1.80	2.00	
	SPI1	1.71	1.42	1.50	
	SYSCFG/VREFBUF/COMP	0.55	0.50	0.50	
	TIM1	8.41	6.96	7.50	
	TIM8	8.83	7.33	8.00	
	TIM15	3.96	3.29	3.50	
	TIM16	3.24	2.67	3.00	
	TIM17	2.94	2.46	2.50	
	USART1 independent clock domain	5.20	4.29	5.50	
	USART1 APB clock domain	1.70	1.50	1.60	

Table 50. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB2	All APB2 on	55.40	41.33	46.00	µA/MHz
ALL		234.98	195.83	235.70	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…I) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

The consumption for the peripherals when using SMPS can be found using STM32CubeMX PCC tool.

6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 51* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 51. Low-power mode wakeup timings(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		6	6	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	Wakeup in flash with flash in power-down during low-power sleep mode (SLEEP_PD=1 in FLASH_ACR) and with clock MSI = 2 MHz		7	9	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in flash	Range 1	Wakeup clock MSI = 48 MHz	7.0	11.6	µs
			Wakeup clock HSI16 = 16 MHz	6.2	10.7	
		Range 2	Wakeup clock MSI = 24 MHz	7.3	11.7	
			Wakeup clock HSI16 = 16 MHz	6.2	10.7	
			Wakeup clock MSI = 4 MHz	7.6	13.2	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	2.5	2.9	
			Wakeup clock HSI16 = 16 MHz	2.7	2.9	
		Range 2	Wakeup clock MSI = 24 MHz	3.2	3.6	
			Wakeup clock HSI16 = 16 MHz	2.7	2.9	
			Wakeup clock MSI = 4 MHz	5.7	13.2	

Table 51. Low-power mode wakeup timings(1) (continued)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run mode in flash	Range 1	Wakeup clock MSI = 48 MHz	8.4	9.4	µs
			Wakeup clock HSI16 = 16 MHz	7.8	8.4	
		Range 2	Wakeup clock MSI = 24 MHz	8.7	9.6	
			Wakeup clock HSI16 = 16 MHz	7.8	8.3	
			Wakeup clock MSI = 4 MHz	8.0	12.9	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	5.5	5.9	
			Wakeup clock HSI16 = 16 MHz	6.6	7.0	
		Range 2	Wakeup clock MSI = 24 MHz	6.1	6.5	
			Wakeup clock HSI16 = 16 MHz	6.6	7.0	
			Wakeup clock MSI = 4 MHz	8.5	12.8	
	Wake up time from Stop 1 mode to Low-power run mode in flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock MSI = 2 MHz	13.8	20.0	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			11.8	22.0	
$t_{WUSTOP2}$	Wake up time from Stop 2 mode to Run mode in flash	Range 1	Wakeup clock MSI = 48 MHz	8.9	9.8	µs
			Wakeup clock HSI16 = 16 MHz	8.3	9.2	
		Range 2	Wakeup clock MSI = 24 MHz	9.3	10.2	
			Wakeup clock HSI16 = 16 MHz	8.2	9.2	
			Wakeup clock MSI = 4 MHz	14.2	16.1	
	Wake up time from Stop 2 mode to Run mode in SRAM1	Range 1	Wakeup clock MSI = 48 MHz	6.1	7.1	
			Wakeup clock HSI16 = 16 MHz	7.2	8.1	
		Range 2	Wakeup clock MSI = 24 MHz	6.8	7.8	
			Wakeup clock HSI16 = 16 MHz	7.2	8.2	
			Wakeup clock MSI = 4 MHz	8.4	16.7	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock MSI = 8 MHz	15.3	23.2	µs
			Wakeup clock MSI = 4 MHz	21.3	30.5	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock MSI = 8 MHz	15.3	23.1	µs
			Wakeup clock MSI = 4 MHz	21.3	30.6	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock MSI = 4 MHz	305.9	322.3	µs

1. Guaranteed by characterization results.

Table 52. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode(2)	Code run with MSI 2 MHz	5	7	µs
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2(3)	Code run with MSI 24 MHz	20	40	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.
3. Time until VOSF flag is cleared in PWR_SR2.

Table 53. Wakeup time using USART/LPUART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baud rate permitting to wakeup up from Stop mode when USART/LPUART clock source is HSI16	Stop 0 mode	-	1.7	µs
		Stop 1 mode and Stop 2 mode	-	8.5	

1. Guaranteed by design.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

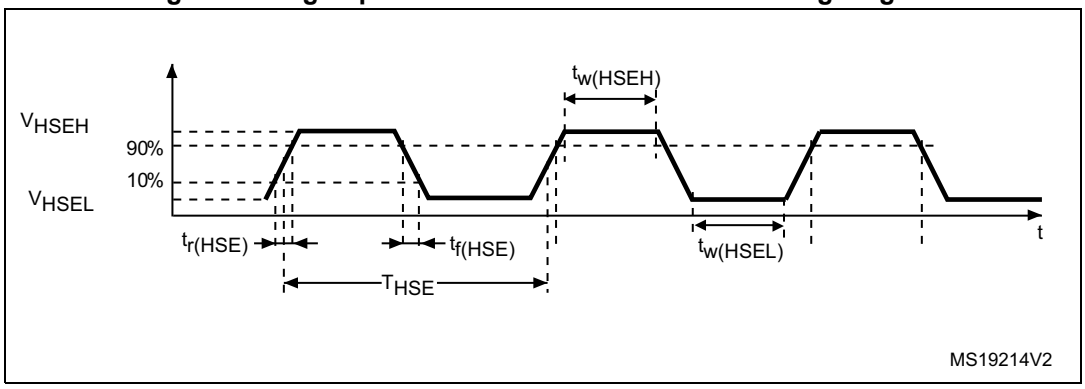
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 26*.

Table 54. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 26. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

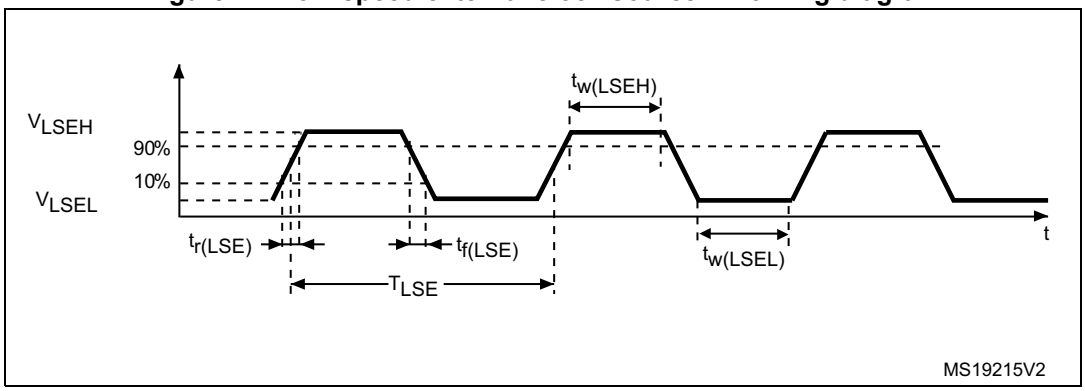
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 27*.

Table 55. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 27. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 56*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 56. HSE oscillator characteristics(1)

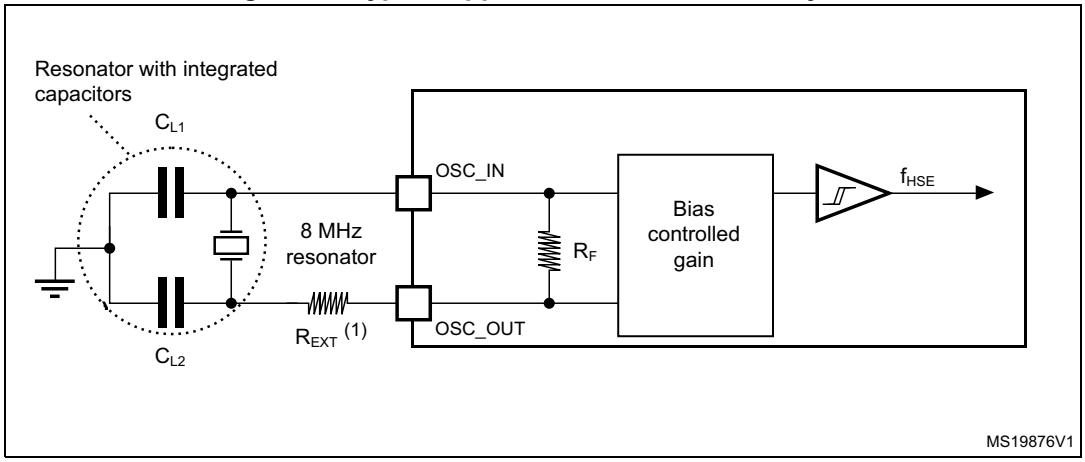
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 28*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 28. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 57*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

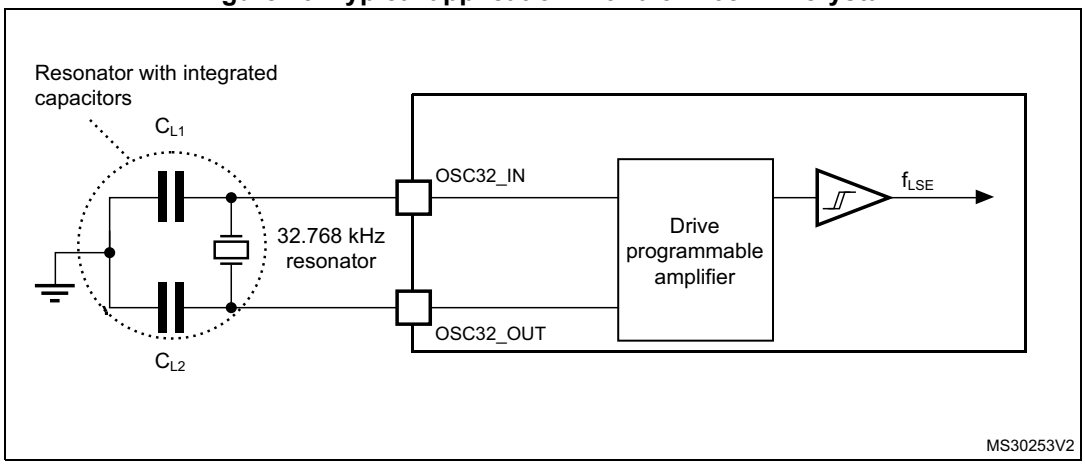
Table 57. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 29. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 58* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 58. HSI16 oscillator characteristics(1)

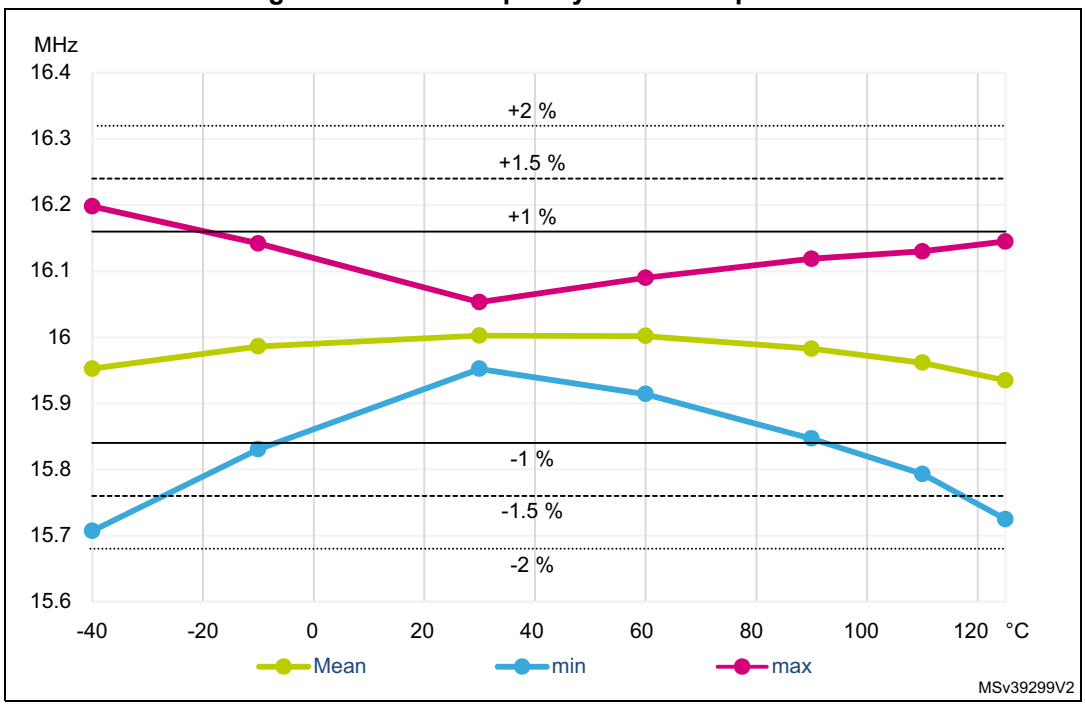
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%

Table 58. HSI16 oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su}(HSI16)^{(2)}$	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
$t_{stab}(HSI16)^{(2)}$	HSI16 oscillator stabilization time	-	-	3	5	µs
$I_{DD}(HSI16)^{(2)}$	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 30. HSI16 frequency versus temperature



Multi-speed internal (MSI) RC oscillator

Table 59. MSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	MSI frequency after factory calibration, done at V_{DD}=3 V and T_A=30 °C	MSI mode	Range 0	98.7	100	101.3	kHz
			Range 1	197.4	200	202.6	
			Range 2	394.8	400	405.2	
			Range 3	7896	800	810.4	
			Range 4	0.987	1	1.013	MHz
			Range 5	1.974	2	2.026	
			Range 6	3.948	4	4.052	
			Range 7	7.896	8	8.104	
			Range 8	15.79	16	16.21	
			Range 9	23.69	24	24.31	
			Range 10	31.58	32	32.42	
			Range 11	47.38	48	48.62	
		PLL mode XTAL= 32.768 kHz	Range 0	-	98.304	-	kHz
			Range 1	-	196.608	-	
			Range 2	-	393.216	-	
			Range 3	-	786.432	-	
			Range 4	-	1.016	-	MHz
			Range 5	-	1.999	-	
			Range 6	-	3.998	-	
			Range 7	-	7.995	-	
			Range 8	-	15.991	-	
			Range 9	-	23.986	-	
			Range 10	-	32.014	-	
			Range 11	-	48.005	-	
$\Delta_{TEMP}(MSI)^{(2)}$	MSI oscillator frequency drift over temperature	MSI mode	T_A= -0 to 85 °C	-3.5	-	3	%
			T_A= -40 to 125 °C	-8	-	6	

Table 59. MSI oscillator characteristics(1) (continued)

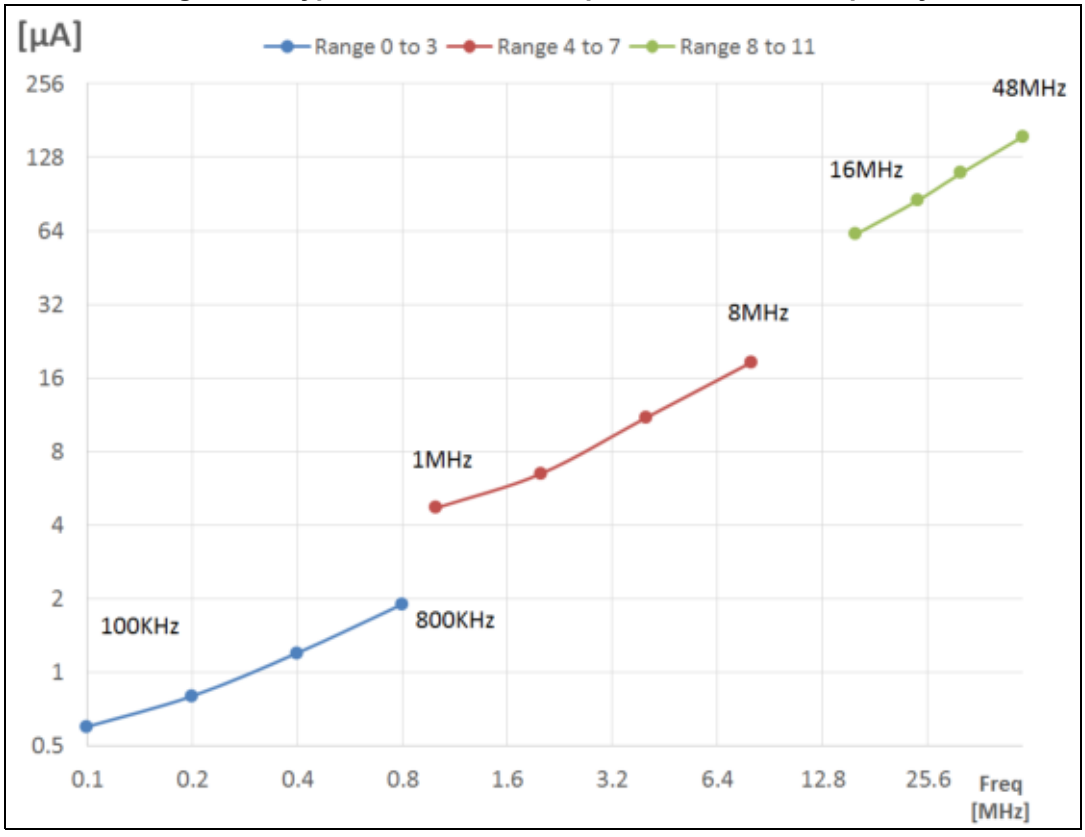
Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1.2	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(4)}$	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
CC jitter(MSI)(4)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(4)	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(4)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(4)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Table 59. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{DD}(MSI)(4)	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1	µA
			Range 1	-	-	0.8	1.2	
			Range 2	-	-	1.2	1.7	
			Range 3	-	-	1.9	2.5	
			Range 4	-	-	4.7	6	
			Range 5	-	-	6.5	9	
			Range 6	-	-	11	15	
			Range 7	-	-	18.5	25	
			Range 8	-	-	62	80	
			Range 9	-	-	85	110	
			Range 10	-	-	110	130	
			Range 11	-	-	155	190	

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Guaranteed by design.

Figure 31. Typical current consumption versus MSI frequency



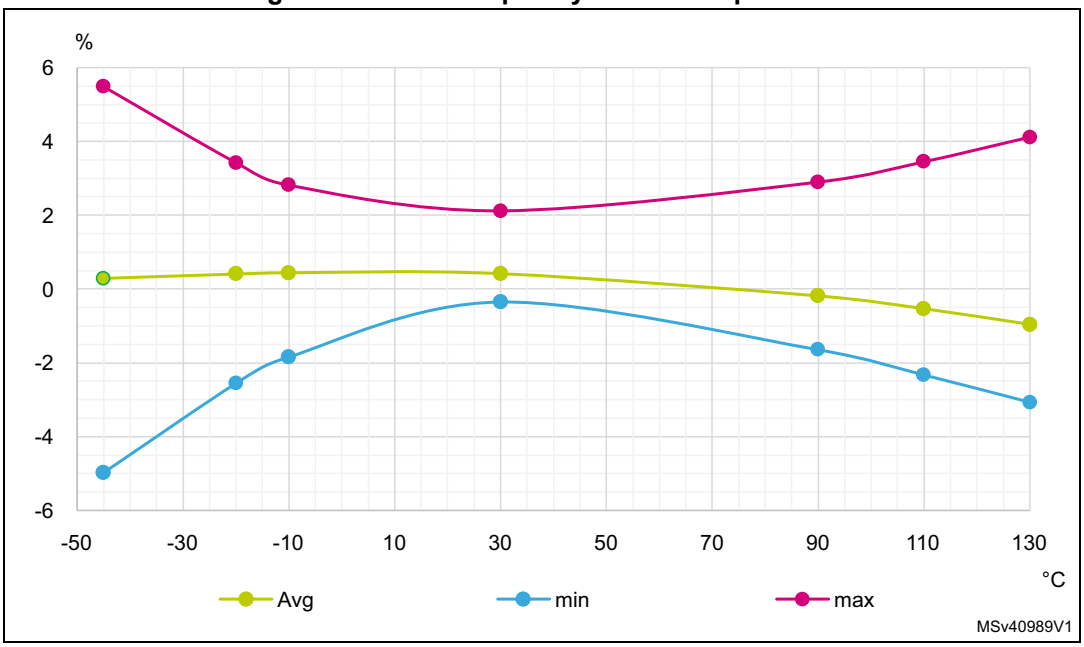
High-speed internal 48 MHz (HSI48) RC oscillator

Table 60. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, TA = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 32. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 61. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(2)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)$(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 62* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 62. PLL, PLLSAI1, PLLSAI2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	4	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%

Table 62. PLL, PLLSAI1, PLLSAI2 characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{PLL_P_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1	2.0645	-	80	MHz
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL_Q_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
$f_{PLL_R_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1	8	-	80	MHz
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	64	-	344	MHz
		Voltage scaling Range 2	64	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 80 MHz	-	40	-	±ps
	RMS period jitter		-	30	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 64 MHz	-	150	200	µA
		VCO freq = 96 MHz	-	200	260	
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between the 3 PLLs.

6.3.10 Flash memory characteristics

Table 63. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	µs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms

Table 63. Flash memory characteristics(1) (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 µs)	-	
		Erase mode	7 (for 41 µs)	-	

1. Guaranteed by design.

Table 64. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 65*. They are based on the EMS levels and classes defined in application note AN1709.

Table 65. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 80 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 80 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 66. EMI characteristics for f_{HSE} = 8 MHz and f_{HCLK} = 80 MHz

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak(1)	V_{DD} = 3.6 V, T_A = 25 °C, BGA169 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	3	dBµV
			30 MHz to 130 MHz	-2	
			130 MHz to 1 GHz	0	
			1 GHz to 2 GHz	8	
	Level(2)		0.1 MHz to 30 MHz	1.5	-

1. Refer to AN1709 “EMI radiated test” section.
2. Refer to AN1709 “EMI level classification” section.

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 67. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 68. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 69*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 69. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins except PA4, PA5, PB0, PF12, PF13, OPAMP1_V1NM, OPAMP2_V1NM	-5	NA(2)	mA
	Injected current on pins PB0, PF12, PF13	0	NA(2)	
	Injected current on OPAMP1_V1NM, OPAMP2_V1NM	0	0	
	Injected current on PA4, PA5 pins	-5	0	

1. Guaranteed by characterization.
2. Injection is not possible

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 70* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Note: For information on GPIO configuration, refer to the application note AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption" available from the ST website www.st.com.

Table 70. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.3xV_{DDIOx}$ (2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.39xV_{DDIOx}$ - 0.06 (3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	$0.43xV_{DDIOx}$ - 0.1 (3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	$0.17xV_{DDIOx}$ (3)	
V_{IH}(1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	$0.7xV_{DDIOx}$ (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	$0.49xV_{DDIOX}$ + 0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	$0.61xV_{DDIOX}$ + 0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	$0.77xV_{DDIOX}$ (3)	-	-	
V_{hys}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	

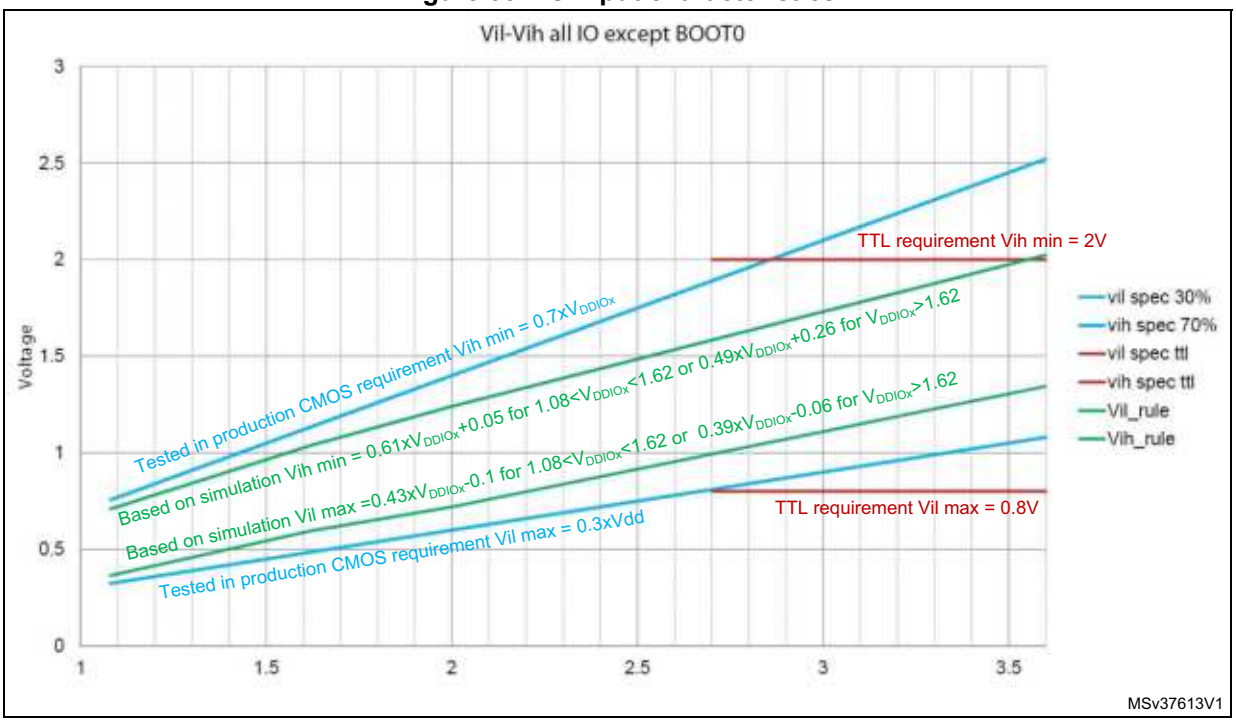
Table 70. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}(4)	FT_xx input leakage current(3)(5)	$V_{IN} \le Max(V_{DDXXX})$(6)(7)	-	-	±100	nA
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(6)(7)	-	-	650	
		$Max(V_{DDXXX})+1$ V < $V_{IN} \le 5.5$ V(6)(7)	-	-	200	
	FT_lu, FT_u, PB2 and PC3 IO	$V_{IN} \le Max(V_{DDXXX})$ (6)(7)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} \le Max(V_{DDXXX})+1$ V(6)(7)	-	-	2500(3)	
		$Max(V_{DDXXX})+1$ V < $V_{IN} \le 5.5$ V(6)(7)	-	-	250	
	TT_xx input leakage current	$V_{IN} \le Max(V_{DDXXX})$(6)	-	-	±150	
		$Max(V_{DDXXX}) \le V_{IN} < 3.6$ V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current (UFBGA132 only)	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 33: I/O input characteristics*.
2. Guaranteed by test production.
3. Guaranteed by design.
4. This value represents the pad leakage of the IO itself. The total product pad leakage is provided by this formula: $I_{Total_Ileak_max}$ = 10 µA + [number of IOs where V_{IN} is applied on the pad] x I_{lkg}(Max).
5. All FT_xx GPIOs except FT_lu, FT_u, PB2 and PC3.
6. $Max(V_{DDXXX})$ is the maximum value of all the I/O supplies.
7. To sustain a voltage higher than Min(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
8. Refer to I_{bias} in *Table 86: OPAMP characteristics* for the values of the OPAMP dedicated input leakage current.
9. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 33* for standard I/Os, and in *Figure 33* for 5 V tolerant I/Os.

Figure 33. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

GPIOs PC13, PC14 and PC15 are supplied through the power switch, limiting source capability up to 3 mA only.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 19: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 19: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 71. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA(3) $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(4)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA(5) $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(4)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(4)	Output low level voltage for an I/O pin	PC13, PC14 and PC15 $\|I_{IO}\|$ = 3 mA $V_{DDIOx} \geq 2.7$ V	-	0.07	
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DDIOx}-0.35	-	
V_{OL}(4)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA(5) $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(4)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA(3) $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(4)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(4)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(4)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 19: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. PC13, PC14 and PC15 are tested/characterized at their maximum current of 3 mA.
4. Guaranteed by design.
5. Not applicable to PC13, PC14 and PC15.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 34* and *Table 72*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 72. I/O AC characteristics(1)(2)

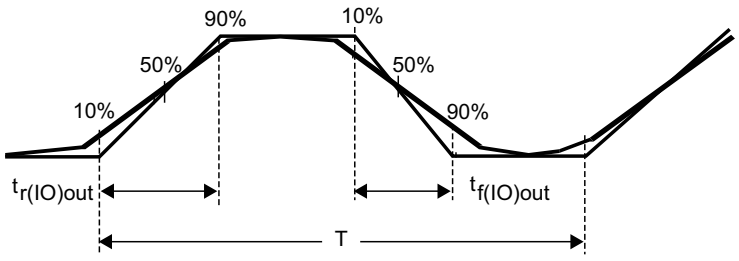
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 72. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0351 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

Figure 34. I/O AC characteristics definition(1)



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

MS32132V4

1. Refer to *Table 72: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

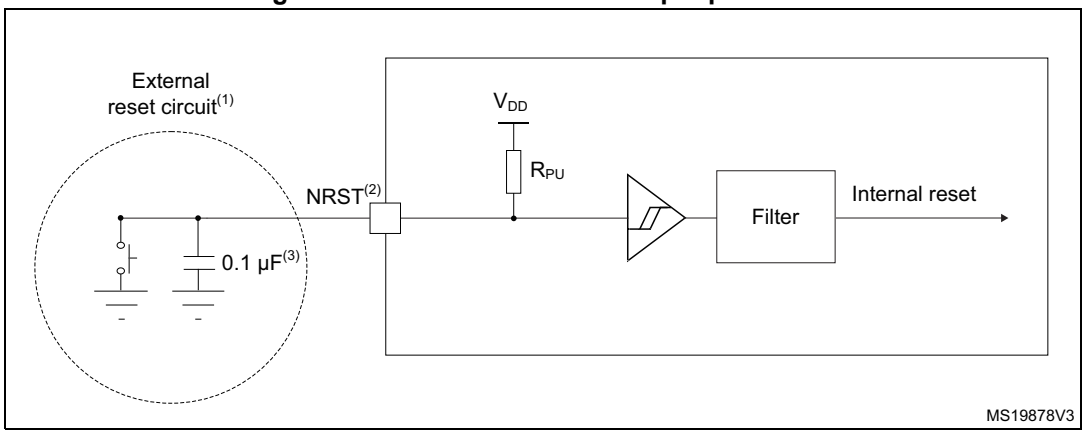
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 73. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 35. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 73*. Otherwise the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.16 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 74. EXTI Input Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

6.3.17 Analog switches booster

Table 75. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

6.3.18 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 76* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 22: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 76. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	0.14	-	80	MHz
		Range 2	0.14	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	

Table 76. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

The maximum value of R_{AIN} can be found in *Table 77*.

Table 77. Maximum ADC R_{AIN}(1)(2)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	31.25	100	N/A
	6.5	81.25	330	100
	12.5	156.25	680	470
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	4700	3900
	247.5	3093.75	12000	10000
	640.5	8006.75	39000	33000
10 bits	2.5	31.25	120	N/A
	6.5	81.25	390	180
	12.5	156.25	820	560
	24.5	306.25	1500	1200
	47.5	593.75	2200	1800
	92.5	1156.25	5600	4700
	247.5	3093.75	12000	10000
	640.5	8006.75	47000	39000
8 bits	2.5	31.25	180	N/A
	6.5	81.25	470	270
	12.5	156.25	1000	680
	24.5	306.25	1800	1500
	47.5	593.75	2700	2200
	92.5	1156.25	6800	5600
	247.5	3093.75	15000	12000
	640.5	8006.75	50000	50000
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.

2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. Fast channels correspond for ADCx_INPx to PC0, PC1, PC2, PC3, PA0 and for ADCx_INNx to PC1, PC2, PC3, PA0.
4. Slow channels correspond to all ADC inputs except Fast channels.

Table 78. ADC accuracy - limited test conditions 1(1)(2)(3)(4)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+}$ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 78. ADC accuracy - limited test conditions 1[(1)(2)(3)(4)] (continued)

Sym-bol	Parameter	Conditions[(5)]			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The above table gives the ADC performance in 12-bit mode.
5. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 79. ADC accuracy - limited test conditions 2(1)(2)(3)(4)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	4	6.5	LSB
				Slow channel (max speed)	-	4	6.5	
			Differential	Fast channel (max speed)	-	3.5	5.5	
				Slow channel (max speed)	-	3.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	4.5	
				Slow channel (max speed)	-	1	5	
			Differential	Fast channel (max speed)	-	1.5	3	
				Slow channel (max speed)	-	1.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	2.5	6	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	3.5	
				Slow channel (max speed)	-	1.5	3.5	
			Differential	Fast channel (max speed)	-	1	3	
				Slow channel (max speed)	-	1	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.5	-	bits
				Slow channel (max speed)	10	10.5	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65	-	dB
				Slow channel (max speed)	62	65	-	
			Differential	Fast channel (max speed)	66	67.4	-	
				Slow channel (max speed)	66	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66	-	
				Slow channel (max speed)	64	66	-	
			Differential	Fast channel (max speed)	66.5	68	-	
				Slow channel (max speed)	66.5	68	-	

Table 79. ADC accuracy - limited test conditions 2(1)(2)(3)(4) (continued)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 2 V ≤ V_{DDA}	Single ended	Fast channel (max speed)	-	-74	-65	dB
				Slow channel (max speed)	-	-74	-67	
			Differential	Fast channel (max speed)	-	-79	-70	
				Slow channel (max speed)	-	-79	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The above table gives the ADC performance in 12-bit mode.
5. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 80. ADC accuracy - limited test conditions 3(1)(2)(3)(4)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 80. ADC accuracy - limited test conditions 3(1)(2)(3)(4) (continued)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The above table gives the ADC performance in 12-bit mode.
5. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 81. ADC accuracy - limited test conditions 4(1)(2)(3)(4)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 81. ADC accuracy - limited test conditions 4(1)(2)(3)(4) (continued)

Sym-bol	Parameter	Conditions(5)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = $_{REF+}$ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	-71	-69	dB
				Slow channel (max speed)	-	-71	-69	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The above table gives the ADC performance in 12-bit mode.
5. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 36. ADC accuracy characteristics

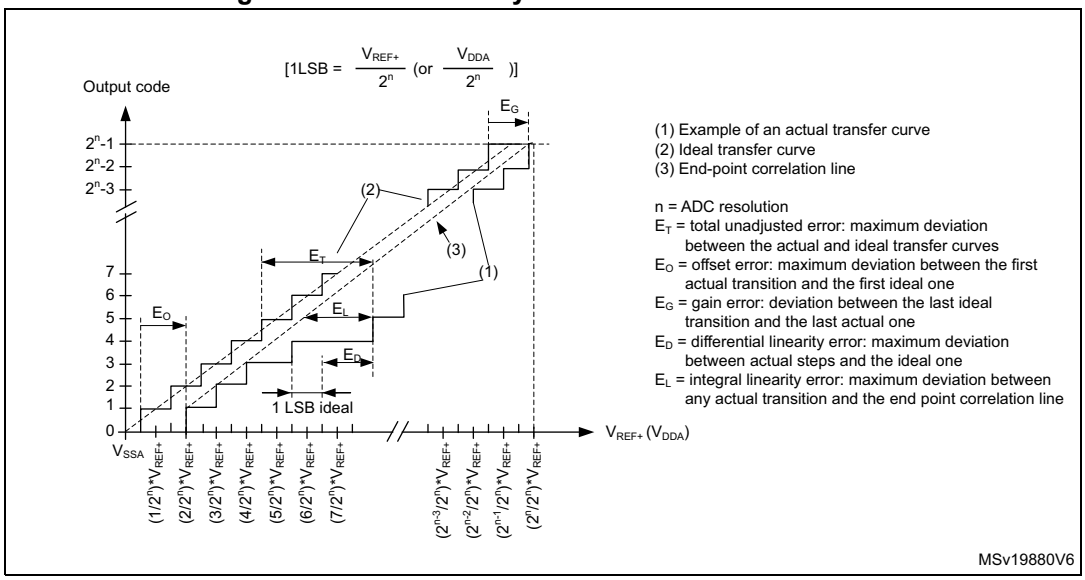
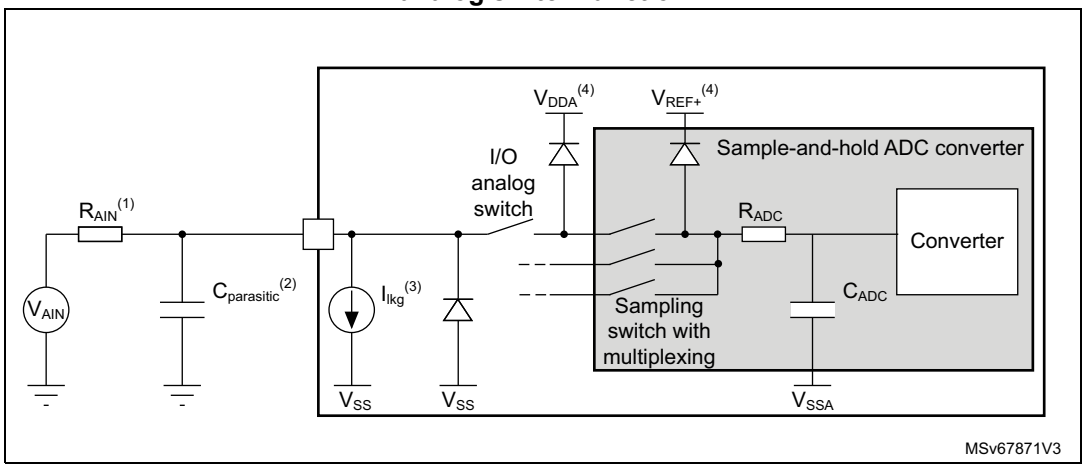


Figure 37. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. Refer to *Table 76: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 70: I/O static characteristics*). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 70: I/O static characteristics* for the values of I_{lkg}.
4. Refer to *Figure 23: Power supply scheme*.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 23: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.19 Digital-to-Analog converter characteristics

Table 82. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF (no resistive load on DAC1_OUTx pin or internal connection)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF (no resistive load on DAC1_OUTx pin or internal connection)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC1_OUTx output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC1_OUTx reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 82. DAC characteristics(1) (continued)

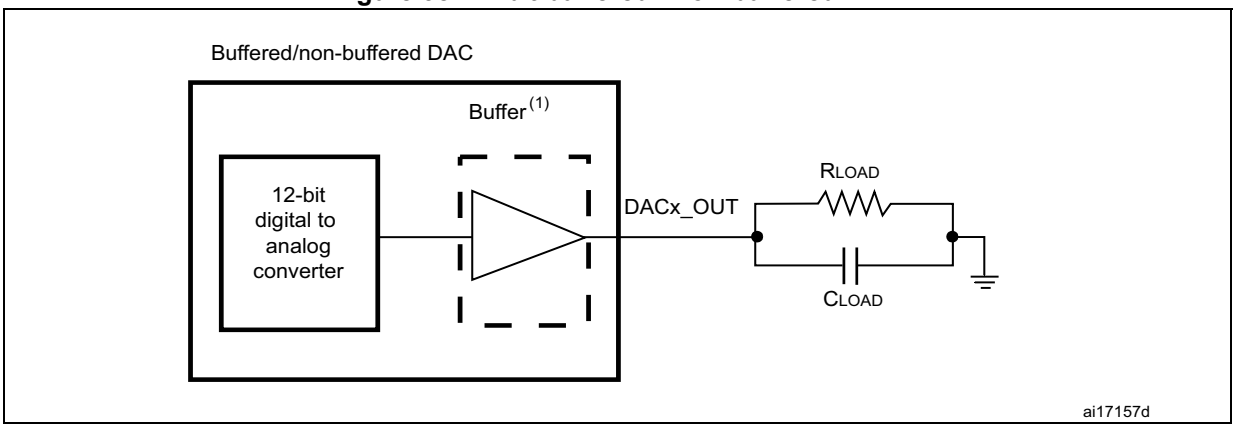
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W_to_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC1_OUTx for a small variation of the input code (1 LSB) DAC_MCR:MODEx[2:0] = 000 or 001 DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 50 pF, RL ≥ 5 kΩ CL ≤ 10 pF		1 1.4	-	-	µs
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DAC1_OUTx reaches final value ±1LSB)	DAC1_OUTx pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC1_OUTx pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC1_OUTx pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Table 82. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 70: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0351 reference manual for more details.

Figure 38. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 83. DAC accuracy(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity (2)	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		guaranteed			
INL	Integral non linearity(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800(3)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001(4)	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error(5)	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 83. DAC accuracy(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

6.3.20 Voltage reference buffer characteristics

Table 84. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046(3)	2.048	2.049(3)	
			V_{RS} = 1	2.498(3)	2.5	2.502(3)	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent series resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	$T_{coeff_vrefint}$ + 50	ppm/ °C
		0 °C < TJ < +50 °C		-	-	$T_{coeff_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(4)		-	300	350	µs
		CL = 1.1 µF(4)		-	500	650	
		CL = 1.5 µF(4)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	-	8	-	mA

Table 84. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which therefore follows (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.21 Comparator characteristics

Table 85. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		4	8	16	
		Medium hysteresis		8	15	30	
		High hysteresis		15	27	52	

Table 85. COMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	
I_{bias}	Comparator input bias current	-		-	-	-(4)	nA

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 25: Embedded internal voltage reference*.
3. Guaranteed by characterization results.
4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in *Table 70: I/O static characteristics*.

6.3.22 Operational amplifiers characteristics

Table 86. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	25 °C, No Load on output.	-	-	±1.5	mV
		All voltage/Temp.	-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	-	±5	-	µV/°C
		Low-power mode	-	±10	-	
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-	-	0.8	1.1	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-	-	1	1.35	

Table 86. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

Table 86. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input (all packages except UFBGA132 and UFBGA169 only)		-	-	(3)	nA
		Dedicated input (UFBGA132 and UFBGA169 only)	T_J ≤ 75 °C	-	-	1	
			T_J ≤ 85 °C	-	-	3	
			T_J ≤ 105 °C	-	-	8	
			T_J ≤ 125 °C	-	-	15	
PGA gain(2)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode(4)	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/ 2	-	MHz
		Gain = 4	-	-	GBW/ 4	-	
		Gain = 8	-	-	GBW/ 8	-	
		Gain = 16	-	-	GBW/ 16	-	

Table 86. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	Normal mode	at 1 kHz, Output loaded with 4 kΩ	-	500	-	nV/√Hz
		Low-power mode	at 1 kHz, Output loaded with 20 kΩ	-	600	-	
		Normal mode	at 10 kHz, Output loaded with 4 kΩ	-	180	-	
		Low-power mode	at 10 kHz, Output loaded with 20 kΩ	-	290	-	
I_{DDA}(OPAMP)(2)	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode	-	120	260	µA
		Low-power mode		-	45	100	

1. Guaranteed by design, unless otherwise specified.
2. Guaranteed by characterization results.
3. Mostly I/O leakage, when used in analog mode. Refer to I_{lkg} parameter in *Table 70: I/O static characteristics*.
4. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

6.3.23 Temperature sensor characteristics

Table 87. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.24 V_{BAT} monitoring characteristics

Table 88. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	3×39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 89. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

6.3.25 LCD controller characteristics

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 90. LCD controller characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7		-	3.62	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	µF
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
I_{LCD}(2)	Supply current from V_{DD} at V_{DD} = 2.2 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	µA
	Supply current from V_{DD} at V_{DD} = 3.0 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	

Table 90. LCD controller characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VLCD}	Supply current from V_{LCD} (V_{LCD} = 3 V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	µA
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High resistor value for Low drive resistive network		-	5.5	-	MΩ
R_{LN}	Total Low resistor value for High drive resistive network		-	240	-	kΩ
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	3/4 V_{LCD}	-	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage		-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage		-	0	-	

1. Guaranteed by design.
2. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.

6.3.26 DFSDM characteristics

Unless otherwise specified, the parameters given in *Table 91* for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x VDD

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (DFSDM1_CKINy, DFSDM1_DATINy, DFSDM1_CKOUT for DFSDM).

Table 91. DFSDM characteristics(1)

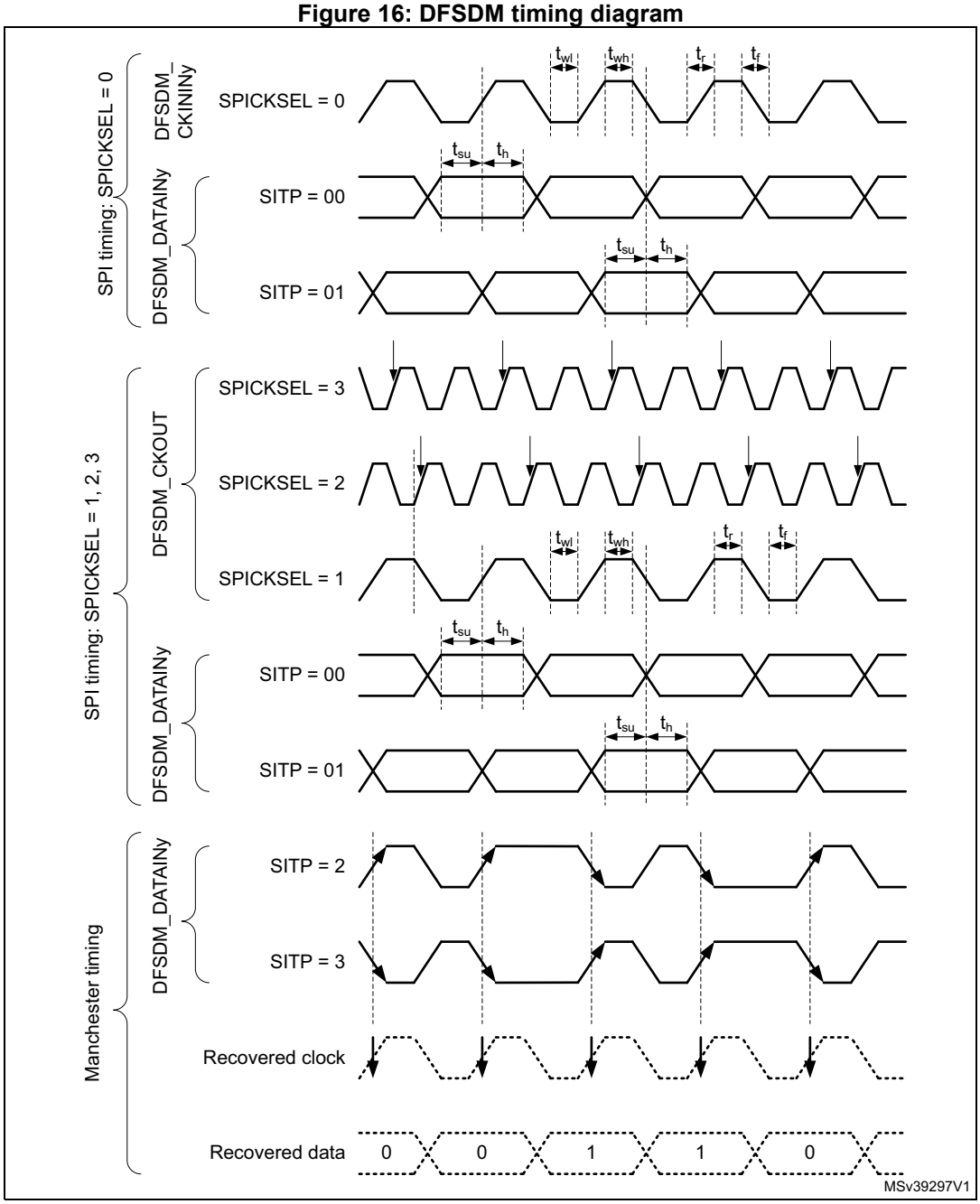
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	-	-	-	f_{SYSCLK}	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 01)	-	-	20 ($f_{DFSDMCLK}$/4)	
f_{CKOUT}	Output clock frequency	-	-	-	20	

Table 91. DFSDM characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$DuCy_{CKOUT}$	Output clock frequency duty cycle	1.62 < V_{DD} < 3.6 V	Even division CKOUTDIV[7:0] = n 1,3,5,..	45	50	55	%
			Odd division CKOUTDIV[7:0] = n 2,4,6,..	(((n/2+1)/ (n+1))*100) -5	((n/2+1)/ (n+1))*100	(((n/2+1)/ (n+1))*100) +5	
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)		T_{CKIN} / 2 - 0.5	T_{CKIN}/ 2	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)		2	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0)		0	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] ≠ 0)		(CKOUT DIV+1) x $T_{DFSDMCLK}$	-	2 x CKOUT DIV x $T_{DFSDMCLK}$	

1. Data based on characterization results, not tested in production.

Figure 16: DFSDM timing diagram



6.3.27 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 92. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 93. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 94. WWDG min/max timeout value at 80 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0512	3.2768	ms
2	1	0.1024	6.5536	
4	2	0.2048	13.1072	
8	3	0.4096	26.2144	

6.3.28 Communication interfaces characteristics

I^2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 95. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 96* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 22: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 96. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range 1	-	-	40	MHz
		Master mode receiver/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range 1			16	
		Master mode transmitter 1.71 V < V_{DD} < 3.6 V Voltage Range 1			40	
		Slave mode receiver 1.71 V < V_{DD} < 3.6 V Voltage Range 1			40	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range 1			31(2)	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range 1			18.5(2)	
		Voltage Range 2			13	
		1.08 V < V_{DDIO2} < 1.32 V(3)			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	$4xT_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	$2xT_{PCLK}$	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	ns
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range 1	-	13	15.5	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 1	-	13	26.5	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 2	-	13	30	
-		Slave mode 1.08 V < V_{DDIO2} < 1.32 V(3)	-	26	60	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.
3. SPI mapped on Port G.

Figure 39. SPI timing diagram - slave mode and CPHA = 0

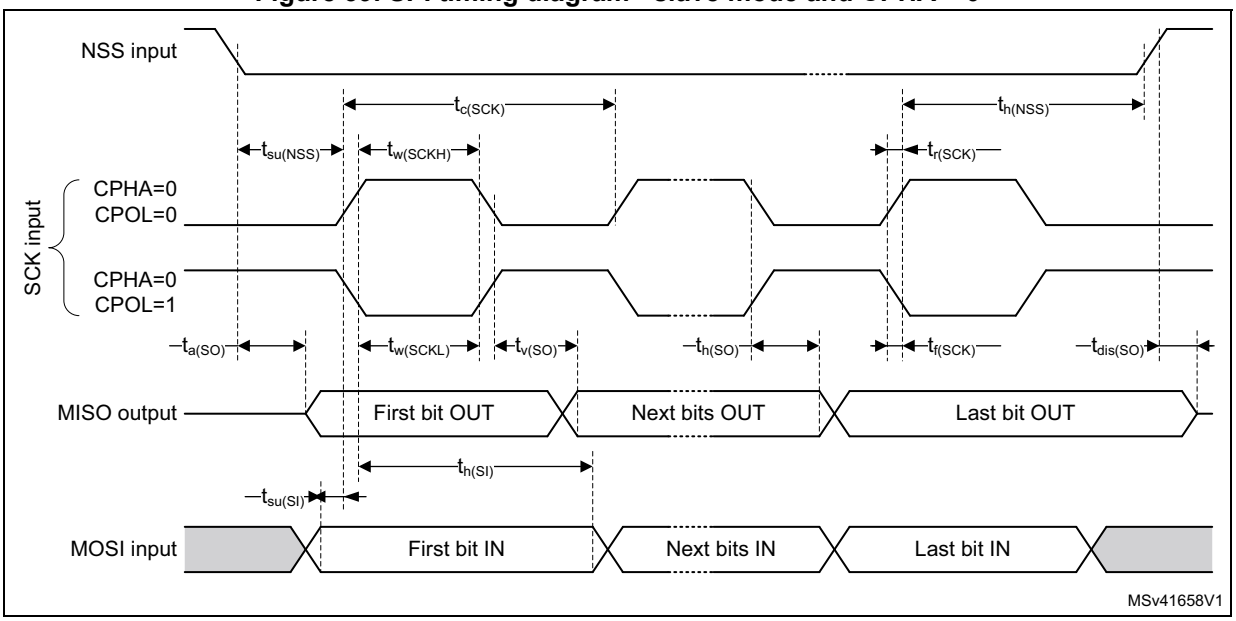
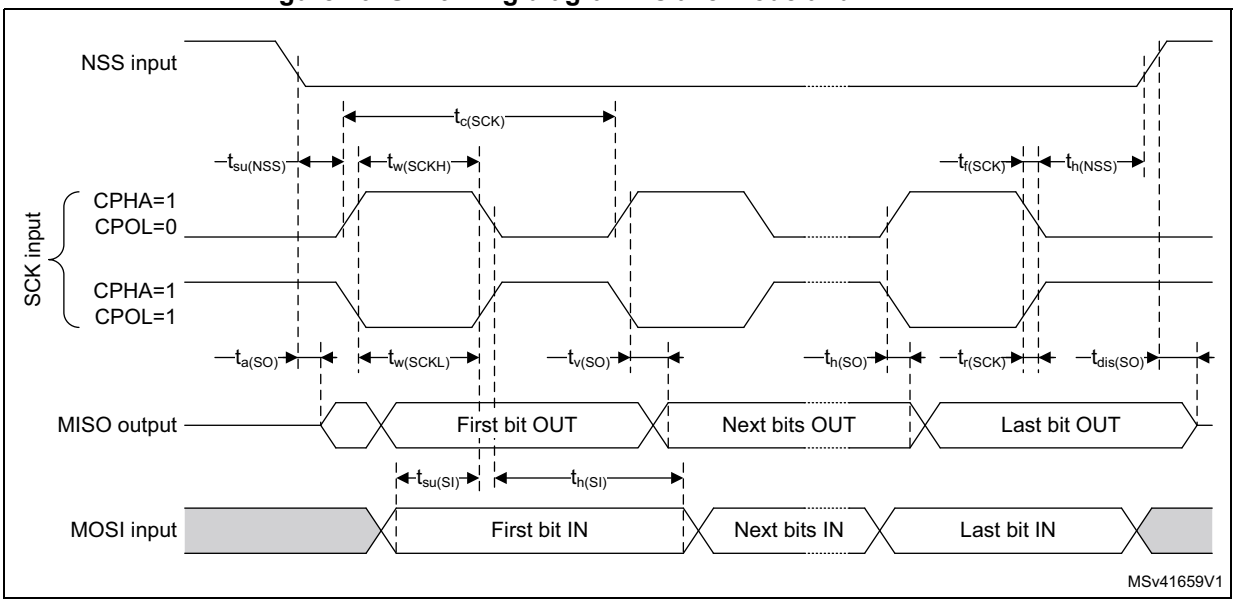
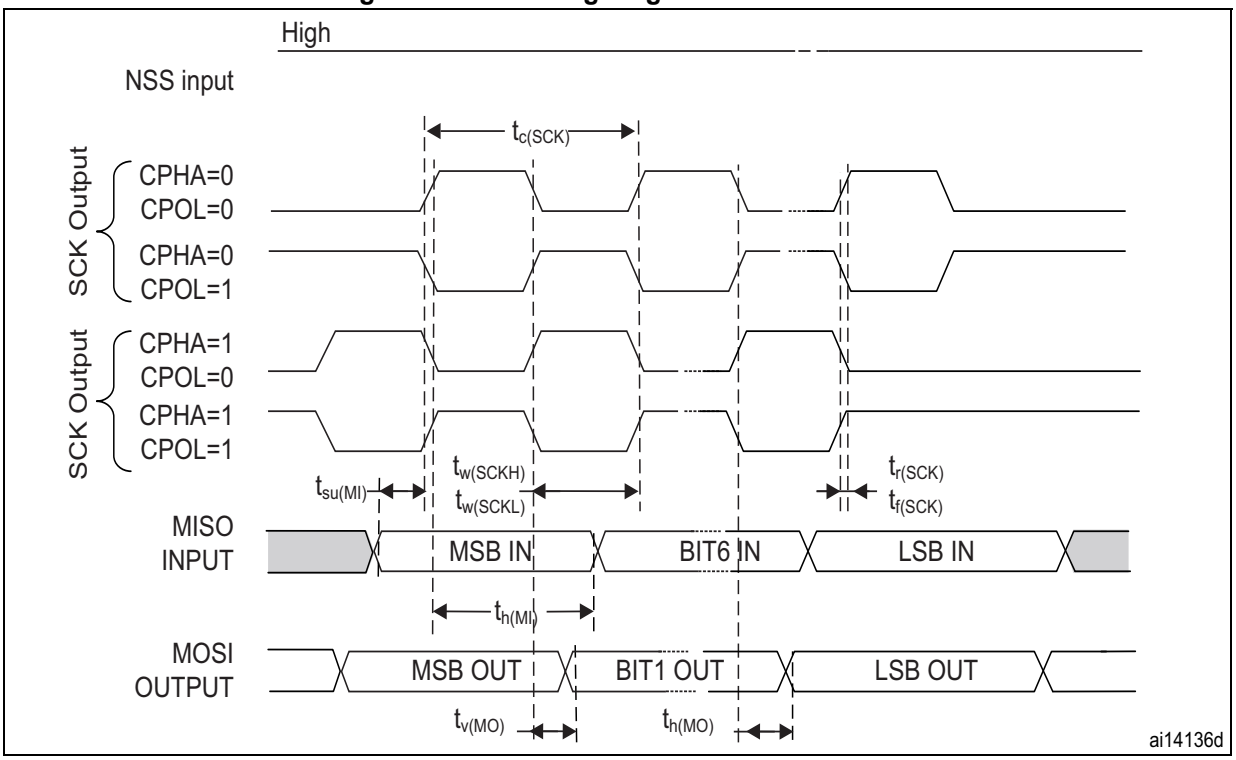


Figure 40. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 41. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Quad SPI characteristics

Unless otherwise specified, the parameters given in *Table 97* and *Table 98* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 97. Quad SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 V < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.71 V < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 V < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.71 V < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	

Table 97. Quad SPI characteristics in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=0	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	1.5	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	4	-	-	
		Voltage Range 2	6.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	1	1.5	
		Voltage Range 2	-	3	5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Table 98. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 V < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		2 V < V_{DD} < 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	48	
		1.71 V < V_{DD} < 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		1.71 V < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	

Table 98. QUADSPI characteristics in DDR mode(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK} = 48 MHz, presc= 1		$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{sf(IN)}$;$t_{sr(IN)}$	Data input setup time	Voltage Range 1 and 2		3.5	-	-	
$t_{hf(IN)}$; $t_{hr(IN)}$	Data input hold time			6.5	-	-	
$t_{vr(OUT)}$	Data output valid time on rise edge	Voltage Range 1	DHHC = 0	-	4.5	5.5	
			DHHC = 1		$t_{(CK)}/2+1$	$t_{(CK)}/2+1.5$	
		Voltage Range 2			9.5	14	
$t_{vf(OUT)}$	Data output valid time on falling edge	Voltage Range 1	DHHC = 0	-	5	6	
			DHHC = 1		$t_{(CK)}/2+1$	$t_{(CK)}/2+1.5$	
		Voltage Range 2			15	18	
$t_{hr(OUT)}$	Data output hold time on rise edge	Voltage Range 1	DHHC = 0	4	-	-	
			DHHC = 1	$t_{(CK)}/2+0.5$	-	-	
		Voltage Range 2		8	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	Voltage Range 1	DHHC = 0	3.5	-	-	
			DHHC = 1	$t_{(CK)}/2+0.5$	-	-	
		Voltage Range 2		13		-	

1. Guaranteed by characterization results.

Figure 42. Quad SPI timing diagram - SDR mode

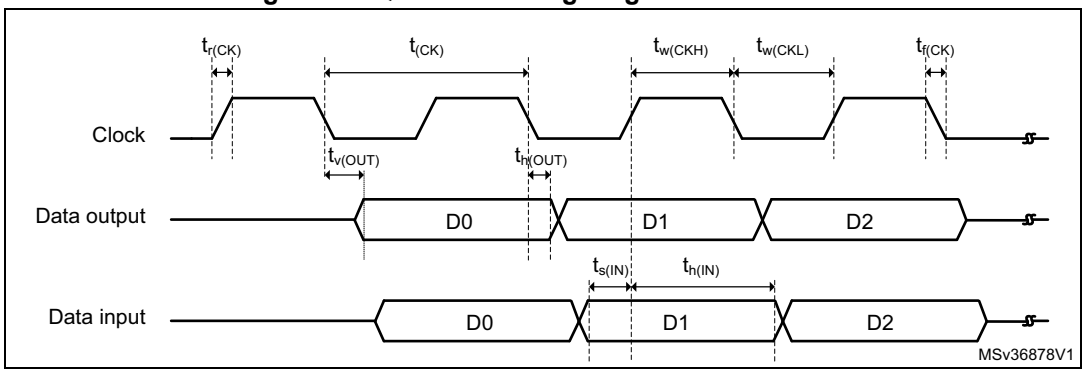
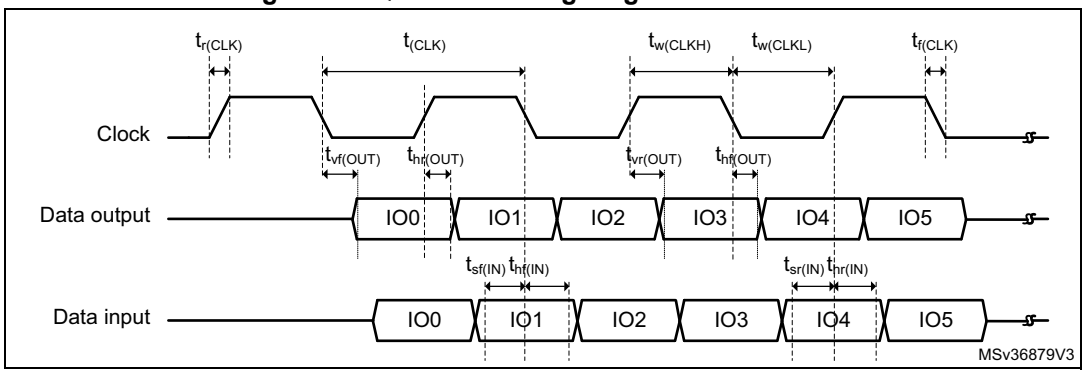


Figure 43. Quad SPI timing diagram - DDR mode



SAI characteristics

Unless otherwise specified, the parameters given in *Table 99* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 99. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	21.5	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	13.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	13.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	13	
		1.08 V ≤ V_{DD} ≤ 1.32 V	-	7	

Table 99. SAI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	22	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	1	-	ns
$t_{su(SD_B_SR)}$		Slave receiver	1	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD_B_SR)}$		Slave receiver	2	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	36	
		Slave transmitter (after enable edge) 1.8 V < V_{DD} <1.32 V	-	68	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	23	ns
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	35	
		Master transmitter (after enable edge) 1.08 V ≤ V_{DD} ≤ 1.32 V	-	70	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 44. SAI master timing waveforms

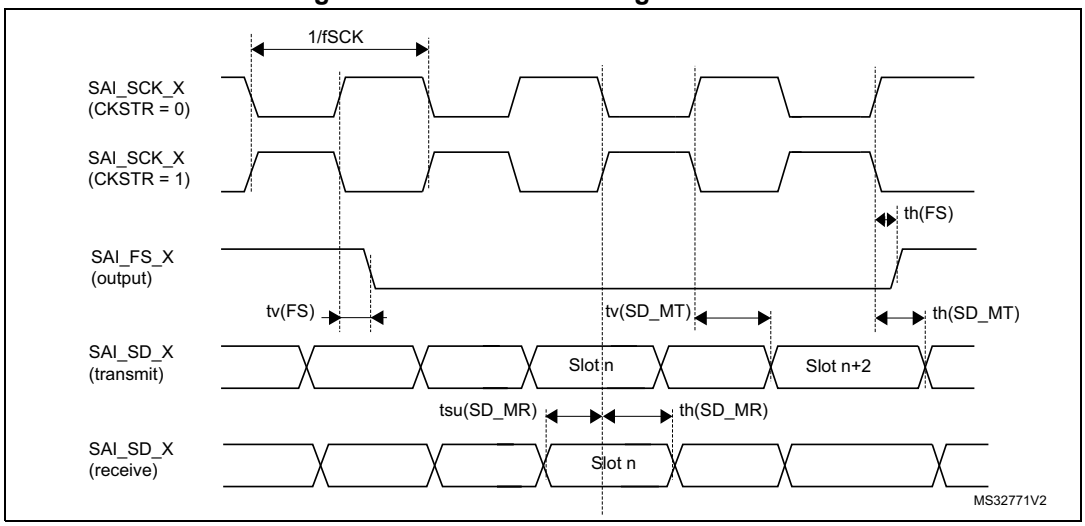
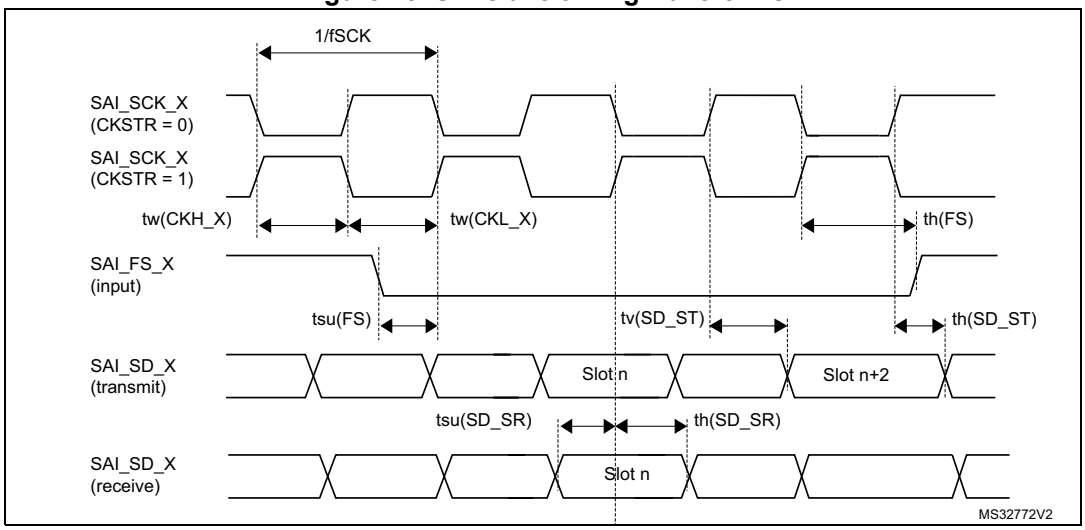


Figure 45. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 100* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Table 100. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	12	13	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	10	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 25 MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 25 MHz	3.5	-	-	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 25 MHz	-	3	5	ns
t_{OHD}	Output hold default time SD	f_{PP} = 25 MHz	0	-	-	ns

1. Guaranteed by characterization results.

Table 101. eMMC dynamic characteristics, V_{DD} = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	16.5	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20pF.

Figure 46. SDIO high-speed mode

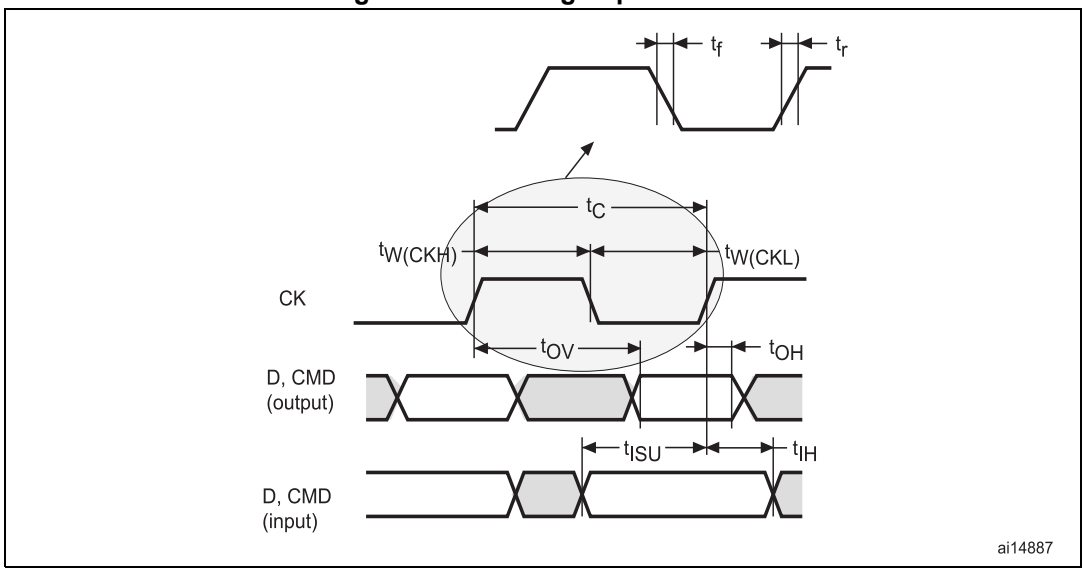
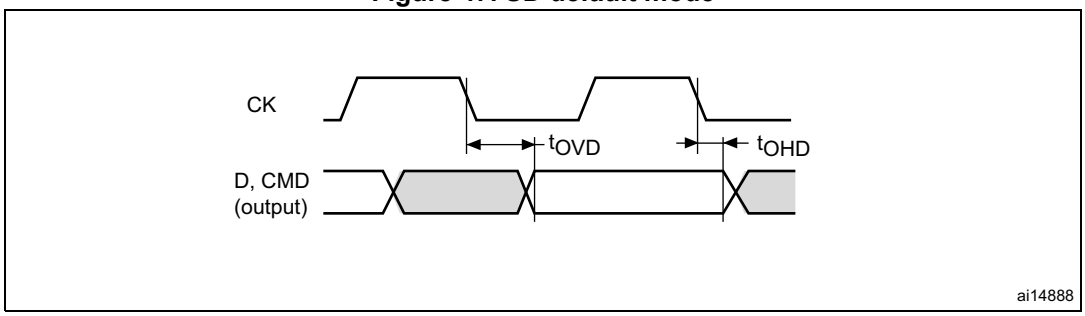


Figure 47. SD default mode



USB OTG full speed (FS) characteristics

The STM32L496xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 102. USB OTG DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDUSB}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
V_{DI}(3)	Differential input sensitivity	Over VCM range	0.2	-	-	V
V_{CM}(3)	Differential input common mode range	Includes V_{DI} range	0.8	-	2.5	
V_{SE}(3)	Single ended receiver input threshold	-	0.8	-	2.0	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}(3)	Pull down resistor on PA11, PA12 (USB_FS_DP/DM)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ

Table 102. USB OTG DC electrical characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
R_{PU}(3)	Pull up resistor on PA12 (USB_FS_DP)	V_{IN} = V_{SS}, during idle	0.9	1.25	1.575	kΩ
	Pull up resistor on PA12 (USB_FS_DP)	V_{IN} = V_{SS} during reception	1.425	2.25	3.09	kΩ
	Pull up resistor on PA10 (OTG_FS_ID)	-	-	-	14.5	kΩ

1. All the voltages are measured from the local ground potential.
2. The USB OTG full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG full speed drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at its default state (floating input), not as alternate function. A typical 200 µA current consumption of the sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 48. USB OTG timings – Definition of data signal rise and fall time

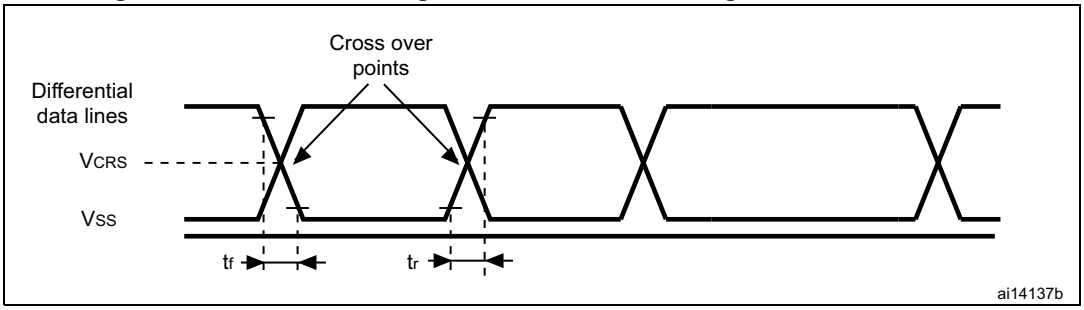


Table 103. USB OTG electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{rfmLS}	Rise/ fall time matching in LS	t_r/t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF	4	20	ns
t_{rfmFS}	Rise/ fall time matching in FS	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations refer to USB Specification - Chapter 7 (version 2.0).

3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 104. USB BCD DC electrical characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-	300	µA
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V
VLGC	Logic threshold	-	0.8		2.0	V
VDAT_REF	Data detect voltage	-	0.25	-	0.4	V
VDP_SRC	D+ source voltage	-	0.5	-	0.7	V
VDM_SRC	D- source voltage	-	0.5	-	0.7	V
IDP_SINK	D+ sink current	-	25	-	175	µA
IDM_SINK	D- sink current	-	25	-	175	µA

1. Guaranteed by design.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.29 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 105* to *Table 118* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 49 through *Figure 52* represent asynchronous waveforms and *Table 105* through *Table 112* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

Figure 49. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

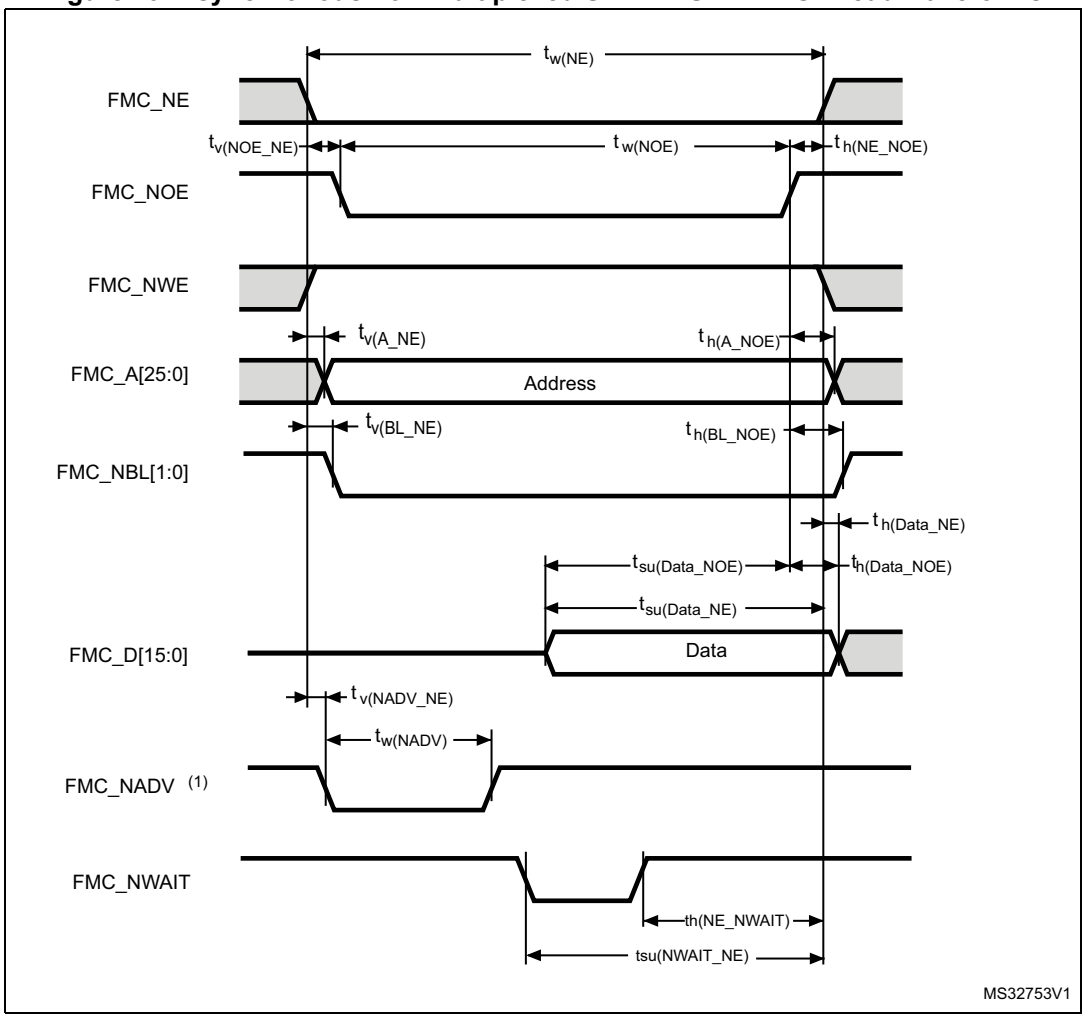


Table 105. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$2T_{HCLK}$-1	$2T_{HCLK}$+1	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{HCLK}$-1	$2T_{HCLK}$+1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-1	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	T_{HCLK}-1	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 106. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$7T_{HCLK}$-1	$7T_{HCLK}$+1	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$-1	$5T_{HCLK}$+1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	T_{HCLK}-0.5	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$+1.5	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 50. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

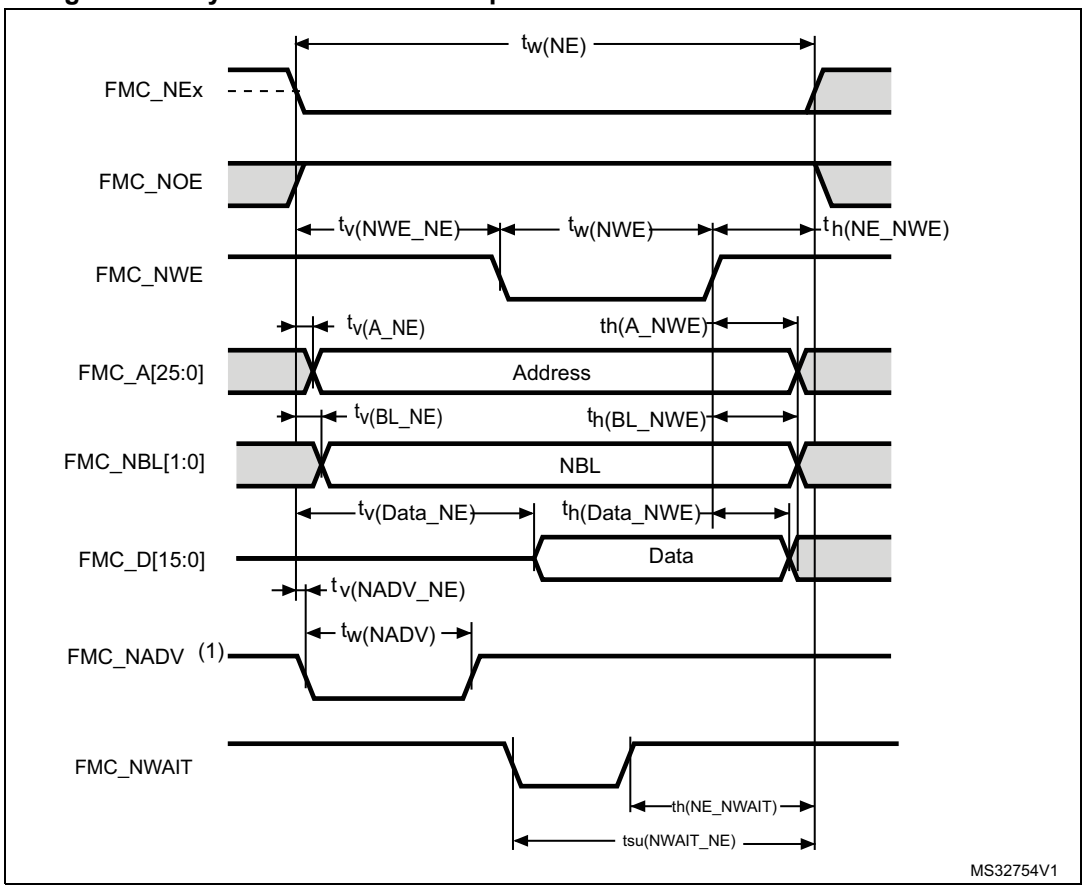


Table 107. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$-1	$3T_{HCLK}$+1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-1	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}-1.5	T_{HCLK}+ 0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}-0.5	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}-0.5	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK}+3	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK}+0.5	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 108. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$-1	$8T_{HCLK}$+1	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{HCLK}$-1.5	$6T_{HCLK}$+0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$-1	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 51. Asynchronous multiplexed PSRAM/NOR read waveforms

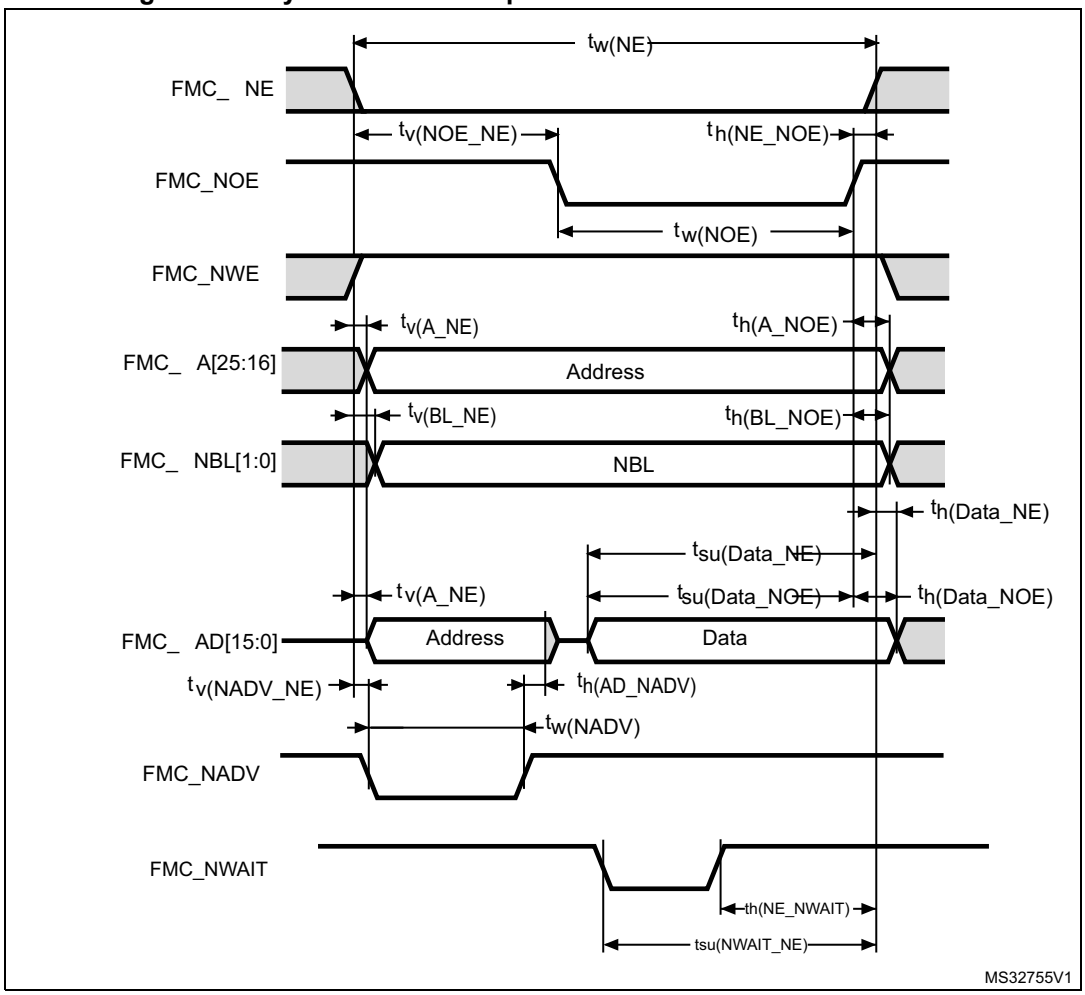


Table 109. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{HCLK}$ -1	$3T_{HCLK}$+1	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{HCLK}$	$2T_{HCLK}$+0.5	
$t_{w(NOE)}$	FMC_NOE low time	T_{HCLK} - 1	T_{HCLK}+1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK} - 0.5	T_{HCLK}+1	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	T_{HCLK} + 0.5	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	T_{HCLK} - 0.5	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	T_{HCLK}-1	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	T_{HCLK}-1	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 110. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{HCLK}$+ 1	$8T_{HCLK}$+ 1	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{HCLK}$ - 1.5	$5T_{HCLK}$+ 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{HCLK}$ +0.5	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$+1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 52. Asynchronous multiplexed PSRAM/NOR write waveforms

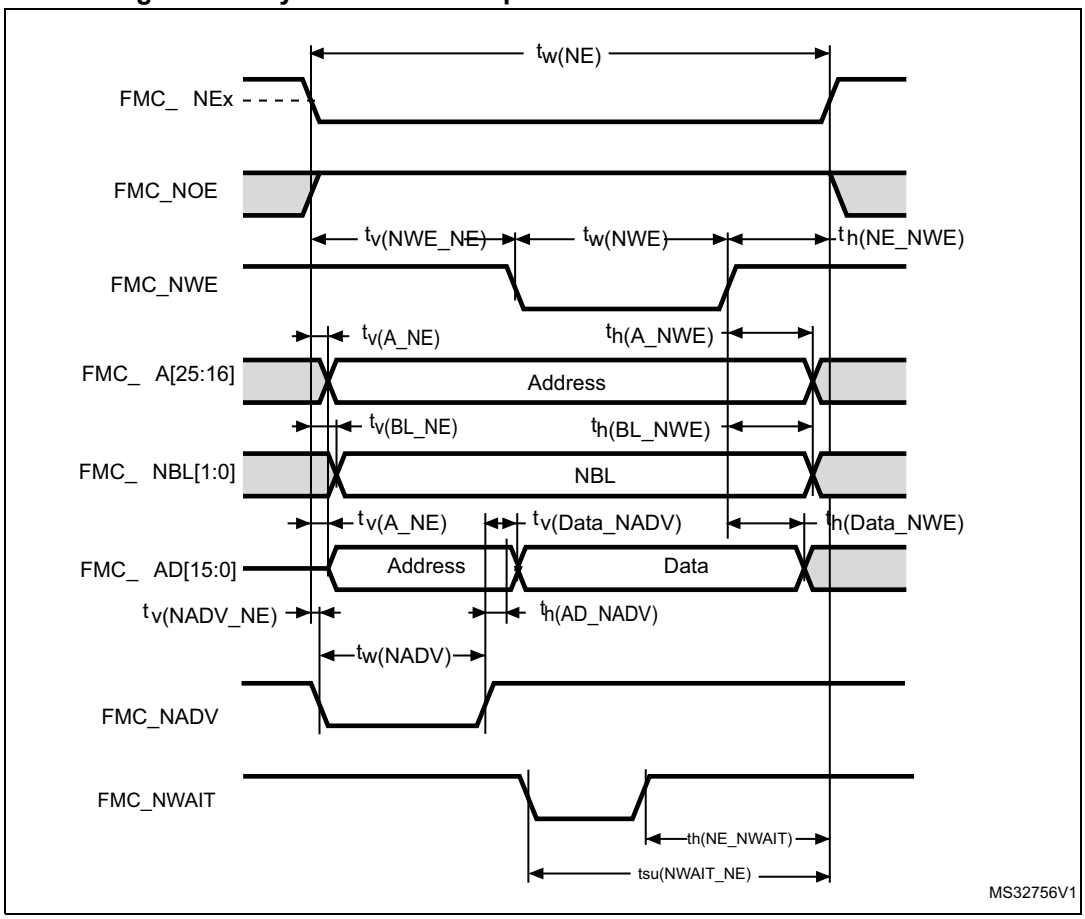


Table 111. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-1	$4T_{HCLK}$+1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-1	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	$2xT_{HCLK}$-0.5	$2xT_{HCLK}$+ 0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK}-0.5	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}	T_{HCLK}+1	
$t_{h(AD_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	T_{HCLK}+ 0.5	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK}+ 0.5	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK}- 0.5	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK} +3	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK} +0.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 112. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$- 1	$9T_{HCLK}$+ 1	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$- 0.5	$7T_{HCLK}$+ 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$+ 2	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$- 1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 53 through *Figure 56* represent synchronous waveforms and *Table 113* through *Table 116* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 53. Synchronous multiplexed NOR/PSRAM read timings

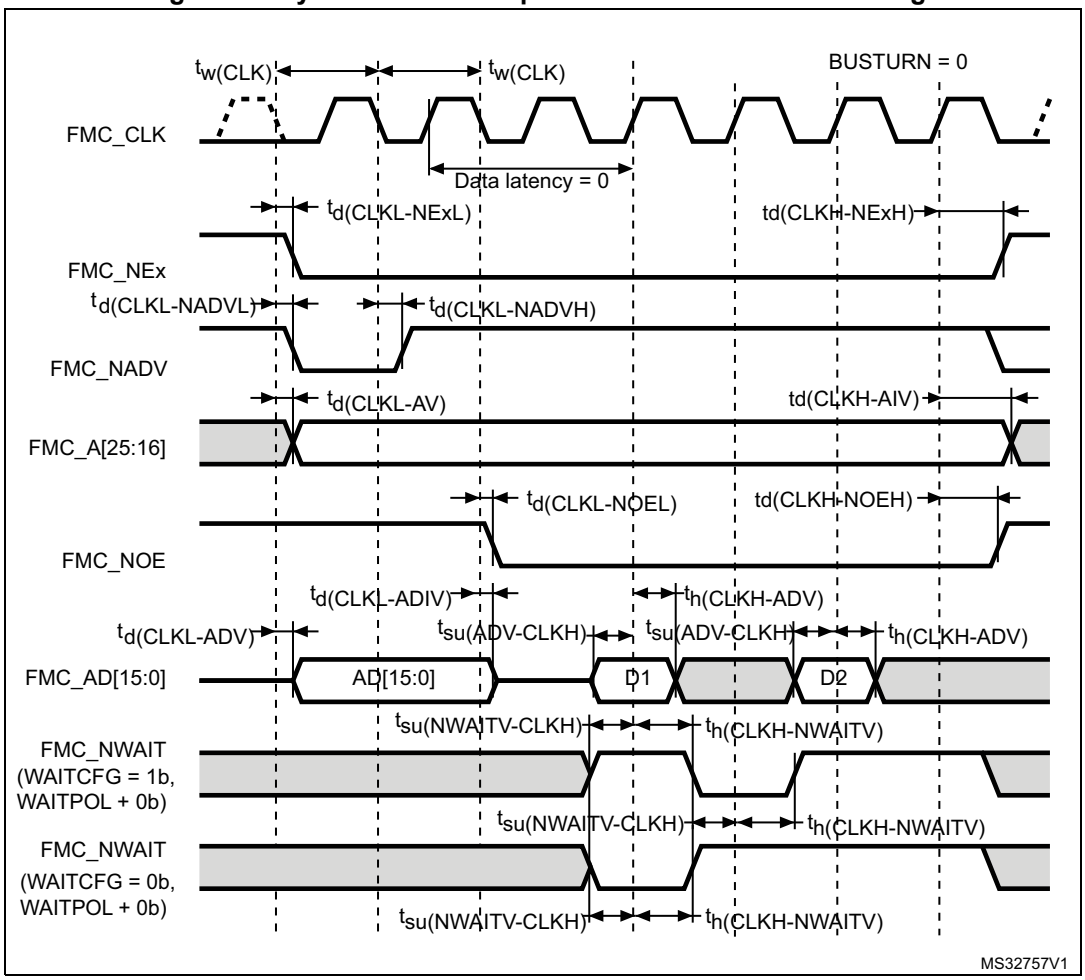


Table 113. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}+0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	1	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 54. Synchronous multiplexed PSRAM write timings

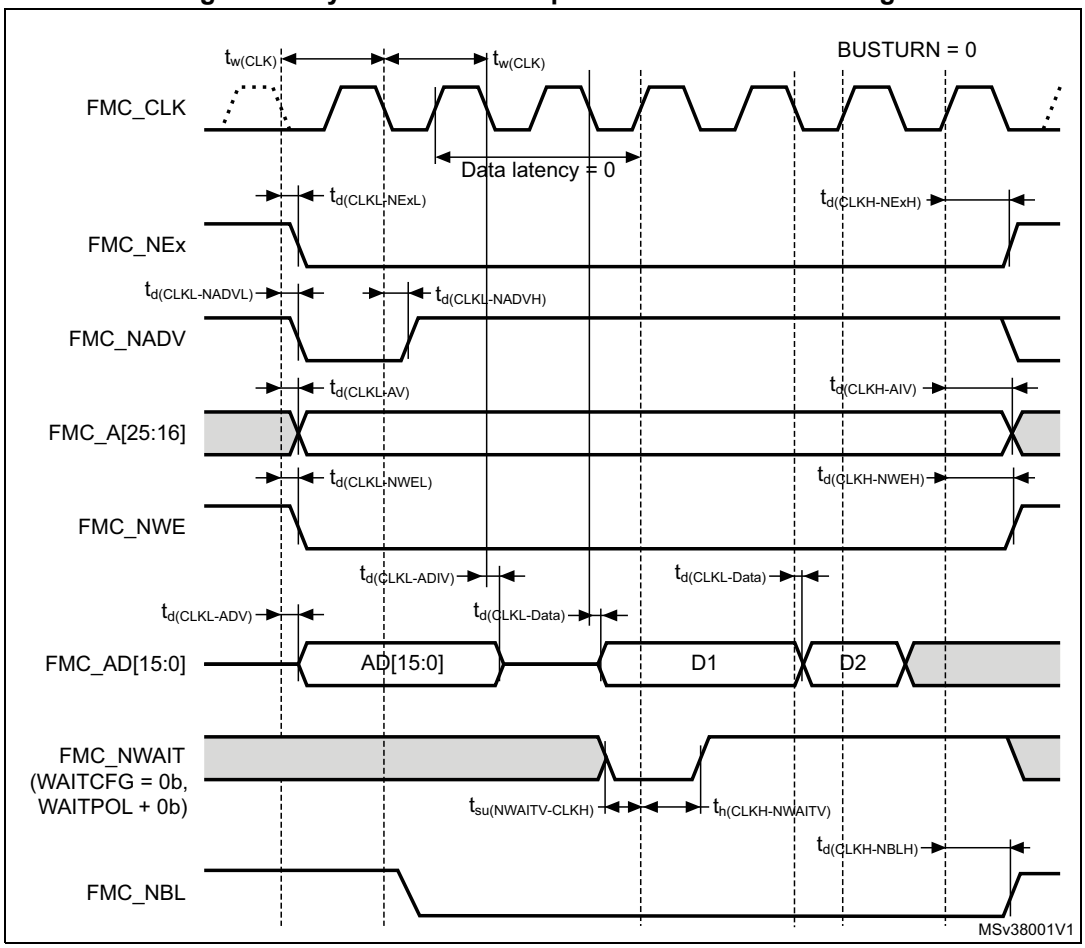


Table 114. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$- 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+ 0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+ 0.5	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	2	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+ 0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 55. Synchronous non-multiplexed NOR/PSRAM read timings

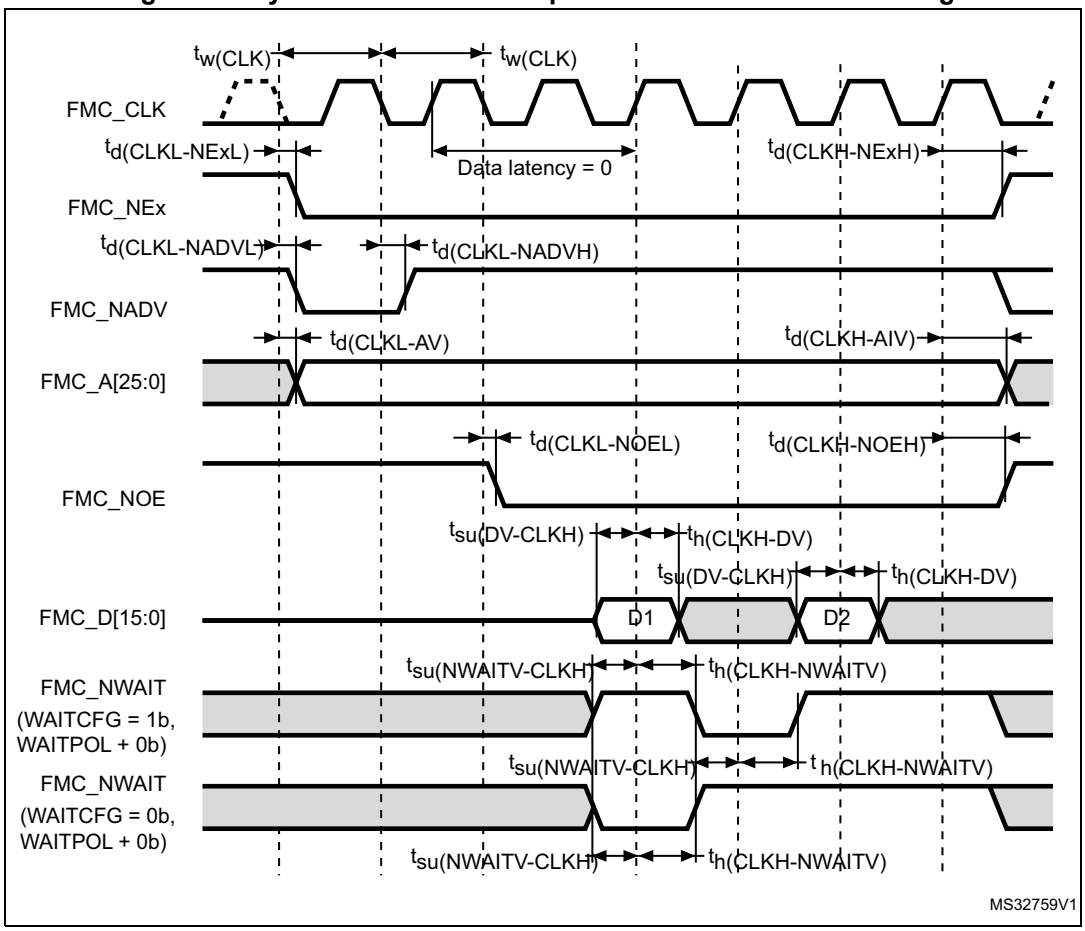


Table 115. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	T_{HCLK}-0.5	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	1	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	3.5	-	

Table 115. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 56. Synchronous non-multiplexed PSRAM write timings

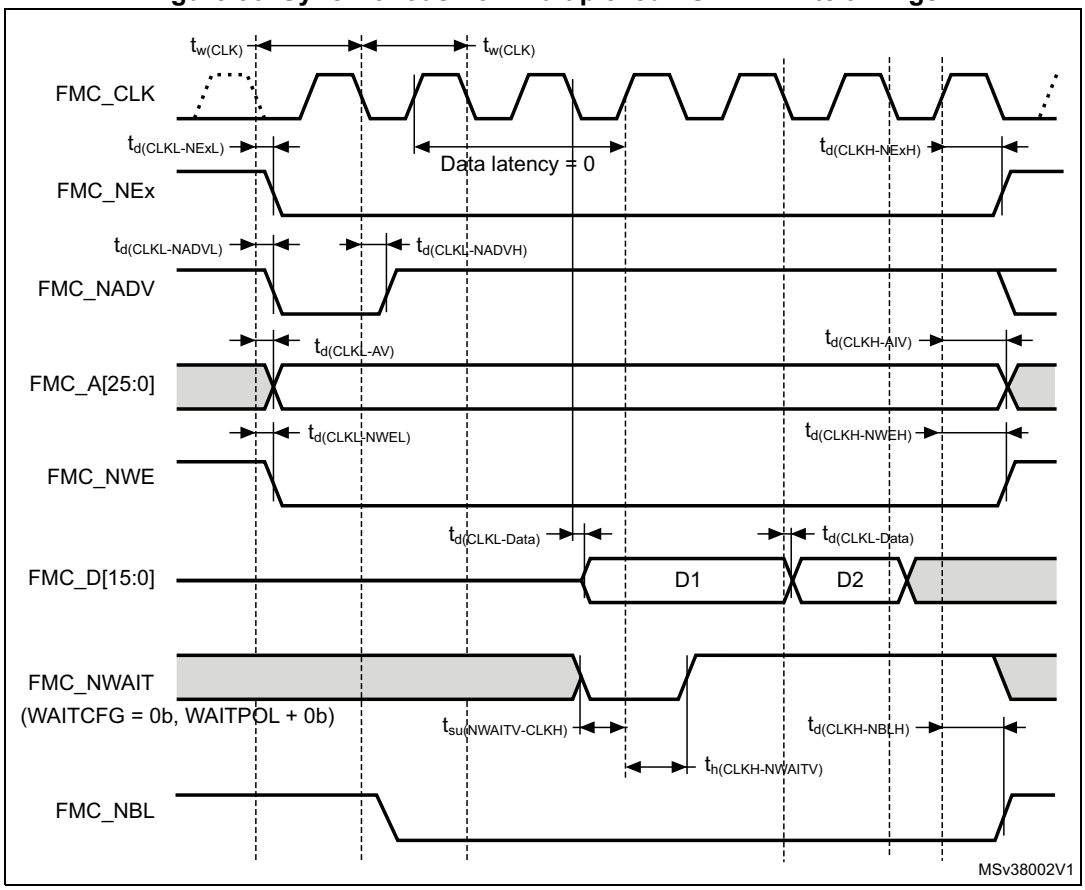


Table 116. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 57 through *Figure 60* represent synchronous waveforms, and *Table 117* and *Table 118* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 57. NAND controller waveforms for read access[a]

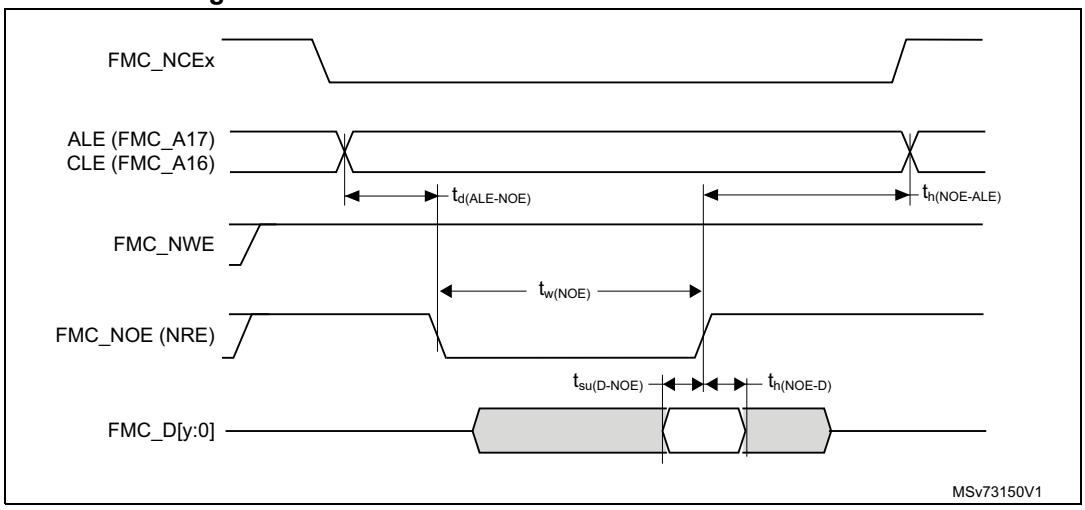
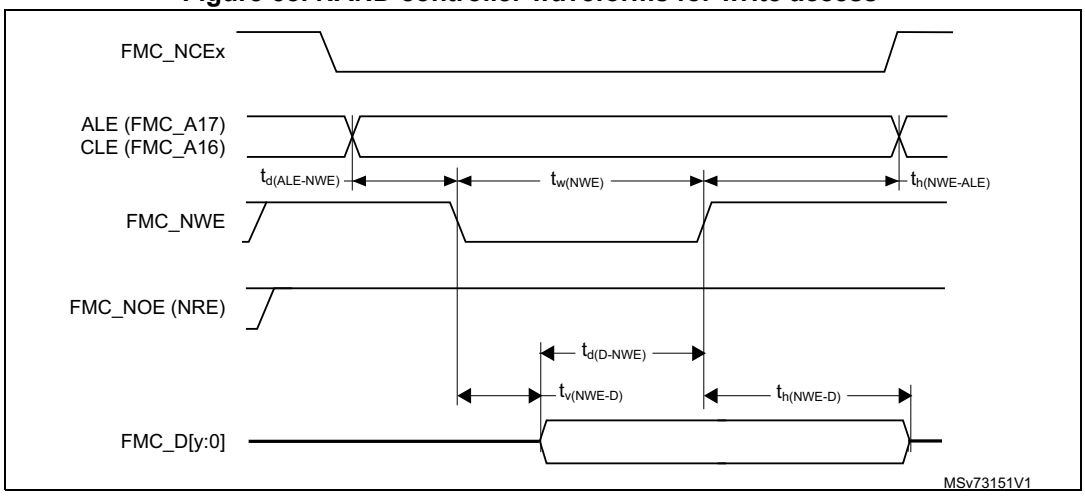


Figure 58. NAND controller waveforms for write access[a]



a. y=7 or 15 depending on NAND flash memory interface

Figure 59. NAND controller waveforms for common memory read access

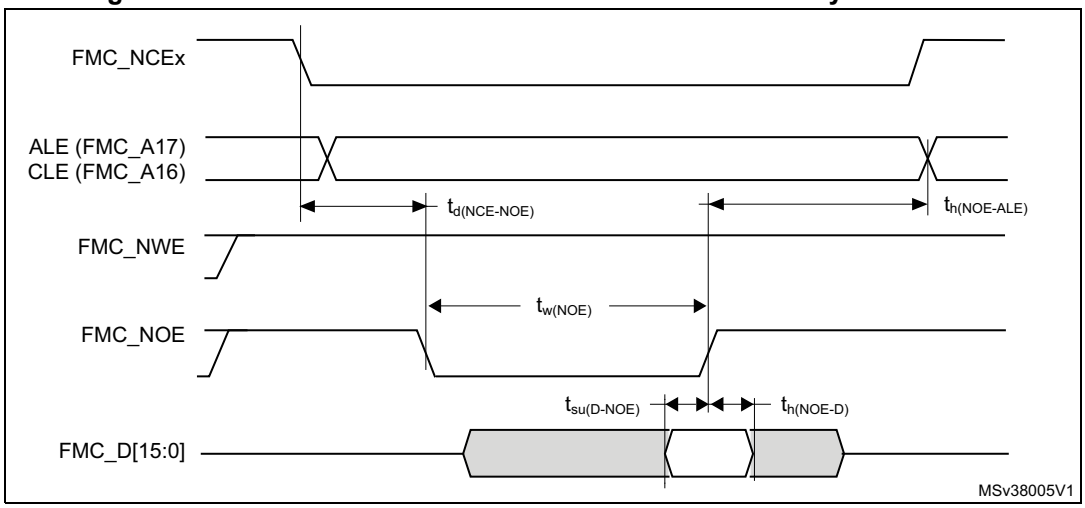


Figure 60. NAND controller waveforms for common memory write access

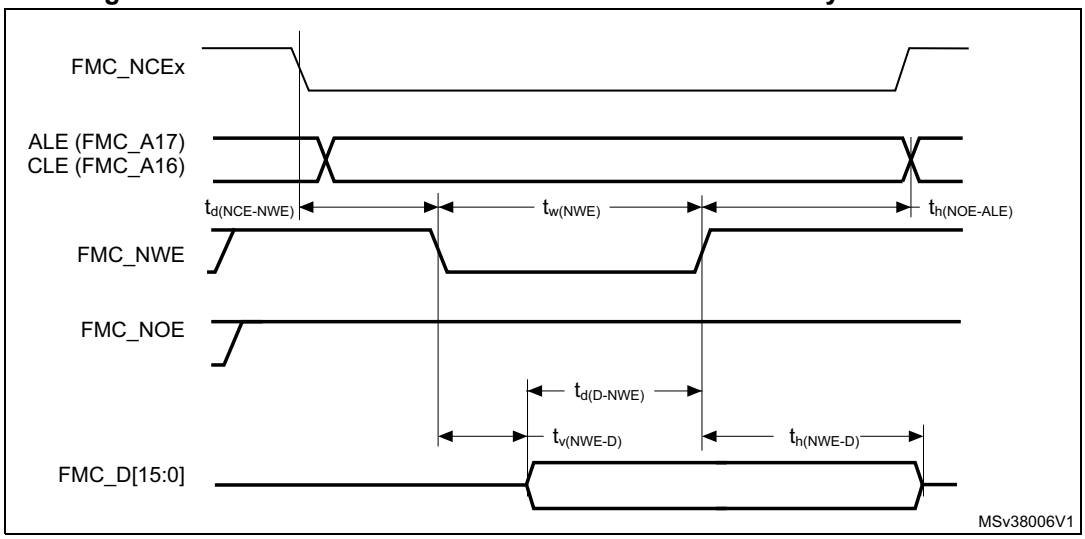


Table 117. Switching characteristics for NAND flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$4T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 118. Switching characteristics for NAND flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$+1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.30 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 119* for DCMI are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in *Table 21*, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data format: 14 bits
- Capacitive load C=30pF

Figure 61. DCMI timing diagram

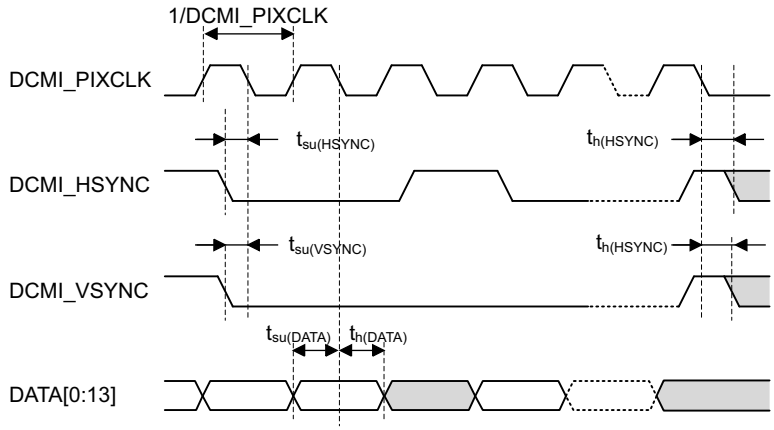


Table 119. DCMI characteristics(1)

Symbol	Parameter	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}	-	0.4	
DCMI_PIXCLK	Pixel clock input	-	32	MHz
D_{pixel}	Pixel clock input duty cycle	30	70	%

Table 119. DCMI characteristics(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(DATA)}$	Data input setup time	4	-	ns
$t_{h(DATA)}$	Data hold time	5	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input setup time	3	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	DCMI_HSYNC/DCMI_VSYNC input hold time	3	-	

1. Data based on characterization results, not tested in production.

6.3.31 SWPMI characteristics

The Single Wire Protocol Master Interface (SWPMI) and the associated SWPMI_IO transceiver are compliant with the ETSI TS 102 613 technical specification.

Table 120. SWPMI electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SWPSTART}$	SWPMI regulator startup time	SWP Class B 2.7 V ≤ V_{DD} ≤ 3,3V	-	-	300	µs
t_{SWPBIT}	SWP bit duration	V_{CORE} voltage range 1	500	-	-	ns
		V_{CORE} voltage range 2	620	-	-	

6.3.32 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 121* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Figure 62. SDIO high-speed mode

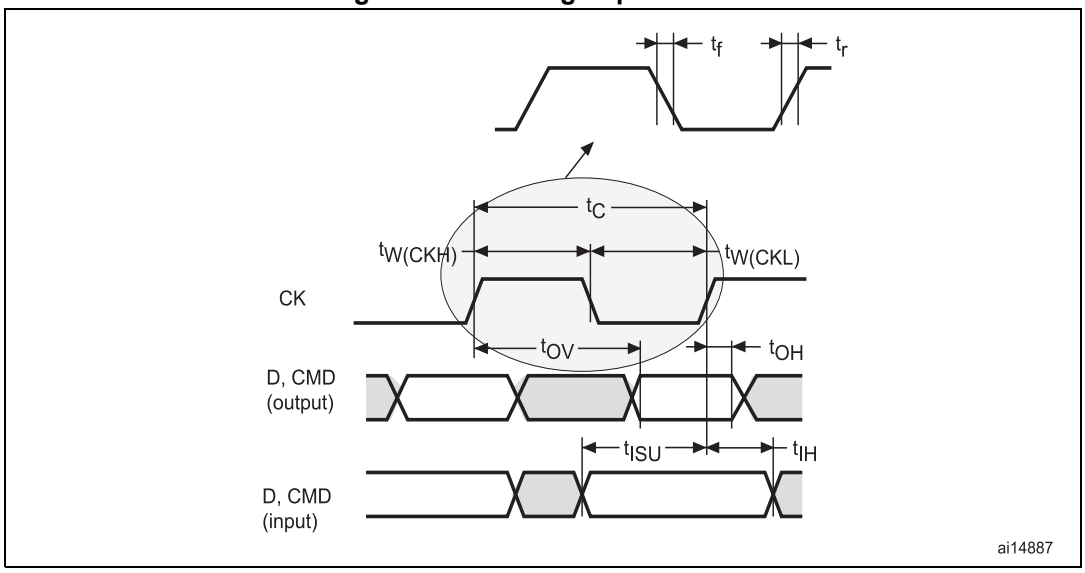


Figure 63. SD default mode

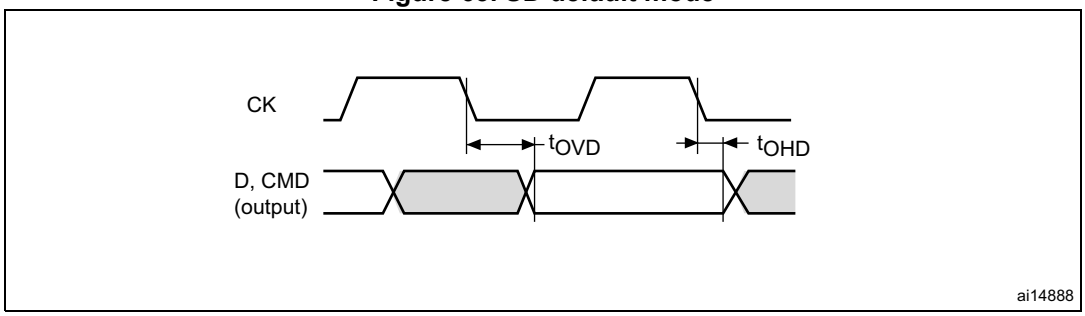


Table 121. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode		0		50	MHz
-	SDIO_CK/fPCLK2 frequency ratio		-	-	4/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	8	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	12	13	ns
t_{OH}	Output hold time HS	fpp =50 MHz	10	-	-	

Table 121. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp =25 MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	fpp =25 MHz	3	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =25 MHz	-	3	5	ns
t_{OHD}	Output hold default time SD	fpp =25 MHz	0	-	-	

1. Guaranteed by characterization results.

Table 122. SD / MMC dynamic characteristics, V_{DD}=1.71 V to 1.9 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	16.5	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 50 MHz	2	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 50 MHz	4.5	-	-	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 50 MHz	-	4.5	5	ns
t_{OHD}	Output hold default time SD	f_{PP} = 50 MHz	0	-	-	ns

1. Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

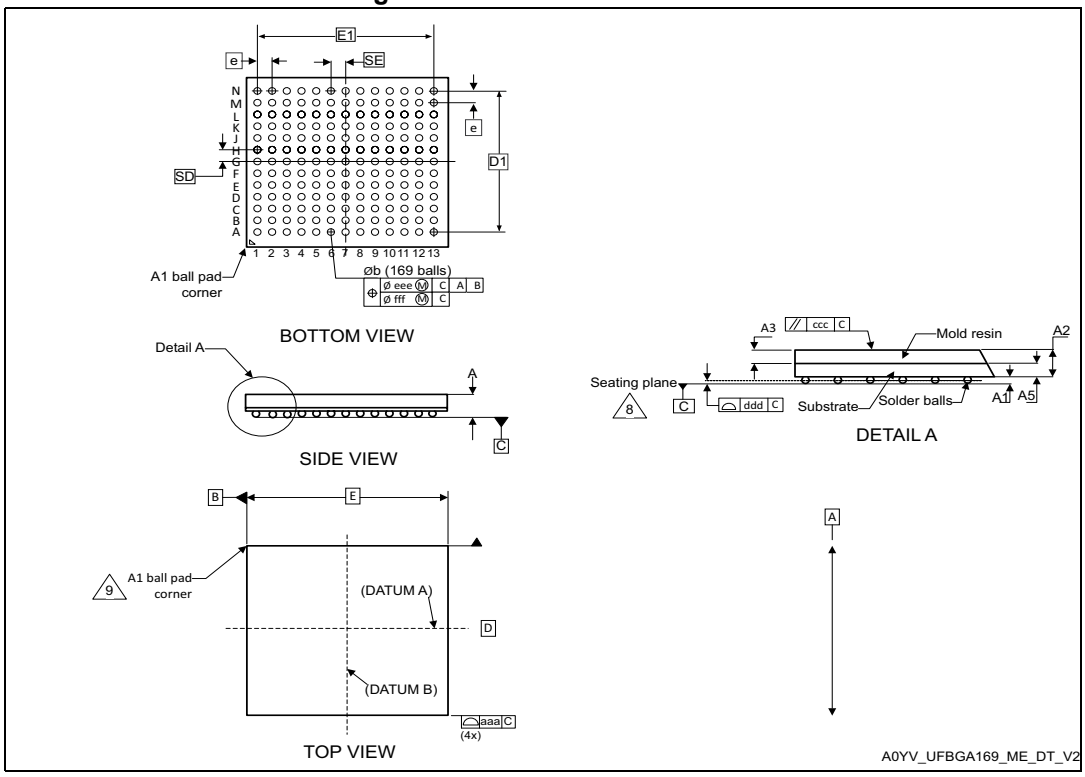
Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

7.2 UFBGA169 package information (A0YV)

This UFBGA is a 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 64. UFBGA169 - Outline



1. Drawing is not to scale.

Table 123. UFBGA169 - Mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217

Table 123. UFBGA169 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 65. UFBGA169 - Recommended footprint

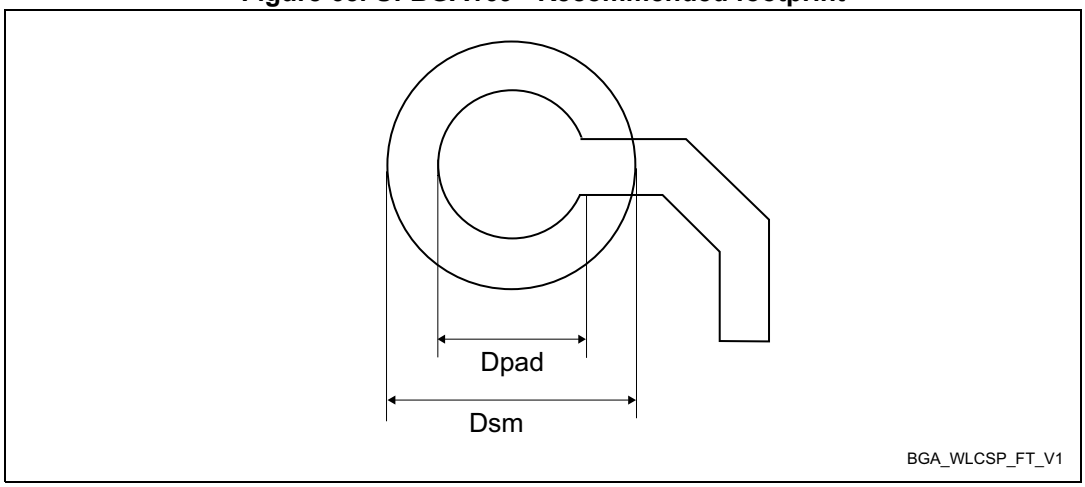


Table 124. UFBGA169 - Recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

7.3 LQFP144 package information (1A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 66. LQFP144 - Outline(15)

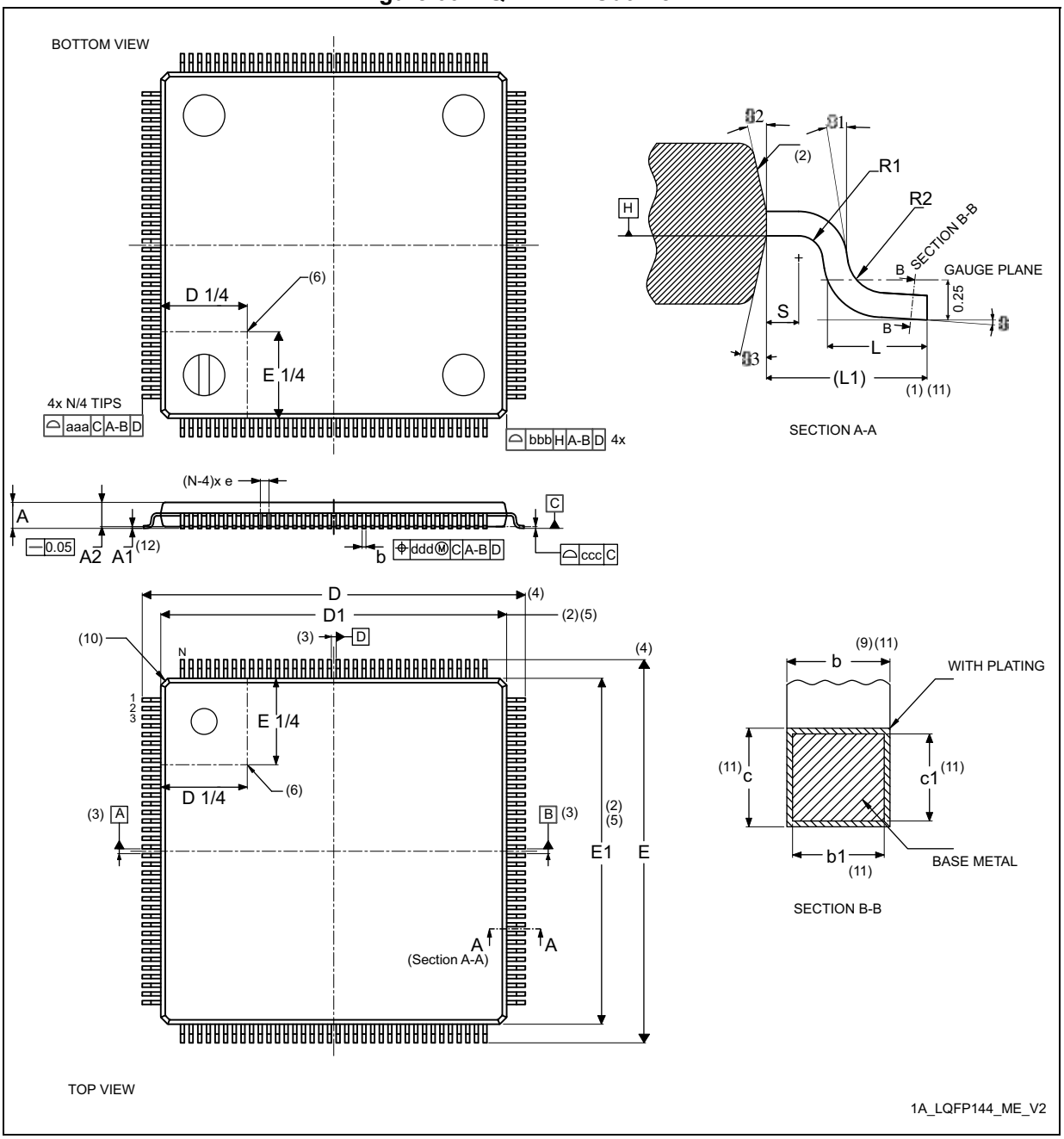


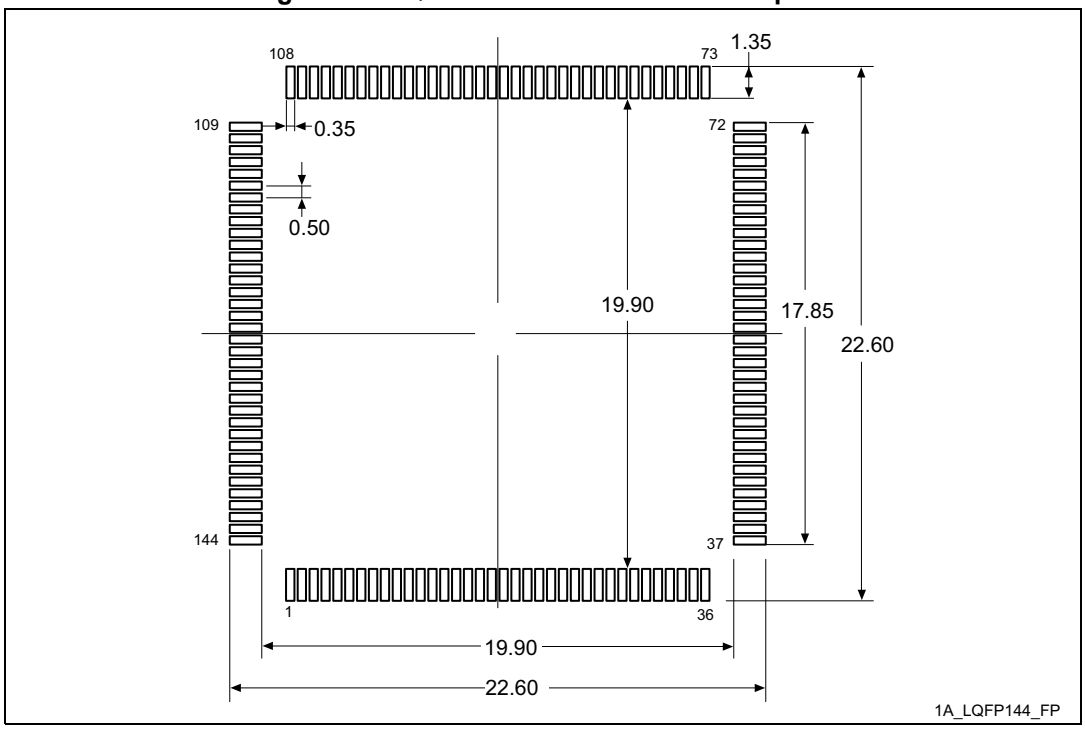
Table 125. LQFP144 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	22.00 BSC			0.8661 BSC		
D1[2][5]	20.00 BSC			0.7874 BSC		
E[4]	22.00 BSC			0.8661 BSC		
E1[2][5]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	144					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 67. LQFP144 - Recommended footprint

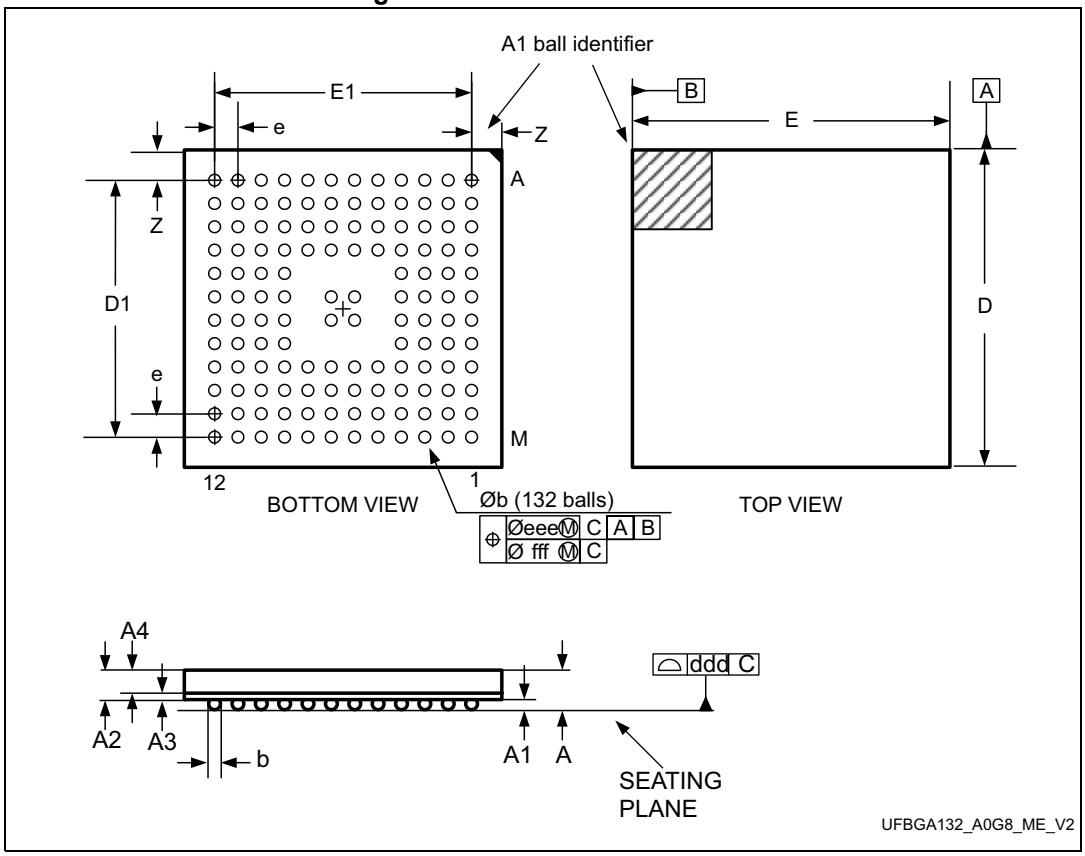


1. Dimensions are expressed in millimeters.
2. L496xG

7.4 UFBGA132 package information (A0G8)

This UFBGA is a 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package

Figure 68. UFBGA132 - Outline



1. Drawing is not to scale.

Table 126. UFBGA132 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

Table 126. UFBGA132 - Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 69. UFBGA132 - Recommended footprint

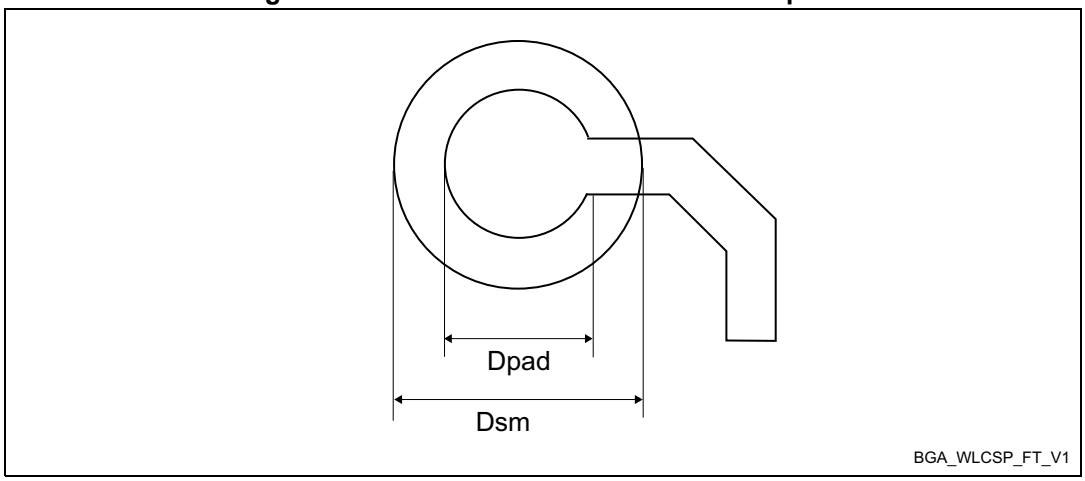


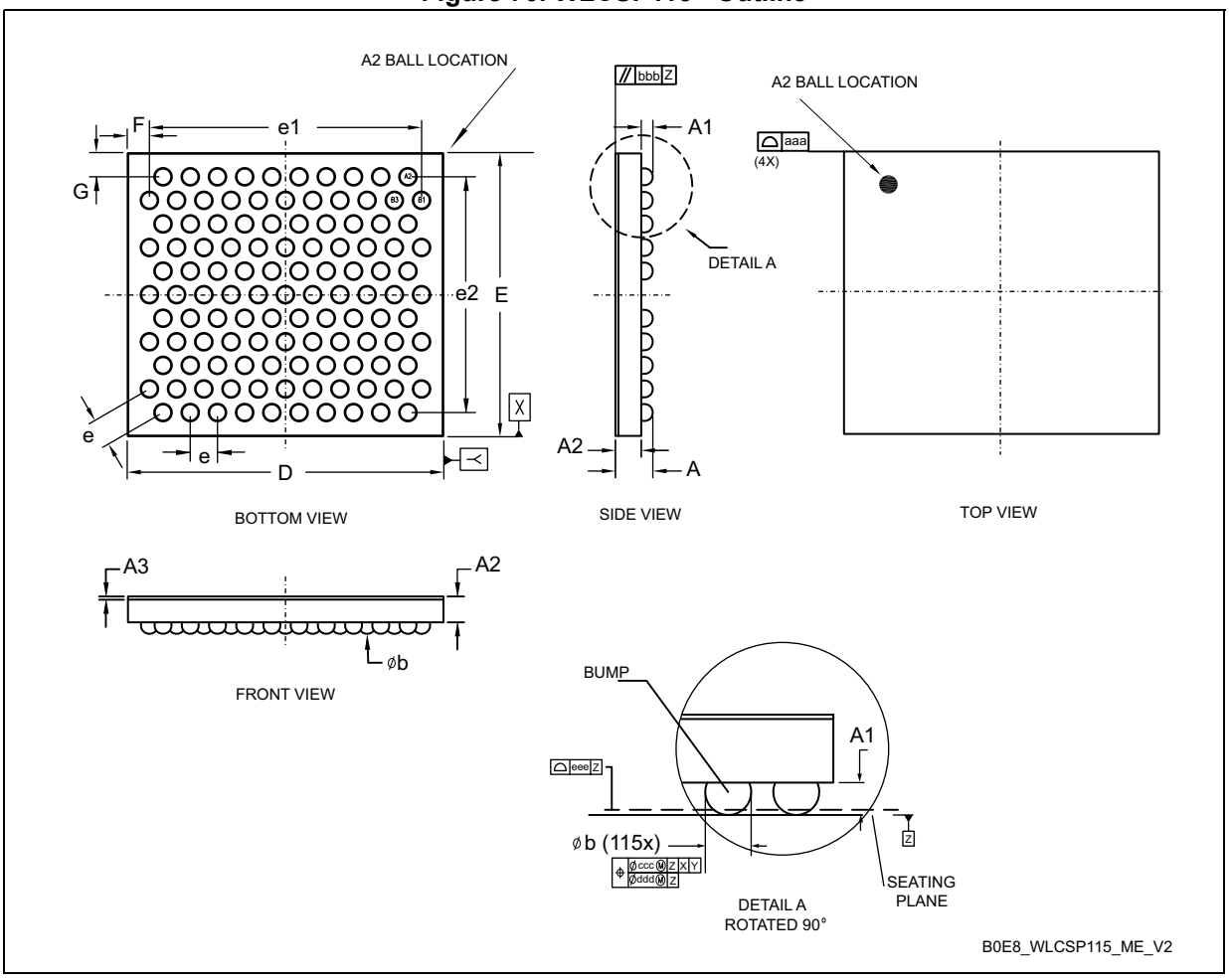
Table 127. UFBGA132 - Recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm
Ball diameter	0.280 mm

7.5 WLCSP115 package information (B0E8)

This WLCSP is a 115 ball, 4.63 x 4.15 mm, 0.4 mm pitch, wafer level chip scale package.

Figure 70. WLCSP115 - Outline



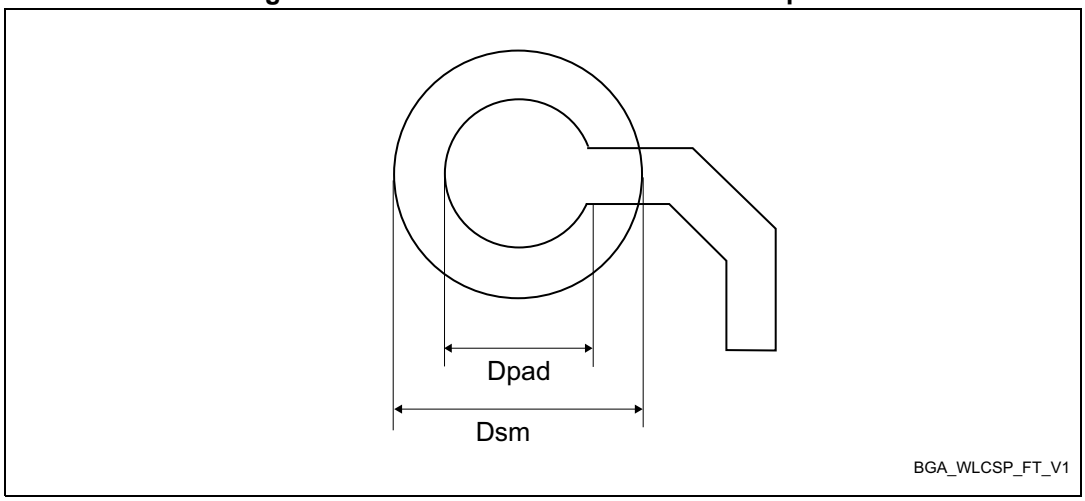
1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

Table 128. WLCSP115 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3[3]	-	0.025	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	4.61	4.63	4.65	0.181	0.182	0.183
E	4.13	4.15	4.17	0.163	0.163	0.164
e	-	0.40	-	-	0.016	-
e1	-	4.00	-	-	0.157	-
e2	-	3.46	-	-	0.136	-
F[4]	-	0.315	-	-	0.012	-
G[4]	-	0.343	-	-	0.014	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc[5]	-	-	0.10	-	-	0.004
ddd[6]	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Calculated dimensions are rounded to the 3rd decimal place
5. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone
6. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones

Figure 71. WLCSP115 - Recommended footprint



1. Dimensions are expressed in millimeters.

Table 129. WLCSP115 - recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

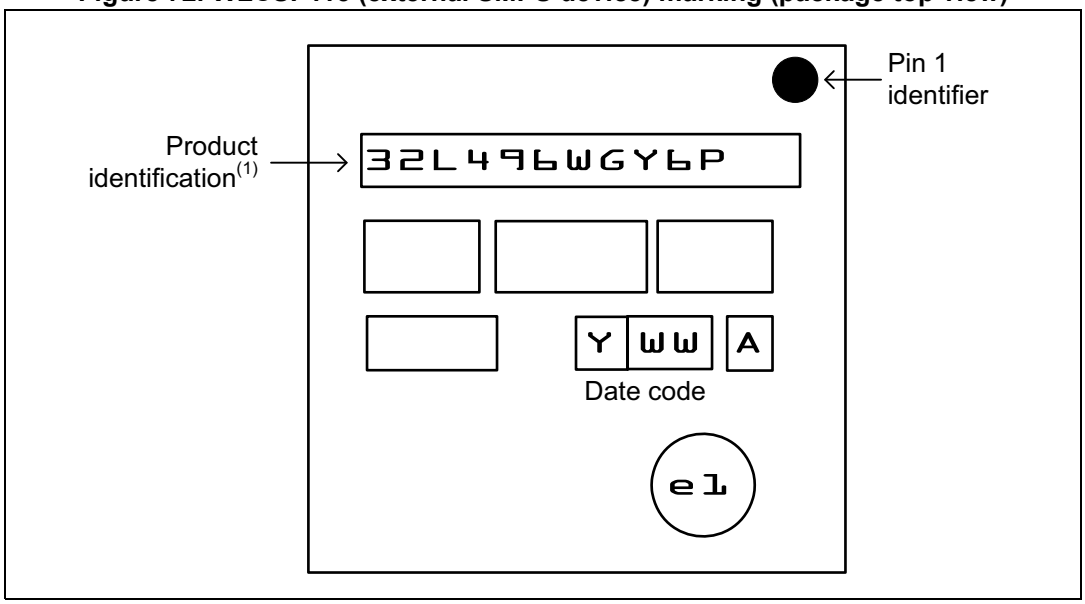
Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 72. WLCSP115 (external SMPS device) marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 LQFP100 package information (1L)

This LQFP is 100 lead, 14 x 14 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 73. LQFP100 - Outline(15)

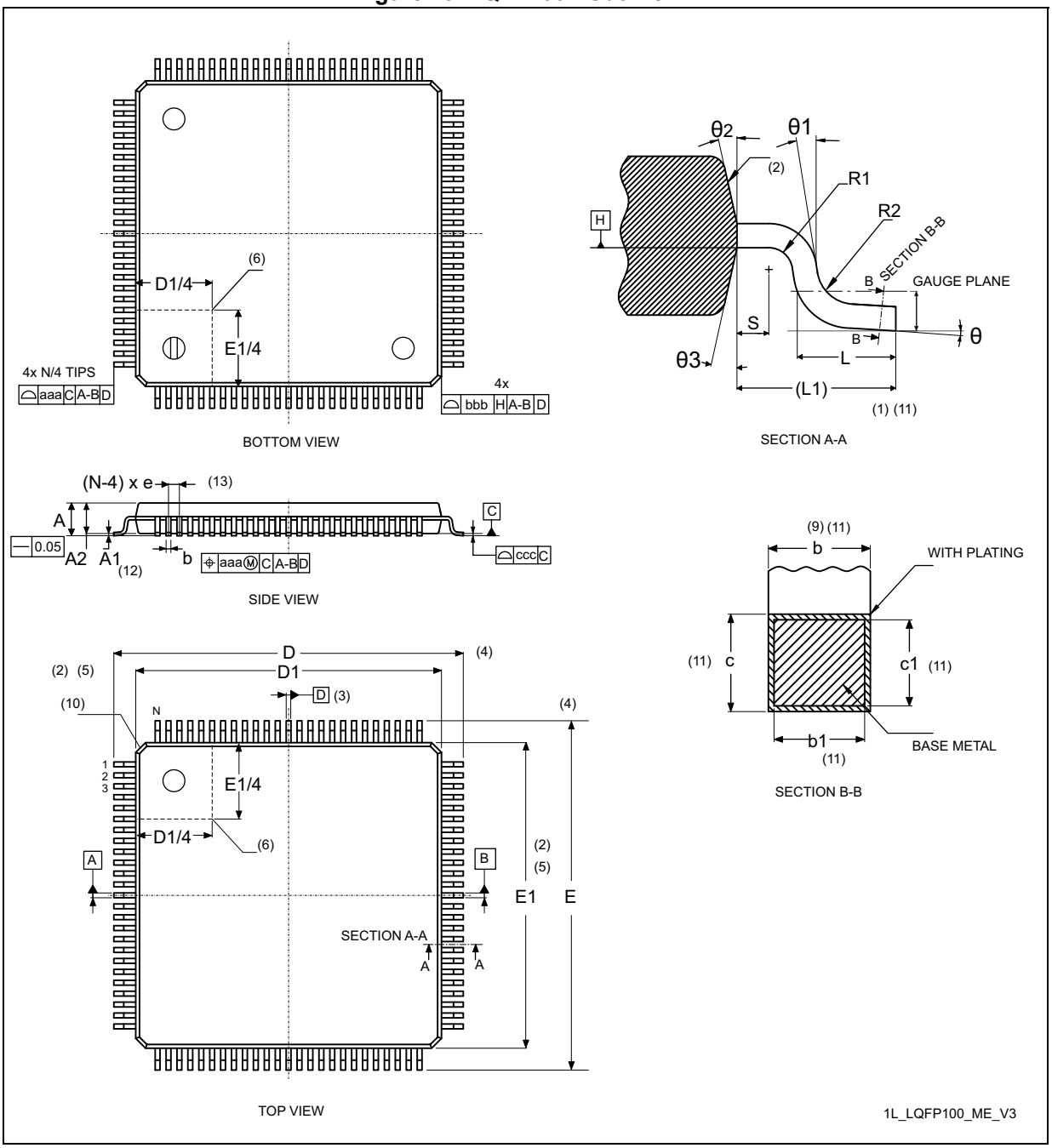


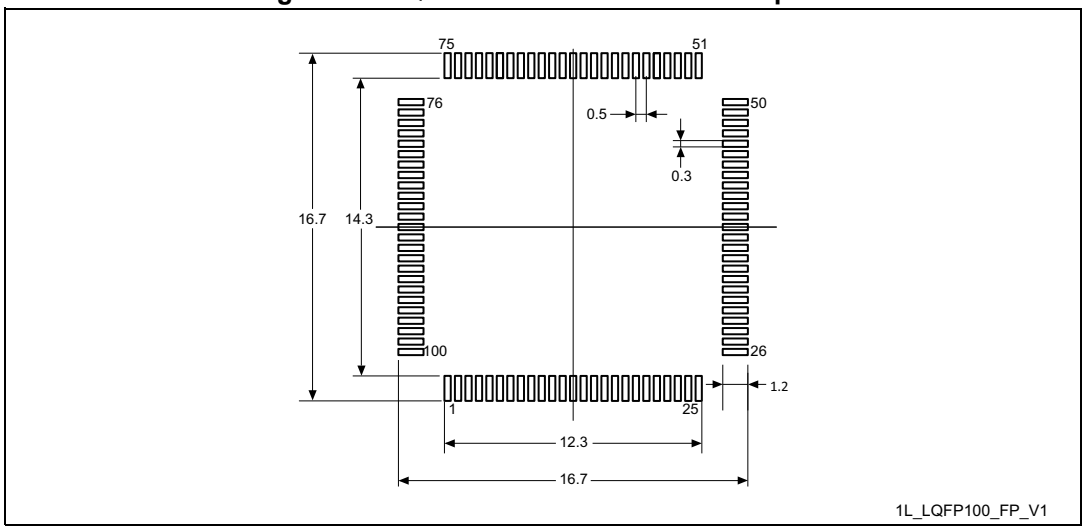
Table 130. LQFP100 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12]	0.05	-	0.15	0.0019	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	16.00			0.6299		
D1[2][5]	14.00			0.5512		
E[4]	16.00			0.6299		
E1[2][5]	14.00			0.5512		
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.177	0.0236	0.0295
L1[1][11]	1.00			-	0.0394	-
N	100					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

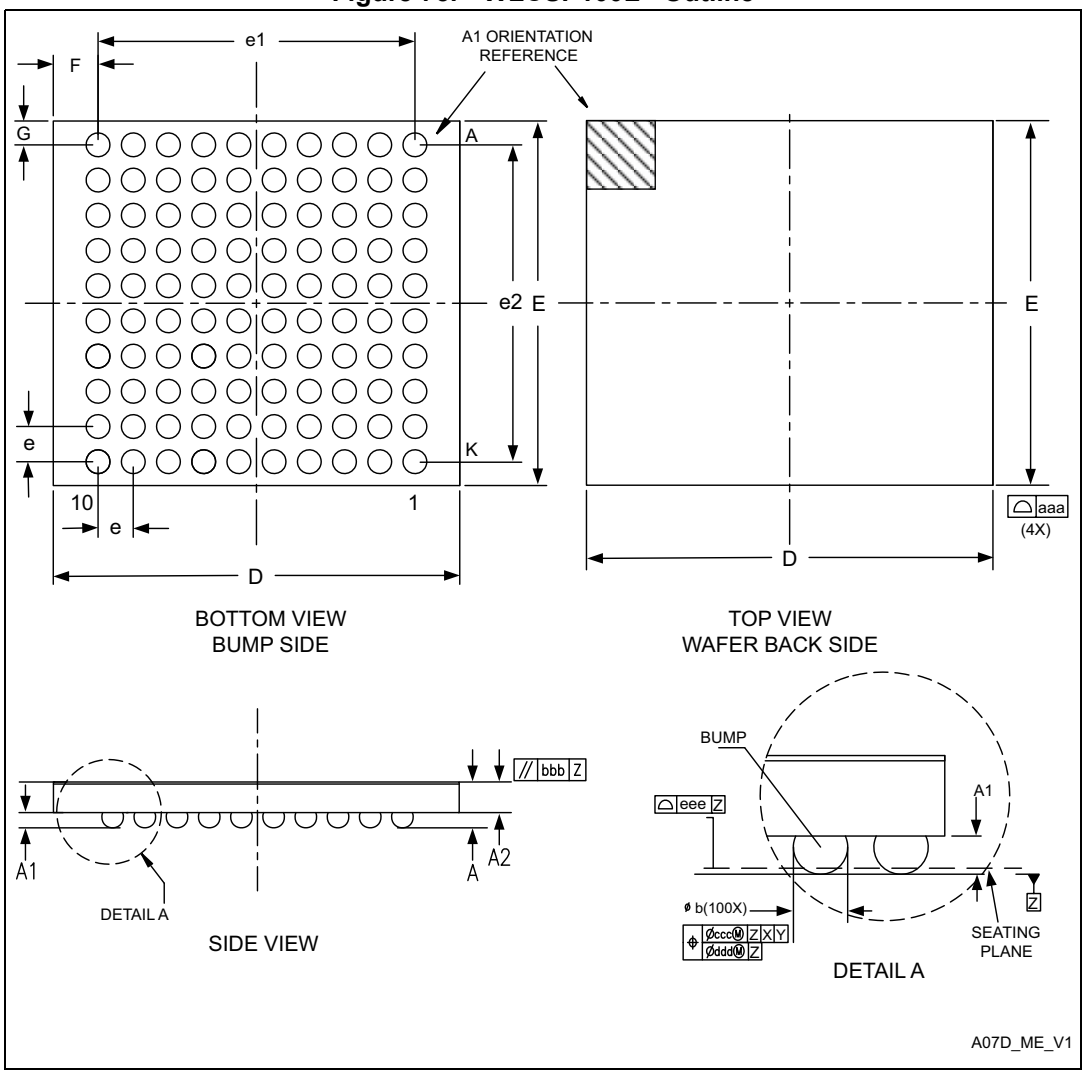
Figure 74. LQFP100 - Recommended footprint



7.7 WLCSP100L package information (A07D)

This WLCSP is a 100 ball 4.618 x 4.142 mm, 0.4 mm pitch wafer level chip scale package.

Figure 75. WLCSP100L - Outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 131. WLCSP100L - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
Ø b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.583	4.618	4.653	0.1804	0.1818	0.1832
E	4.107	4.142	4.177	0.1617	0.1631	0.1644
e	-	0.400	-	-	0.0157	-
e1	-	3.600	-	-	0.1417	-
e2	-	3.600	-	-	0.1417	-
F	-	0.509	-	-	0.0200	-
G	-	0.271	-	-	0.0107	-
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 76. WLCSP100L - Recommended footprint

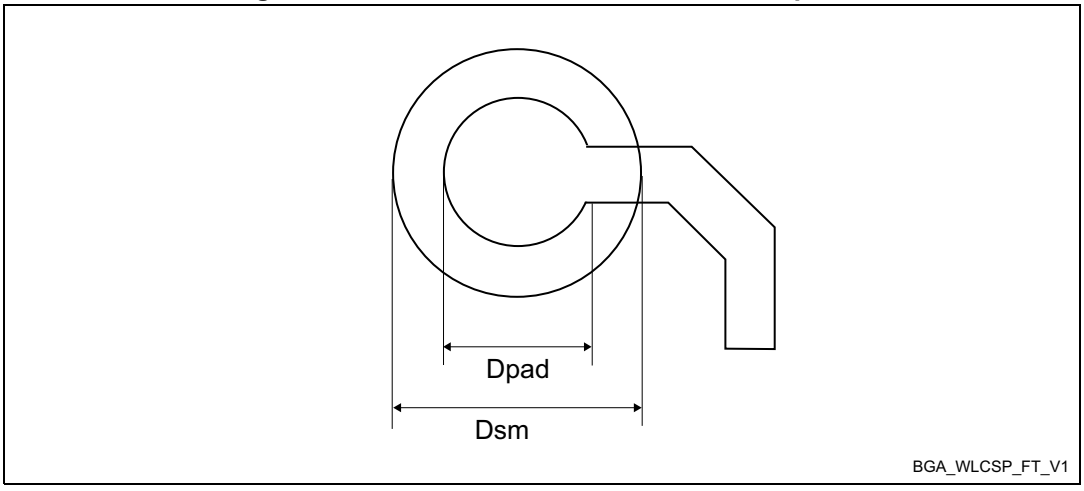


Table 132. WLCSP100L - Recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

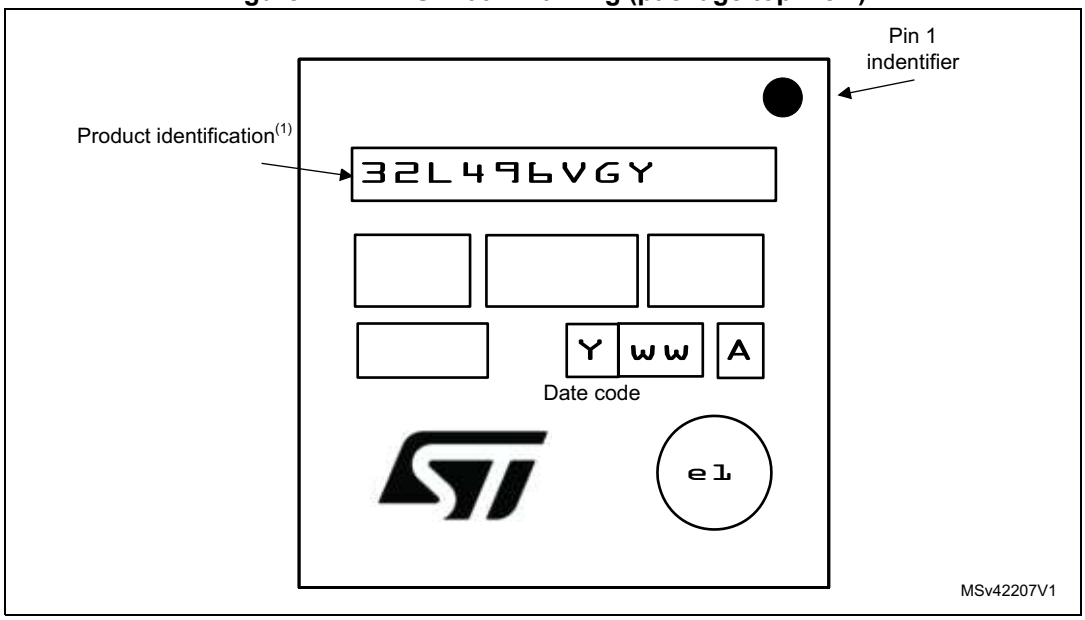
Device marking

The following figures give examples of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

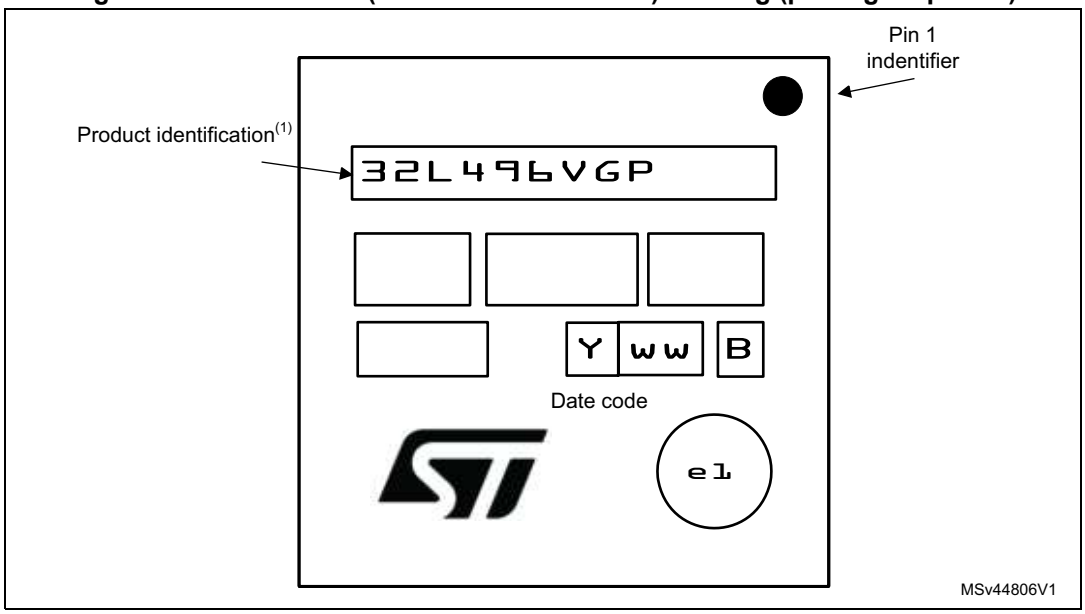
Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 77. WLCSP100L marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Figure 78. WLCSP100L (external SMPS device) marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.
2. SMPS package version only available for 1 MB flash devices STM32L496xG

7.8 LQFP64 package information (5W)

This LQFP is 64-pin, 10 x 10 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Figure 79. LQFP64 - Outline(15)

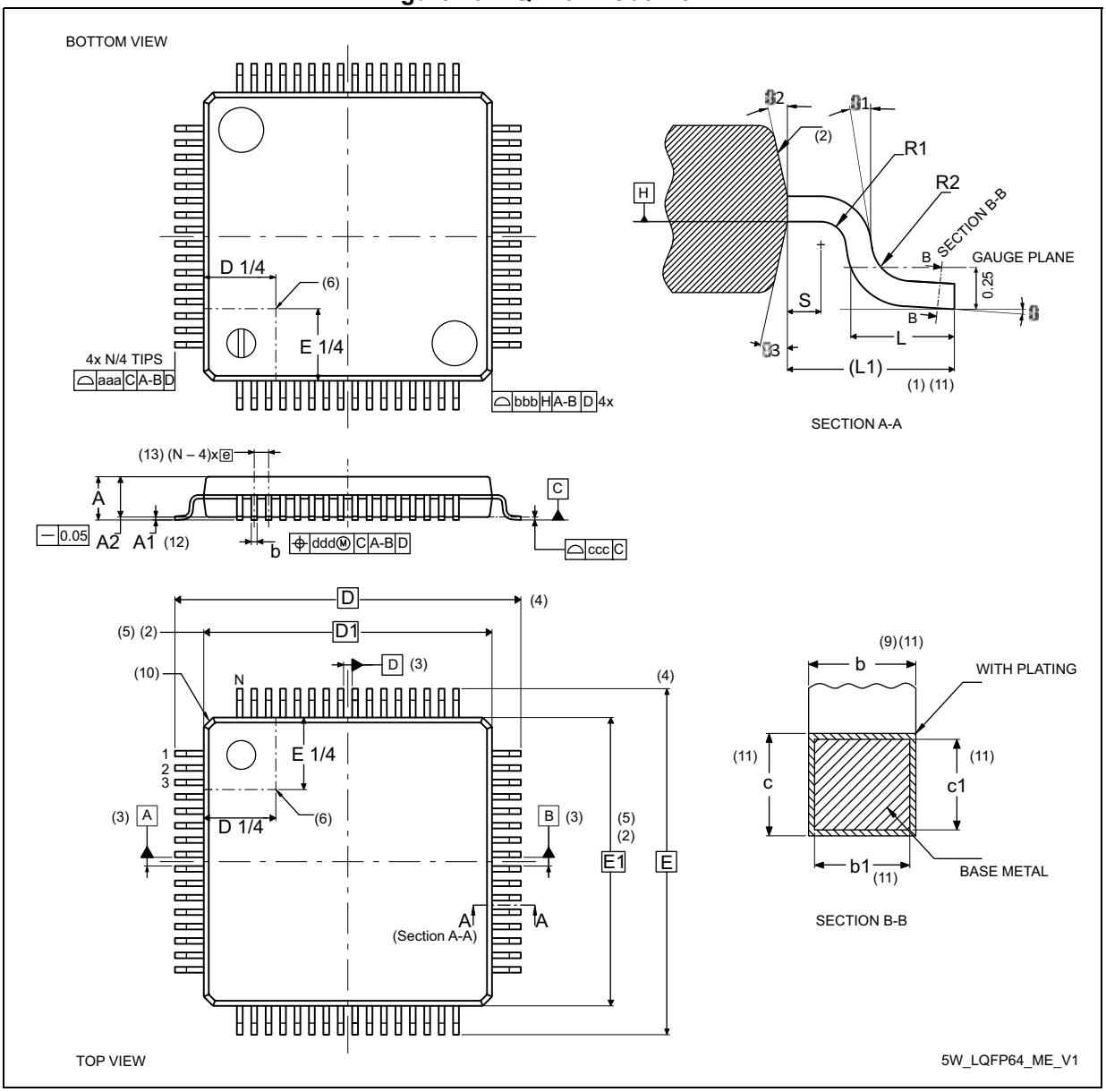


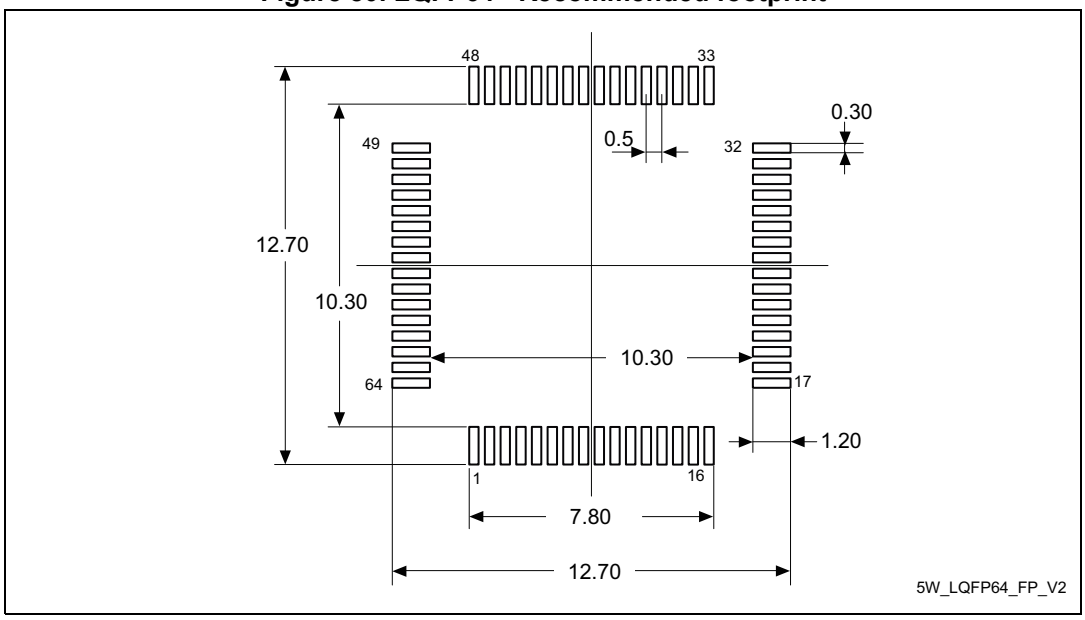
Table 133. LQFP64 - Mechanical data

Symbol	millimeters			inches[14]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0570
b[9][11]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[11]	0.09	-	0.20	0.0035	-	0.0079
c1[11]	0.09	-	0.16	0.0035	-	0.0063
D[4]	12.00 BSC			0.4724 BSC		
D1[2][5]	10.00 BSC			0.3937 BSC		
E[4]	12.00 BSC			0.4724 BSC		
E1[2][5]	10.00 BSC			0.3937 BSC		
e	0.50 BSC			0.1970 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	64					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1]	0.20			0.0079		
bbb[1]	0.20			0.0079		
ccc[1]	0.08			0.0031		
ddd[1]	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 80. LQFP64 - Recommended footprint



1. Dimensions are expressed in millimeters.

7.9 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of all I_{DDXXX} and V_{DDXXX}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 134. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA169 - 7 × 7 mm	52	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm	32	
	Thermal resistance junction-ambient UFBGA132 - 7 × 7 mm	55	
	Thermal resistance junction-ambient WLCSP100L	35.8	
	Thermal resistance junction-ambient LQFP100 - 14 × 14mm	42	
	Thermal resistance junction-ambient LQFP64	45	

7.9.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.9.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32L496xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V = 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 134* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} user can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 3).

Suffix 6: T_{Amax} = T_{Jmax} - (42 °C/W × 447 mW) = 105 - 18.774 = 86.226 °C

Suffix 3: T_{Amax} = T_{Jmax} - (42 °C/W × 447 mW) = 130 - 18.774 = 111.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V

P_{INTmax} = 20 mA × 3.5 V = 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 134* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 8: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

8 Ordering information

Table 135. STM32L496xx ordering information scheme

Example: STM32 L 496 V G T 6 P TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

496 = STM32L496xx

Pin count

R = 64 pins
V = 100 pins
W = 115 pins
Q = 132 pins
Z = 144 pins
A = 169 pins

Flash memory size

G = 1 MByte of flash memory
E = 512 KByte of flash memory

Package

T = LQFP ECOPACK2
I = UFBGA ECOPACK2
Y = CSP ECOPACK2

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)
3 = Industrial temperature range, -40 to 125 °C (130 °C junction)

Option

Blank = Standard production with integrated LDO
P = Dedicated pinout supporting external SMPS
S = New sawing
PS = Dedicated pinout supporting external SMPS and PFAS-free
SC = Dedicated product with integrated LDO, new sawing process, and copper wiring

Packing

TR = Tape and reel (Blank, P or S options)

Table 135. STM32L496xx ordering information scheme (continued)

T = tape and reel (PS or SC options)

xxx = programmed parts

For a list of available options (such as speed, package) or for further information on any aspect of this device contact the nearest ST sales office.

9 Important security notice

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10 Revision history

Table 136. Document revision history

Date	Revision	Changes
22-Feb-2017	1	Initial release.
02-May-2017	2	Updated: – *Features* in cover page, *Section 2: Description*, *Section 6.1.7: Current consumption measurement*, *Section 6.3.18: Analog-to-Digital converter characteristics*, *Section 7.9: Thermal characteristics*, *Section 7.9.2: Selecting the product temperature range* – *Table 2: STM32L496xx family device features and peripheral counts*, *Table 22: General operating conditions*, *Table 44: Current consumption in Stop 2 mode*, *Table 45: Current consumption in Stop 1 mode*, *Table 47: Current consumption in Standby mode*, *Table 48: Current consumption in Shutdown mode*, *Table 51: Low-power mode wakeup timings*, *Table 61: LSI oscillator characteristics*, *Table 82: DAC characteristics*, *Table 135: STM32L496xx ordering information scheme* – note *1.* on *Figure 37*
21-Jun-2017	3	Added note on: *Figure 66: UFBGA169 marking (package top view)*, *Figure 71: LQFP144 (external SMPS device) marking (package top view)*, *Figure 78: WLCSP100L (external SMPS device) marking (package top view)*. Updated *Table 70: I/O static characteristics*. Updated product maturity information from “preliminary data” to “production data”.
04-Jul-2017	4	Updated *Section 3.38: Universal serial bus on-the-go full-speed (OTG_FS)*.
18-Dec-2017	5	Updated *Features*, *Section 3.12: Clocks and startup*, *Table 15: STM32L496xx pin definitions*, *Table 66: EMI characteristics for fHSE = 8 MHz and fHCLK = 80 MHz*, *Table 53: Wakeup time using USART/LPUART*, *Table 70: I/O static characteristics*, *Table 76: ADC characteristics*. Added *Figure 12: STM32L496Qx, external SMPS device, UFBGA132 ballout*(1)(2), *Section 6.3.16: Extended interrupt and event controller input (EXTI) characteristics*, *USB OTG full speed (FS) characteristics*, *Figure 75: UFBGA132 (external SMPS device) marking (package top view)*.
10-Jan-2018	6	Updated *Table 15: STM32L496xx pin definitions*.
14-Feb-2018	7	Updated *Table 8: Temperature sensor calibration values*
15-May-2018	8	Updated: *Figure 1: STM32L496xx block diagram*, *Figure 5: Clock tree*, *Section 3.10.1: Power supply schemes*, *Table 5: Functionalities depending on the working mode*, *Table 19: Voltage characteristics*, *Table 18: STM32L496xx memory map and peripheral register boundary addresses*, *Section 3.17: Analog to digital converter (ADC)*, *Section 6.3.2: Operating conditions at power-up / power-down*, *Table 82: DAC characteristics*, *Table 86: OPAMP characteristics*. Added: *Figure 4: Power-up/down sequence*.
16-Jul-2018	9	Updated *Figure 16: STM32L496Vx WLCSP100L pinout*(1)(2), *Figure 17: STM32L496Vx, external SMPS device, WLCSP100L pinout*(1)(2), *Table 15: STM32L496xx pin definitions*, *Figure 69: UFBGA132 - Recommended footprint*, *Figure 76: WLCSP100L - Recommended footprint*.

Table 136. Document revision history (continued)

Date	Revision	Changes
25-Sep-2018	10	Updated *Section 3.40: Flexible static memory controller (FSMC)*, *Table 15: STM32L496xx pin definitions*, *Table 16: Alternate function AF0 to AF7*. Added *Figure 15: STM32L496Vx, external SMPS device, LQFP100 pinout*(1), *Figure 19: STM32L496Rx, external SMPS, LQFP64 pinout*(1), *Figure 82: LQFP100 (external SMPS device) marking (package top view)*, *Figure 7.9: Thermal characteristics*.
20-Jan-2020	11	Updated *Table 19: Voltage characteristics* and *Table 135: STM32L496xx ordering information scheme*.
19-Jan-2021	12	Updated document title and image on cover page. Updated *Features*, *Section 2: Description*, *Section 3.8: Boot modes*, *Section 3.25: True random number generator (RNG)*, *Section 6.3.14: I/O port characteristics* and *Section 8: Ordering information*. Added *Note:* in *Section 4: Pinouts and pin description*, Introduced WLCSP115 package, hence added *Figure 13: STM32L496Wx, external SMPS device, WLCSP115 ballout*(1)(2) and *Section 7.5: WLCSP115 package information (B0E8)*. Updated *Table 1: Device summary*, *Table 2: STM32L496xx features and peripherals*, *Table 15: STM32L496xx pin definitions*, *Table 85: COMP characteristics*, *Table 88: V_{BAT} monitoring characteristics* and *Table 91: DFSDM characteristics*. Minor text edits across the whole document.
04-Feb-2021	13	Updated *Figure 16: STM32L496Vx WLCSP100L pinout*(1)(2) and *Table 15: STM32L496xx pin definitions*
22-Apr-2021	14	Added errata sheet reference in *Section 1: Introduction*. Updated *Section 3.8: Boot modes*. Updated *Section 3.25: True random number generator (RNG)*. Updated *Section 3.33: Serial peripheral interface (SPI)*. Updated *Section 6.3.14: I/O port characteristics*. Updated *Section 7: Package information*.
24-Aug-2021	15	Changed MSI oscillator drift maximum value for range 8 to 1 to 1.2% in *Table 59: MSI oscillator characteristics*. Added GPIOs PC13, PC14 and PC15 specificities in *Section : Output driving current*. Updated *Figure 34: I/O AC characteristics definition*(1) in *Section : Input/output AC characteristics*. Updated *Table 71: Output voltage characteristics* in *Section : Output voltage levels*. Updated *Figure 36: ADC accuracy characteristics* and added notes below figure; updated *Figure 37: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function* as well as notes below figure. Renamed e1 length into e2 in *Figure 70: WLCSP115 - Outline*.
08-Jul-2022	16	Added footnote in *Table 2: STM32L496xx features and peripherals*. Updated *Figure 7: STM32L496Ax UFBGA169 pinout*(1)(2). Updated *Figure 8: STM32L496Ax, external SMPS device, UFBGA169 pinout*(1)(2). Updated *Figure 9: STM32L496Zx LQFP144 pinout*(1)(2). Updated *Figure 10: STM32L496Zx, external SMPS device, LQFP144 pinout*(1)(2). Updated *Figure 11: STM32L496Qx UFBGA132 ballout*(1)(2).

Table 136. Document revision history (continued)

Date	Revision	Changes
08-Jul-2022	16 (continued)	Updated *Figure 14: STM32L496Vx LQFP100 pinout*[(1)]. Updated *Figure 16: STM32L496Vx WLCSP100L pinout*[(1)(2)]. Updated *Figure 17: STM32L496Vx, external SMPS device, WLCSP100L pinout*[(1)(2)]. Updated *Table 19: Voltage characteristics*. Updated *Table 22: General operating conditions*. Updated *Section : I/O system current consumption*. Updated *Table 66: EMI characteristics for fHSE = 8 MHz and fHCLK = 80 MHz*. Updated *Section 6.3.18: Analog-to-Digital converter characteristics*. Added footnote to *Table 78: ADC accuracy - limited test conditions 1*. Added footnote to *Table 79: ADC accuracy - limited test conditions 2*. Added footnote to *Table 80: ADC accuracy - limited test conditions 3*. Added footnote to *Table 81: ADC accuracy - limited test conditions 4*. Updated *Figure 36: ADC accuracy characteristics*. Updated *Figure 37: Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function*. Updated *Figure 41: SPI timing diagram - master mode*. Updated *Section 7: Package information*. Added *Section 9: Important security notice*.
14-Nov-2022	17	Updated *Figure 13: STM32L496Wx, external SMPS device, WLCSP115 ballout*[(1)(2)].
06-Jun-2024	18	Updated: – Document title – *Section : Features* – *Section 2: Description* – *Section Table 2.: STM32L496xx features and peripherals* – *Section Figure 1.: STM32L496xx block diagram* – *Section Table 18.: STM32L496xx memory map and peripheral register boundary addresses* – *Section Table 50.: Peripheral current consumption* – *Section Table 135.: STM32L496xx ordering information scheme* Added: – *Section 3.27: HASH hardware accelerator (HASH)*
07-Jun-2024	19	Updated *Section Table 135.: STM32L496xx ordering information scheme*
01-Oct-2025	20	Updated *Section Table 135.: STM32L496xx ordering information scheme*

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