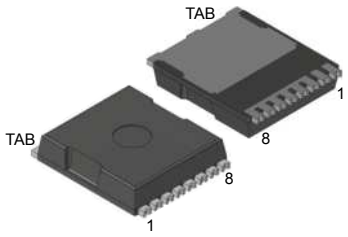
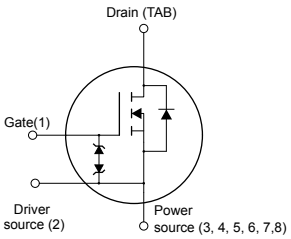
STO67N60M6

Datasheet

N-channel 600 V, 45 mΩ typ., 57 A MDmesh M6 Power MOSFET in a TO-LL package



TO-LL



N-chG1DS2PS345678DTABZ

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO67N60M6	600 V	54 mΩ	57 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link
STO67N60M6

Product summary	
Order code	STO67N60M6
Marking	67N60M6
Package	TO-LL
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D[1]	Drain current (continuous) at T_C = 25 °C	57	A
	Drain current (continuous) at T_C = 100 °C	36	
I_{DM}[2]	Drain current (pulsed)	227	A
P_{TOT}	Total power dissipation at T_C = 25 °C	357	W
dv/dt[3]	Peak diode recovery voltage slope	15	V/ns
dv/dt[4]	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 long leads.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 57 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V*
4. *V_{DD} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.35	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient[1]	43	°C/W
	Thermal resistance, junction-to-ambient[2]	22	

1. *When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.*
2. *When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	760	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS}= 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 28.5 A		45	54	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz	-	3035	-	pF
C_{oss}	Output capacitance		-	110	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	750	-	pF
R_g	Intrinsic gate resistance	f = 250 kHz, open drain	-	3.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 57 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	75.1	-	nC
Q_{gs}	Gate-source charge		-	20.3	-	nC
Q_{gd}	Gate-drain charge		-	34.6	-	nC

1. *$C_{oss\ eq.}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 28.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	22	-	ns
t_r	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	82.1	-	ns
t_f	Fall time		-	10.2	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		57	A
I_{SDM}(1)	Source-drain current (pulsed)		-		227	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 57 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 57 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	340		ns
Q_{rr}	Reverse recovery charge		-	5.6		µC
I_{RRM}	Reverse recovery current		-	29.5		A
t_{rr}	Reverse recovery time	I_{SD} = 57 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	510		ns
Q_{rr}	Reverse recovery charge		-	12		µC
I_{RRM}	Reverse recovery current		-	39.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

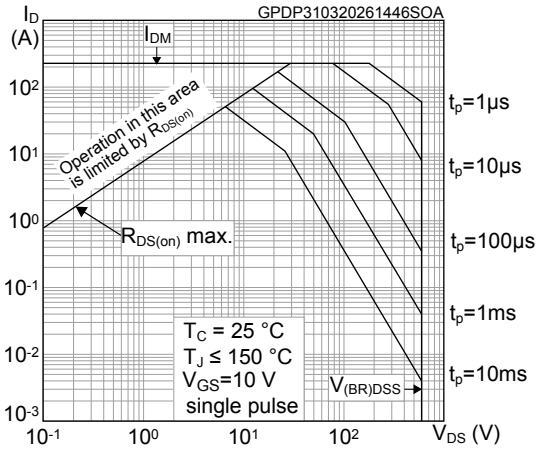


Figure 2. Maximum transient thermal impedance

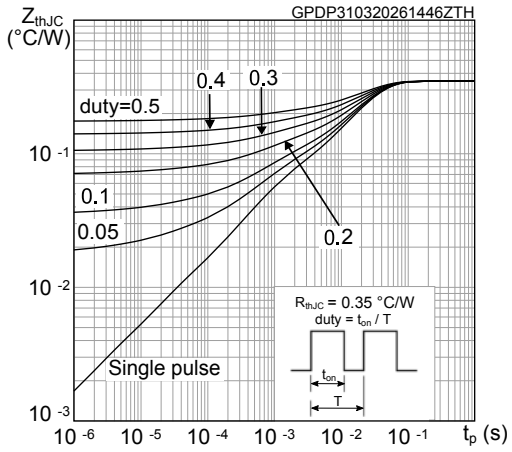


Figure 3. Typical output characteristics

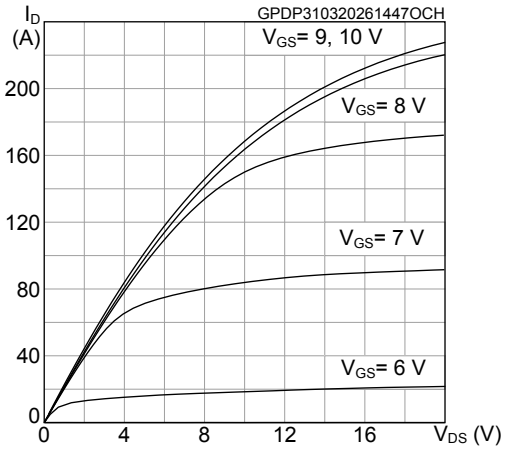


Figure 4. Typical transfer characteristics

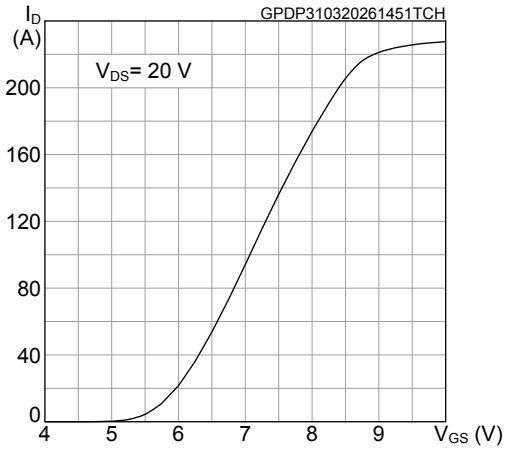


Figure 5. Typical gate charge characteristics

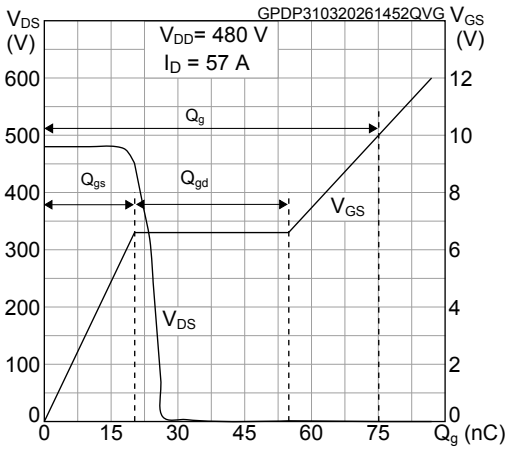


Figure 6. Typical capacitance characteristics

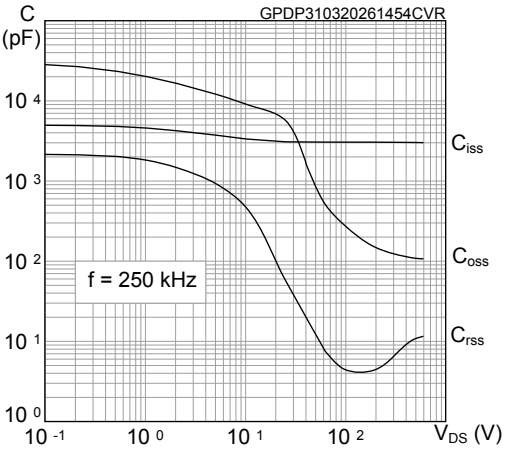


Figure 7. Typical drain-source on-resistance

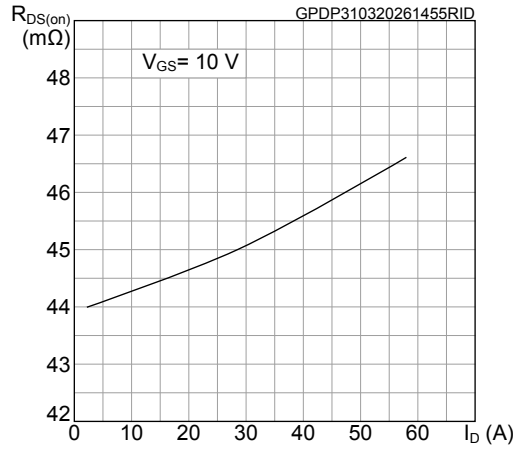


Figure 8. Normalized on-resistance vs temperature

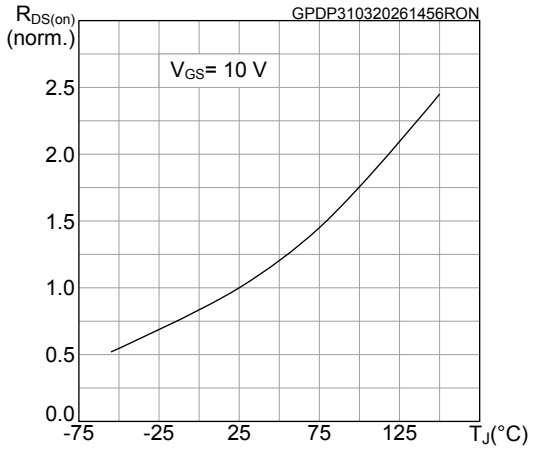


Figure 9. Normalized gate threshold vs temperature

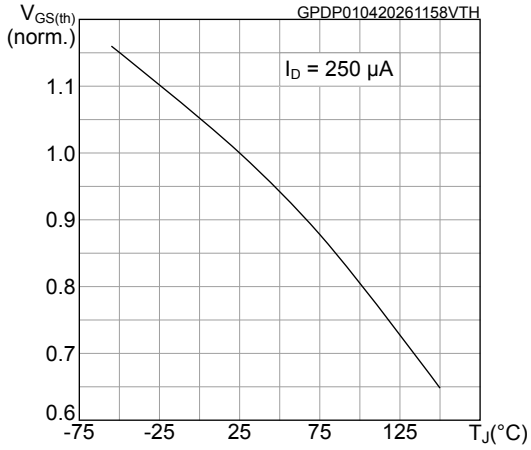


Figure 10. Normalized breakdown voltage vs temperature

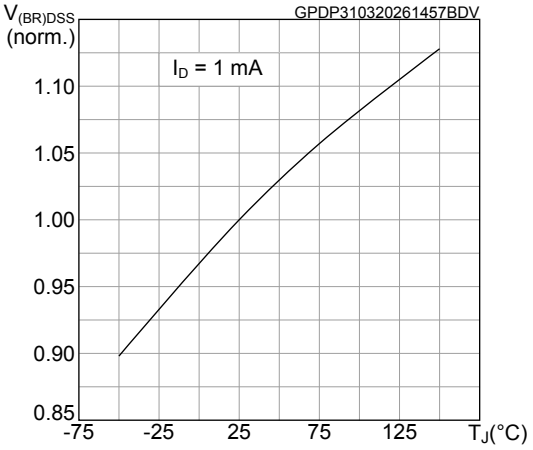


Figure 11. Typical reverse diode forward characteristics

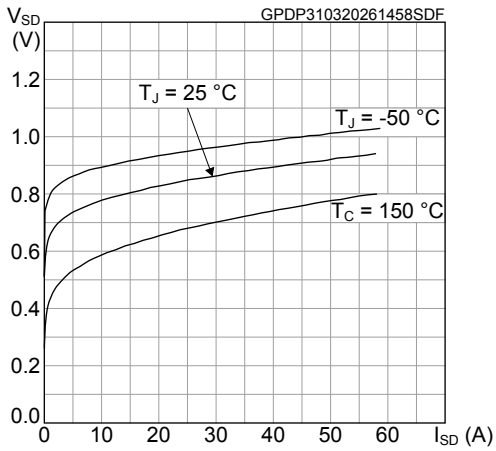
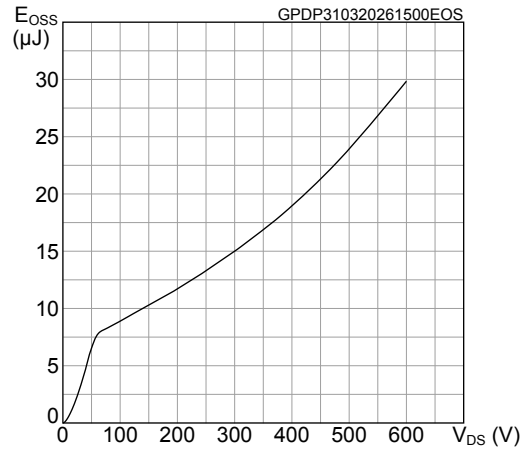


Figure 12. Typical output capacitance stored energy



3 Test circuits

Figure 13. Test circuit for resistive load switching times

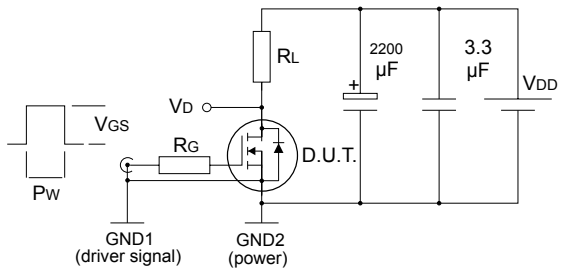


Figure 14. Test circuit for gate charge behavior

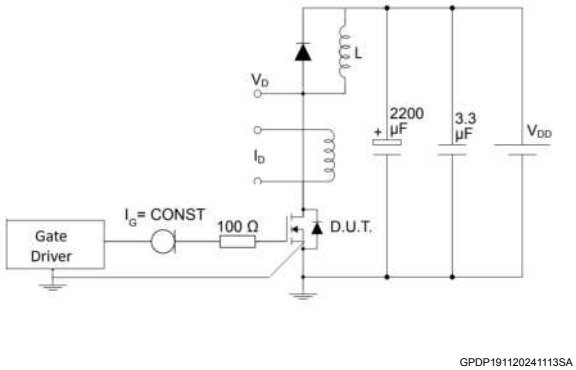


Figure 15. Test circuit for inductive load switching and diode recovery times

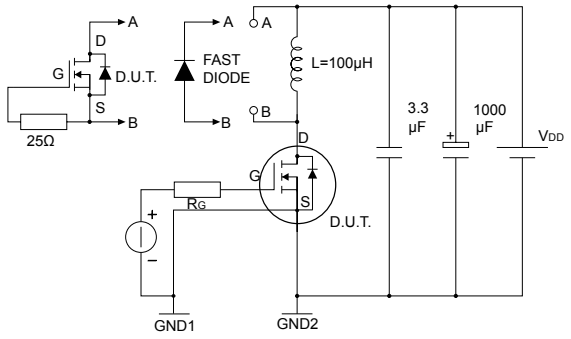


Figure 16. Unclamped inductive load test circuit

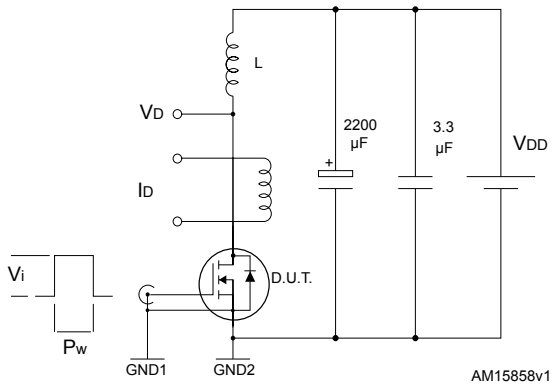


Figure 17. Unclamped inductive waveform

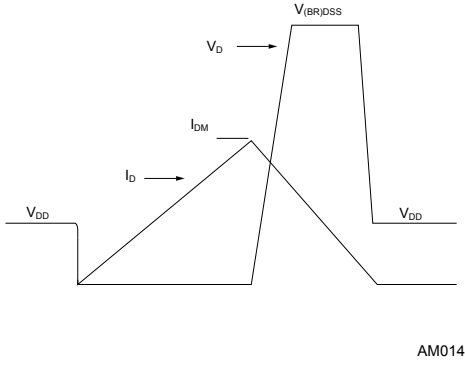
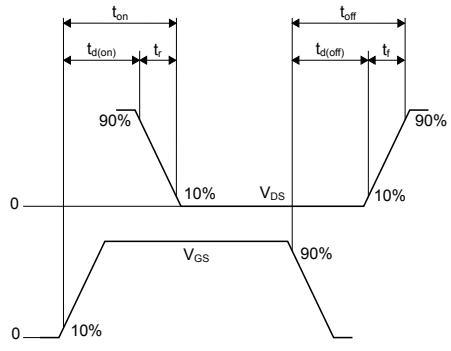


Figure 18. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL package information

Figure 19. TO-LL package outline

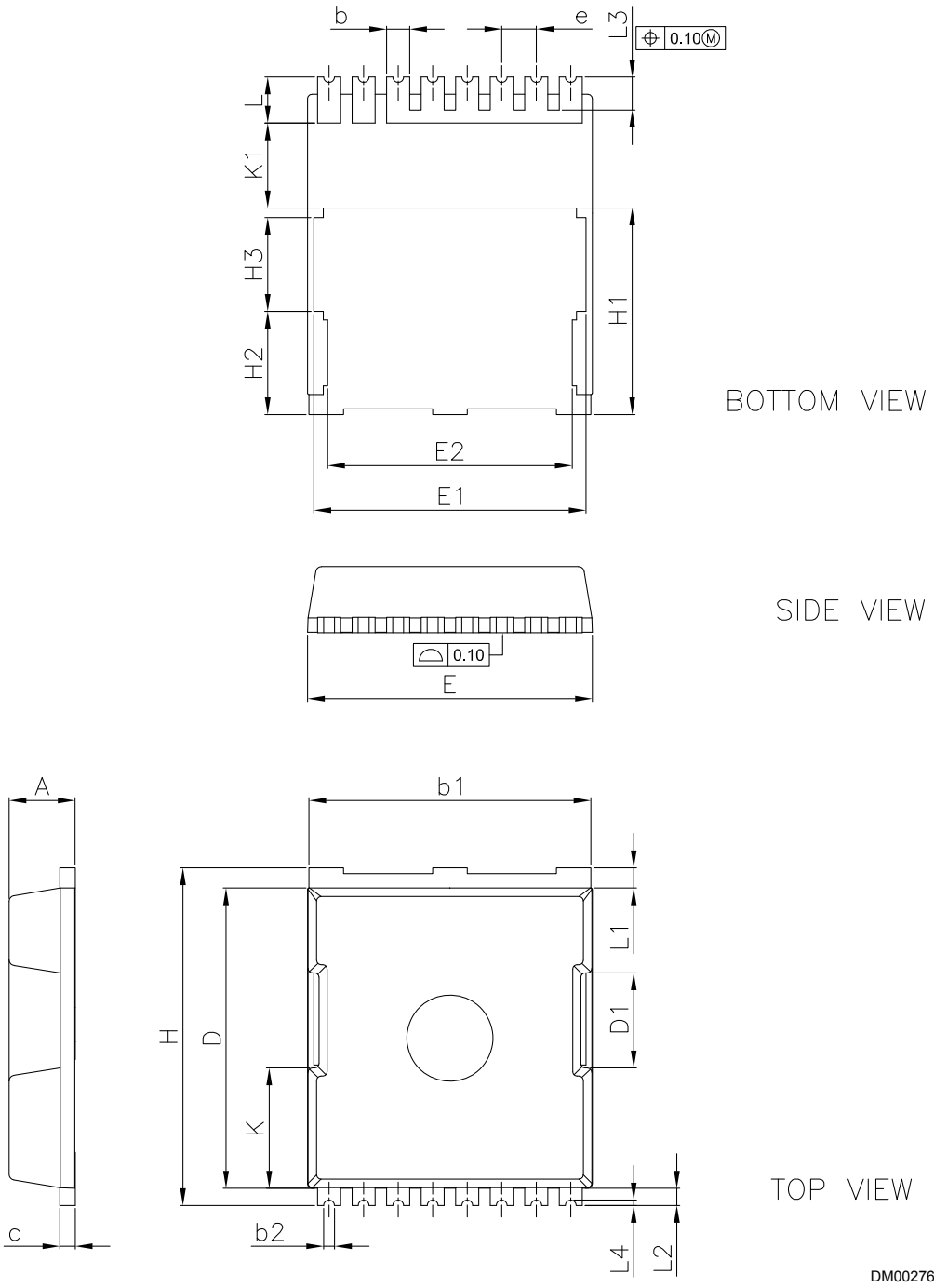
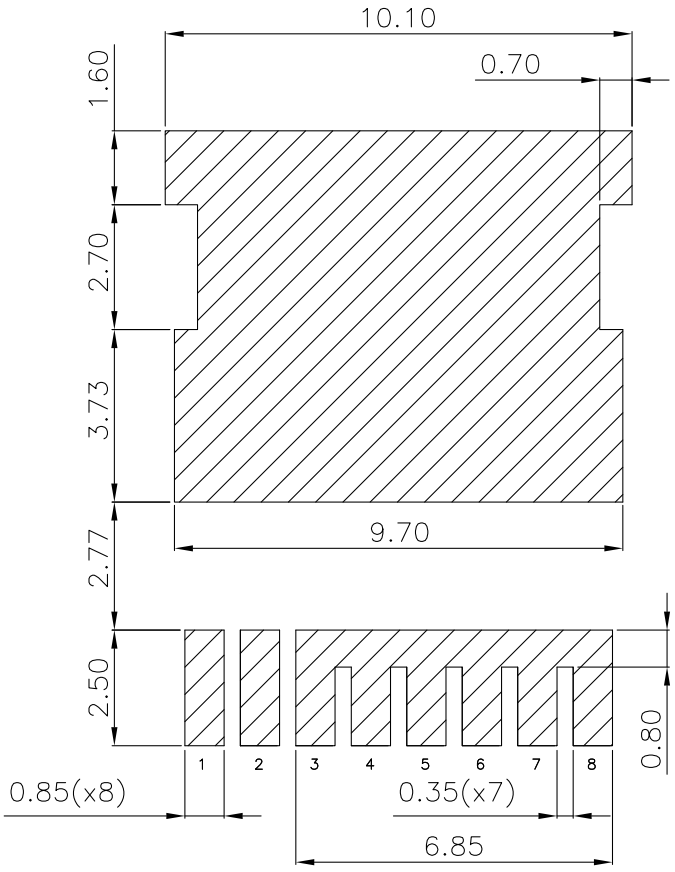


Table 8. **TO-LL package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.60	0.80	0.90
b1	9.70	9.80	9.90
b2	0.20		0.50
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	9.31	9.46	9.61
E2	8.35	8.50	8.65
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	7.00	7.15	7.30
H2	3.34	3.59	3.84
H3	3.11	3.26	3.41
K	4.03	4.18	4.33
K1	2.85	2.95	3.05
L	1.45	1.60	1.75
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
L4	0.05		0.40

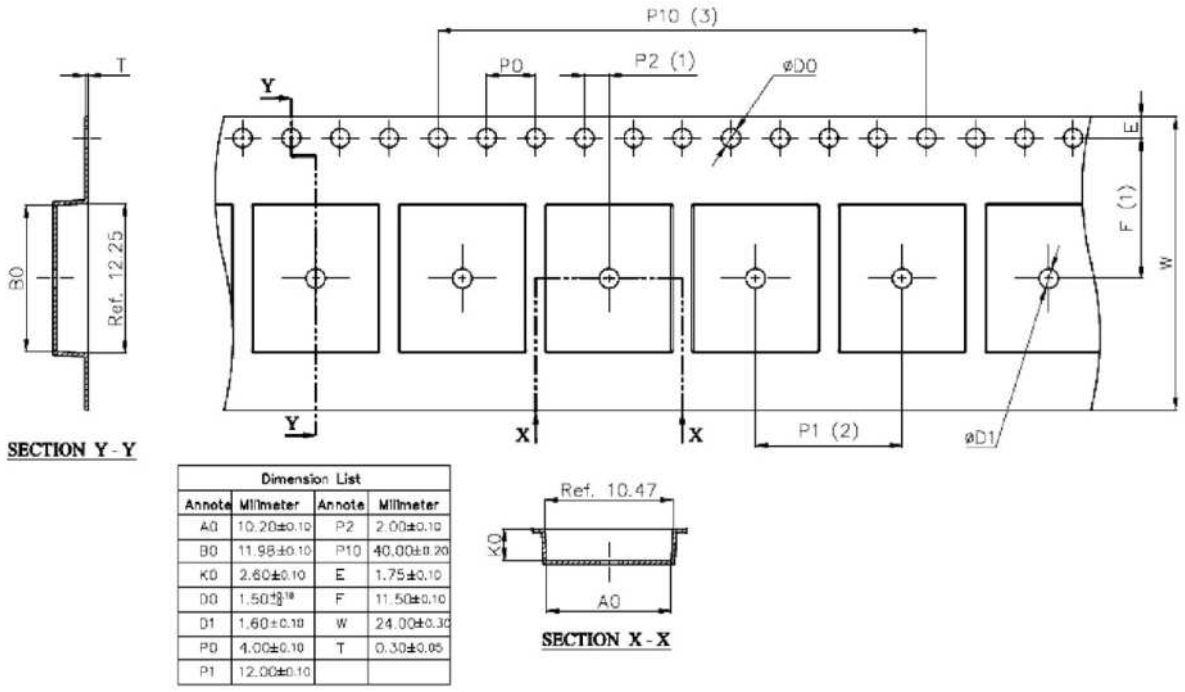
Figure 20. **TO-LL recommended footprint (dimensions are in mm)**



DM00276569_10_FP

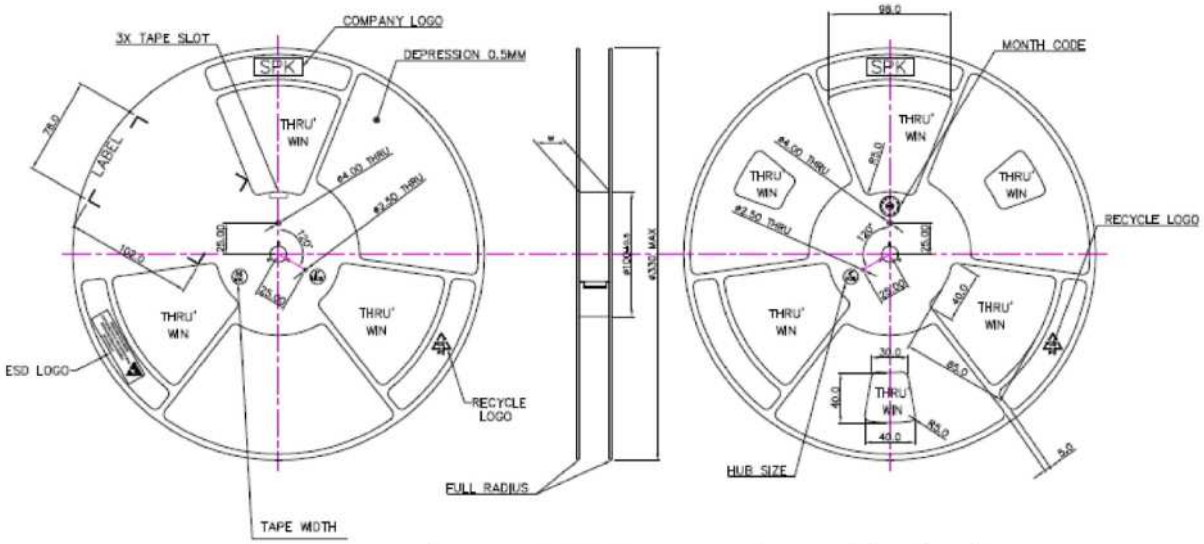
4.2 TO-LL packing information

Figure 21. **Carrier tape outline and dimensions**



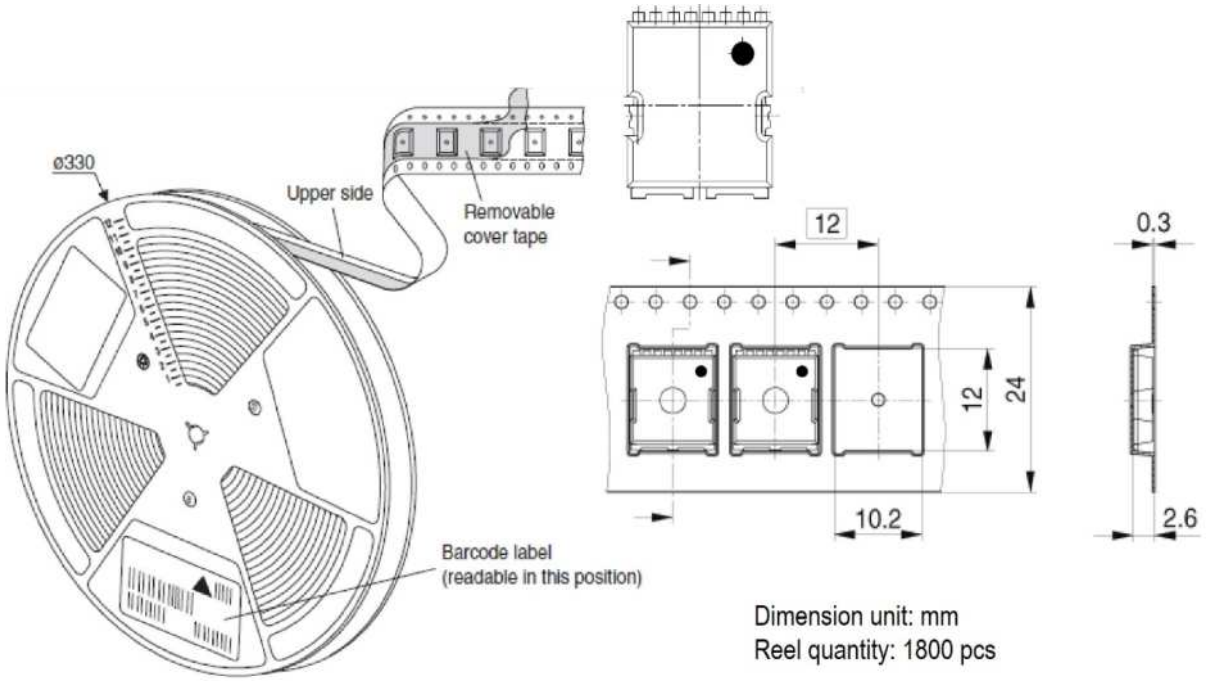
Dimension List			
Annote	Millmeter	Annote	Millmeter
A0	10.20±0.10	P2	2.00±0.10
B0	11.98±0.10	P10	40.00±0.20
K0	2.60±0.10	E	1.75±0.10
D0	1.50$^{+0.10}_{0}$	F	11.50±0.10
D1	1.60±0.10	W	24.00±0.30
P0	4.00±0.10	T	0.30±0.05
P1	12.00±0.10		

Figure 22. **Reel outline and dimensions**



SPECIFICATION							
TAPE WIDTH	W	U	X	V	Y	Z	P
24mm	24.4	1.50	24.5	20.0	0.55	6.00	2

Figure 23. **TO-LL orientation in tape pocket**



Revision history

Table 9. **Document revision history**

Date	Version	Changes
18-Dec-2019	1	First release.
29-Apr-2021	2	Updated title and *Device summary* in cover page. Updated *Section 4 Package information*. Minor text changes.
09-Apr-2026	3	Updated TO-LL package drawing on cover page. Updated Section *1: Electrical ratings, Section 2: Electrical characteristics,, Section 2.1: Electrical characteristics (curves)* and *Section 3: Test circuits.* Updated *Section 4: Package information*.
27-Apr-2026	4	Updated Table 3. Avalanche characteristics. Updated Table 5. Dynamic.

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