Off-Line PRC Controllers with Integrated Power MOSFET

STR-A6100 Series

Description

The STR-A6100 series are power ICs for switching power supplies, incorporating a MOSFET and a current mode PRC controller IC.

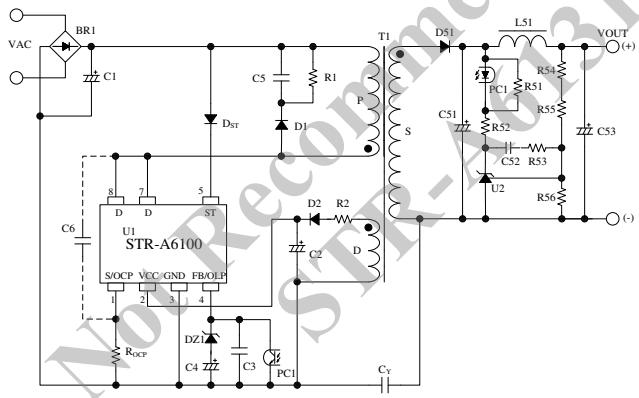
PRC (Pulse Ratio Control) controls on-time with fixed off-time.

The IC includes a startup circuit and a standby function to achieve the low standby power. The rich set of protection features helps to realize low component counts, and high performance-to-cost power supply.

Features

- Current Mode Type Pulse Ratio Control
- Auto Standby Function
  Normal Operation ---------- PRC Mode
  Standby ---------- Burst Oscillation Mode
- No Load Power Consumption < 40mW
- Leading Edge Blanking Function
- Auto Bias Function
- Protections
  Overcurrent Protection (OCP); pulse-by-pulse
  Overload Protection (OLP); auto-restart
  Overvoltage Protection (OVP); latched shutdown
  Thermal Shutdown Protection (TSD); latched shutdown

Typical Application



Applications

- White goods
- Auxiliary SMPS
- Low power SMPS, etc.

Packages

DIP7 DIP8



Not to Scale

Selection Guide

- Package

Part Number	DIP7	DIP8
STR-A6131	–	Yes
STR-A6131M	–	Yes
STR-A6153E	Yes	Yes
STR-A6151	Yes	Yes
STR-A6151M	Yes	Yes
STR-A6159	Yes	Yes
STR-A6159M	Yes	–
STR-A6169	Yes	Yes

- Specifications

Part Number	Fixed off-time	Auto bias function	Startup resistance
STR-A61××	8 µs	Yes	–
STR-A61××M	11.5 µs	–	–
STR-A61××E	11.5 µs	–	Yes*

* ST pin does not need Diode.

- Power MOSFET Electrical Characteristics and output power, P_{OUT} [1]

Part Number	V_{DSS} (min.)	$R_{DS(ON)}$ (max.)	P_{OUT} (Open frame)	
			AC220V	AC85 ~265V
STR-A6131	500 V	3.95 Ω	13 W[2]	15 W[3]
STR-A6131M				
STR-A6153E	650 V	1.9 Ω	22 W	18 W
STR-A6151		3.95 Ω	15 W	13 W
STR-A6151M				
STR-A6159		6 Ω	13 W	10 W
STR-A6159M				
STR-A6169	800 V	19.2 Ω	8 W	5 W

[1] The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, ON Duty, and thermal design affect the output power. It may be less than the value stated here.

[2] AC100V

[3] AC120V

Not Recommended for New Designs; STR-A6131, STR-A6131M

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Not Recommended for New Designs.
STR-A6131, STR-A6131M

1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A is 25 °C, 7 pin = 8 pin

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Notes
Drain Peak Current (1)	I_{DPEAK}	Single pulse	8 – 1	3.2	A	A6131/31M
				2.5		A6151/51M
				3.4		A6153E
				1.8		A6159/59M
				1.2		A6169
Maximum Switching Current (2)	I_{DMAX}	(3)	8 – 1	3.2	A	A6131/31M
				2.5		A6151/51M
				3.4		A6153E
				1.8		A6159/59M
				1.2		A6169
Avalanche Energy (4) (5)	E_{AS}	I_{LPEAK} = 2.1 A	8 – 1	32	mJ	A6131/31M
		I_{LPEAK} = 2.5 A		72		A6151/51M
		I_{LPEAK} = 3.4 A		136		A6153E
		I_{LPEAK} = 1.8 A		24		A6159/59M
		I_{LPEAK} = 1.2 A		7		A6169
S/OCP Pin Voltage	V_{OCP}		1 – 3	− 0.5 to 6	V	
VCC Pin Voltage	V_{CC}		2 – 3	35	V	
FB/OLP Pin Voltage	$V_{FB/OLP}$		4 – 3	− 0.5 to 10	V	
ST Pin Voltage	V_{ST}		5 – 3	− 0.3 to 600	V	
MOSFET Power Dissipation (6)	P_{D1}	(7)	8 – 1	1.35	W	
Control Part Power Dissipation (8)	P_{D2}	$V_{CC} \times I_{CC}$	2 – 3	0.15	W	A61×× A61××M
				0.46		A6153E
Frame Temperature in operation	T_F			− 20 to 125	°C	Recommended operation temperature T_F = 115 °C (max.)
Operating Ambient Temperature	T_{OP}		—	− 20 to 125	°C	
Storage Temperature	T_{stg}		—	− 40 to 125	°C	
Junction Temperature	T_{ch}		—	150	°C	

Not Recommended for New Designs, STR-A6131, STR-A6131M

2. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.

(1) Refer to Figure 3-1 SOA Temperature Derating Coefficient Curve
(2) Maximum Switching Current is Drain current that is limited by the $V_{GS(th)}$ of internal MOSFET and the gate drive voltage of internal control IC setting. T_A = −20 to 125 °C
(3) STR-A61×× : $V_{1\text{-}3}$ = 0.86 V, STR-A61××M/E : $V_{1\text{-}3}$ = 1.28 V
(4) Refer to Figure 3-2 Avalanche Energy Derating Coefficient Curve
(5) Single pulse, V_{DD} = 99 V, L = 20 mH
(6) Refer to Section 3.3 Ta-P_{D1} curve
(7) When embedding this hybrid IC onto the printed circuit board (cupper area in a 15 mm × 15 mm)
(8) Refer to Section 3.4 Ta-P_{D2} curve

- Unless otherwise specified, T_A = 25 °C, V_{CC} = 20 V, 7 pin = 8 pin

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Notes
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		2 − 3	16	17.5	19.2	V	
Operation Stop Voltage (1)	$V_{CC(OFF)}$		2 − 3	9	10	11	V	
Circuit Current in Operation	$I_{CC(ON)}$		2 − 3	−	−	4	mA	
Circuit Current in Non Operation	$I_{CC(OFF)}$	V_{CC} = 14 V	2 − 3	−	−	50	µA	
Auto Bias Threshold Voltage (1) (2)	$V_{CC(BIAS)}$		2 − 3	9.6	10.6	11.6	V	A61××
$V_{CC(BIAS)} - V_{CC(OFF)}$ (2)	−		−	0.2	−	−	V	A61××
Startup Current	$I_{STARTUP}$	V_{CC} = 15 V	2 − 3	− 1230	− 790	− 340	µA	
ST Pin Leakage Current	$I_{START(leak)}$		5 − 3	−	−	30	µA	
PRC Operation								
Maximum OFF Time	$t_{OFF(MAX)}$		8 − 3	7.3	8	8.7	µs	A61××
				10.5	11.5	12.5		A61××M A6153E
Standby Operation								
Burst Threshold Voltage	V_{BURST}		4 − 3	0.70	0.79	0.88	V	A61××
				0.66	0.75	0.84		A61××M A6153E
Protection Operation								
Leading Edge Blanking Time	t_{BW}		−	200	320	480	ns	
OCP Threshold Voltage	$V_{OCP(TH)}$		1 − 3	0.69	0.77	0.86	V	A61××
				0.96	1.13	1.28		A61××M A6153E
OLP Threshold Voltage	V_{OLP}		4 − 3	6.5	7.2	7.9	V	
FB/OLP Pin Source Current in OLP Operation	I_{OLP}		4 − 3	−35	−26	−18	µA	A61××
				−34.1	−26	−18.2		A61××M A6153E
FB/OLP Pin Maximum Source Current	$I_{FB(MAX)}$		4 − 3	−388	−300	−227	µA	A61××
				−390	−300	−220		A61××M A6153E
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		2 − 3	28.7	31.2	34.1	V	
Latched Shutdown Keep Current	$I_{CC(H)}$		2 − 3	−	−	200	µA	
Latched Shutdown Release Threshold Voltage	$V_{CC(La.OFF)}$		2 − 3	6.6	7.3	8.0	V	
Thermal Shutdown Operating Temperature	$T_{j(TSD)}$		−	135	−	−	°C	

(1) $V_{CC(BIAS)} > V_{CC(OFF)}$ always.

(2) STR-A61××M and STR-A6153E do not have the Auto Bias Threshold voltage because auto bias function is not included.

Not Recommended for New Designs.
STR-A6131, STR-A6131M

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Notes
MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}	I_D = 300 µA	8 – 1	500	–	–	V	A6131/31M
				650	–	–		A6151/51M A6159/59M A6153E
				800	–	–		A6169
Drain Leakage Current	I_{DSS}	$V_D = V_{DSS}$	8 – 1	–	–	300	µA	
On Resistance	$R_{DS(ON)}$	I_D = 0.4 A	8 – 1	–	–	1.9	Ω	A6153E
				–	–	3.95		A6131/31M A6151/51M
				–	–	6		A6159/59M
				–	–	19.2		A6169
Switching Time	t_f	V_D = 10V	8 – 1	–	–	250	ns	
Thermal Characteristics								
Thermal Resistance (3)	θ_{ch-F}		–	–	–	52	°C/W	

(3) θ_{ch-F} is thermal resistance between channel and frame. Frame temperature (T_F) is measured at the base of pin 3.

Not Recommended for New Designs.
STR-A6131, STR-A6131M

3. Performance Curves

3.1 Derating Curves

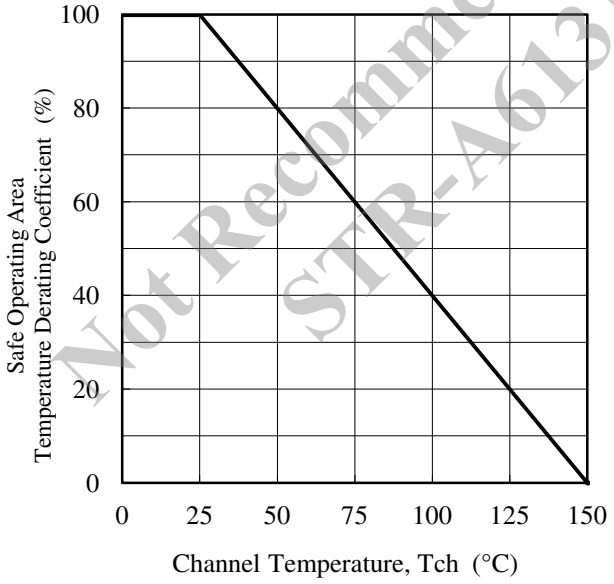


Figure 3-1 SOA Temperature Derating Coefficient Curve

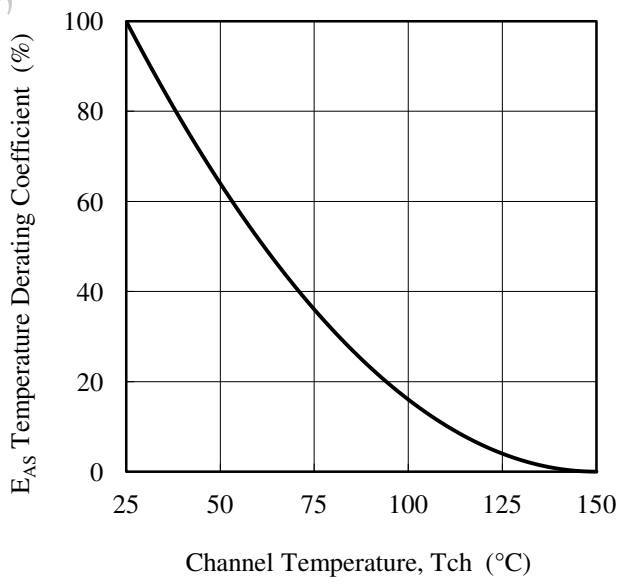
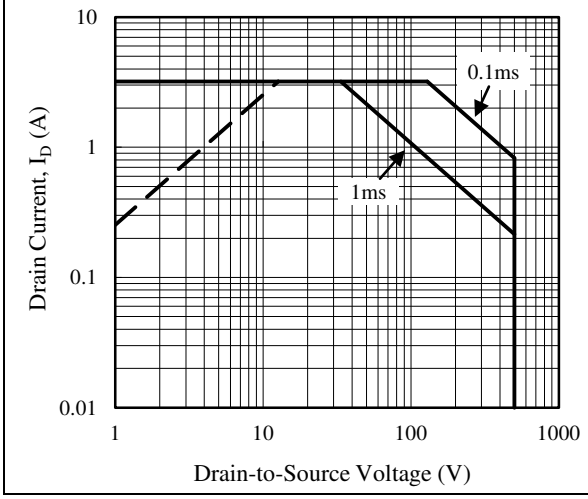


Figure 3-2 Avalanche Energy Derating Coefficient Curve

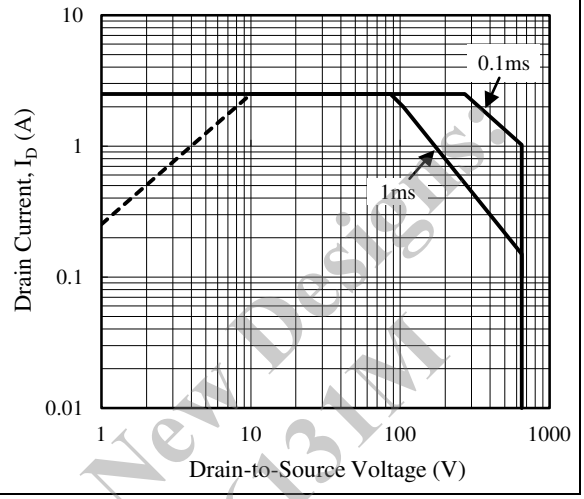
3.2 MOSFET Safe Operating Area Curves

- When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 3-1.
- The broken line in the safe operating area curve is the drain current curve limited by on-resistance.
- Unless otherwise specified, T_A = 25 °C, Single pulse

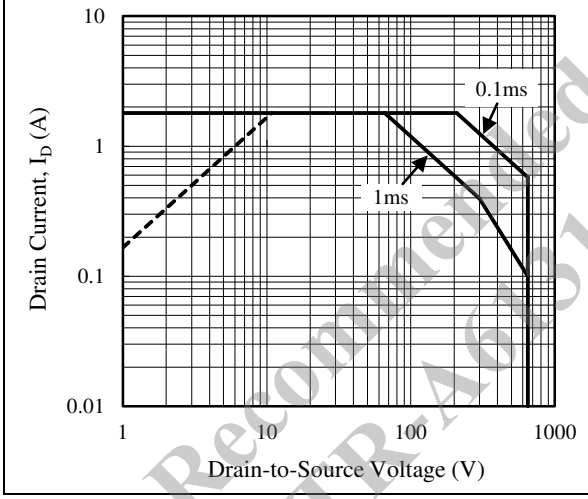
● **STR-A6131 / 31M**



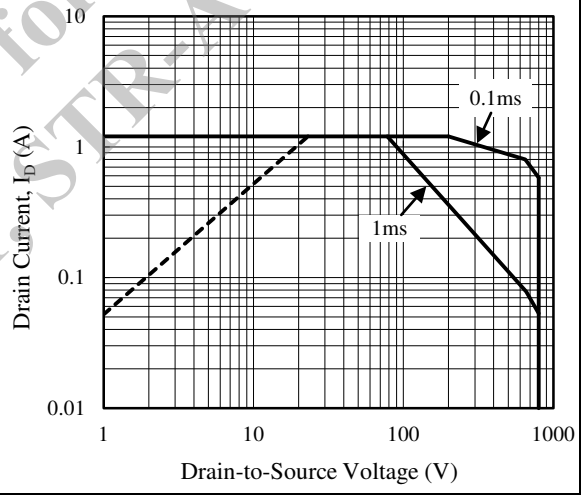
● **STR-A6151 / 51M**



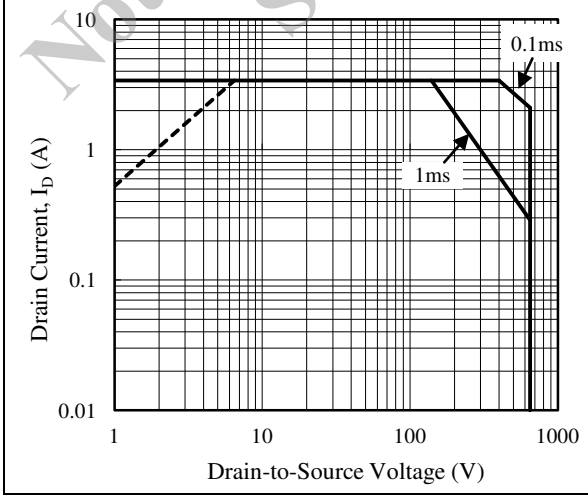
● **STR-A6159 / 59M**



● **STR-A6169**

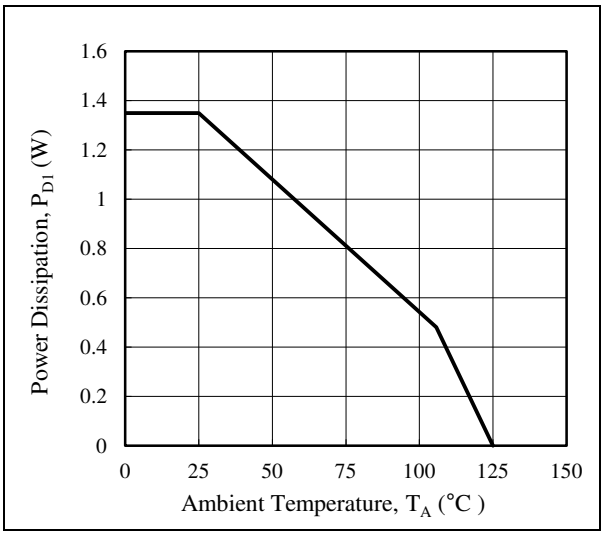


● **STR-A6153E**

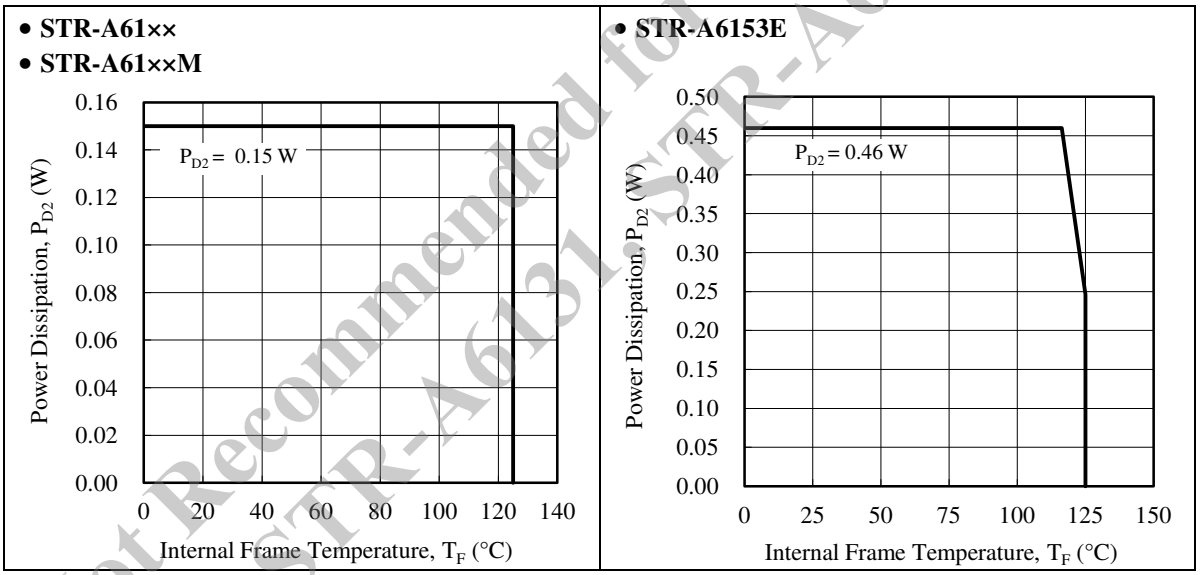


Not Recommended for New Designs, STR-A6131, STR-A6131M

3.3 Ambient Temperature versus Power Dissipation, P_{D1} Curves



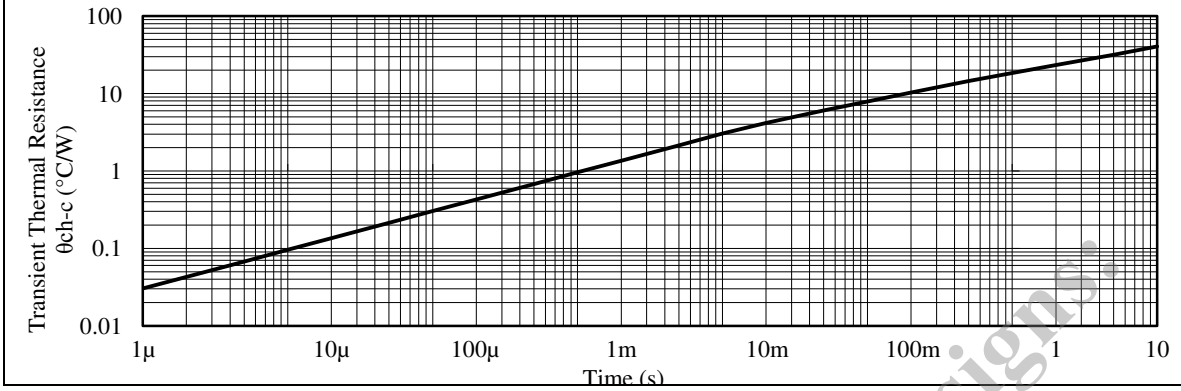
3.4 Internal Frame Temperature versus Power Dissipation, P_{D2} Curves



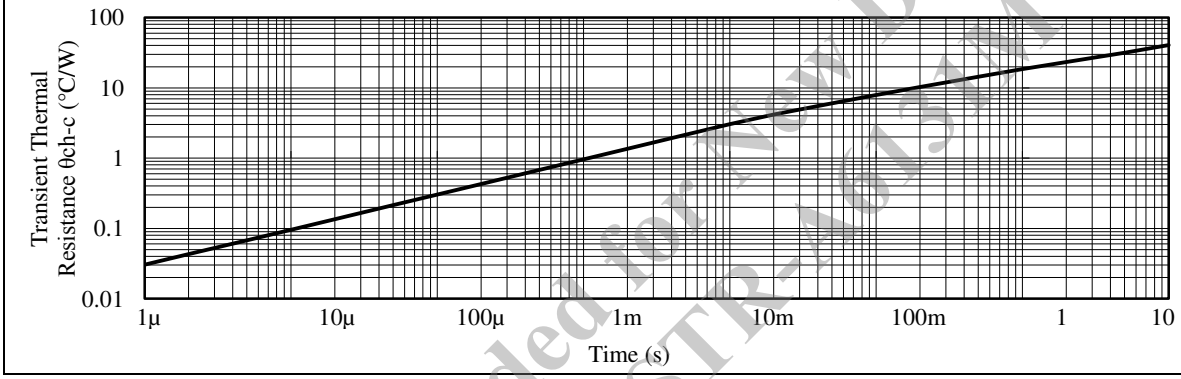
Not Recommended for New Designs:
STR-A6131, STR-A6131M

3.5 Transient Thermal Resistance Curves

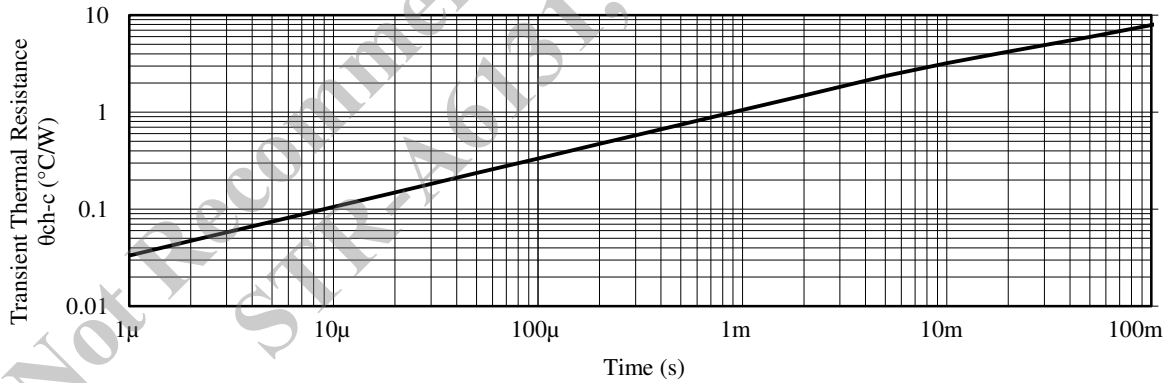
• **STR-A6131 / 31M**



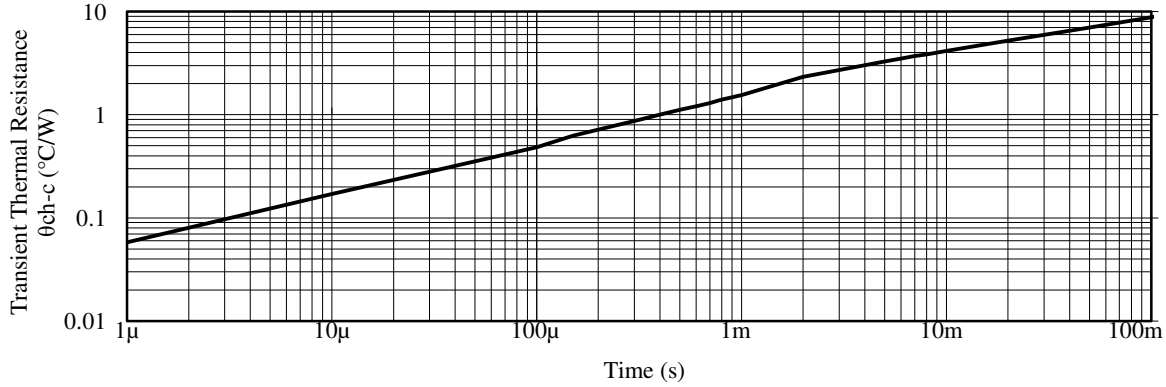
• **STR-A6151 / 51M**



• **STR-A6159 / 59M**

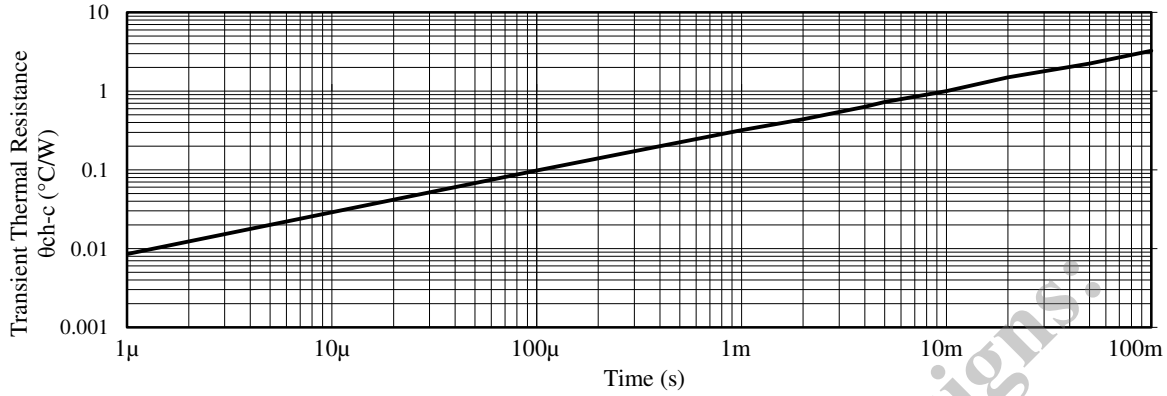


• **STR-A6169**



Not Recommended for New Designs, STR-A6131, STR-A6131M

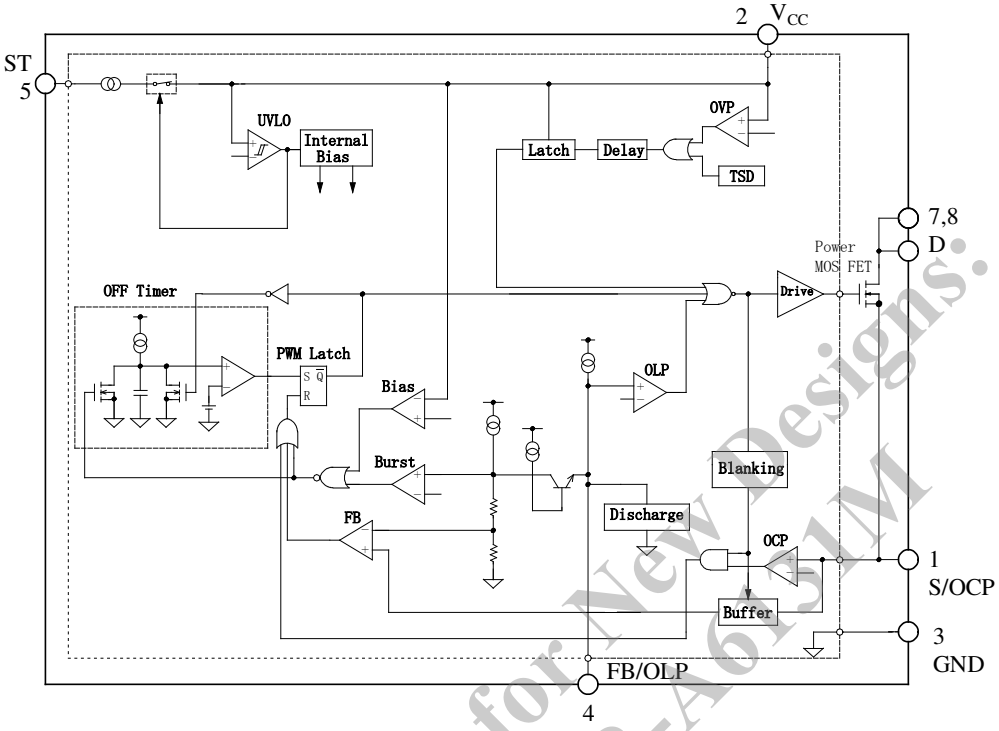
• **STR-A6153E**



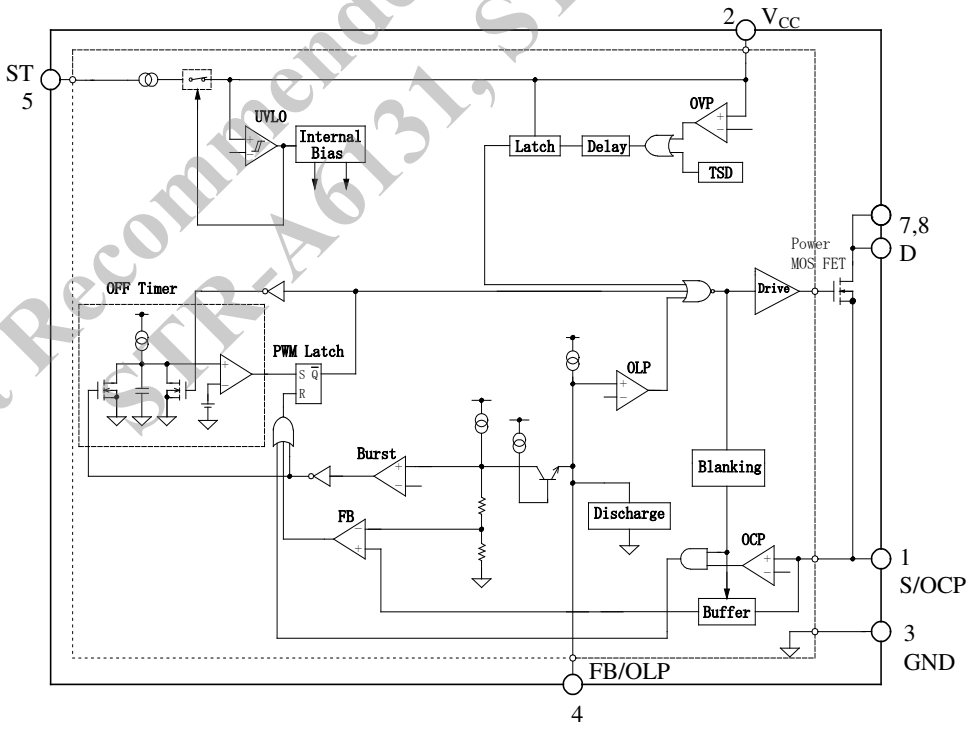
Not Recommended for New Designs;
STR-A6131, STR-A6131M

4. Block Diagram

STR-A61××

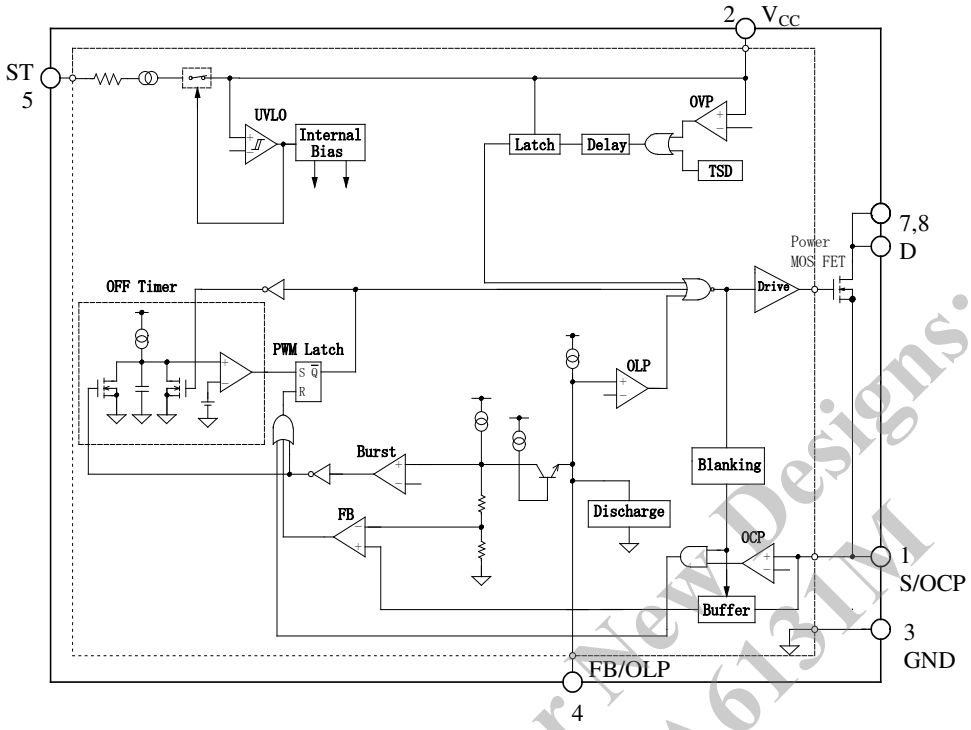


STR-A61××M



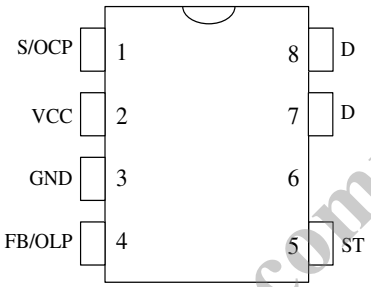
Not Recommended for New Designs.
STR-A6131, STR-A6151M

STR-A6153E



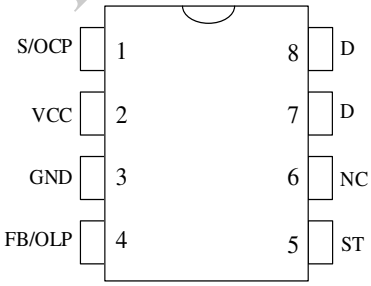
5. Pin Configuration Definitions

- DIP7



Pin	Name	Descriptions
1	S/OCP	MOSFET source and input of overcurrent protection (OCP) signal
2	VCC	Power supply voltage input for control part and input of overvoltage protection (OVP) signal
3	GND	Ground
4	FB /OLP	Input of constant voltage control signal and input of over load protection (OLP) signal
5	ST	Startup current input
6	–	(Pin removed)
7	D	Power MOSFET drain
8		

- DIP8



Pin	Name	Descriptions
1	S/OCP	MOSFET source and input of overcurrent protection (OCP) signal
2	VCC	Power supply voltage input for control part and input of overvoltage protection (OVP) signal
3	GND	Ground
4	FB /OLP	Input of constant voltage control signal and input of over load protection (OLP) signal
5	ST	Startup current input
6	NC	–
7	D	Power MOSFET drain
8		

Not Recommended for New Designs.
STR-A6131, STR-A6131M

6. Typical Application

- The PCB traces of D pins should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D pin and the S/OCP pin.
- As shown in Figure 6-2, STR-A6153E does not need diode connected to ST pin.

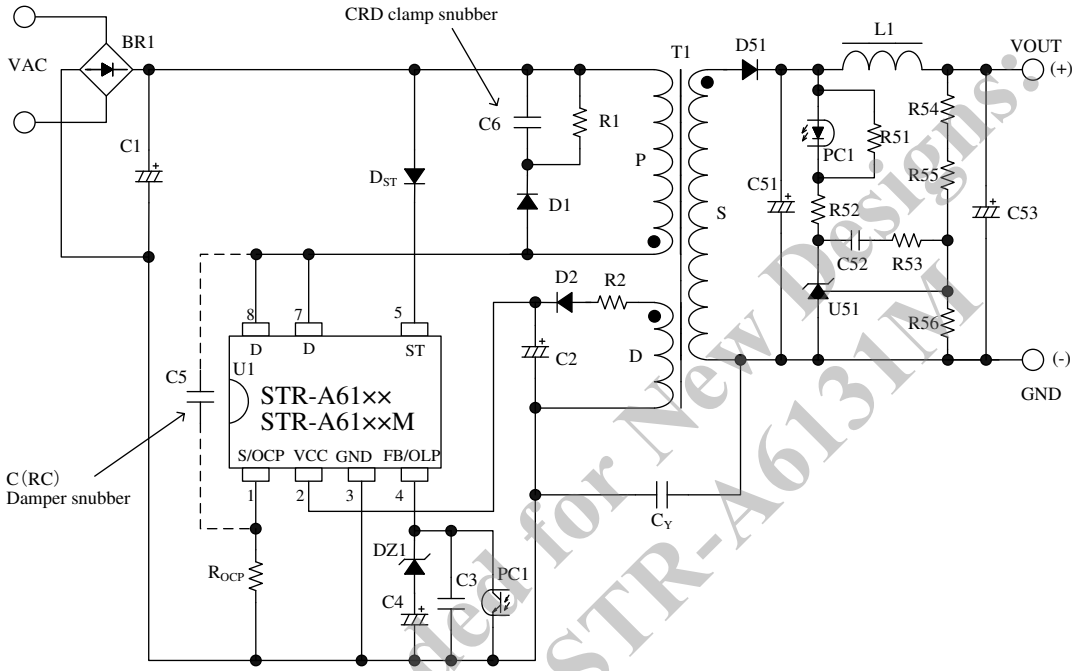


Figure 6-1 Typical application (STR-A61××/ STR-A61××M)

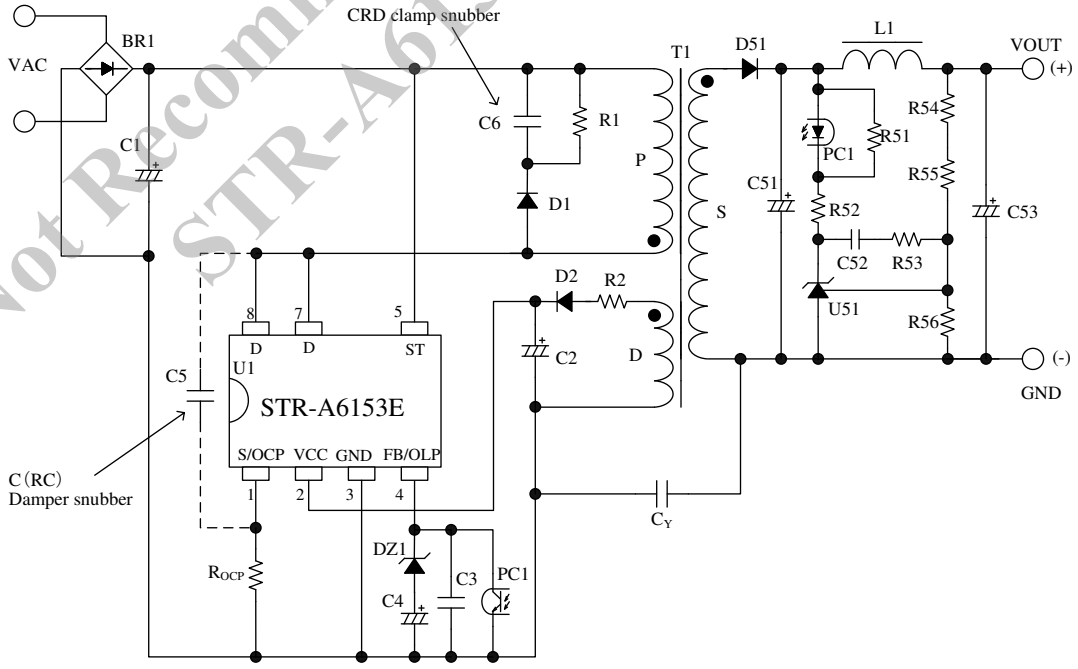
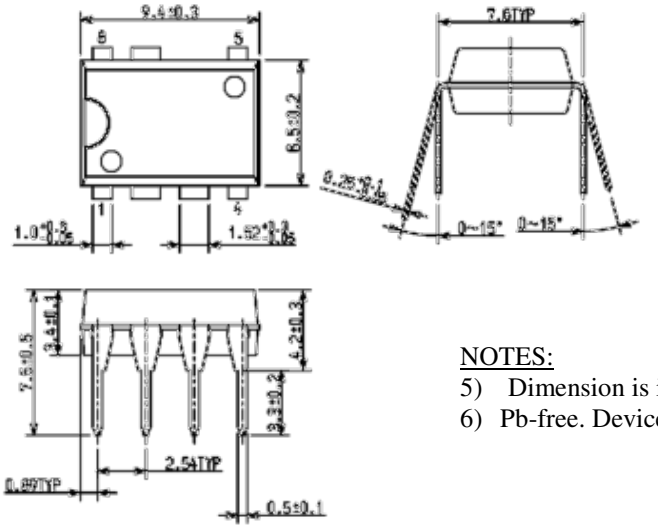


Figure 6-2 Typical application (STR-A6153E)

Not Recommended for New Designs.
STR-A6131, STR-A6131M

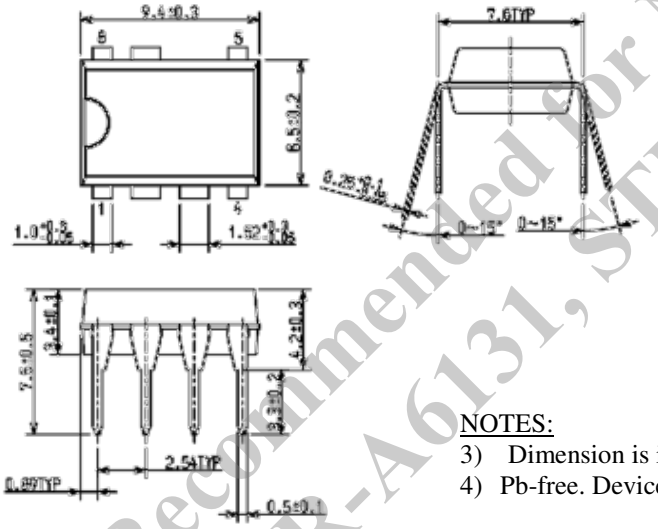
7. Physical Dimensions

- DIP7 (Type A)



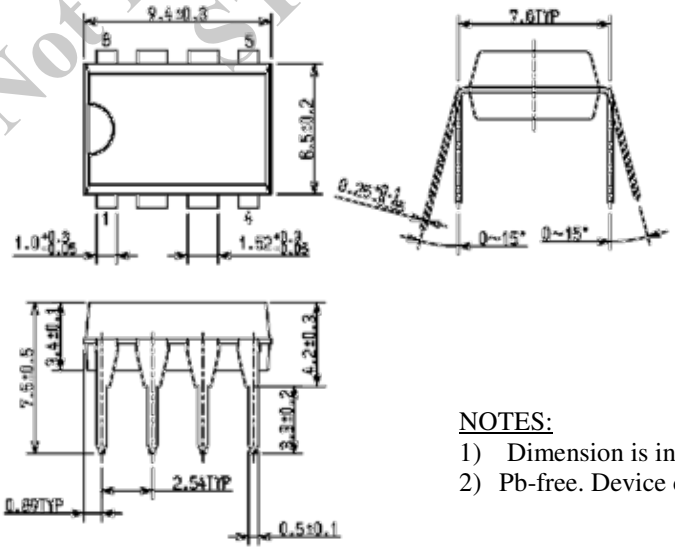
NOTES:
5) Dimension is in millimeters
6) Pb-free. Device composition compliant with the RoHS directive

- DIP7 (Type B)



NOTES:
3) Dimension is in millimeters
4) Pb-free. Device composition compliant with the RoHS directive

- DIP8

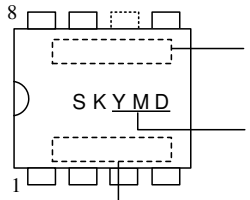


NOTES:
1) Dimension is in millimeters
2) Pb-free. Device composition compliant with the RoHS directive

Not Recommended for New Designs: STR-A6131, STR-A6131M

8. Marking Diagram

- STR-A6131/51/59/69/31M/59M/51E

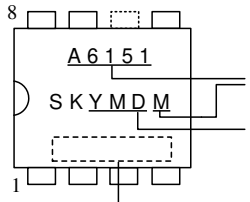


Part Number
(A61xx / A6153E A6131M / A6159M)

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is a period of days:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

- STR-A6151M



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is a period of days:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

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9. Operational Description

- All of the parameter values used in these descriptions are typical values of STR-A6151, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

9.1 Startup Operation

Figure 9-1 shows the circuit around VCC pin. Figure 9-2 shows VCC pin voltage behavior during the startup period.

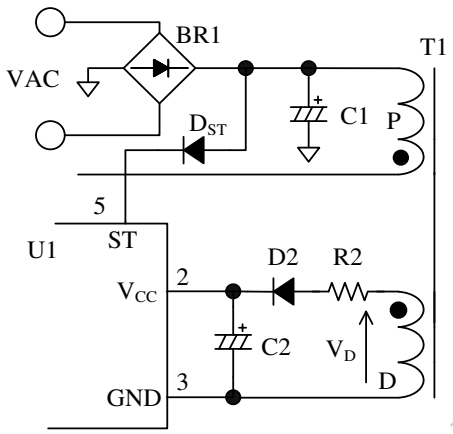


Figure 9-1. VCC pin peripheral circuit

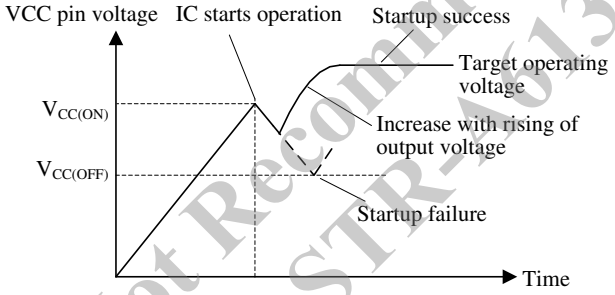


Figure 9-2. VCC pin voltage during startup period

The IC incorporates the startup circuit. The circuit is connected to ST pin. During the startup process, the constant current, $I_{STARTUP}$ = − 790 μA, charges C2 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 17.5 V, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. Since the Operation Stop Voltage $V_{CC(OFF)}$ = 10 V is low, the auxiliary winding voltage reaches to setting value before VCC pin voltage decreases to $V_{CC(OFF)}$. Thus control circuit continues the operation. The voltage from the auxiliary winding D in Figure 9-1 becomes a power source to the control circuit in operation.

The approximate value of auxiliary winding voltage is about 15 V to 20 V, taking account of the winding turns of D winding so that VCC pin voltage becomes Equation (2) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 11.6(\mathrm{V}) < V_{CC} < 28.7(\mathrm{V}) \quad (1)$$

The startup time of IC is determined by C2 capacitor value. The approximate startup time tSTART is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left| I_{STRATUP} \right|} \quad (2)$$

where,

t_{START} : Startup time of IC (s)

$V_{CC(INT)}$: Initial voltage on VCC pin (V)

9.2 Undervoltage Lockout (UVLO)

Figure 9-3 shows the relationship of VCC pin voltage and circuit current ICC. When VCC pin voltage increases to $V_{CC(ON)}$ = 17.5 V, the control circuit starts switching operation and the circuit current ICC increases. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 10 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

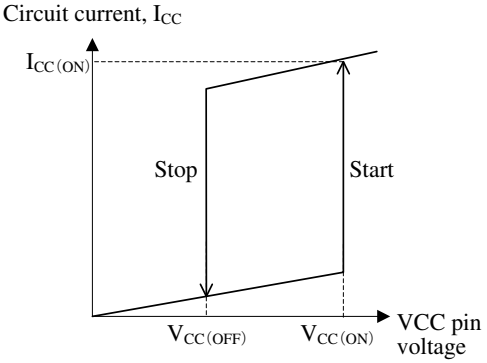


Figure 9-3. Relationship between VCC pin voltage and I_{CC}

9.3 Constant Output Voltage Control

Figure 9-4 shows FB/OLP pin peripheral circuit, Figure 9-5 shows the waveform of I_D and FB comparator input.

The IC achieves the constant voltage control of the power supply output by PRC (Pulse Ratio Control). PRC

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controls on-time with fixed off-time. In addition, the IC uses the peak-current-mode control method, which enhances the response speed and provides the stable operation.

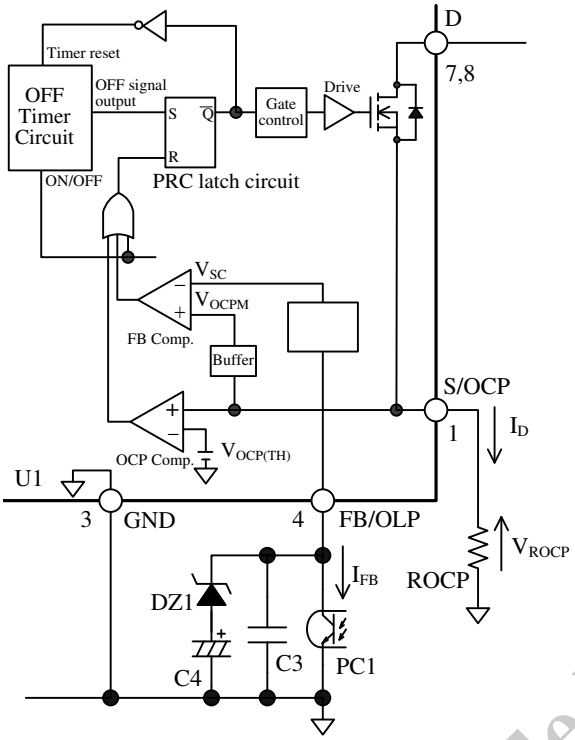


Figure 9-4. FB/OLP pin peripheral circuit

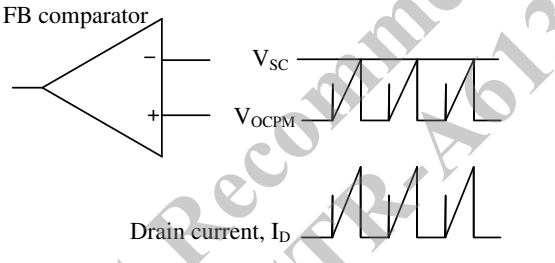


Figure 9-5. The waveform of I_D and FB comparator input

The internal fixed off-time, t_{OFF} is made from internal off timer circuit, the turn-on timing of power MOSFET depends on t_{OFF}.

- Turn-on
  After the period of t_{OFF}, OFF signal output becomes High, $\overline{Q}$ of PRC latch circuit is latched to Low. As a result, turn-on signal is input to the gate control circuit, and power MOSFET turns on.

- Tuen-off
  When the OCP comparator or the FB comparator resets the PRC latch circuit, $\overline{Q}$ of PRC latch circuit is latched to High. As a result, turn-off signal is input to the gate control circuit, and power MOSFET turns off.

The IC controls the peak value of V_{OCPM} voltage to be close to target voltage (V_{SC}), comparing V_{OCPM} with V_{SC} by internal FB comparator.

V_{OCPM} is amplified V_{ROCP} voltage that is a detection voltage by current detection resistor, R_{OCP}.

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{OCPM} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

9.4 Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or overcurrent protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this operation, Leading Edge Blanking Time, t_{BW} = 320 ns is built-in.

In the period of t_{BW}, the IC does not respond to the surge voltage in turning on the power MOSFET.

9.5 Auto Standby Function

Automatic standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 25% of the maximum drain current (it is in the Overcurrent Protection state). The operation mode becomes burst oscillation, as shown in Figure 9-6. The 25% of the maximum drain current corresponds to the Burst Threshold Voltage of FB/OLP pin, V_{BURST} = 0.79 V (0.75 V for STR-A61××M and STR-A6153E).

Burst oscillation mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

Generally, to improve efficiency under light load

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conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

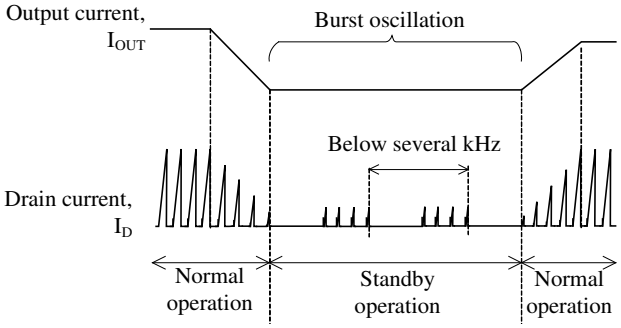


Figure 9-6. Auto Standby mode timing

9.6 Auto Bias Function (STR-A61xx)

STR-A61xx includes the auto bias function. The function becomes active during burst oscillation mode. When VCC pin voltage decreases to the Auto Bias Threshold Voltage, $V_{CC(BIAS)}$ = 10.6 V, during burst oscillation mode, the IC shifts to PRC operation so that VCC pin voltage does not decrease. As a result, the IC achieves stable standby operation.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary winding and/or reducing the value of R2 in Figure 10-2 (refer to Section 10.1 Peripheral Components for a detail of R2).

9.7 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage, $V_{OCP(TH)}$ = 0.77 V (1.13 V for STR-A61××M and STR-A6153E).

Figure 9-7 shows the output characteristics. When OCP becomes active, the output voltage decreases and the auxiliary winding voltage, V_D decreases in proportion to the output voltage.

When VCC pin voltage decreases to $V_{CC(OFF)}$ = 10 V, the control circuit stops operation by UVLO circuit, and reverts to the state before startup. After that, VCC pin voltage is increased by Startup Current, $I_{STARTUP}$. When VCC pin voltage increases to $V_{CC(ON)}$ = 17.5 V, the IC restarts the operation. Thus the intermittent operation by UVLO is repeated in OCP operation.

The IC usually has some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the actual peak of drain current is. As a result, the detection voltage becomes higher than $V_{OCP(TH)}$. Thus, the output current depends on the AC input voltage in OCP operation (refer to Figure 9-7).

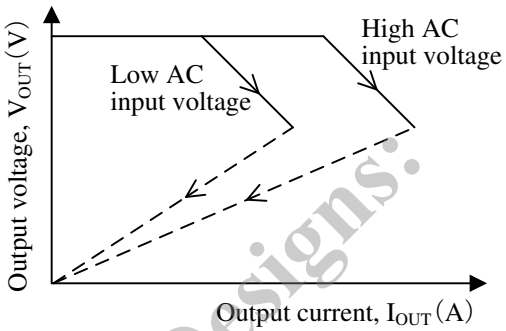


Figure 9-7. Output characteristic curve

When the multi outputs transformer is used, there is the case that the auxiliary winding voltage, V_D does not decrease and the intermittent operation is not started, even if output voltage decreases in OCP operation. This is due to the poor coupling of transformer. In this case, the overload protection (OLP) becomes active. (refer to Section 9.8.)

9.8 Overload Protection (OLP)

Figure 9-8 shows the FB/OLP pin peripheral circuit. Figure 9-9 shows the OLP operational waveforms.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 7.2 V or more for the OLP delay time, t_{DLY} or more, the OLP function is activated and the IC stops switching operation. t_{DLY} is calculated using Equation (3).

$$t_{DLY} = C4 \times \frac{(V_{OLP} - V_Z)}{I_{OLP}} \quad (3)$$

there,

t_{DLY}: OLP delay time

V_Z: zener voltage of zener diode, DZ1

I_{OLP}: FB/OLP Pin Source Current in OLP Operation is − 26 µA

After the switching operation stops, VCC pin voltage decreases to Operation Stop Voltage $V_{CC(OFF)}$ = 10 V and the intermittent operation by UVLO is repeated.

This intermittent operation reduces the stress of parts such as power MOSFET and secondary side rectifier

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diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

As shown in Figure 9-9, t_{DLY} should be longer than t_{START} which is the period until the output voltage becomes constant. If t_{DLY} is shorter than t_{START}, the power supply may not start due to OLP operation.

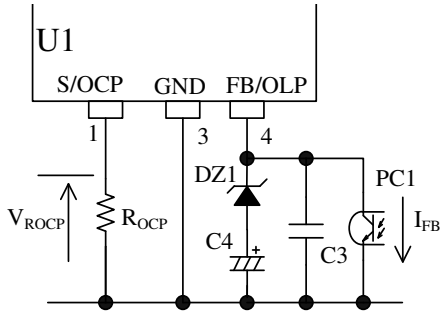


Figure 9-8. FB/OLP pin peripheral circuit

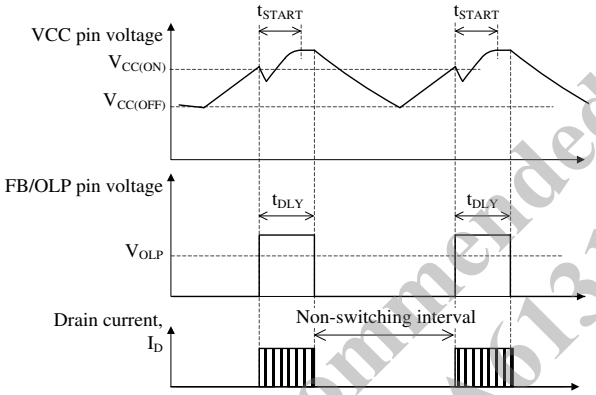


Figure 9-9. OLP operational waveforms

9.9 Overvoltage Protection (OVP)

Figure 9-10 shows the OVP operational waveforms.

When a voltage between VCC pin and GND terminal increases to $V_{CC(OVP)}$ = 31.2 V or more, OVP function is activated. When the OVP function is activated, the IC stops switching operation at the latched state.

After that, VCC pin voltage is decreased by circuit current of IC. When VCC pin voltage becomes $V_{CC(OFF)}$ = 10 V or less, VCC pin voltage is increased by Startup Current. When VCC pin voltage increases to $V_{CC(ON)}$ = 17.5 V, the circuit current increases and VCC pin voltage decreases. In this way, VCC pin voltage goes up and down between $V_{CC(OFF)}$ and $V_{CC(ON)}$ during the latched state, excessive increase of VCC pin voltage is prevented.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(La.OFF)}$ = 7.3 V.

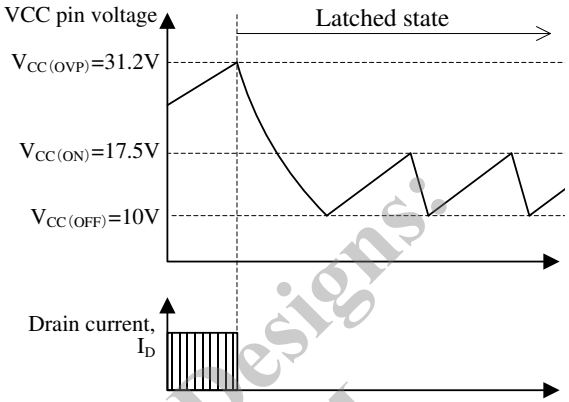


Figure 9-10. OVP operational waveforms

If output voltage detection circuit becomes open, the output voltage of secondary side increases. In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions can be detected because the VCC pin voltage is proportional to output voltage. The approximate value of output voltage VOUT(OVP) in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 31.2 \quad (4)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

9.10 Thermal Shutdown Function (TSD)

When the temperature of control circuit increases to Tj(TSD) = 135 °C or more, Thermal Shutdown function is activated. When the TSD function is activated, the IC stops switching operation at the latched state (see the Section 9.9). Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(La.OFF)}$ = 7.3 V.

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10.Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

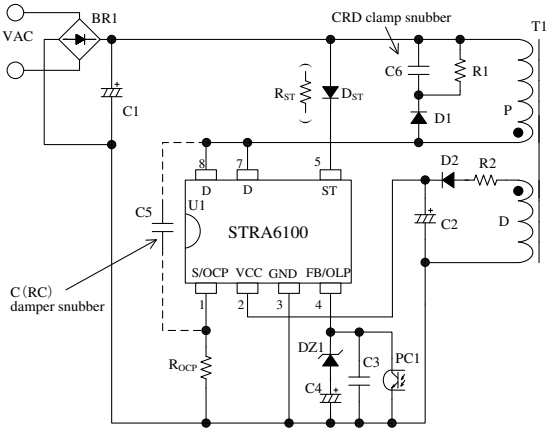


Figure 10-1. The IC peripheral circuit

● **Electrolytic Capacitor**

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

● **S/OCP Pin Peripheral Circuit**

Choose a type of low internal inductance because a high frequency switching current flows to R_{OCP} in Figure 10-1, and of properly allowable dissipation.

● **VCC Pin Peripheral Circuit**

The value of C2 in Figure 10-1 is generally recommended to be 10μ to 47μF (refer to Section 9.1, because the startup time is determined by the value of C2). In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 10-2), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off. For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 10-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

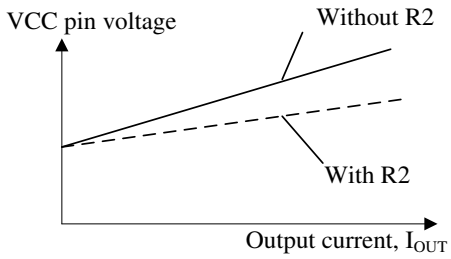


Figure 10-2. Variation of VCC pin voltage and power

● **FB/OLP Pin Peripheral Circuit**

Figure 10-1 performs high frequency noise rejection and phase compensation, and should be connected close to these pins. The value of C3 is recommended to be about 2200p to 0.01μF.

In order to make the value of C3 low and make the output response fast, DZ1 and C4 are connected.

DZ1 prevents C4 charging in normal operation. The zener voltage of DZ1, V_Z should be set higher than FB/OLP pin voltage in normal operation. Usually, the value of V_Z is about 4.7 V to 5.6 V.

C4 is for OLP delay time, t_{DLY} setting. If C4 is too small, the power supply may not start due to OLP operation (see Section 9.8). The value of C4 is about 4.7 μF to 22 μF.

C3, C4 and DZ1 should be selected based on actual operation in the application.

● **ST Pin Peripheral Circuit**

When STR-A61×× and STR-A61××M are used, D_{ST} or R_{ST} should be connected to ST pin as shown in Figure 10-1. D_{ST} and R_{ST} prevent negative voltage from applying to ST pin. If ST pin voltage becomes under −0.3 V, the power supply may not start. The value of D_{ST} and R_{ST} should be selected based on actual operation in the application.

Recommended value of R_{ST} is 33 kΩ,

Recommended characteristics of D_{ST} is as follows:

Characteristics	Recommended range
Peak Reverse Voltage, V_{RM}	> 35 V
Forward current, I_F	> 1.5 mA
Reverse Recovery Time, t_{rr}	< 27 μs
Reverse Leakage Current, I_R	< 100 μA

● **Snubber Circuit**

In case the serge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 10-1);

- A clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P.
- A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D pin and the GND pin.
  In case the damper snubber circuit is added, this components should be connected near D pin and S/OCP pin.

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● **Phase Compensation**

A typical phase compensation circuit with a secondary shunt regulator (U51) is shown in Figure 10-3.

C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047 µF to 0.47 µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

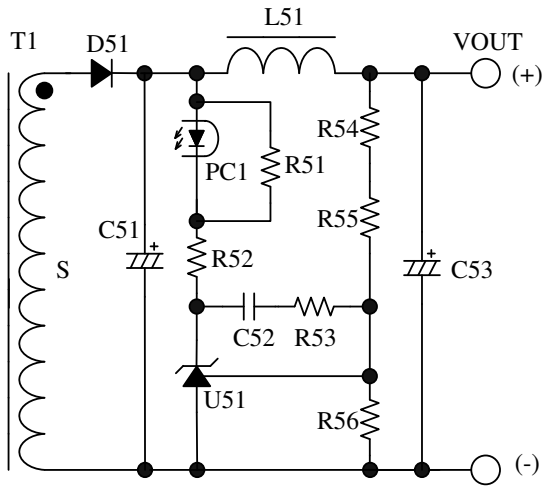


Figure 10-3. Peripheral circuit around secondary shunt regulator (U51)

• **Transformer**

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection function (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3…) should be maximized to improve the line-regulation of those outputs.

Figure 10-4 shows the winding structural examples of two outputs.

Winding structural example (a):

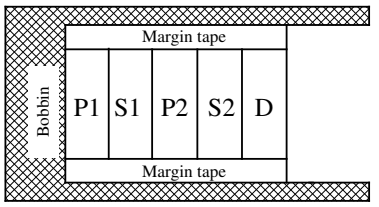
S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.

D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

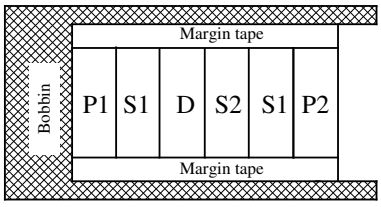
Winding structural example (b)

P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.

D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.



Winding structural example (a)



Winding structural example (b)

Figure 10-4. Winding structural examples

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10.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-5 shows the circuit design example.

(1) Main Circuit Trace Layout: S/OCP pin to R_{OCP} to C1 to T1 (winding P) to D pin
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible. If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 10-5 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout: GND pin to C2 (negative) to T1 (winding D) to R2 to D2 to C2 (positive) to VCC pin
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) R_{OCP} Trace Layout
R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 10-5) which is close to the base of R_{OCP}.

(5) FB/OLP Trace Layout
The components connected to FB/OLP pin should be as close to FB/OLP pin as possible. The trace between the components and FB/OLP pin should be as short as possible.

(6) Secondary Rectifier Smoothing Circuit Trace Layout: T1 (winding S) to D51 to C51
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the D pin trace act as a heatsink, its traces should be as wide as possible.

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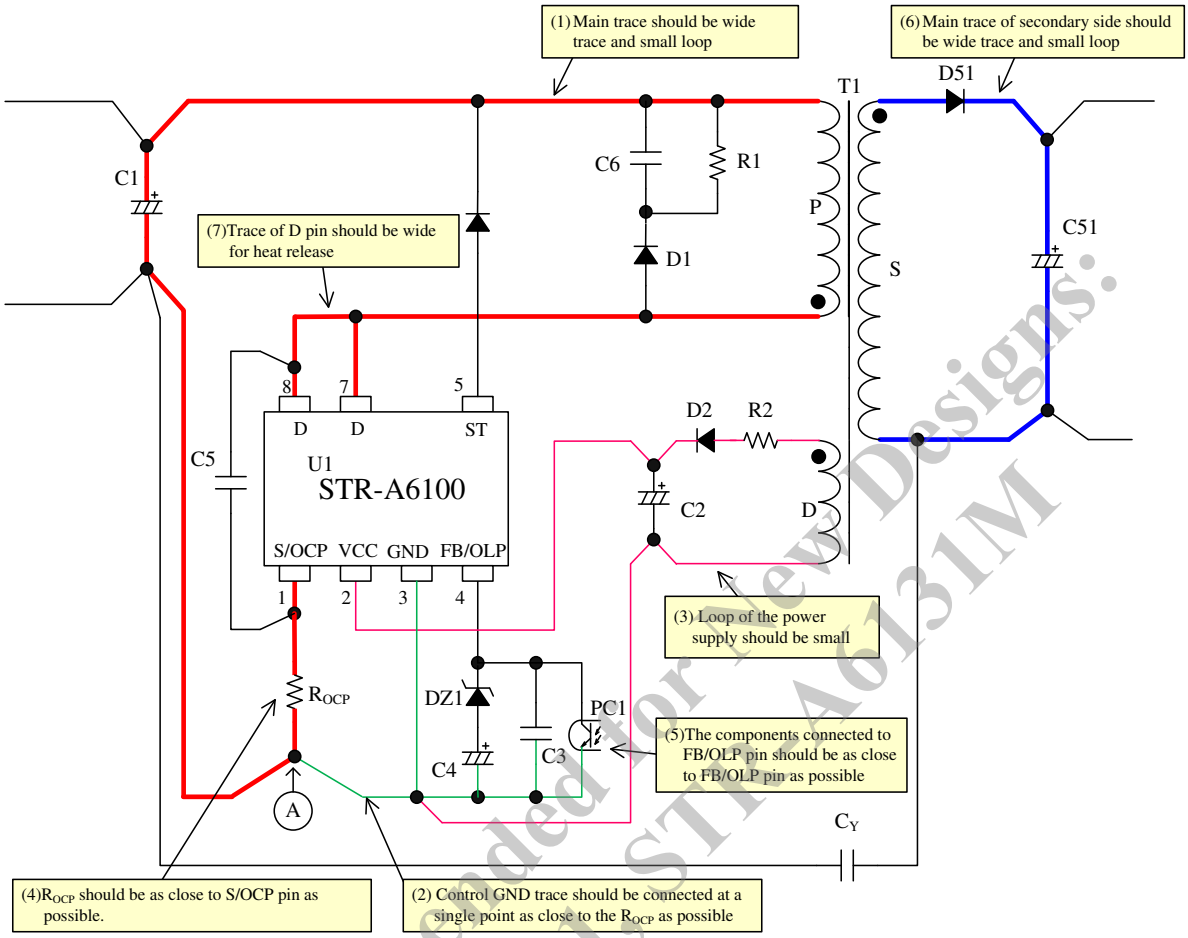


Figure 10-5. Example of peripheral circuit around the IC

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11.Pattern Layout Example

The following show the PCB pattern layout example and the circuit schematic with STR-A6100 series (DIP7).

Top view

Bottom view

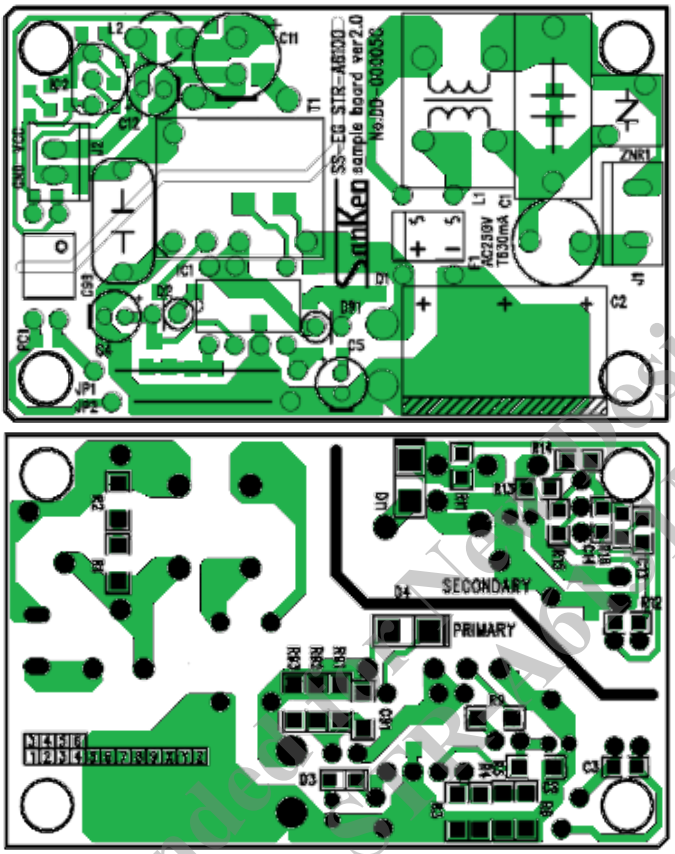


Figure 11-1 PCB circuit trace layout example

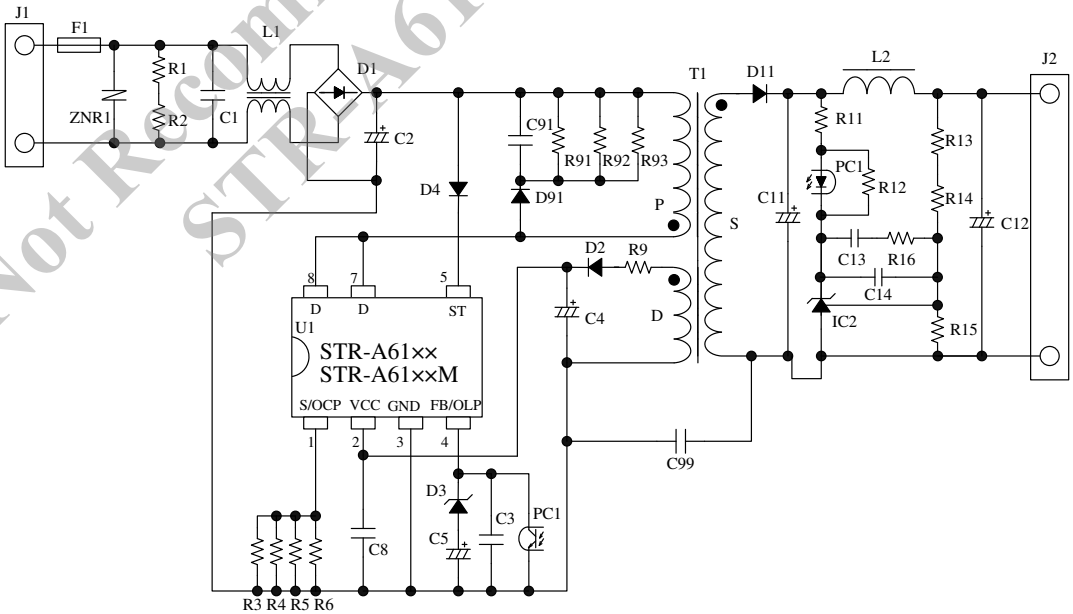


Figure 11-2 Circuit schematic for PCB circuit trace layout

The above circuit symbols correspond to these of Figure 11-1.

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12.Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

- Power supply specification

IC	STR-A6159
Input voltage	AC 85 V to AC 265 V
Maximum output power	5 W
Output	5 V / 1 A

- Circuit schematic
  Refer to Figure 11-2

- Bill of materials

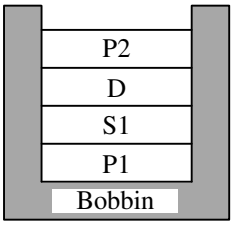
Symbol	Part type	Ratings(1)	Recommended Sanken Parts	Symbol	Part type	Ratings(1)	Recommended Sanken Parts
F1	Fuse	AC 250 V, 500 mA		R6	General, chip	10 Ω, 1/4 W	
L1 (2)	CM inductor	16.5 mH		R9 (2)	General, chip	0 Ω, 1/4 W	
ZNR1 (2)	Varistor	Open		R91	Metal oxide, chip	270 kΩ, 1/4 W	
D1	General	600 V, 1 A	AM01A (Axial)	R92	Metal oxide, chip	270 kΩ, 1/4 W	
D2	Fast recovery	200 V, 1 A	AL01Z	R93	Metal oxide, chip	270 kΩ, 1/4 W	
D3	Zener, chip	5.1 V		PC1	Photo-coupler	PC123 or equiv	
D4	General, chip	200 V, 1 A		IC1	IC	—	STR-A6159
D91	Fast recovery	1000 V, 0.2 A	EG01C	T1	Transformer	See the specification	
C1 (2)	Film	0.15 µF, 270 V		L2 (2)	Inductor	2.2 µF	
C2	Electrolytic	22 µF, 450 V		D11	Schottky, chip	60 V, 2 A	SJPB-H6
C3	Ceramic, chip	4700 pF, 50 V		C11	Electrolytic	680 µF, 10 V	
C4	Electrolytic	22 µF, 50 V		C12	Electrolytic	220 µF, 10 V	
C5	Electrolytic	2.2 µF, 50 V		C13	Ceramic, chip	0.1 µF, 50 V	
C8 (2)	Ceramic, chip	0.33 µF, 50 V		C14 (2)	Ceramic, chip	Open	
C91	Ceramic, chip	1000 pF, 630 V		R11	General, chip	220 Ω, 1/8 W	
C99 (2)	Ceramic, Y1	2200 µF, AC 250 V		R12	General, chip	1.5 kΩ, 1/8 W	
R1 (2)	General, chip	Open		R13 (2)	General, chip, 1%	0 Ω, 1/8 W	
R2 (2)	General, chip	Open		R14	General, chip, 1%	10 kΩ, 1/8 W	
R3	General, chip	10 Ω, 1/4 W		R15	General, chip, 1%	10 kΩ, 1/8 W	
R4	General, chip	10 Ω, 1/4 W		R16	General, chip	47kΩ, 1/8 W	
R5	General, chip	10 Ω, 1/4 W		IC2	Shunt regulator	V_{REF} = 2.5 V TL431 or equiv	

(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

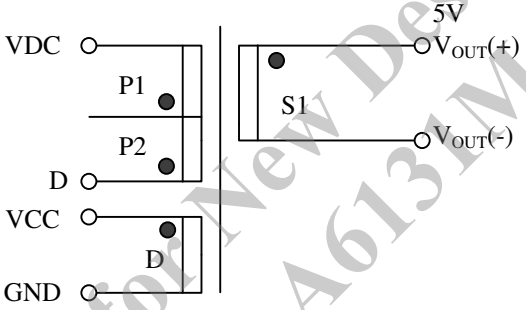
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- Transformer specification
  - Primary inductance, L_P : 3.1 mH
  - Core size : EI-16
  - Al-value : 114 nH/N^2 (Center gap of about 0.188 mm)
  - Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction
Primary winding	P1	66	φ 0.18 UEW	Double-layer, solenoid winding
Primary winding	P2	99	φ 0.18 UEW	Triple-layer, solenoid winding
Auxiliary winding	D	29	φ 0.18 UEW	Solenoid winding
Output	S1	11	φ 0.4 × 3 TIW	Solenoid winding



Cross-section view



● : Start at this pin

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