Quasi-Resonant Controllers with Integrated Power MOSFET

STR-Y6700 Series

General Descriptions

The STR-Y6700 series are power ICs for switching power supplies, incorporating a MOSFET and a quasi-resonant controller IC.

Including an auto standby function in the controller, the product achieves the low standby power by the automatic switching between the quasi-resonant operation in normal operation, one bottom-skip operation under medium to light load conditions and the burst-oscillation under light load conditions.

The product achieves high cost-performance power supply systems with few external components.

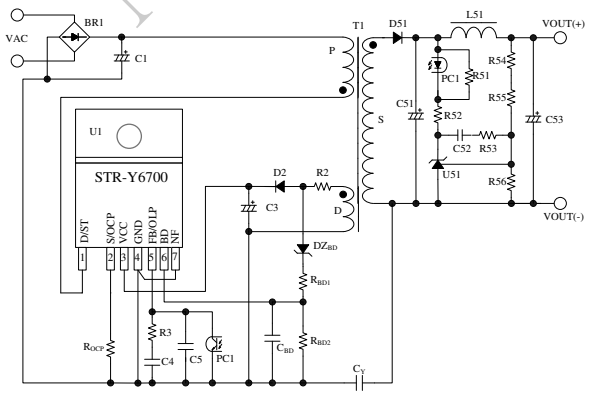
Features

- Multi-mode Control
  The optimum operation depending on load conditions is changed automatically and is achieved high efficiency operation across the full range of loads.

  Operation Mode
  Normal load ----------Quasi-resonant mode
  Medium to light load----------One bottom-skip mode
  Light load ---------- Burst oscillation mode
  (Auto standby function)
- No load power consumption
  P_{IN} < 30 mW (100VAC)
  P_{IN} < 50 mW (230VAC)
- Leading Edge Blanking Function
- Bias Assist Function
- Built-in startup circuit reduces
- Protections
  Overcurrent Protection 1 (OCP1): Pulse-by-Pulse, with Input Compensation Function
  Overcurrent Protection 2 (OCP2)[1]: Latched shutdown
  Overload Protection (OLP): Latched shutdown
  Overvoltage Protection (OVP): Latched shutdown
  Thermal Shutdown Protection (TSD): Latched shutdown

[1] Products with the last letter "A" don't have the OCP2 function.

Typical Application



Package

TO220F-7L



Not to Scale

Lineup

- Electrical Characteristics

Products	V_{DSS}(min.)	$R_{DS(ON)}$(max.)
STR–Y6735 STR–Y6735A	500 V	0.8 Ω
STR–Y6753	650 V	1.9 Ω
STR–Y6754		1.4 Ω
STR–Y6766 STR–Y6766A	800 V	1.7 Ω
STR–Y6765		2.2 Ω
STR–Y6763 STR–Y6763A		3.5 Ω

- Output Power, P_{OUT}[2]

Products	P_{OUT} (Open frame)	
	380VDC	85~265VAC
STR–Y6735 STR–Y6735A	120 W(100VAC)	–
STR–Y6753	100 W	60 W
STR–Y6754	120 W	67 W
STR–Y6766 STR–Y6766A	140 W	80 W
STR–Y6765	120 W	70 W
STR–Y6763 STR–Y6763A	80 W	50 W

[2] The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, ON Duty, and thermal design affect the output power. It may be less than the value stated here.

Applications

- White goods
- Office automation equipment
- Industrial equipment

Not Recommended for New Designs

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1. Absolute Maximum Ratings

- Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).
- Unless otherwise specified T_A = 25 °C

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Remarks
Drain Peak Current(1)	I_{DPEAK}	Single pulse	1 – 2	6.7	A	STR–Y6763 / 63A
				8.9		STR–Y6765
				9.2		STR–Y6753
				10.5		STR–Y6766 / 66A
				11.0		STR–Y6754
				14.6		STR–Y6735 / 35A
Maximum Switching Current(2)	I_{DMAX}	Single pulse Ta= −20 to 125°C	1 – 2	6.7	A	STR–Y6763 / 63A
				8.9		STR–Y6765
				9.2		STR–Y6753
				10.5		STR–Y6766 / 66A
				11.0		STR–Y6754
				14.6		STR–Y6735 / 35A
Avalanche Energy(3)(4)	E_{AS}	I_{LPEAK}=2.3A	1 – 2	60	mJ	STR–Y6763 / 63A
		I_{LPEAK}=2.6A		77		STR–Y6765
		I_{LPEAK}=2.9A		99		STR–Y6753
		I_{LPEAK}=3.2A		116		STR–Y6766 / 66A
		I_{LPEAK}=4.1A		198		STR–Y6754
		I_{LPEAK}=3.5A		152		STR–Y6735 / 35A
D/ST Pin Voltage	$V_{STARTUP}$		1 − 4	−1.0 to V_{DSS}	V	
S/OCP Pin Voltage	V_{OCP}		2 – 4	−2.0 to 6.0	V	
VCC Pin Voltage	V_{CC}		3 – 4	35	V	
FB/OLP Pin Voltage	V_{FB}		5 – 4	−0.3 to 7.0	V	
FB/OLP Pin Sink Current	I_{FB}		5 – 4	10.0	mA	
BD Pin Voltage	V_{BD}		6 – 4	− 6.0 to 6.0	V	
Power Dissipation(5)	P_{D1}	With infinite heatsink	1 – 2	19.9	W	STR–Y6763 / 63A
				21.8		STR–Y6765
				20.2		STR–Y6753
				23.6		STR–Y6766 / 66A
				21.5		STR–Y6735 / 35A STR–Y6754
		Without heatsink	1 – 2	1.8	W	
Control Part Power Dissipation	P_{D2}	V_{CC}×I_{CC}	3 – 4	0.8	W	
Internal Frame Temperature in Operation	T_F		−	−40 to 115	°C	
Operating Ambient Temperature	T_{OP}		−	−40 to 115	°C	
Storage Temperature	T_{stg}		−	−40 to 125	°C	
Junction Temperature	T_{ch}		−	150	°C	

(1) Refer to 3.3 MOSFET Safe Operating Area Curves
(2) The maximum switching current is the drain current determined by the drive voltage of the IC and threshold voltage (V_{th}) of the MOSFET.
(3) Refer to Figure 3-2 Avalanche Energy Derating Coefficient Curve
(4) Single pulse, V_{DD} = 99 V, L = 20 mH
(5) Refer to 3.2 T_A-P_{D1}curves.

Not Recommended for New Designs

2. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A = 25 °C, V_{CC} = 20 V

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		3 − 4	13.8	15.1	17.3	V	
Operation Stop Voltage[1]	$V_{CC(OFF)}$		3 − 4	8.4	9.4	10.7	V	
Circuit Current in Operation	$I_{CC(ON)}$		3 − 4	−	1.3	3.7	mA	
Circuit Current in Non-Operation	$I_{CC(OFF)}$	V_{CC} = 13 V	3 − 4	−	4.5	50	µA	
Startup Circuit Operation Voltage	$V_{START(ON)}$		1 − 4	42	57	72	V	
Startup Current	$I_{CC(STARTUP)}$	V_{CC} = 13 V	3 − 4	− 4.5	− 3.1	− 1.0	mA	
Startup Current Biasing Threshold Voltage	$V_{CC(BIAS)}$		3 − 4	9.5	11.0	12.5	V	
PWM Switching Frequency	f_{OSC}		1 − 4	18.4	21.0	24.4	kHz	
Soft Start Operation Duration	t_{SS}		1 − 4	−	6.05	−	ms	
Normal Operation								
Bottom-Skip Operation Threshold Voltage 1	$V_{OCP(BS1)}$		2 − 4	0.487	0.572	0.665	V	
Bottom-Skip Operation Threshold Voltage 2	$V_{OCP(BS2)}$		2 − 4	0.200	0.289	0.380	V	
Quasi-Resonant Operation Threshold Voltage 1	$V_{BD(TH1)}$		6 − 4	0.14	0.24	0.34	V	
Quasi-Resonant Operation Threshold Voltage 2[2]	$V_{BD(TH2)}$		6 − 4	0.07	0.17	0.27	V	
Maximum Feedback Current	$I_{FB(MAX)}$		5 − 4	−320	−205	−120	µA	
Standby Operation								
Standby Operation Threshold Voltage	$V_{FB(STBOP)}$		5 − 4	0.45	0.80	1.15	V	
Protected Operation								
Maximum On-Time	$t_{ON(MAX)}$		1 − 4	30.0	40.0	50.0	µs	
Leading Edge Blanking Time	$t_{ON(LEB)}$		1 − 4	−	455	−	ns	STR–Y6735 / 35A/ 65/ 66/ 54
				−	470	−		STR–Y6763 / 63A/ 53
Overcurrent Detection 1 Threshold Voltage in Input Compensation Operation	$V_{OCP(L)}$	V_{BD} = –3V	2 − 4	0.560	0.660	0.760	V	
Overcurrent Detection 1 Threshold Voltage in Normal Operation	$V_{OCP(H)}$	V_{BD} = 0V	2 − 4	0.820	0.910	1.000	V	
Overcurrent Detection 2 Threshold Voltage	$V_{OCP(La.OFF)}$		2 − 4	1.65	1.83	2.01	V	Products without the last letter "A"

[1] $V_{CC(OFF)} < V_{CC(BIAS)}$ always.
[2] $V_{BD(TH2)} < V_{BD(TH1)}$ always.

Not Recommended for New Designs

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
BD Pin Source Current	$I_{BD(O)}$		6 − 4	− 250	− 83	− 30	µA	
OLP Bias Current	$I_{FB(OLP)}$		5 − 4	− 15	− 10	− 5	µA	
OLP Threshold Voltage	$V_{FB(OLP)}$		5 − 4	5.50	5.96	6.40	V	
FB Pin Maximum Voltage in Feedback Operation	$V_{FB(MAX)}$		5 − 4	3.70	4.05	4.40	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		3− 4	28.5	31.5	34.0	V	
Thermal Shutdown Operating Temperature	$T_{j(TSD)}$		−	135	−	−	°C	
MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}	I_{DS}=300µA	1 – 2	500	−	−	V	STR-Y6735 / 35A
				650	−	−		STR-Y6753 / 54
				800	−	−		STR-Y6763 / 63A / 65 /66 /66A
Drain Leakage Current	I_{DSS}	V_{DS}=V_{DSS}	1 – 2	−	−	300	µA	
On Resistance	$R_{DS(ON)}$		1 – 2	−	−	0.8	Ω	STR-Y6735 / 35A
				−	−	1.4		STR–Y6754
						1.7		STR–Y6766 / 66A
						1.9		STR–Y6753
						2.2		STR–Y6765
				−	−	3.5		STR–Y6763 / 63A
Switching Time	t_f		1 – 2	−	−	250	ns	STR–Y6753 / 63 / 63A
				−	−	300	ns	STR-Y6735 / 35A / 54 / 66 / 66A / 65
Thermal Resistance								
Channel to Frame Thermal Resistance(3)	θ_{ch-F}		−	−	2.4	2.7	°C/W	STR-Y6735 / 35A / 54
				−	1.9	2.2		STR–Y6766 / 66A
				−	2.7	3.1		STR–Y6753
				−	2.3	2.6		STR–Y6765
				−	2.8	3.2		STR–Y6763 / 63A
Channel to Case Thermal Resistance(4)	θ_{ch-C}		−	−	5.1	5.9	°C/W	STR-Y6735 / 35A / 54
				−	4.6	5.3		STR–Y6766 / 66A
				−	5.4	6.2		STR–Y6753
				−	5.0	5.8		STR–Y6765
				−	5.5	6.3		STR–Y6763 / 63A

Not Recommended for New Designs

(3) θ_{ch-F} is thermal resistance between channel and internal frame.
(4) θ_{ch-C} is thermal resistance between channel and case. Case temperature is measured at the backside surface.

3. Performance Curves

3.1 Derating Curves

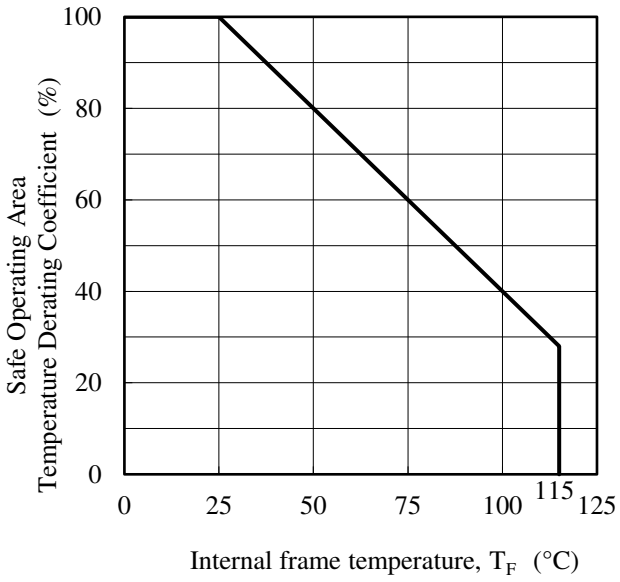


Figure 3-1 SOA Temperature Derating Coefficient Curve

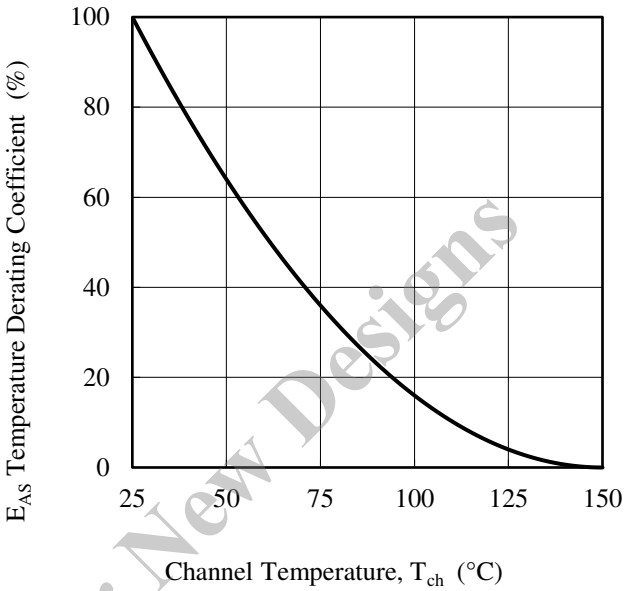
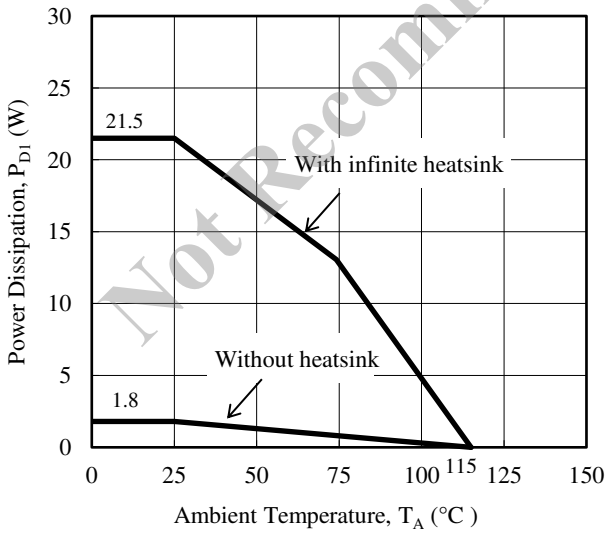


Figure 3-2 Avalanche Energy Derating Coefficient Curve

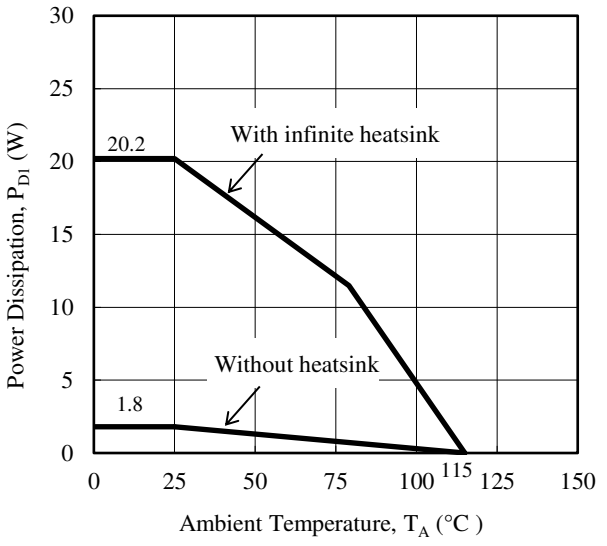
Not Recommended for New Designs

3.2 Ambient Temperature versus Power Dissipation Curves

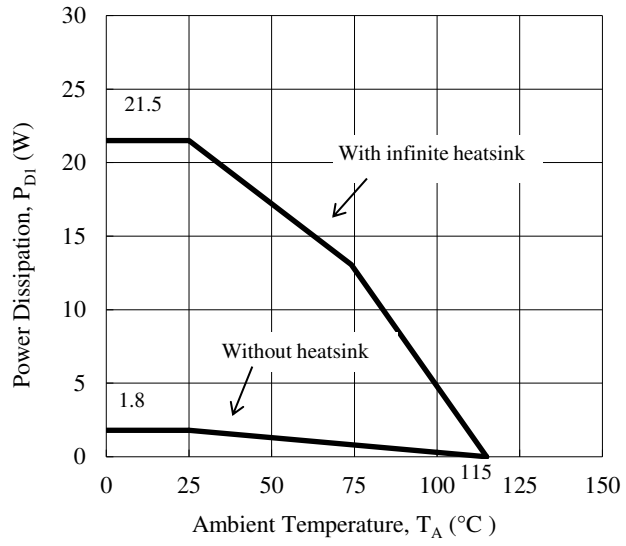
• **STR–Y6735、STR–Y6735A**



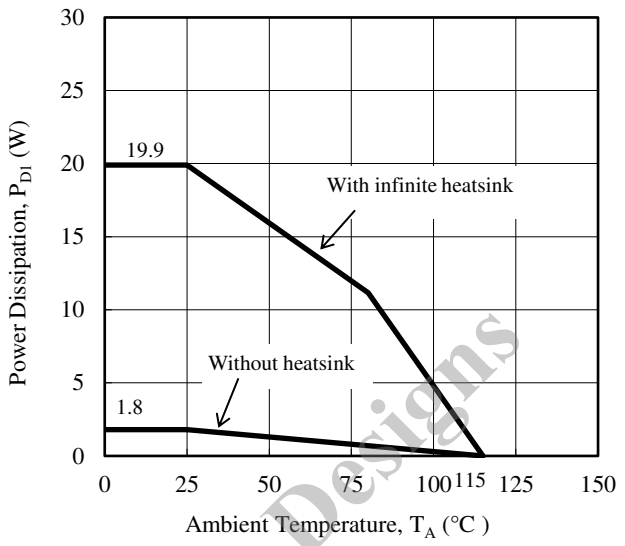
• **STR–Y6753**



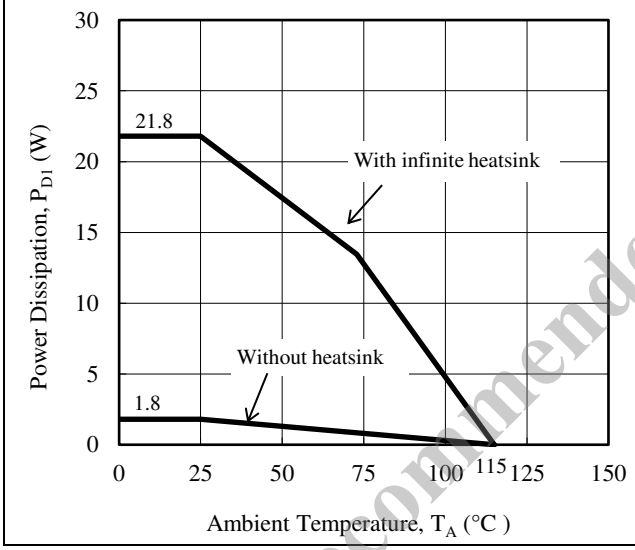
• **STR–Y6754**



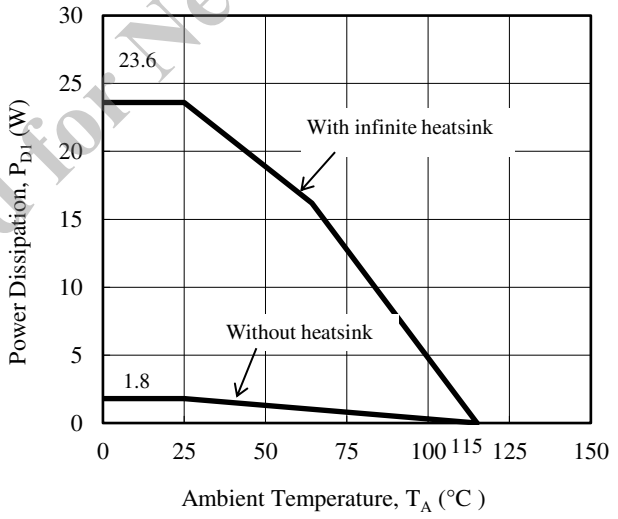
• **STR–Y6763、STR–Y6763A**



• **STR–Y6765**



• **STR–Y6766、STR–Y6766A**

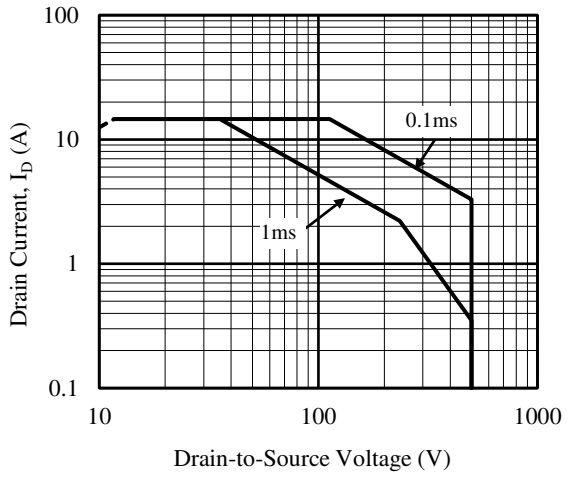


Not Recommended for New Designs

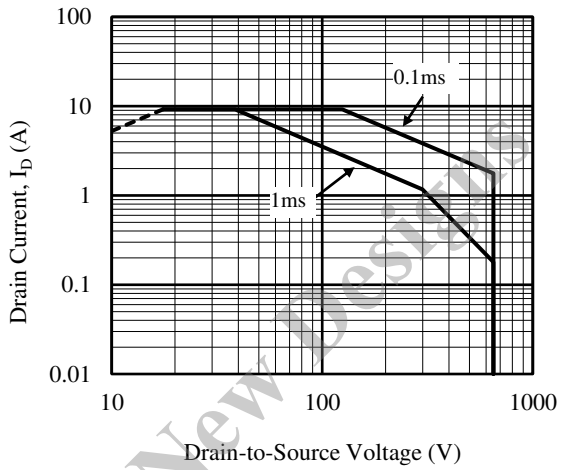
3.3 MOSFET Safe Operating Area Curves

- When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 3-1.
- The broken line in the safe operating area curve is the drain current curve limited by on-resistance.
- Unless otherwise specified, T_A = 25 °C, Single pulse

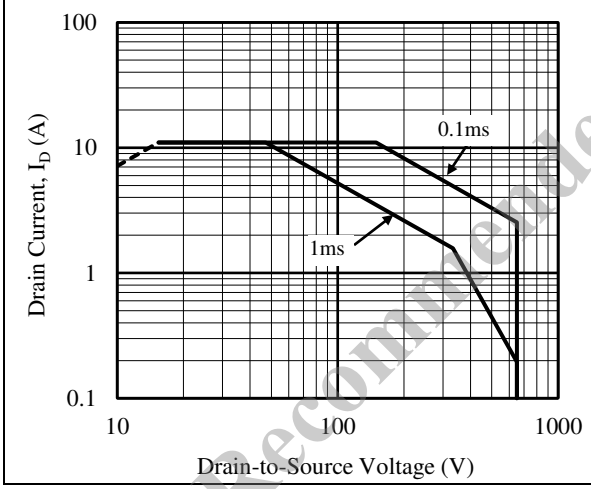
• STR–Y6735, STR–Y6735A



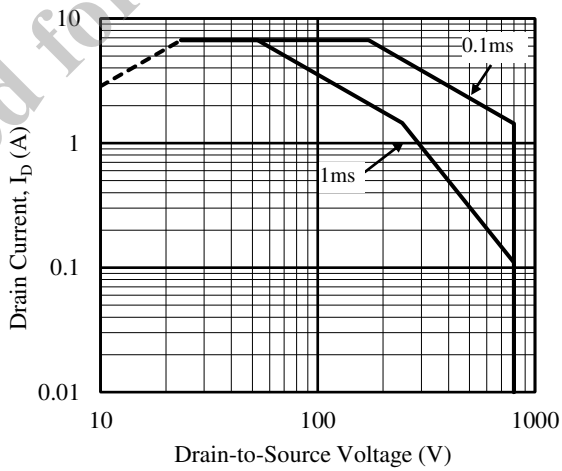
• STR–Y6753



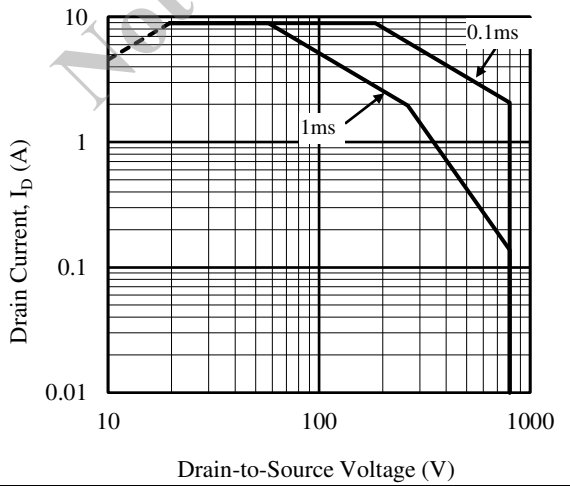
• STR–Y6754



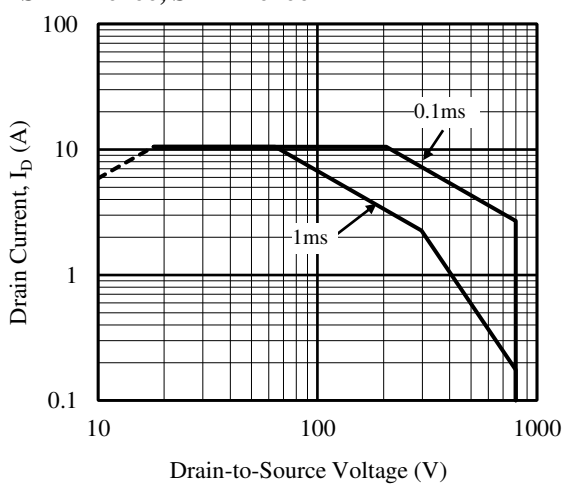
• STR–Y6763, STR–Y6763A



• STR–Y6765



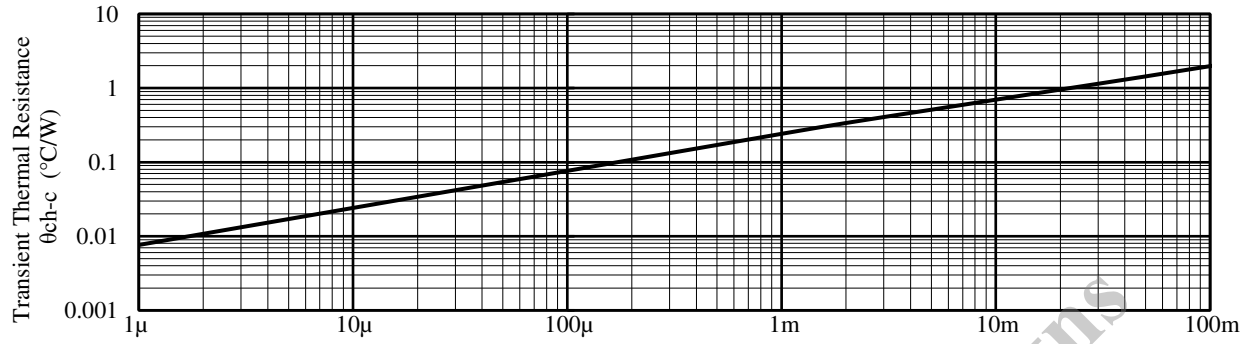
• STR–Y6766, STR–Y6766A



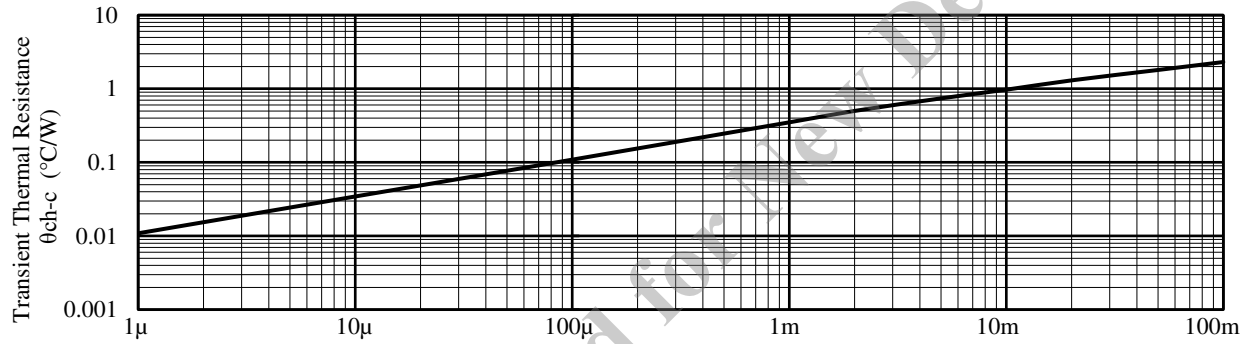
Not Recommended for New Designs

3.4 Transient Thermal Resistance Curves

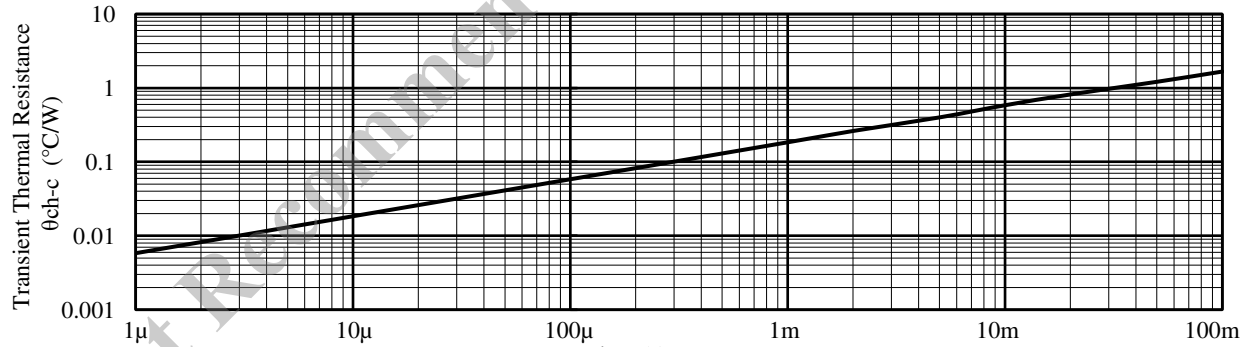
• **STR–Y6735, STR–Y6735A, STR–Y6754, STR–Y6765**



• **STR–Y6753, STR–Y6763, STR–Y6763A**

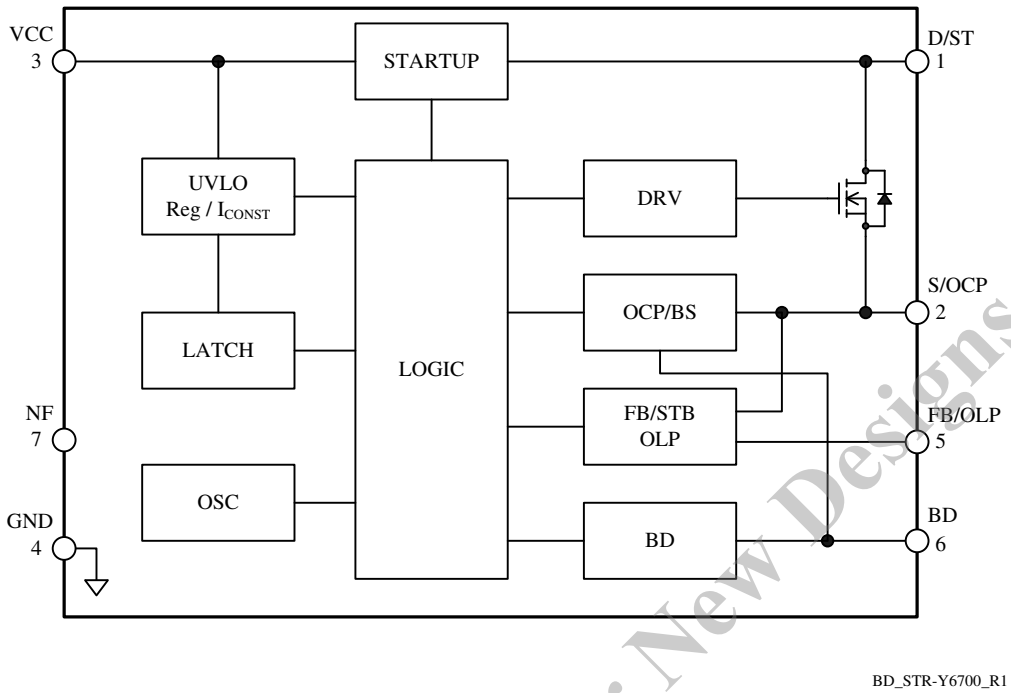


• **STR–Y6766, STR–Y6766A**

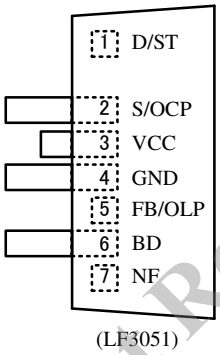


Not Recommended for New Designs

4. Block Diagram



5. Pin Configuration Definitions



Pin	Name	Descriptions
1	D/ST	MOSFET drain and startup current input
2	S/OCP	MOSFET source and overcurrent protection (OCP) signal input
3	VCC	Power supply voltage input for control part and overvoltage protection (OVP) signal input
4	GND	Ground
5	FB/OLP	Constant voltage control signal input and over load protection (OLP) signal input
6	BD	Bottom Detection signal input, Input Compensation detection signal input
7	NF*	(Non-function)

*For stable operation, NF pin should be connected to GND pin, using the shortest possible path.

Not Recommended for New Designs

6. Typical Application

- The PCB traces D/ST pins should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that D/ST pin has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.
- For stable operation, NF pin should be connected to GND pin, using the shortest possible path.

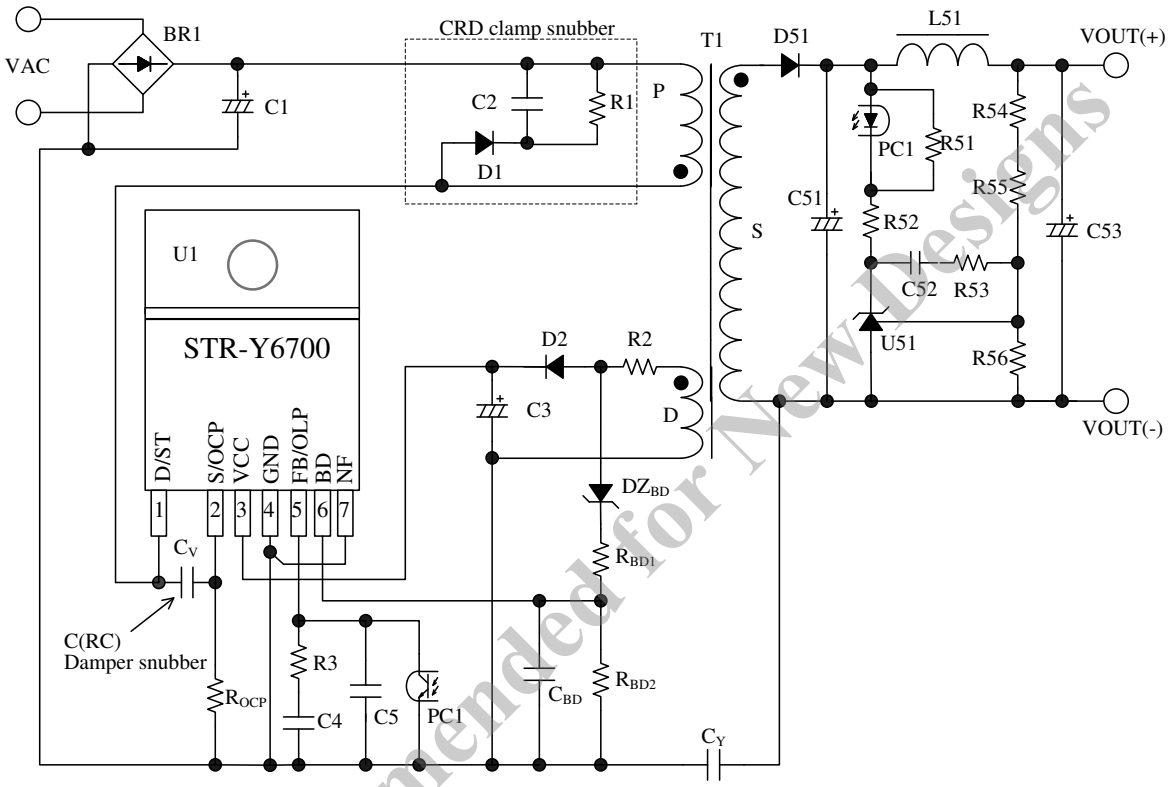
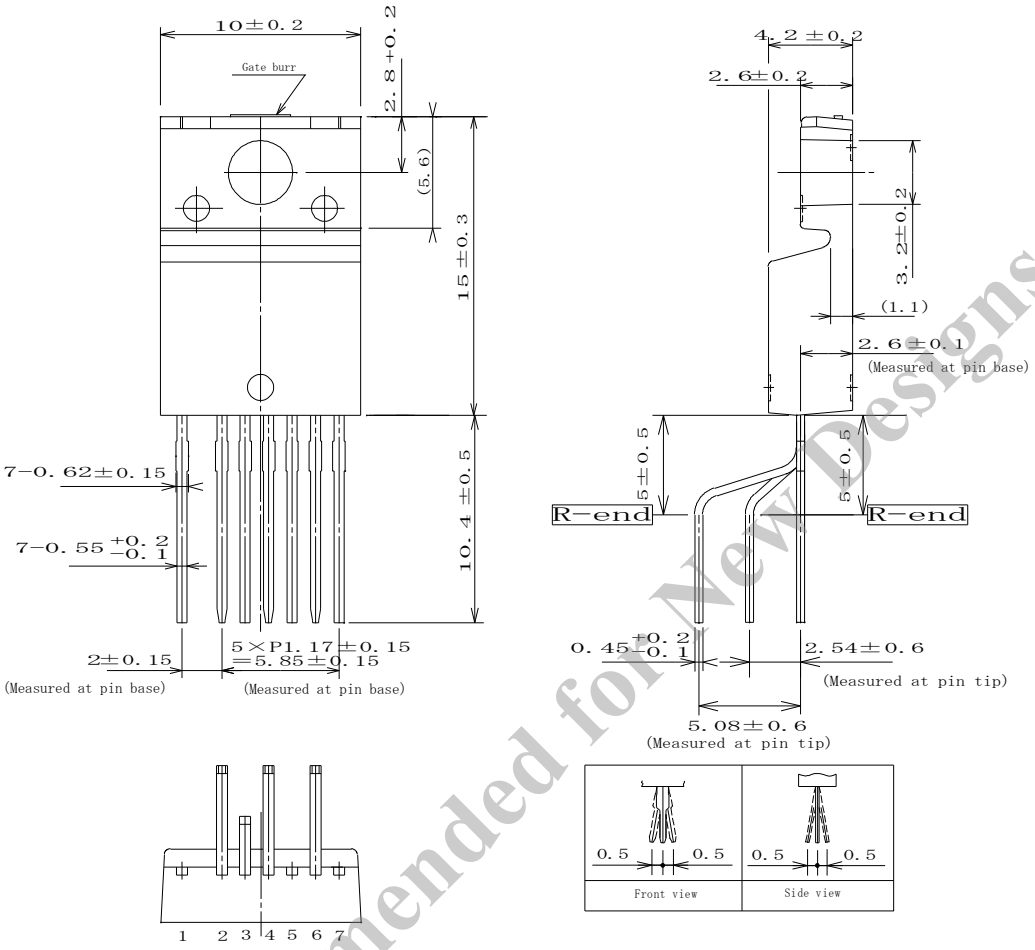


Figure 6-1 Typical application

Not Recommended for New Designs

7. Physical Dimensions

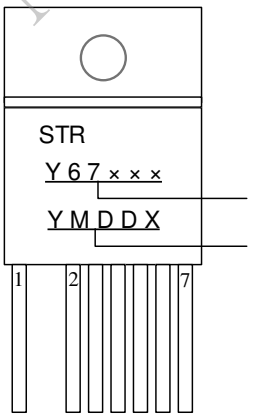
• TO220F-7L



NOTES :
1) Dimension is in millimeters.
2) Leadform: LF No.3051
3) Gate burr indicates protrusion of 0.3 mm (max.).
4) Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Not Recommended for New Designs

8. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N or D)
DD is the day of the month (01 to 31)
X is the control number

9. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

9.1 Startup Operation

Figure 9-1 shows the circuit around IC. Figure 9-2 shows the start up operation.

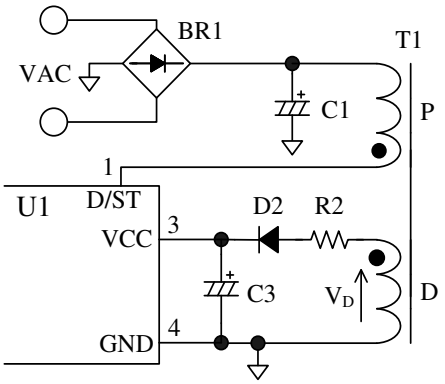


Figure 9-1 VCC pin peripheral circuit

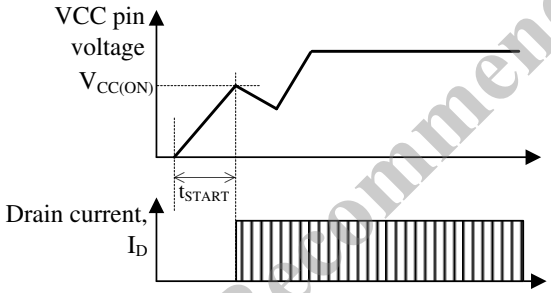


Figure 9-2 Startup operation

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{START(ON)}$ = 57 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{CC(STARTUP)}$ = − 3.1 mA, charges C3 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.1 V, the control circuit starts operation. During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 9-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate value of auxiliary winding voltage is about 20 V, taking account of the winding turns of D winding so that VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 12.5\ (\text{V}) < V_{CC} < 28.5\ (\text{V}) \quad (1)$$

The startup time of IC is determined by C3 capacitor value. The approximate startup time t_{START} (shown in Figure 9-2) is calculated as follows:

$$t_{START} = C3 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left| I_{CC(STRATUP)} \right|} \quad (2)$$

where,
t_{START} : Startup time of IC (s)
$V_{CC(INT)}$: Initial voltage on VCC pin (V)

9.2 Undervoltage Lockout (UVLO)

Figure 9-3 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.4 V, the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

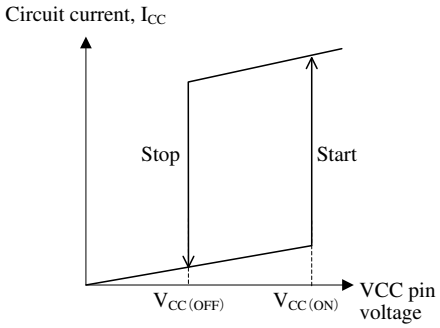


Figure 9-3 Relationship between VCC pin voltage and I_{CC}

9.3 Bias Assist Function

By the Bias Assist Function, the startup failure is prevented and the latched state is kept.

The Bias Assist function is activated, when the VCC voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 11.0 V, in either of following condition:
the FB pin voltage is the Standby Operation Threshold Voltage, $V_{FB(STBOP)}$ = 0.80 V or less
or the IC is in the latched state due to activating the protection function.

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When the Bias Assist Function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the Bias Assist Function, the value of C3 connected to VCC pin can be small. Thus, the startup time and the response time of the OVP become shorter.

The operation of the Bias Assist Function in startup is as follows. It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 9-4 shows VCC pin voltage behavior during the startup period.

After VCC pin voltage increases to $V_{CC(ON)}$ = 15.1 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. At the same time, the auxiliary winding voltage V_D increases in proportion to output voltage. These are all balanced to produce VCC pin voltage.

When VCC pin voltage is decrease to $V_{CC(OFF)}$ = 9.4 V in startup operation, the IC stops switching operation and a startup failure occurs.

When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to the Standby Operation Threshold Voltage, $V_{FB(STBOP)}$ = 0.80 V, or less, the IC stops switching operation and VCC pin voltage decreases. When VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist function is activated and the startup failure is prevented.

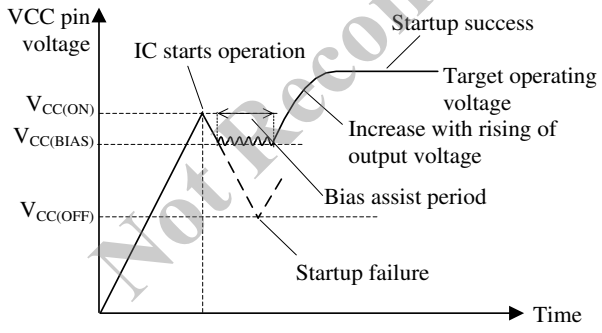

Figure 9-4 VCC pin voltage during startup period

9.4 Soft Start Function

Figure 9-5 shows the behavior of VCC pin voltage, drain current and BD pin voltage during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start is fixed to t_{SS} = 6.05 ms. During the soft start period, over current threshold is increased step-wisely (4 steps). This function reduces the voltage and the current stress of MOSFET and secondary side rectifier diode.

During the soft start operation period, the operation is in PWM operation, at an internally set operation frequency, f_{OSC} = 21.0 kHz.

Until BD pin voltage becomes the following condition after the soft start time, the switching operation is PWM control of f_{OSC} = 21.0 kHz.

When BD pin voltage, V_{BD}, becomes the following condition, the IC starts quasi-resonant operation.

Quasi-resonant operation starting condition

- $V_{BD} \geq V_{BD(TH1)}$ = 0.24 V
- The effective pulse width of quasi-resonant signal is 1.0 µs or more (refer to Figure 9-12)

After the soft start period, D/ST pin current, I_D, is limited by the overcurrent protection (OCP), until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

When t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the OLP operation (OLP).

Thus, the t_{OLP} must be set longer than t_{LIM} (refer to Section 9.12).

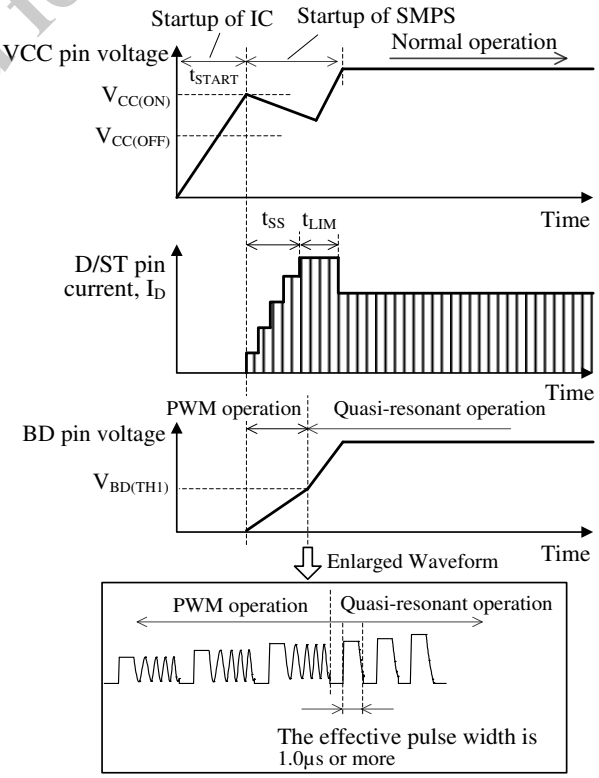

Figure 9-5 V_{CC} and I_D and V_{BD} behavior during startup

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9.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 9-6 and Figure 9-7. V_{SC} is generated by the FB/OLP pin voltage.

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

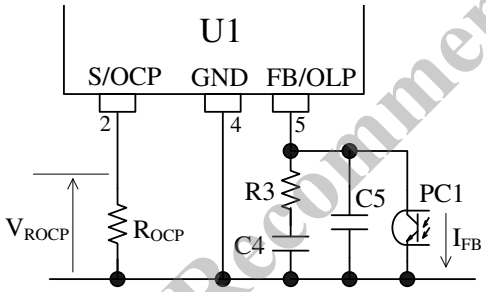

Figure 9-6 FB/OLP pin peripheral circuit

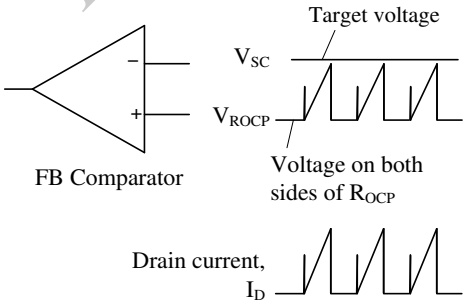

Figure 9-7 Drain current, I_D, and FB comparator operation in steady operation

9.6 Leading Edge Blanking Function

The IC uses the peak-current-mode control method for the constant voltage control of output.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or overcurrent protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, $t_{ON(LEB)}$ is built-in. During $t_{ON(LEB)}$, the OCP threshold voltage becomes $V_{OCP(La.OFF)}$ = 1.83 V in order not to respond to the turn-on drain current surge (refer to Section 9.11).

9.7 Quasi-Resonant Operation and Bottom-On Timing Setup

9.7.1 Quasi-Resonant Operation

Using quasi-resonant operation, switching loss and switching noise are reduced and it is possible to obtain converters with high efficiency and low noise. This IC performs quasi-resonant operation during one bottom-skip operation.

Figure 9-8 shows the circuit of a flyback converter. The meaning of symbols in Figure 9-8 is shown in Table 9-1. A flyback converter is a system that transfers the energy stored in the transformer to the secondary side when the primary side power MOSFET is turned off. After the energy is completely transferred to the secondary, when the power MOSFET keeps turning off, the V_{DS} begins free oscillation based on the L_P and C_V.

The quasi-resonant operation is the bottom-on operation that the power MOSFET turns-on at the bottom point of free oscillation of V_{DS}.

Figure 9-9 shows an ideal V_{DS} waveform during bottom-on operation.

The delay time, t_{ONDLY}, is the time from starting free oscillation of V_{DS} to power MOSFET turn-on. The t_{ONDLY} of an ideal bottom-on operation is half cycle of the free oscillation, and is calculated using Equation (3).

$$t_{ONDLY} \fallingdotseq \pi\sqrt{L_P \times C_V} \quad (3)$$

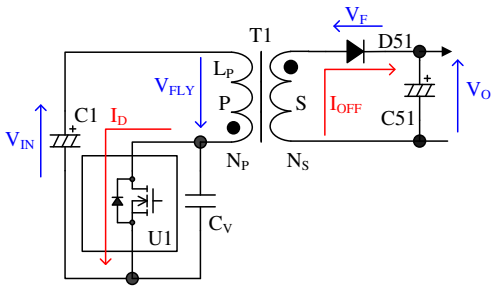

Figure 9-8 Basic flyback converter circuit

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Table 9-1 The meaning of symbols in Figure 9-8

Symbol	Descriptions
V_{IN}	Input voltage
V_{FLY}	Flyback voltage $V_{FLY} = \frac{N_P}{N_S} \times (V_O + V_F)$
V_{DS}	The voltage between Drain and Source of power MOSFET
N_P	Primary side number of turns
N_S	Secondary side number of turns
V_O	Output voltage
V_F	Forward voltage drop of the secondary side rectifier
I_D	Drain current of power MOSFET
I_{OFF}	Current which flows through the secondary side rectifier when power MOSFET is off
C_V	Voltage resonant capacitor
L_P	Primary side inductance

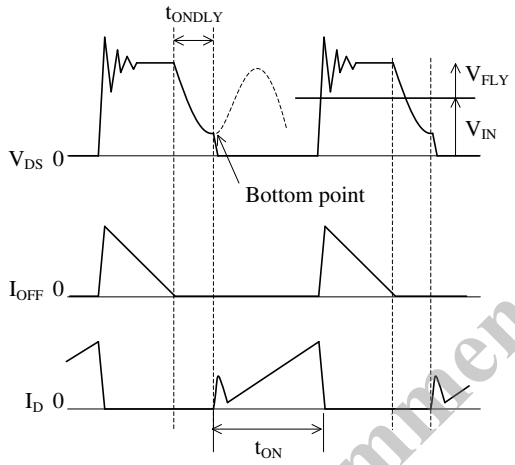

Figure 9-9 Ideal bottom-on operation waveform

9.7.2 Bottom-On Timing Setup

BD pin detects the signal of bottom-on timing and input compensation of OCP1 (refer to Section 9.11.3). Figure 9-10 shows the BD pin peripheral circuit, Figure 9-11 shows the waveform of auxiliary winding voltage.

The quasi-resonant signal, V_{REV2}, is proportional to auxiliary winding voltage, V_D and is calculated as follows:

$$V_{REV2} = \frac{R_{BD2}}{R_{BD1} + R_{BD2}} \times (V_{REV1} - V_F) \quad (4)$$

where,
V_{REV1}: Flyback voltage of auxiliary winding D
V_F: Forward voltage drop of Z_{BD}

The BD pin detects the bottom point using the V_{REV2}.

The threshold voltage of quasi-resonant operation has a hysteresis. $V_{BD(TH1)}$ is Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH2)}$ is Quasi-Resonant Operation Threshold Voltage 2.

When the BD pin voltage, V_{REV2}, increases to $V_{BD(TH1)}$ = 0.24 V or more at the power MOSFET turns-off, the power MOSFET keeps the off-state. After that, the V_{DS} decreases by the free oscillation. When the V_{DS} decreases to $V_{BD(TH2)}$ = 0.17 V, the power MOSFET turns-on and the threshold voltage goes up to $V_{BD(TH1)}$ automatically to prevent malfunction of the BD pin from noise interference.

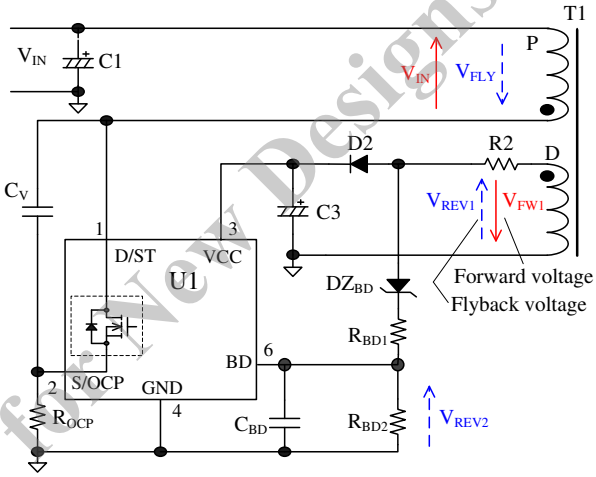

Figure 9-10 BD pin peripheral circuit

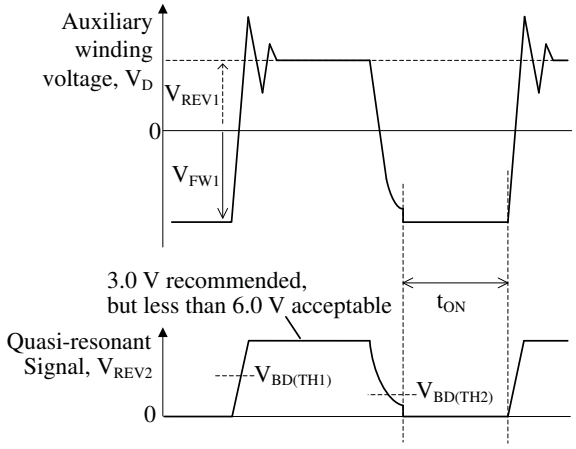

Figure 9-11 The waveform of auxiliary winding voltage

- R_{BD1} and R_{BD2} Setup
  R_{BD1} and R_{BD2} should be set so that V_{REV2} becomes the following range:
  Under the lowest condition of VCC pin voltage in power supply specification, $V_{REV2} \geq V_{BD(TH1)}$= 0.34 V(max.).
  Under the highest condition of VCC pin voltage in

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power supply specification, V_{REV2} < 6.0 V (Absolute maximum rating of the BD pin) and the effective pulse width of quasi-resonant signal is 1.0 µs or more (refer to Figure 9-12).
The value of V_{REV2} is recommended about 3.0 V.

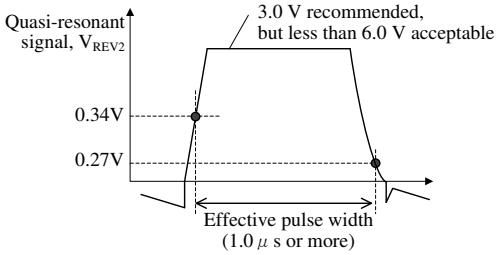

Figure 9-12 The effective pulse width of quasi-resonant signal

- C_{BD} Setup
  The delay time, t_{ONDLY}, until which the power MOSFET turns on, is adjusted by the value of C_{BD}, so that the power MOSFET turns on at the bottom-on of V_{DS} (refer to Figure 9-9).
  The initial value of C_{BD} is set about 1000 pF. C_{BD} is adjusted while observing the actual operation waveforms of V_{DS} and I_D under the maximum input voltage and the maximum output power (If a voltage probe is connected to BD pin, the bottom point may misalign).
  If the turn-on point precedes the bottom of the V_{DS} signal (see Figure 9-13), after confirming the initial turn-on point, delay the turn-on point by increasing the C_{BD} value gradually, so that the turn-on will match the bottom point of V_{DS}.

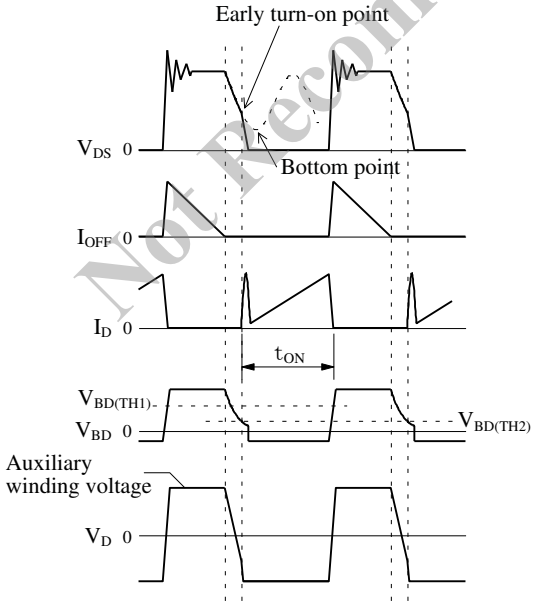

Figure 9-13 When the turn-on of a V_{DS} waveform occurs before a bottom point

In the converse situation, if the turn-on point lags behind the V_{DS} bottom point (Figure 9-14), after confirming the initial turn-on point, advance the turn-on point by decreasing the C_{BD} value gradually, so that the turn-on will match the bottom point of V_{DS}.

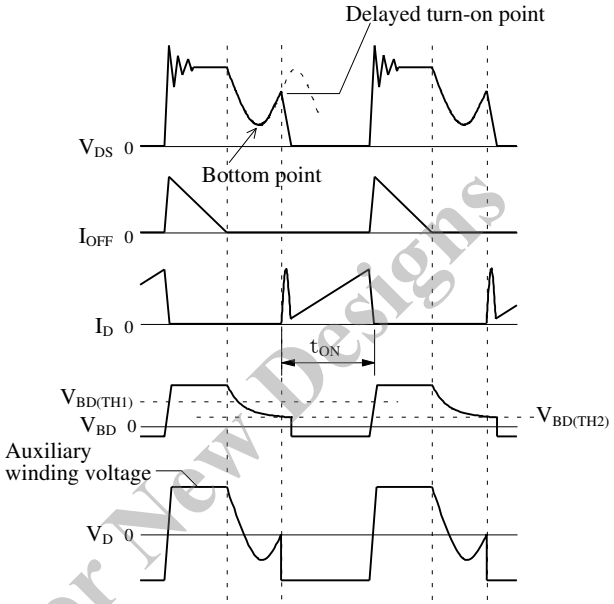

Figure 9-14 When the turn-on of a V_{DS} waveform occurs after a bottom point

9.8 BD Pin Blanking Time

Since the auxiliary winding voltage is input to the BD pin, BD pin voltage may be affected from the surge voltage ringing when the power MOSFET turns off. If the IC detects the surge voltage as quasi-resonant signal, the IC may repeatedly turn the power MOSFET on and off at high frequency. This result in an increase of the MOSFET power dissipation and temperature, and it can be damaged.

The BD pin has a blanking period of 250 ns (max.) to avoid detecting voltage during this period.

The poor coupling (the high leakage inductance) tends to happen in a low output voltage transformer design with high N_P/ N_S turns ratio (N_P and N_S indicate the number of turns of the primary winding and secondary winding, respectively), and the surge voltage ringing of BD pin occurs easily (see Figure 9-15).

If the surge voltage continues longer than BD pin blanking period and the high frequency operation of power MOSFET occurs, the following adjustments are required so that the surge period of BD pin is less than 250 ns.

In addition, the BD pin waveform during operation should be measured by connecting test probes as short to the BD pin and the GND pin as possible, in order to measure any surge voltage correctly.

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- C_{BD} must be connected near the BD pin and the GND pin.
- The circuit trace loop between the BD pin and the GND pin must be separated from any traces carrying high current
- The coupling of the primary winding and the auxiliary winding must be good
- The clamping snubber circuit (refer to Figure 6-1) must be adjusted properly.

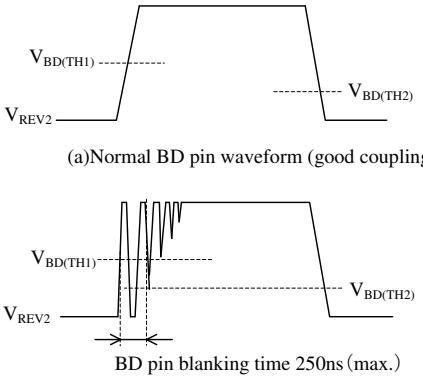

Figure 9-15 The difference of BD pin voltage, V_{REV2}, waveform by the coupling condition of the transformer

9.9 Multi-mode Control

When the output power decreases, the usual quasi-resonant control increases the switching frequency and the switching loss.

Thus, The IC has the multi-mode control to achieve high efficiency operation across the full range of loads.

The automatic multi-mode control changes among the following three operational modes according to the output loading state: normal quasi-resonant operation in heavy load, one bottom-skip quasi-resonant operation in medium to light load, and burst oscillation operation (auto standby function) in light load.

9.9.1 One Bottom-Skip Quasi-Resonant Operation

The one bottom-skip function limits the rise of the power MOSFET operation frequency in medium to light load in order to reduce the switching loss.

Figure 9-17 shows the operation state transition diagram of the output load from light load to heavy load. Figure 9-18 shows the state transition diagram from heavy load to light load.

As shown in Figure 9-16, in the process of the increase and decrease of load current, hysteresis is imposed at the time of each operational mode change. For this reason, the switching waveform does not become unstable near the threshold voltage of a change, and this enables the IC to switch in a stable operation.

Before the one bottom-skip point changed from heavy to light load, or after that done from light to heavy load, the switching frequency of the normal quasi-resonant operation becomes higher and the switching loss of power MOSFET increases. Thus, the temperature of the power MOSFET should be checked at higher switching frequency of the operation changing point in maximum AC input voltage.

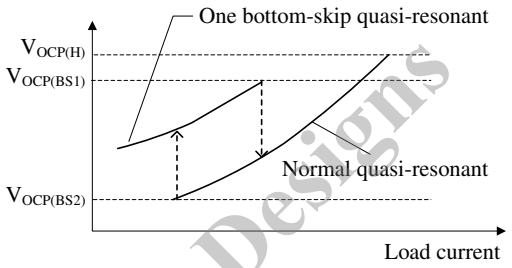

Figure 9-16 Hysteresis at the operational mode change

- The mode is changed from one bottom-skip quasi-resonant operation to normal quasi-resonant operation (light load to heavy load).
  When load is increased from one bottom-skip operation, the MOSFET peak drain current value will increase, and the positive pulse width will widen. Also, the peak value of the S/OCP pin voltage increases. When the load is increased further and the S/OCP pin voltage rises to $V_{OCP(BS1)}$, the mode is changed to normal quasi-resonant operation (see Figure 9-17).

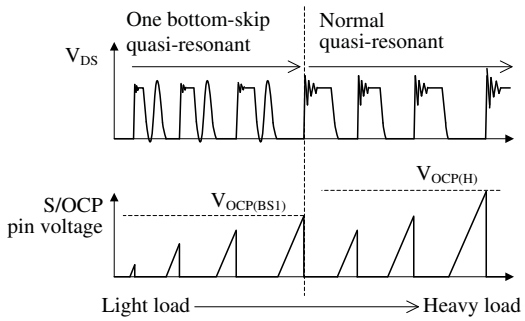

Figure 9-17 Operation state transition diagram from light load to heavy load conditions

- The mode is changed from normal quasi-resonant operation to one bottom-skip quasi-resonant operation (heavy load to light load).
  When load is decreased from normal quasi-resonant operation, the MOSFET peak drain current value will decrease, and the positive pulse width will narrow. Also, the peak value of the S/OCP pin voltage decreases. When load is reduced further and the S/OCP pin voltage falls to $V_{OCP(BS2)}$, the mode is

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changed to one bottom-skip quasi-resonant operation (see Figure 9-18).

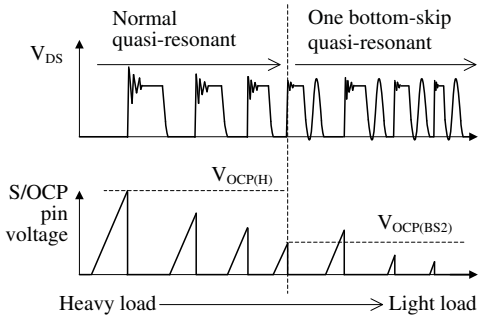

Figure 9-18 Operation state transition diagram from heavy load to light load conditions

Figure 9-19 shows the effective pulse width of normal quasi-resonant signal, and Figure 9-20 shows the effective pulse width of one bottom-skip quasi-resonant signal. In order to perform stable normal quasi-resonant operation and one bottom-skip operation, it is necessary to ensure that the pulse width of the quasi-resonant signal is 1 µs or more under the conditions of minimum input voltage and minimum output power.

The pulse width of the quasi-resonant signal, V_{REV2}, is defined as the period from the maximum specification of $V_{BD(TH1)}$, 0.34 V, on the rising edge, to the maximum specification of $V_{BD(TH2)}$, 0.27 V on the falling edge of the pulse.

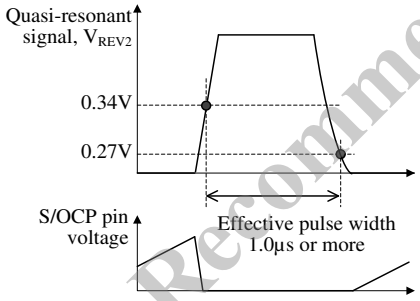

Figure 9-19 The effective pulse width of normal quasi-resonant signal

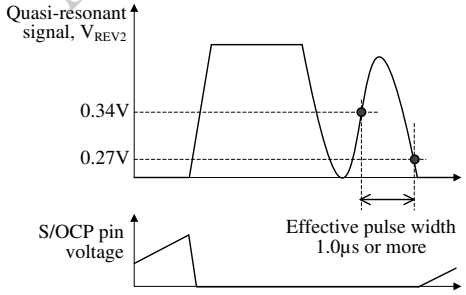

Figure 9-20 The effective pulse width of one bottom-skip quasi-resonant signal

9.9.2 Automatic Standby Mode Function

The S/OCP pin circuit monitors I_D. Automatic standby mode is activated automatically when I_D reduces under light load conditions at which the S/OCP pin voltage falls to the standby state threshold voltage (about 9% compared to $V_{OCP(H)}$ = 0.910 V).

During standby mode, when the FB/OLP pin voltage falls below $V_{FB(STBOP)}$, the IC stops switching operation, and the burst oscillation mode will begin, as shown in Figure 9-21.

Burst oscillation mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst oscillation mode, audible noises can be reduced.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 11.0 V during the transition to the burst oscillation mode, the Bias Assist function is activated and stabilizes the Standby mode operation, because $I_{CC(STARTUP)}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary winding and/or reducing the value of R2 in Figure 10-2 (refer to Section 10.1 Peripheral Components for a detail of R2).

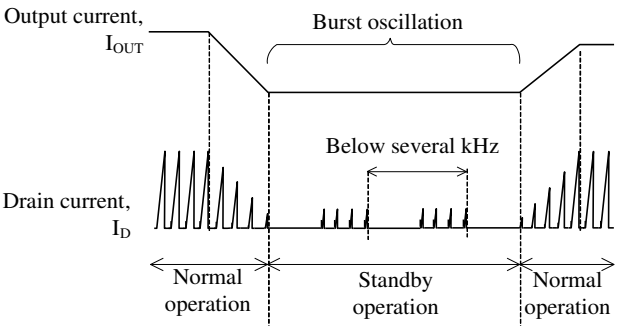

Figure 9-21 Auto Standby mode timing

9.10 Maximum On-Time Limitation Function

When the input voltage is low or in a transient state such that the input voltage turns on or off, the on-time of the incorporated power MOSFET is limited to the maximum on-time, $t_{ON(MAX)}$ = 40.0 µs in order to prevent the decreasing of switching frequency. Thus, the peak drain current is limited, and the audible noise of the transformer is suppressed.

In designing a power supply, the on-time must be less

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than $t_{ON(MAX)}$ (see Figure 9-22).

If such a transformer is used that the on-time is $t_{ON(MAX)}$ or more, under the condition with the minimum input voltage and the maximum output power, the output power would become low. In that case, the transformer should be redesigned taking into consideration the following:

- Inductance, L_P, of the transformer should be lowered in order to raise the operation frequency.
- Lower the primary and the secondary turns ratio, N_P / N_S, to lower the duty cycle.

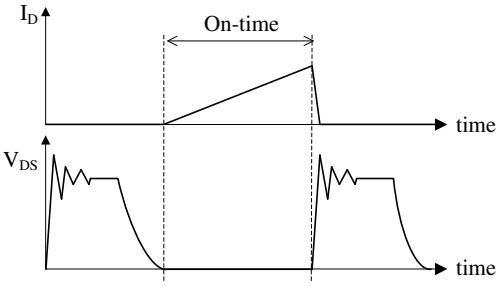

Figure 9-22 Confirmation of maximum on-time

9.11 Overcurrent Protection (OCP)

The IC has an Overcurrent Protection 1 (OCP1) and an Overcurrent Protection 2 (OCP2).

OCP1 function: pulse-by-pulse, with Input Compensation Function. The OCP2 function: In case output winding is shorted etc., the IC stops switching operation at the latched state. The products with the last letter "A" don't have the OCP2 function.

9.11.1 Overcurrent Protection 1 (OCP1)

OCP1 detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage. During Leading Edge Blanking Time (t_{BW}), OCP1 is disabled. When power MOSFET turns on, the surge voltage width of S/OCP pin should be less than $t_{ON(LEB)}$, as shown in Figure 9-23. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (refer to Section 10.3).

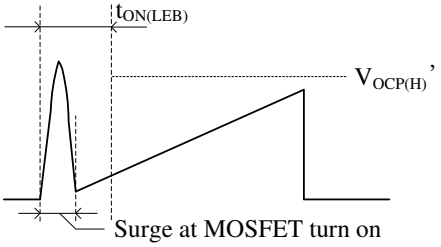

Figure 9-23 S/OCP pin voltage

In addition, if a C (RC) damper snubber of Figure 9-24 is used, reduce the capacitor value of damper snubber. If the turn-on timing isn't fitted to a V_{DS} bottom point, adjustments are required (refer to Section 9.7.2).

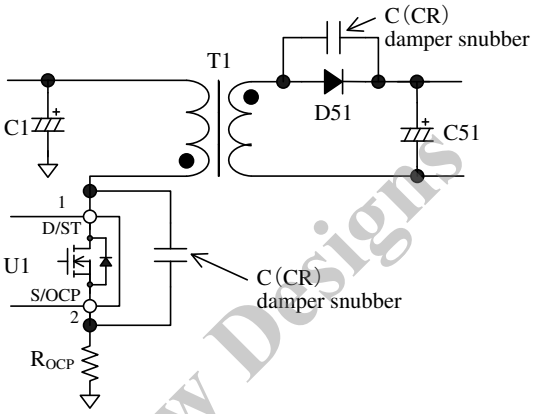

Figure 9-24 Damper snubber circuit

9.11.2 Overcurrent Protection 2 (OCP2)

The products with the last letter "A" don't have the OCP2 function.

As the protection for an abnormal state, such as an output winding being shorted or the withstand voltage of secondary rectifier being out of specification, when the S/OCP pin voltage reaches $V_{OCP(La.OFF)}$ = 1.83 V, the IC stops switching operation immediately, in latch mode.

This overcurrent protection also operates during the leading edge blanking.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

9.11.3 OCP1 Input Compensation Function

The usual control ICs have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to overcurrent detection threshold voltage. Thus, the peak current has some variation depending on the AC input voltage in OCP1 state.

When using a quasi-resonant converter with universal input (85 to 265 VAC), if the output power is set constant, then because higher input voltages have higher frequency, the on-time is reduced. Thus, the peak current in OCP1 state tends to be affected by propagation delay in the higher input voltage.

If the IC does not have Input Compensation Function, the output current at OCP1 point in the maximum input voltage, $I_{OUT(OCP)}$, becomes about double of I_{OUT} (Figure

Not Recommended for New Designs

9-25 “without input compensation”). I_{OUT} is the target output current considered with maximum output power in the minimum input voltage.

In order to suppress this variability, this IC has the overcurrent input compensation function.

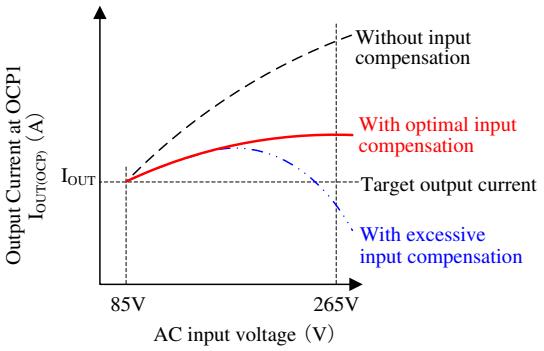

Figure 9-25 OCP1 input compensation

Figure 9-26 shows the OCP1 input compensation circuit. The value of input compensation is set by BD pin peripheral circuit.

By OCP1 Input Compensation Function, Overcurrent Detection 1 Threshold Voltage in Normal Operation, $V_{OCP(H)}$ = 0.910 V, is compensated depending on an AC input voltage.

The forward voltage of auxiliary winding D, V_{FW1}, is proportional to AC input voltage. As shown in Figure 9-26, the voltage obtained by subtracting zener voltage, V_Z, of DZ_{BD} from V_{FW1} is biased by either end of R_{BD1} and R_{BD2}, and thus the BD pin voltage is provided the voltage on R_{DB2} divided by the divider of R_{BD1} and R_{BD2}.

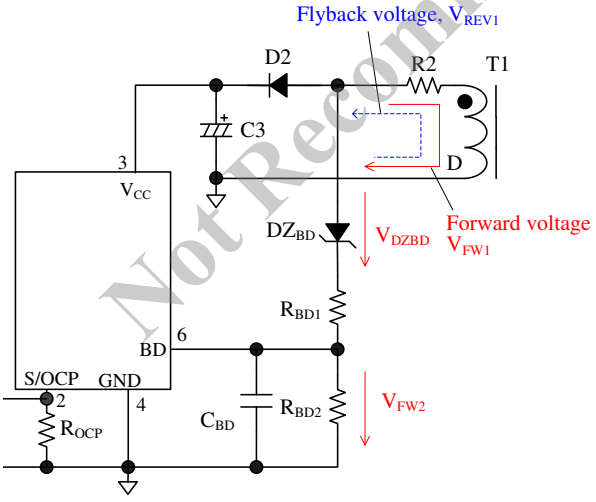

Figure 9-26 OCP input compensation circuit

Figure 9-27 shows the each voltage waveform for the input voltage in normal quasi-resonant operation.

When $V_{DZBD} \geq V_{FW1}$ (Point A), No input compensation required, V_{FW2} remains zero, and the detection voltage for an overcurrent event is the Overcurrent 1 Detection Threshold Voltage in Normal Operation, $V_{OCP(H)}$.

When $V_{DZBD} < V_{FW1}$ (Point B through Point D), the input voltage is increased and V_{FW1} exceeds the Zener voltage, V_Z, of DZ_{BD}. V_{FW2} will be produced as a negative voltage to compensate $V_{OCP(H)}$.

The value of V_{FW2} should be adjusted so that the difference between I_{OUT} and $I_{OUT(OCP)}$ is minimized as shown in Figure 9-25 “With optimal input compensation”. If the excessive input compensation, $I_{OUT(OCP)}$ may become less than I_{OUT} (Figure 9-25 “With excessive input compensation”). Thus, value of V_{FW2} must be adjusted so that $I_{OUT(OCP)}$ remains more than I_{OUT}, across the input voltage range.

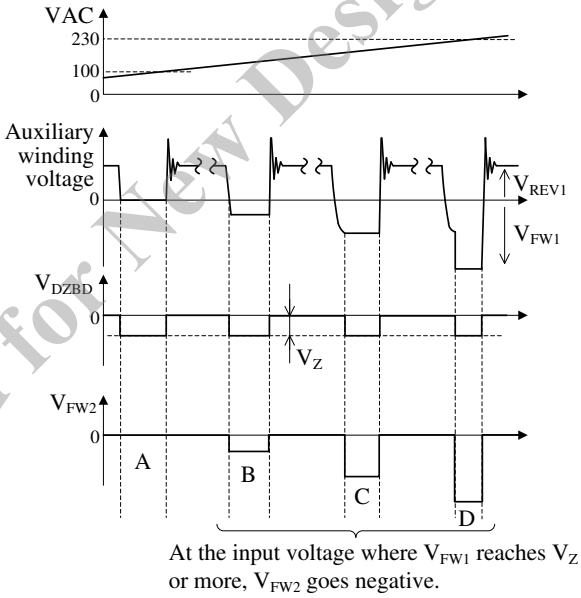

Figure 9-27 Each voltage waveform for the input voltage in normal quasi-resonant operation

Setup of BD pin peripheral components (DZ_{BD}, R_{BD1} and R_{BD2}) is as follows:

1) $V_{IN(AC)C}$ Setup
$V_{IN(AC)C}$ is the AC input voltage that starts input compensation. In general specification, $V_{IN(AC)C}$ is set 120 VAC to 170 VAC.

2) V_Z Setup
$V_{IN(AC)C}$ is adjusted by the zener voltage, V_Z, of DZ_{BD}. The V_{FW1} at $V_{IN(AC)C}$ is calculated by using Equation (5). V_Z is set from the result.

$$V_{FW1} = \frac{N_D}{N_P} \times V_{IN(AC)C} \times \sqrt{2} = V_Z \quad (5)$$

where,
N_P: Primary side number of turns
N_D: Secondary side number of turns

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3) R_{BD1} and R_{BD2} Setup.
The recommended value of R_{BD2} is 1.0 kΩ.
In general specification, R_{BD1} is set by using result of Equation (6) so that V_{FW2} = −3.0 V at maximum AC input voltage.

$$R_{BD1} = \frac{R_{BD2}}{|V_{FW2}|} \times \left(\frac{N_D}{N_P} \times V_{IN(AC)MAX} \times \sqrt{2} - V_Z - |V_{FW2}| \right) \quad (6)$$

where,
V_{FW2}: BD pin voltage (−3.0 V)
N_P: Primary side winding number of turns
N_D: Auxiliary winding number of turns
$V_{IN(AC)MAX}$: Maximum AC input voltage
V_Z: Zener voltage of DZ_{BD}

4) $V_{OCP(H)}$' is the overcurrent threshold voltage after input compensation. Figure 9-28 shows a relationship of $V_{OCP(H)}$' and BD pin voltage,V_{FW2}.
V_{FW2} at maximum AC input voltage is calculated by using Equation (7). $V_{OCP(H)}$' and this variation are gotten by using the result from Figure 9-28.
When $V_{OCP(H)}$' including variation becomes the Bottom-Skip Operation Threshold Voltage 1, $V_{OCP(BS1)}$ = 0.572 V, or less, the operation of IC is one bottom-skip only and the output current may be less than target output current, I_{OUT}.

$$|V_{FW2}| = \frac{R_{BD2}}{R_{BD1} + R_{BD2}} \times \left(|V_{FW1}| - V_Z \right) = \frac{R_{BD2}}{R_{BD1} + R_{BD2}} \times \left(\left| \frac{N_D}{N_P} \times V_{IN(AC)MAX} \times \sqrt{2} \right| - V_Z \right) \quad (7)$$

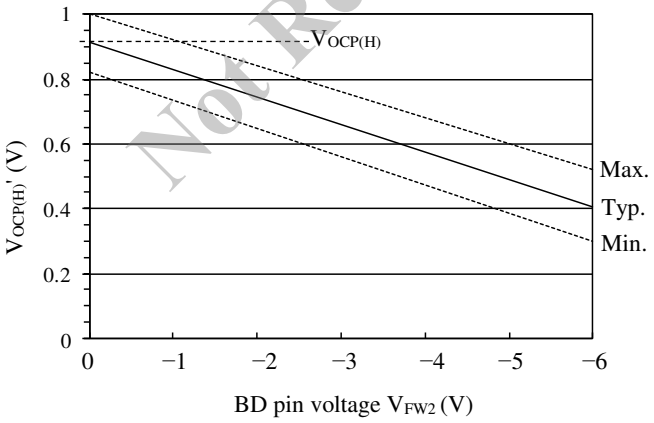

Figure 9-28 Overcurrent threshold voltage after input compensation, $V_{OCP(H)}$'
(reference for design target values)

5) V_{REV2} is calculated by using Equation (8) and is checked to be the Quasi-Resonant Operation Threshold Voltage 1, $V_{BD(TH1)}$ = 0.34 V (max.), or more (refer to Figure 9-11).

$$V_{REV2} = \frac{R_{BD2}}{R_{BD1} + R_{BD2}} \times \left(V_{REV1} - V_F \right) \geq 0.34 \text{ V} \quad (8)$$

where,
V_{REV1}: Flyback voltage of auxiliary wining
V_F: Forward voltage drop of DZ_{BD}

6) The BD pin voltage, which includes surge voltage, must be observed within the absolute maximum rating of the BD pin voltage (−6.0 to 6.0 V) in the actual operation at the maximum input voltage.

< BD Pin Peripheral Components Value Selection Reference Example >

Setting value:
Input voltage: $V_{IN(AC)}$ = 85VAC to 265VAC,
AC input voltage that starts input compensation: $V_{IN(AC)C}$ = 120 VAC,
Primary side winding number of turns: N_P = 40 T,
Auxiliary winding number of turns: N_D = 5 T
Forward voltage of auxiliary winding: V_{FW1} = 20 V

V_{FW1} is calculated by using Equation (5) as follows:

$$V_{FW1} = \frac{N_D}{N_P} \times V_{IN(AC)C} \times \sqrt{2} = \frac{5}{40} \times 120\sqrt{2} = 21.2\text{V}$$

Thus, zener voltage of DZ_{BD} is chosen to be 22 V of the E series.

When V_{FW2} = −3.0 V at maximum input voltage, 265VAC, R_{BD1} is calculated by using Equation (6) as follows:

$$R_{BD1} = \frac{R_{BD2}}{|V_{FW2}|} \times \left(\frac{N_D}{N_P} \times V_{IN(AC)MAX} \times \sqrt{2} - V_Z - |V_{FW2}| \right) = \frac{1\text{k}}{|-3|} \times \left(\frac{5}{40} \times 265\sqrt{2} - 22 - |-3| \right) = 7.28\text{k}\,\Omega$$

Thus, R_{BD1} is chosen to be 7.5 kΩ of the E series.

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When R_{BD2} = 1.0 kΩ, $|V_{FW2}|$ value at 265 VAC is calculated by using Equation (7) as follows:

$$|V_{FW2}| = \frac{R_{BD2}}{R_{BD1}+R_{BD2}} \times \left(|V_{FW1}| - V_Z\right)$$

$$= \frac{1k}{7.5k+1k} \times \left(\frac{5}{40} \times 265\sqrt{2} - 22\right) = 2.92V$$

Referring to Figure 9-28, when V_{FW2} is compensated to –2.92 V, the overcurrent threshold voltage after input compensation, $V_{OCP(H)}$', is set to about 0.66 V (typ).

When setting R_{BD2} = 1.0 kΩ, R_{BD1} = 7.5 kΩ, V_F = 0.7 V, and V_{REV1} = 20 V, V_{REV2} is calculated by using Equation (8) as follows:

$$V_{REV2} = \frac{R_{BD2}}{R_{BD1}+R_{BD2}} \times \left(V_{REV1} - V_F\right)$$

$$= \frac{1k}{1k+7.5k} \times (20 - 0.7) = 2.27V$$

V_{REV2} is $V_{BD(TH1)}$ = 0.34 V (max.) or more.

9.11.4 When Overcurrent Input Compensation is Not Required

When the input voltage is narrow range, or provided from PFC circuit, the variation of the input voltage is small. Thus, the variation of OCP point may become less than that of the universal input voltage specification.

When overcurrent input compensation is not required, the input compensation function can be disabled by substituting a high-speed diode for the zener diode, DZ_{BD}, and by keeping BD pin voltage from being minus voltage. In addition, Equation (9) shows the reverse voltage of a high-speed diode. The peak reverse voltage of high-speed diode selection should take account of its derating.

$$V_{FW1} = \frac{N_D}{N_P} \times V_{IN(AC)MAX} \times \sqrt{2} \quad (9)$$

where,
V_{FW1}: Forward voltage of auxiliary wining
N_P: Primary side number of turns
N_D: Secondary side number of turns
$V_{IN(AC)MAX}$: Maximum AC input voltage

9.12 Overload Protection (OLP)

Figure 9-29 shows the FB/OLP pin peripheral circuit, Figure 9-29 shows each waveform for Overload Protection (OLP) operation.

When the peak drain current of I_D is limited by Overcurrent Protection 1 operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C4 connected to the FB/OLP pin and the FB/OLP pin voltage, $V_{FB/OLP}$, increases.

When $V_{FB/OLP}$ increases to the FB Pin Maximum Voltage in Feedback Operation, $V_{FB(MAX)}$ = 4.05 V, or more, C4 is charged by $I_{FB(OLP)}$ = − 10 μA. When $V_{FB/OLP}$ increases to the OLP Threshold Voltage, $V_{FB(OLP)}$ = 5.96 V, the OLP function is activated, the IC stops switching operation in the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

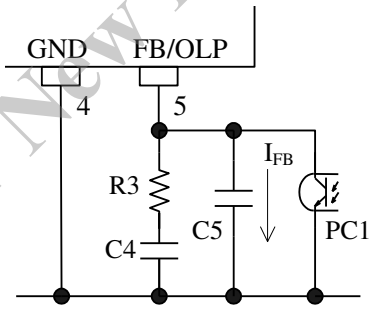

Figure 9-29 FB/OLP pin peripheral circuit

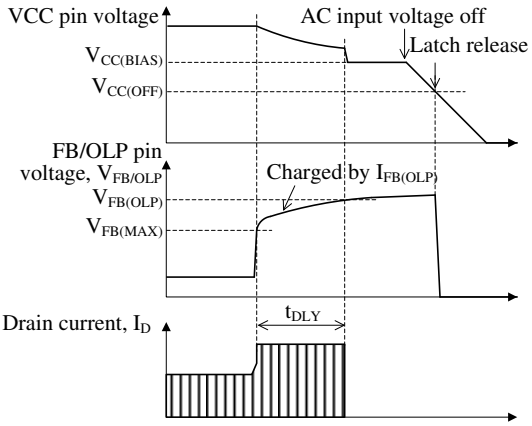

Figure 9-30 OLP operation waveforms

The time of the FB/OLP pin voltage from $V_{FB(MAX)}$ to $V_{FB(OLP)}$ is defined as the OLP delay time, t_{DLY}. Because the capacitor C5 for phase compensation is small compared to C4, the approximate value of t_{DLY} is calculated by Equation (10). When C4 = 4.7 μF, the value of t_{DLY} would be approximately 0.9 s. The recommended value of R3 is 47 kΩ.

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$$t_{DLY} \fallingdotseq \frac{\left(V_{FB(OLP)} - V_{FB(MAX)}\right) \times C4}{\left|I_{FB(OLP)}\right|}$$

$$t_{DLY} \fallingdotseq \frac{\left(5.96V - 4.05V\right) \times C4}{\left|-10\mu A\right|} \quad (10)$$

To enable the overload protection function to initiate an automatic restart, 220 kΩ is connected between the FB/OLP pin and ground, as a bypass path for $I_{FB(OLP)}$, as shown in Figure 9-31. Thus, the FB/OLP pin is kept under $V_{FB(OLP)}$ in OLP state.

In OLP state as an output shorted, the output voltage and VCC pin voltage decrease. During the operation, Bias Assist Function is disabled. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops operation. After that, the IC reverts to the initial state by UVLO circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ by startup current. Thus the intermittent operation by UVLO is repeated in OLP state without latched operation as shown in Figure 9-32.

The intermittent oscillation is determined by the cycle of the charge and discharge of the capacitor C3 connected to the VCC pin. In this case, the charge time is determined by the startup current from the startup circuit, while the discharge time is determined by the current supply to the internal circuits of the IC.

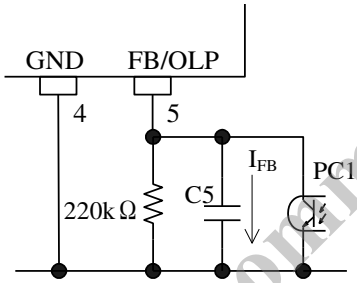

Figure 9-31 FB/OLP pin peripheral circuit (without latched operation)

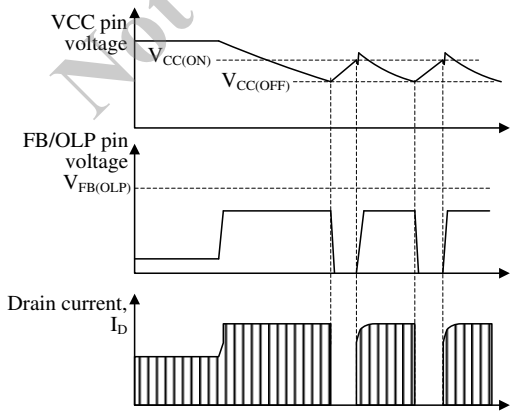

Figure 9-32 OLP operation waveform at output shorted (without latched operation)

9.13 Overvoltage Protection (OVP)

When a voltage between VCC pin and GND pin increases to $V_{CC(OVP)}$ = 31.5 V or more, Overvoltage Protection (OVP) is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

When the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as output voltage detection circuit open can be detected because the VCC pin voltage is proportional to output voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (11).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 31.5 \text{ (V)} \quad (11)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

9.14 Thermal Shutdown (TSD)

When the temperature of control circuit increases to $T_{j(TSD)}$ = 135 °C (min.) or more, Thermal Shutdown (TSD) is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.

Not Recommended for New Designs

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

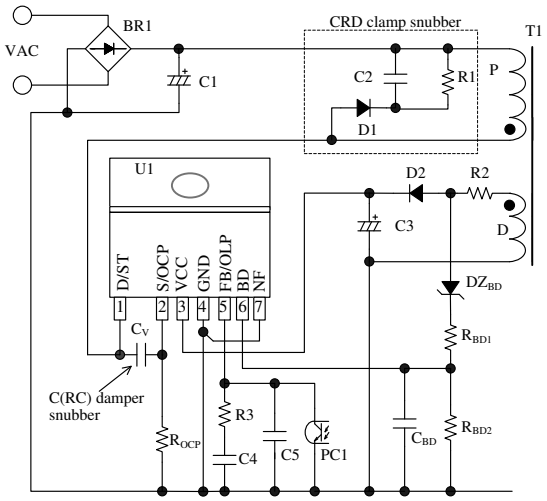

Figure 10-1 The IC peripheral circuit

• Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

• S/OCP Pin Peripheral Circuit

In Figure 10-1, R_{OCP} is the resistor for the current detection. A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

• VCC Pin Peripheral Circuit

The value of C3 in Figure 10-1 is generally recommended to be 10µ to 47µF (refer to Section 9.1 Startup Operation", because the startup time is determined by the value of C3).

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 10-2), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C3 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C3 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 10-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

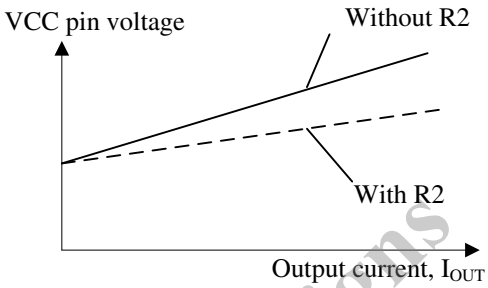

Figure 10-2 Variation of VCC pin voltage and power

• FB/OLP Pin Peripheral Circuit

C5 is for high frequency noise reduction and phase compensation, and should be connected close to these pins. The value of C5 is recommended to be about 470 pF to 0.01µF, and should be selected based on actual operation in the application.

C4 is for the OLP delay time, t_{DLY}, setting (refer to Section 9.12).

The recommended value of R3 is 47 kΩ.

• BD Pin Peripheral Circuit

Since BD pin detects the signal of bottom-on timing and input compensation of OCP1, the values of BD pin peripheral components (DZ_{BD}, R_{BD1}, R_{BD2} and C_{BD}) are considered about both functions and should be adjusted.

Refer to Section 9.7.2 and Section 9.11.3.

• NF Pin

For stable operation, NF pin should be connected to GND pin, using the shortest possible path.

• Snubber Circuit

When the surge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 10-1);

- A clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P.
- A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.
  When the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

• Peripheral Circuit of Secondary Side Shunt Regulator

Figure 10-3 shows the secondary side detection circuit with the standard shunt regulator IC (U51).

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C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047 µF to 0.47 µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

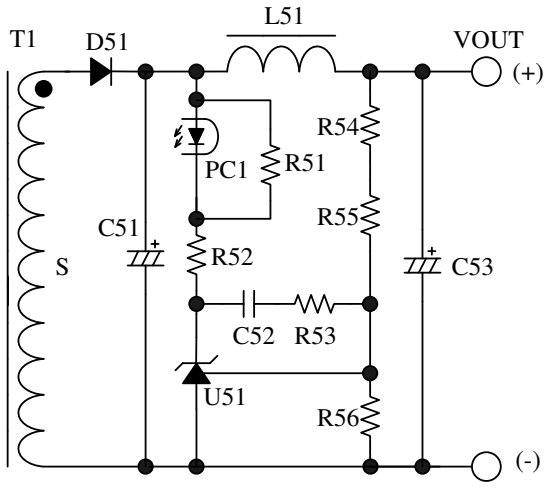


Figure 10-3 Peripheral circuit of secondary side shunt regulator (U51)

- **Transformer**

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection function (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3…) should be maximized to improve the line-regulation of those outputs.

Figure 10-4 shows the winding structural examples of two outputs.

Winding structural example (a):

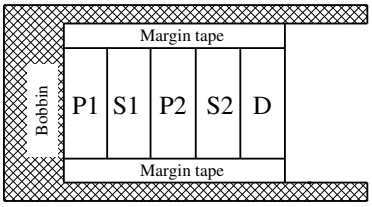
S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.

D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

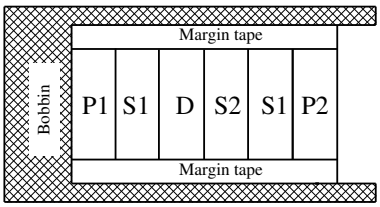
Winding structural example (b)

P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.

D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.



Winding structural example (a)



Winding structural example (b)

Figure 10-4 Winding structural examples

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10.2 Transformer Design

The design of the transformer is fundamentally the same as the power transformer of a Ringing Choke Converter (RCC) system: a self-excitation type flyback converter. However, because the duty cycle will change due to the quasi-resonant operations delaying the turn-on, the duty cycle needs to be compensated.

Figure 10-5 shows the quasi-resonant circuit.

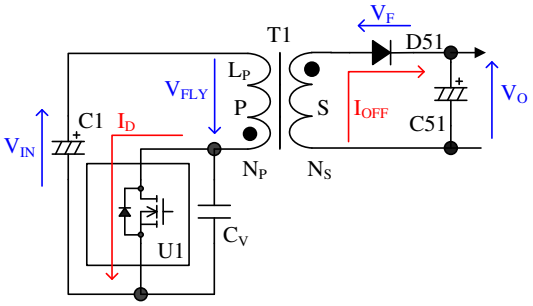

Figure 10-5 Quasi-resonant circuit

The flyback voltage, V_{FLY} is calculated as follows:

$$V_{FLY} = \frac{N_P}{N_S} \times (V_O + V_F) \quad (12)$$

where,
N_P: Primary side number of turns
N_S: Secondary side number of turns
V_O: Output voltage
V_F: Forward voltage drop of D51

The on duty, D_{ON}, at the minimum AC input voltage is calculated as follows:

$$D_{ON} = \frac{V_{FLY}}{V_{IN(MIN)} + V_{FLY}} \quad (13)$$

where,
$V_{IN(MIN)}$: C1 voltage at the minimum AC input voltage
V_{FLY}: Flyback voltage.

The inductance, L_P' on the primary side, taking into consideration the delay time, is calculated using Equation (14).

$$L_P' = \frac{(V_{IN(MIN)} \times D_{ON})^2}{\left(\sqrt{\frac{2P_O \times f_{MIN}}{\eta_1}} + V_{IN(MIN)} \times D_{ON} \times f_{MIN} \times \pi\sqrt{C_V}\right)^2} \quad (14)$$

where,
$V_{IN(MIN)}$: C1 voltage at the minimum AC input voltage
D_{ON}: On-duty at the minimum input voltage
P_O: maximum output power
f_{MIN}: minimum operation frequency
η_1: transformer efficiency
C_V: the voltage resonance capacitor connected between the drain and source of the power MOSFET

Each parameter, such as the peak drain current, I_{DP}, is calculated by the following formulas:

$$t_{ONDLY} = \pi\sqrt{L_P' \times C_V} \quad (15)$$

$$D_{ON}' = D_{ON}(1 - f_{MIN} \times t_{ONDLY}) \quad (16)$$

$$I_{IN} = \frac{P_O}{\eta_2} \times \frac{1}{V_{IN(MIN)}} \quad (17)$$

$$I_{DP} = \frac{2 \times I_{IN}}{D_{ON}'} \quad (18)$$

$$N_P = \sqrt{\frac{L_P'}{\text{Al - value}}} \quad (19)$$

$$N_S = \frac{N_P \times (V_O + V_F)}{V_{FLY}} \quad (20)$$

where,
t_{ONDLY}: Delay time of quasi-resonant operation
I_{IN}: Average input current
η_2: conversion efficiency of the power supply
I_{DP}: peak drain current
D_{ON}': On-duty after compensation
V_O: Secondary side output voltage

The minimum operation frequency, f_{MIN}, can be calculated by the Equation (22):

$$f_{MIN} = \left(\frac{-\sqrt{\frac{2P_O}{\eta_1}} + \sqrt{\frac{2P_O}{\eta_1} + \frac{4\pi(V_{IN(MIN)} \times D_{ON})^2 \times \sqrt{C_V}}{\sqrt{L_P'}}}}{2\pi\sqrt{C_V} \times V_{IN(MIN)} \times D_{ON}} \right)^2 \quad (21)$$

Figure 10-6 shows the Example of NI-Limit versus AL-Value characteristics.

Choose the ferrite core that does not saturate and provides a design margin in consideration of temperature effects and other variations to NI-Limit versus AL-Value characteristics.

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Al-value is calculated by using L_P' and N_P. NI is calculated by using Equation (22).

It is recommended that Al-value and NI provide the design margin of 30 % or more for saturation curve of core.

$$NI = N_P \times I_{DP} \quad (AT) \tag{22}$$

where,
N_P: Primary side number of turns
I_{DP}: Peak switching current

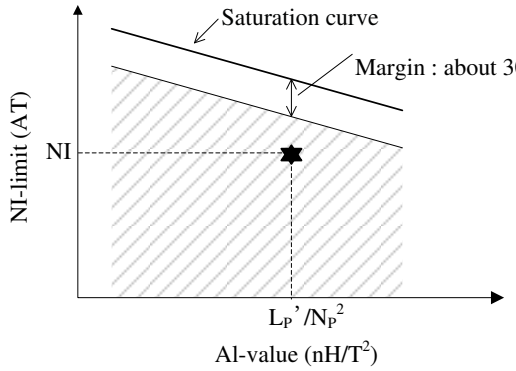

Figure 10-6 Example of NI-Limit versus AL-Value characteristics

10.3 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-7 shows the circuit design example.

(1) Main Circuit Trace Layout
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.
If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 µF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 10-7 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C3 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 µF to 1.0 µF) close to the VCC pin and the GND pin is recommended.

(4) R_{OCP} Trace Layout
R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 10-7) which is close to the base of R_{OCP}.

(5) Peripheral components of the IC
The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

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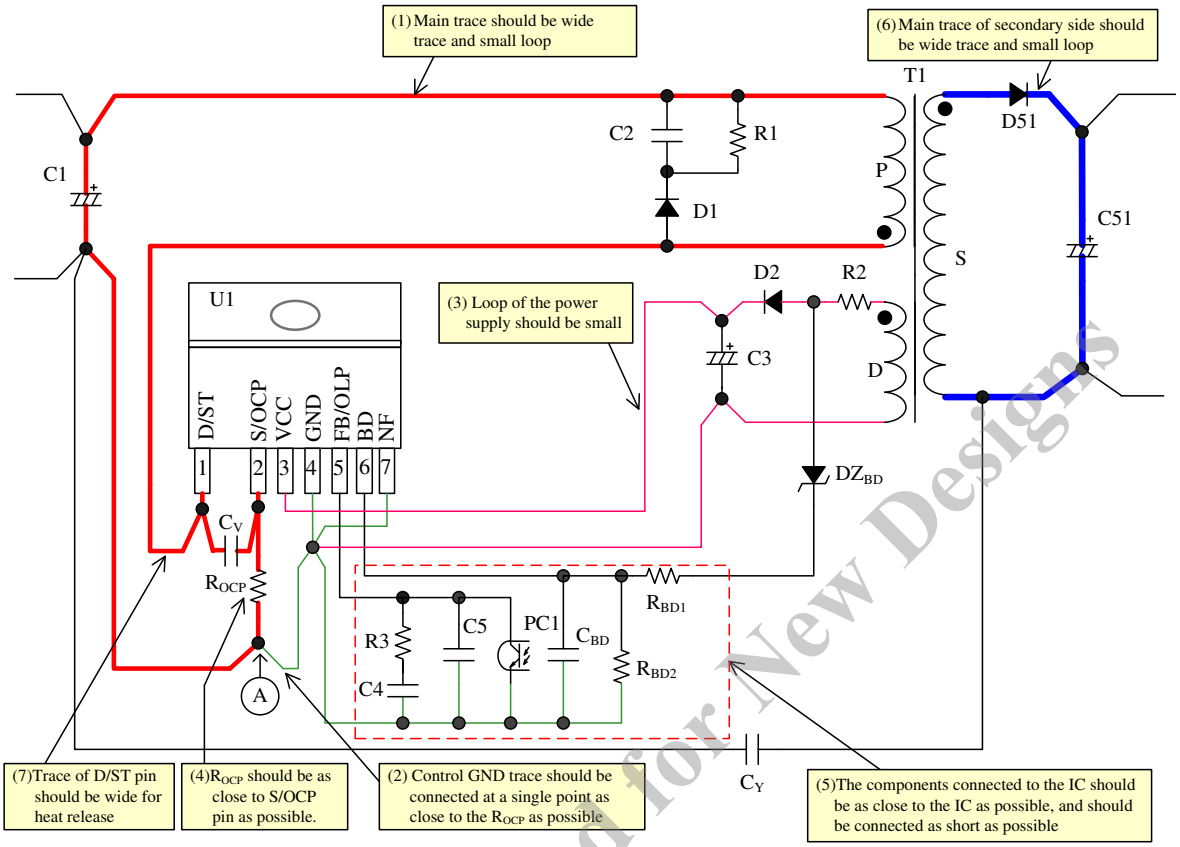

Figure 10-7 Peripheral circuit example around the IC

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11. Pattern Layout Example

The following show the four outputs PCB pattern layout example and the schematic of circuit using STR-Y6700 series. The PCB pattern layout example is made usable to other ICs in common. The parts in Figure 11-2 are only used.

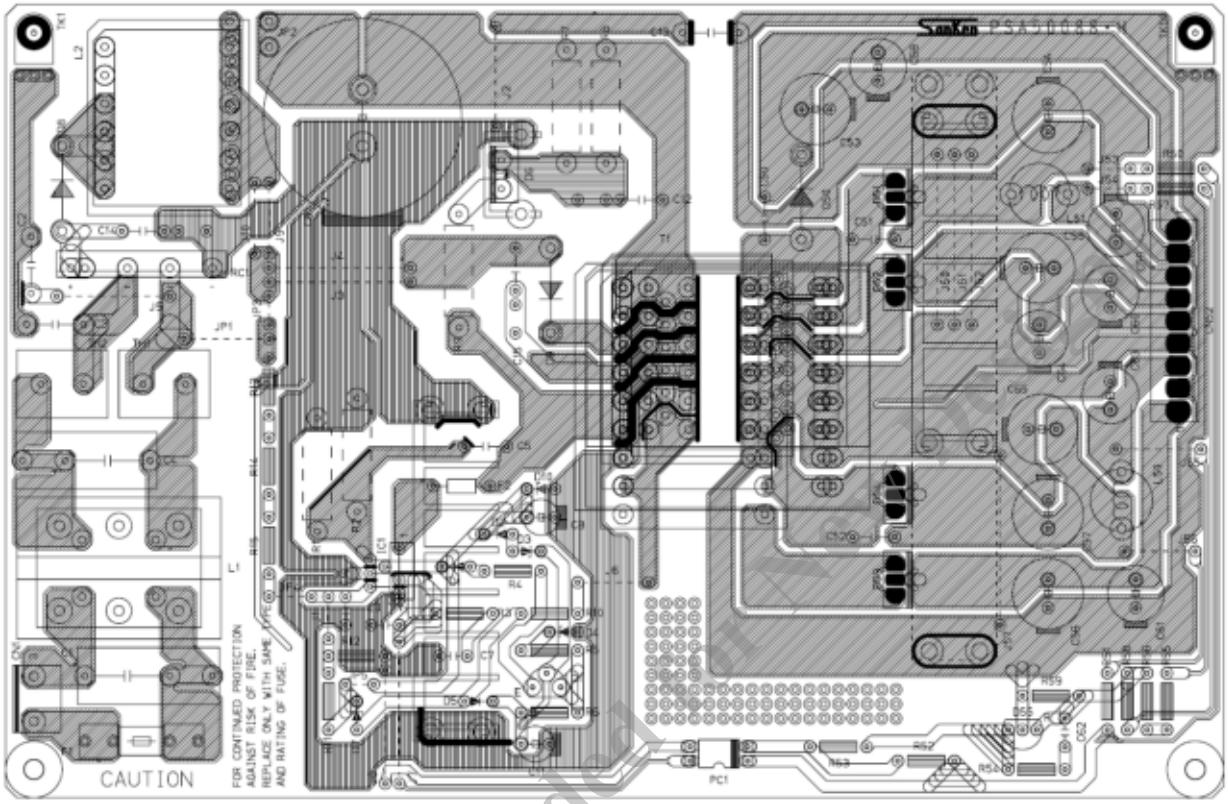

Figure 11-1 PCB circuit trace layout example

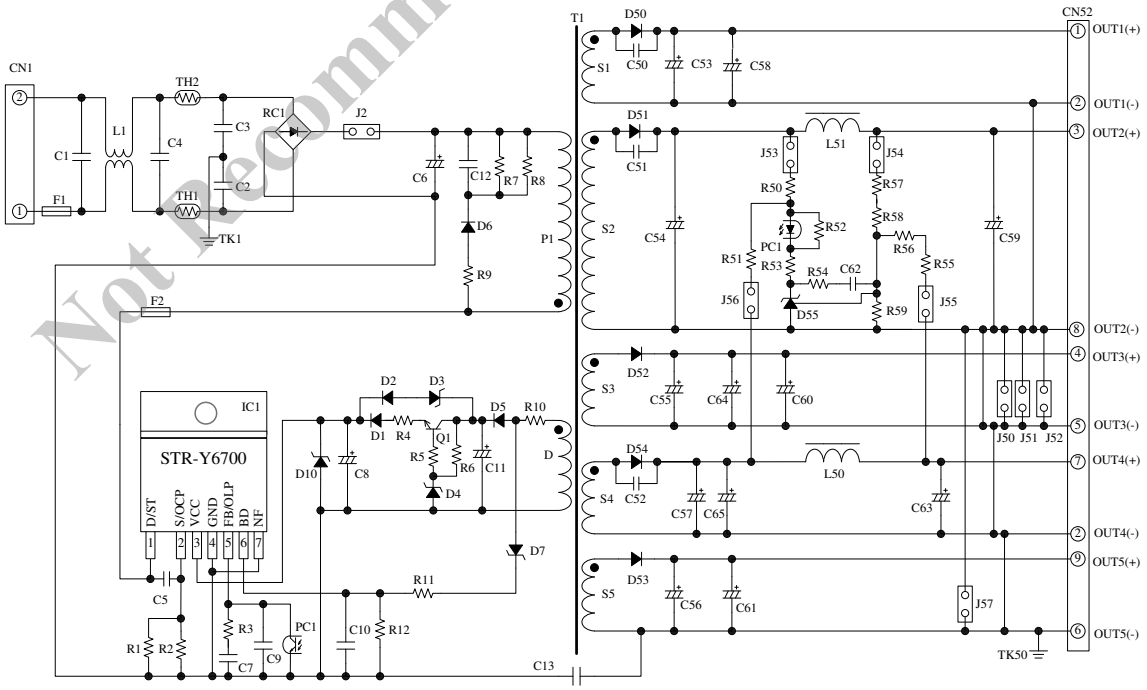

Figure 11-2 Circuit schematic for PCB circuit trace layout

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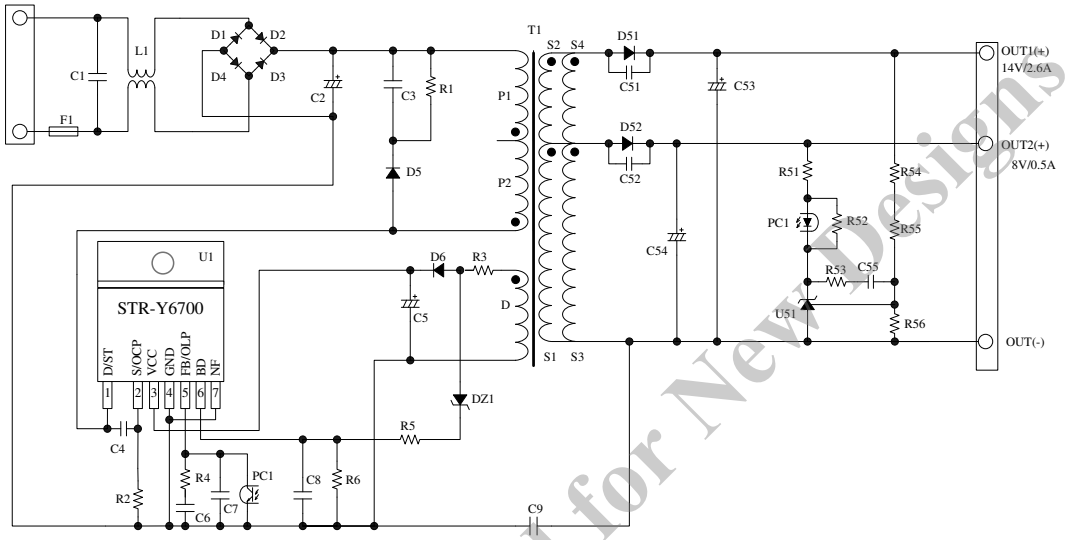
12. Reference Design of Power Supply

● Power supply specification

IC	STR-Y6754
Input voltage	85 VAC to 265 VAC
Maximum output power	40.4 W
Output 1	14 V / 2.6A
Output 2	8 V / 0.5 A

● Circuit schematic



● Bill of materials

Symbol	Part type	Ratings(1)	Recommended Sanken Parts	Symbol	Part type	Ratings(1)	Recommended Sanken Parts
C1 (2)	Film, X2	0.1 µF, 275 V		D52	Schottky	90 V, 1.5 A	EK 19
C2	Electrolytic	220 µF, 400 V		DZ1	Zener	22V	
C3	Ceramic	2200 pF, 630 V		F1	Fuse	250 VAC, 3 A	
C4	Ceramic	100 pF, 2 kV		L1 (2)	CM inductor	3.3 mH	
C5	Electrolytic	22 µF, 50V		PC1	Photo-coupler	PC123or equiv	
C6	Ceramic	4.7 µF, 16 V		R1 (3)	Metal oxide	150 kΩ, 1 W	
C7 (2)	Ceramic	4700 pF, 50V		R2 (2)	General	0.56 Ω, 1 W	
C8 (2)	Ceramic	470 pF, 50V		R3 (2)	General	15 Ω	
C9	Ceramic, Y1	2200 pF, 250 V		R4	General	47 kΩ	
C51	Ceramic	2200 pF, 1 kV		R5 (2)	General	6.8 kΩ	
C52	Ceramic	Open		R6	General	1 kΩ	
C53	Electrolytic	1000 µF, 50 V		R51	General	820 Ω	
C54	Electrolytic	470 µF, 16 V		R52	General	1.5 kΩ	
C55	Ceramic	0.1 µF		R53 (2)	General	22 kΩ	
D1	General	600V, 1A	EM01A	R54 (2)	General	6.8 kΩ	
D2	General	600V, 1A	EM01A	R55	General, 1%	39 kΩ	
D3	General	600V, 1A	EM01A	R56	General, 1%	10 kΩ	
D4	General	600V, 1A	EM01A	T1	Transformer	See the specification	
D5	Fast recovery	1000 V, 0.5 A	EG01C	U1	IC	−	STR-Y6754
D6	Fast recovery	200 V, 1 A	AL01Z	U51	Shunt regulator	V_{REF} = 2.5 V TL431or equiv	
D51	Schottky	150 V, 10 A	FMEN-210B				

(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

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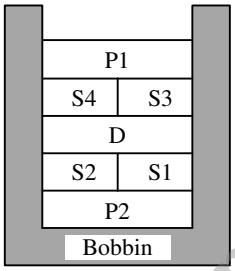
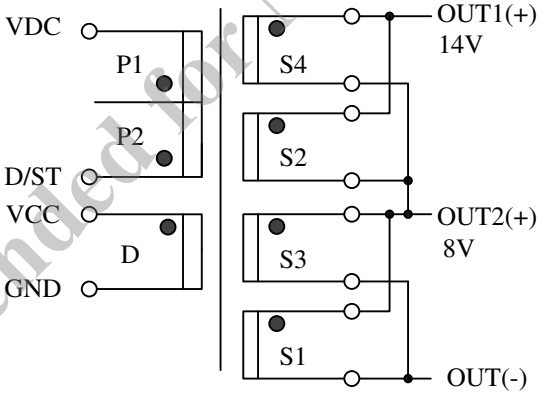
● Transformer specification
- Primary inductance, L_P: 0.95 mH
- Core size: EER28L
- AL-value: 183 nH/N^2 (Center gap of about 0.8 mm)
- Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction
Primary winding 1	P1	43	1EUW – φ 0.30	Two-layer, solenoid winding
Primary winding 2	P2	29	1EUW – φ 0.30	Single-layer, solenoid winding
Auxiliary winding	D	12	TEX – φ 0.23 × 2	Single-layer, Space winding
Output winding 1	S1	5	φ 0.32 × 2	Single-layer, solenoid winding
Output winding 2	S2	3	φ 0.32 × 2	Single-layer, solenoid winding
Output winding 3	S3	5	φ 0.32 × 2	Single-layer, solenoid winding
Output winding 4	S4	3	φ 0.32 × 2	Single-layer, solenoid winding



Cross-section view



● : Start at this pin

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