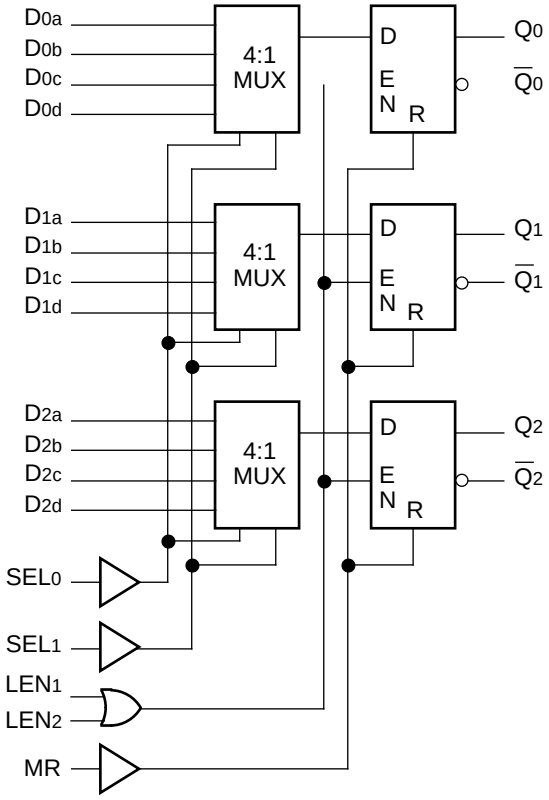
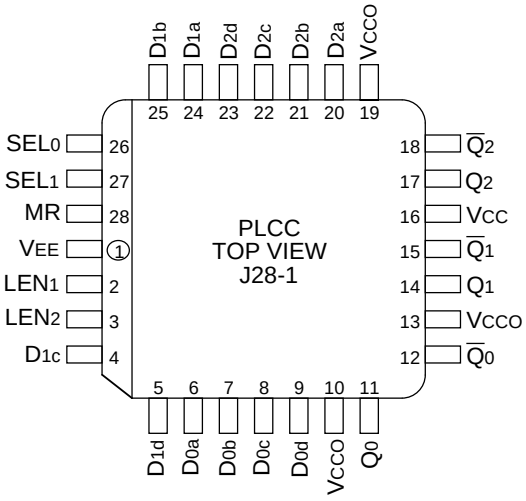
- **900ps max. D to output**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **800ps max. LEN to output**
- **Differential outputs**
- **Asynchronous Master Reset**
- **Dual latch enables**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E156**
- **Available in 28-pin PLCC package**

The SY10/100E156 offer three 4:1 multiplexers followed by latches with differential outputs, designed for use in new, high-performance ECL systems. The two external latch enable signals (LEN_1 and LEN_2) are gated through a logical OR operation before use as control for the three latches. When both LEN_1 and LEN_2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN_1 or LEN_2 (or both) are at a logic HIGH, the outputs are latched.

The multiplexer operation is controlled by the Select (SEL_0, SEL_1) signals which select one of the four bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to take all outputs to a logic LOW.





Pin	Function
D_{0x}–D_{2x}	Input Data
SEL_0, SEL_1	Select Inputs
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_2	True Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Inverted Outputs
V_{CCO}	V_{CC} to Output

1	LEN2	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

SEL0	SEL1	Data
L	L	a
H	L	b
L	H	c
H	H	d

EE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
IIH	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
IEE	Power Supply Current										mA	—
	10E	—	75	90	—	75	90	—	75	90		
	100E	—	75	90	—	75	90	—	86	103		

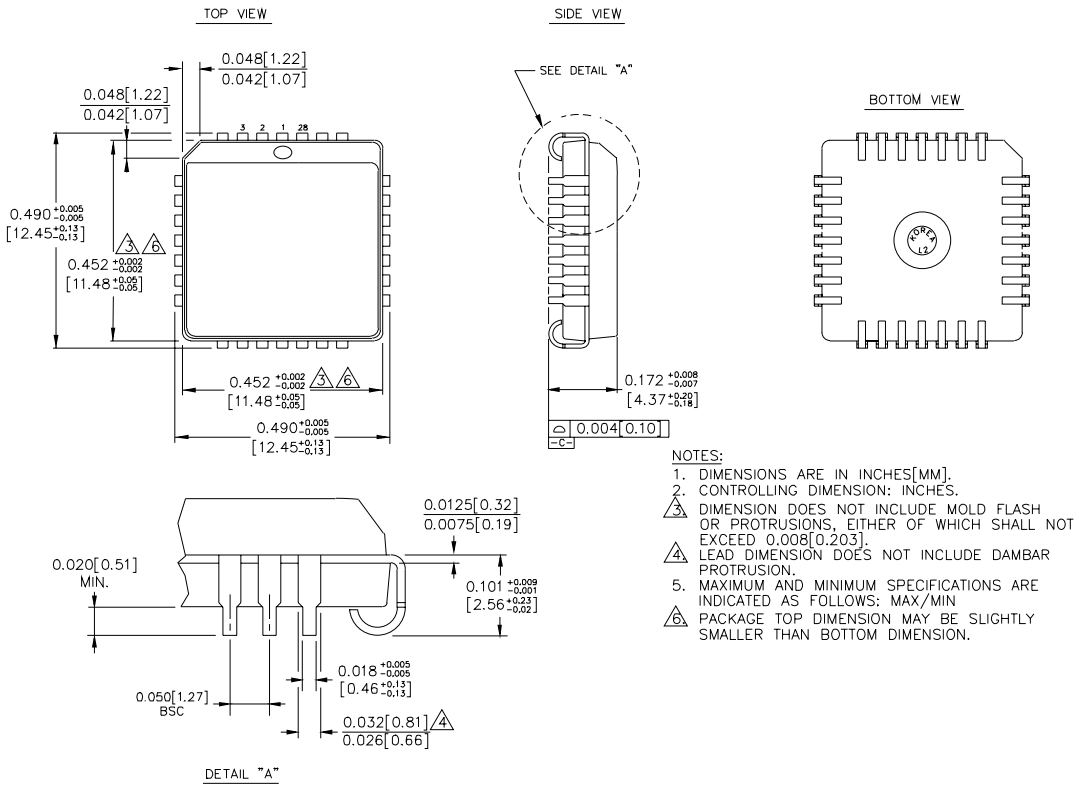
EE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH	Propagation Delay to Output										ps	—
tPHL	D	400	600	900	400	600	900	400	600	900		
	SEL0	550	775	1050	550	775	1050	550	775	1050		
	SEL1	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	800		
	MR	350	600	825	350	600	825	350	600	825		
tS	Set-up Time										ps	—
	D	400	275	—	400	275	—	400	275	—		
	SEL0	700	300	—	700	300	—	700	300	—		
	SEL1	600	400	—	600	400	—	600	400	—		
tH	Hold Time										ps	—
	D	300	–275	—	300	–275	—	300	–275	—		
	SEL0	100	–300	—	100	–300	—	100	–300	—		
	SEL1	200	–400	—	200	–400	—	200	–400	—		
tRR	Reset Recovery Time	800	600	—	800	600	—	800	600	—	ps	—
tPW	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
tskew	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
tr	Rise/Fall Time	275	475	700	275	475	700	275	475	700	ps	—
tf	20% to 80%											

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

Code	Type	Range
SY10E156JC	J28-1	Commercial
SY10E156JCTR	J28-1	Commercial
SY100E156JC	J28-1	Commercial
SY100E156JCTR	J28-1	Commercial



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB http://www.micrel.com

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