2.5V/3.3V/5V 1:5 LVPECL/PECL/ ECL/HSTL 2GHz CLOCK DRIVER WITH 2:1 DIFFERENTIAL INPUT MUX

Precision Edge® SY100EP14U

FEATURES

- **Guaranteed AC parameters over temp/voltage:**
  - **> 2GHz f_{MAX}**
  - **< 25ps within-device skew**
  - **< 275ps tr/tf time**
  - **< 525ps prop delay**
- **2:1 Differential MUX input**
- **Flexible supply voltage: 2.5V/3.3V/5V**
- **Wide operating temperature range: –40°C to +85°C**
- **V_{BB} reference for single-ended or AC-coupled PECL inputs**
- **100K ECL compatible outputs**
- **Inputs accept PECL/LVPECL/ECL/HSTL logic**
- **75kΩ internal input pull-down resistors**
- **Available in a 20-Pin TSSOP package**



ECL Pro™

DESCRIPTION

The SY100EP14U is a high-speed, 2GHz differential PECL/ECL 1:5 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 25ps over temperature and supply voltage. The wide supply voltage operation allows this fanout buffer to operate in 2.5V, 3.3V, and 5V systems. A V_{BB} reference is included for single-supply or AC-coupled PECL/ECL input applications, thus eliminating resistor networks. When interfacing to a single-ended or AC-coupled PECL/ECL input signal, connect the V_{BB} pin to the unused /CLK pin, and bypass the pin to V_{CC} through a 0.01µF capacitor.

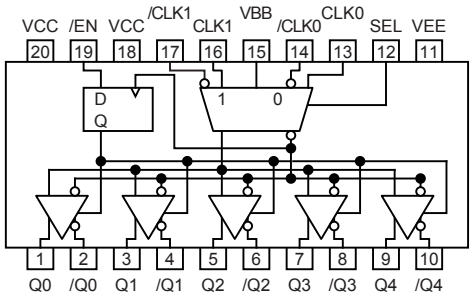
The SY100EP14U features a 2:1 input MUX, making it an ideal solution for redundant clock switchover applications. If only one input pair is used, the other pair may be left floating. In addition, this device includes a synchronous enable pin that forces the outputs into a fixed logic state. Enable or disable state is initiated only after the outputs are in a LOW state, thus eliminating the possibility of a “runt” clock pulse.

The SY100EP14U I/O are fully differential and 100K ECL compatible. Differential 10K ECL logic can interface directly into the SY100EP14U inputs.

The SY100EP14U is part of Micrel’s high-speed clock synchronization family. For applications that require a different I/O combination, consult the Micrel website at www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

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PACKAGE/ORDERING INFORMATION



20-Pin TSSOP

Ordering Information(1)

Part Number	Package Type	Operating Range	Package Marking
SY100EP14UK4C	K4-20-1	Commercial	XEP14U
SY100EP14UK4CTR(2)	K4-20-1	Commercial	XEP14U
SY100EP14UK4I	K4-20-1	Industrial	XEP14U
SY100EP14UK4ITR(2)	K4-20-1	Industrial	XEP14U
SY100EP14UK4G(3)	K4-20-1	Industrial	XEP14U with Pb-Free bar line indicator
SY100EP14UK4GTR(2, 3)	K4-20-1	Industrial	XEP14U with Pb-Free bar line indicator

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin	Function
CLK0, /CLK0 CLK1, /CLK1	PECL, LVPECL, ECL, LVECL, HSTL Clock or Data Inputs. Internal 75kΩ pull-down resistors on CLK0, CLK1, and internal 75kΩ pull-up and 75kΩ pull-down resistors or /CLK0, /CLK1. For single-ended applications, connect signal into CLK0 and/or CLK1 inputs. /CLK0, /CLK1 default condition is V_{CC}/2 when left floating. CLK0, CLK1 default condition is LOW when left floating.
Q0 to Q4 /Q0 to /Q4	LVPECL, PECL, ECL Differential Outputs: Terminate with 50Ω to V_{CC}–2V. For single-ended applications, terminate the unused output with 50Ω to V_{CC}–2V
/EN	LVPECL, PECL, ECL compatible synchronous enable: When /EN goes HIGH, the Q_{OUT} will go LOW and $/Q_{OUT}$ will go HIGH on the next LOW input clock transition. Includes a 75kΩ pull-down. Default state is LOW when left floating. The internal latch is clocked on the falling edge of the input clock (CLK0, CLK1)
SEL	LVPECL, PECL, ECL compatible 2:1 Mux input signal select: When SEL is LOW, CLK0 input pair is selected. When SEL is HIGH, CLK1 input pair is selected. Includes a 75kΩ pull-down. Default state is LOW and CLK0 is selected.
V_{BB}	Output Reference Voltage: Equal to V_{CC}–1.7V (approx.), and used for single-ended input signals or AC-coupled applications. For single-ended PECL, LVPECL applications, bypass with a 0.01µF to V_{CC}. For single-ended LVTTL inputs, bypass to GND. Max. sink/source current is 0.5mA.
V_{CC}	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
V_{EE}	Negative Power Supply: LVPECL, PECL applications, connect to GND.

TRUTH TABLE(1)

CLK0	CLK1	CLK_SEL	/EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

Note 1. On next negative transition of CLK0 or CLK1.

FUNCTION TABLE

CLK_SEL	Active Input
0	CLK0, /CLK0
1	CLK1, /CLK1

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage		6.0	V
V_{IN}	Input Voltage (V_{CC} = 0V, V_{IN} not more negative than V_{EE}) Input Voltage (V_{EE} = 0V, V_{IN} not more positive than V_{CC})		–6.0 to 0 +6.0 to 0	V
I_{OUT}	Output Current	–Continuous –Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current[2]		±0.5	mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)		+260	°C
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
ESD	Mil Std. 883 Human Body Model, All Pins		>1.5k	V
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air (single-layer PCB) –Still-Air (multi-layer PCB) –500lfpm (multi-layer PCB)	115 75 65	°C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)		21	°C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. Due to the limited drive capability, use for inputs of same package only.

DC ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply Voltage										V	
	(PECL)	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5		
	(LVPECL)	2.37	3.3	3.8	2.37	3.3	3.8	2.37	3.3	3.8		
	(ECL)	–4.5	–5.0	–5.5	–4.5	–5.0	–5.5	–4.5	–5.0	–5.5		
	(LVECL)	–3.8	–3.3	–2.37	–3.8	–3.3	–2.37	–3.8	–3.3	–2.37		
I_{CC}	Power Supply Current	—	—	75	—	68	78	—	—	82	mA	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	$V_{IN} = V_{IH}$
I_{IL}	Input LOW Current D	0.5	—	—	0.5	—	—	0.5	—	—	µA	$V_{IN} = V_{IL}$
	/D	–150	—	—	–150	—	—	–150	—	—	µA	$V_{IN} = V_{IL}$
C_{IN}	Input Capacitance (TSSOP)	—	—	—	—	0.75	—	—	—	—	pF	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.5V ±5%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage[2] (Single-ended)	555	—	875	555	—	875	555	—	875	mV	
V_{IH}	Input HIGH Voltage[2] (Single-ended)	1335	—	1620	1335	—	1620	1335	—	1620	mV	
V_{OL}	Output LOW Voltage	555	680	805	555	680	805	555	680	805	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to V_{CC}–2V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[3]	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output varies 1:1 with V_{CC}.

Note 2. V_{BB} reference is not functional for V_{CC} < 3.0V. External V_{BB} equivalent is required.

Note 3. V_{IHCMR} (min) varies 1:1 with V_{EE}, V_{IHCMR} (Max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.3V ±10%; V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV	
V_{OL}	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	50Ω to V_{CC}–2V
V_{BB}	Reference Voltage[2]	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV	V_{CC} = 3.3V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[3]	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output varies 1:1 with V_{CC}.

Note 2. Single-ended input operation is limited $V_{CC} \geq 3.0V$ in LVPECL mode. V_{BB} reference varies 1:1 with V_{CC}.

Note 3. V_{IHCMR} (min) varies 1:1 with V_{EE}, V_{IHCMR} (Max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100KEP) PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV	
V_{IH}	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV	
V_{OL}	Output LOW Voltage	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV	50Ω to V_{CC}–2V
V_{BB}	Output Voltage Reference[2]	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV	V_{CC} = +5.0V
V_{IHCMR}	Input HIGH Voltage[3] Common Mode Range	2.0	—	V_{CC}	2.0	—	V_{CC}	2.0	—	V_{CC}	V	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at V_{CC} = 5.0V. They vary 1:1 with V_{CC}.

Note 2. V_{BB} reference varies 1:1 with V_{CC}.

Note 3. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to V_{CC} ≥ 3.0V in PECL mode.

(100KEP) LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = –2.37V to –3.8V; V_{CC} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-ended)	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV	
V_{IH}	Input HIGH Voltage (Single-ended)	–1165	—	–880	–1165	—	–880	–1165	—	–880	mV	
V_{OL}	Output LOW Voltage	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	–1145	–1020	–0895	–1145	–1020	–0895	–1145	–1020	–0895	mV	50Ω to V_{CC}–2V
V_{BB}	Output Reference Voltage[2]	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV	
V_{IHCMR}	Input HIGH Voltage Common Mode Range[3]	V_{EE} +1.2		0.0	V_{EE} +1.2		0.0	V_{EE} +1.2		0.0	V	

Note 1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}.

Note 2. Single-ended input operation is limited V_{EE} ≤ –3.0V in ECL/LVECL mode. V_{BB} reference varies 1:1 with V_{CC}.

Note 3. V_{IHCMR} (min) varies 1:1 with V_{EE}, V_{IHCMR} (max) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100K) ECL/LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V, V_{EE} = –5.5V to –3.0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV	
V_{IH}	Input HIGH Voltage	–1225	—	–880	–1225	—	–880	–1225	—	–880	mV	
V_{OL}	Output LOW Voltage[2]	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage[2]	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV	50Ω to V_{CC}–2V
V_{BB}	Output Reference Voltage[3]	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV	
V_{IHCMR}	Input HIGH Voltage Common Mode Range[4]	V_{EE} +1.2		0.0	V_{EE} +1.2		0.0	V_{EE} +1.2		0.0	V	

Note 1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}.

Note 2. All loading with 50Ω to V_{CC} –2.0V.

Note 3. Single-ended input operation is limited $V_{EE} \leq$–3.0V in ECL/LVECL mode. V_{BB} reference varies 1:1 with V_{CC}.

Note 4. V_{IHCMR} (min) varies 1:1 with V_{EE}, (max) varies 1:1 with V_{CC}. The V_{IHCMR} is referenced to the most positive side of the differential input signal.

HSTL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.37V to 3.8V; V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	1200	—	—	1200	—	—	1200	—	—	mV
V_{IL}	Input LOW Voltage	—	—	400	—	—	400	—	—	400	mV
V_X	Input Crossover Voltage	680	—	900	680	—	900	680	—	900	mV

AC ELECTRICAL CHARACTERISTICS

LVPECL: V_{CC} = 2.37V to 2.625V, V_{EE} = 0V; PECL: V_{CC} = 4.50V to 5.50V, V_{EE} = 0V;
ECL: V_{EE} = –4.50V to –5.5V, V_{CC} = 0V; LVECL: V_{EE} = –2.37V to –3.8V, V_{CC} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Frequency(1)	2	—	—	2	—	—	2	—	—	GHz
t_{PLH} t_{PHL}	PECL/ECL (V_{CC} = 5V) PropagationDelay to Output IN (Differential) IN (Single-Ended)	 250 —	 330 —	 400 —	 250 —	 330 355	 450 —	 250 —	 330 —	 600 —	 ps ps
	LVPECL/LVECL (V_{CC} = 2.37V to 3.8V) Propagation Delay to Output IN (Differential) IN (Single-Ended)	 275 —	 350 —	 425 —	 275 —	 350 375	 475 —	 275 —	 350 —	 525 —	 ps ps
t_{SKEW}(2)	PECL/ECL (V_{CC} = 5V) Within-Device Skew (Diff.) Part-to-Part Skew (Diff.)	 — —	 25 100	 35 125	 — —	 30 150	 45 175	 — —	 40 175	 50 200	 ps ps
	LVPECL/LVECL (V_{CC} = 2.37V to 3.8V) Within-Device Skew (Diff.) Part-to-Part Skew (Diff.)	 — —	 10 100	 25 125	 — —	 15 150	 25 175	 — —	 15 200	 25 225	 ps ps
t_S	Set-Up Time(3) /EN to CLK	100	50	—	100	50	—	100	50	—	ps
t_H	Hold Time(3) /EN to CLK	200	140	—	200	140	—	200	140	—	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r, t_f	PECL/ECL Output Rise/Fall Times (20% to 80%) LVPECL/LVECL (V_{CC} = 2.37V to 3.8V)	 100 90	 180 130	 240 225	 105 95	 180 130	 270 250	 110 100	 225 150	 300 275	 ps ps

Note 1. f_{MAX} is defined as the maximum toggle frequency. Measured with 750mV input signal, 50% duty cycle, all loading with 50W to V_{CC}–2V.

Note 2. Skew is measured between outputs under identical transitions.

Note 3. Set-up and hold times apply to synchronous applications that intend to enable/disable before then ext clock cycle. For asynchronous applications, set-up and hold time does not apply.

TERMINATION RECOMMENDATIONS

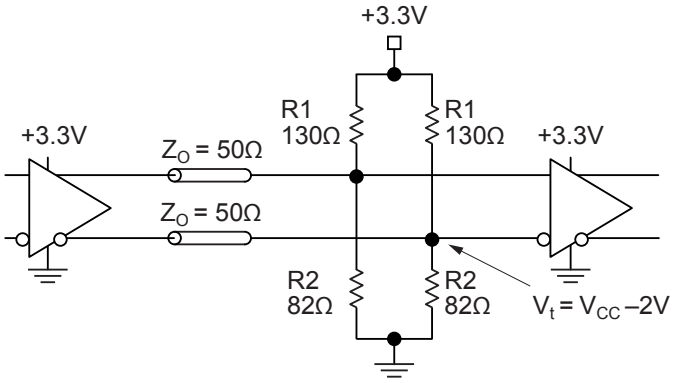


Figure 1. Parallel Termination–Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω

Note 2. For +5.0V systems: R1 = 82Ω, R2 = 130Ω

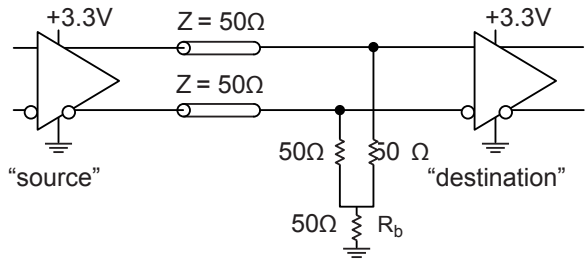


Figure 2. Three-Resistor "Y–Termination"

Note 1. Power-saving alternative to Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.

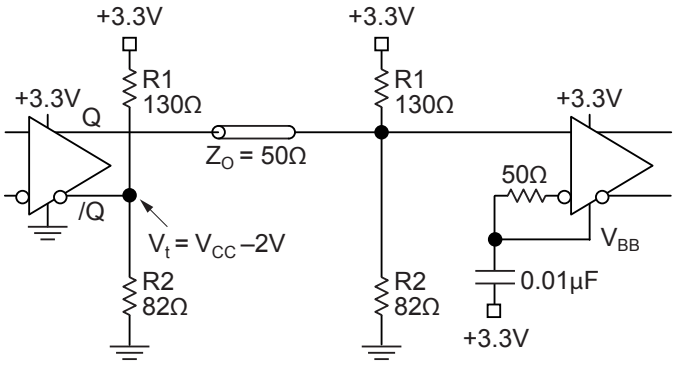


Figure 3. Terminating Unused I/O

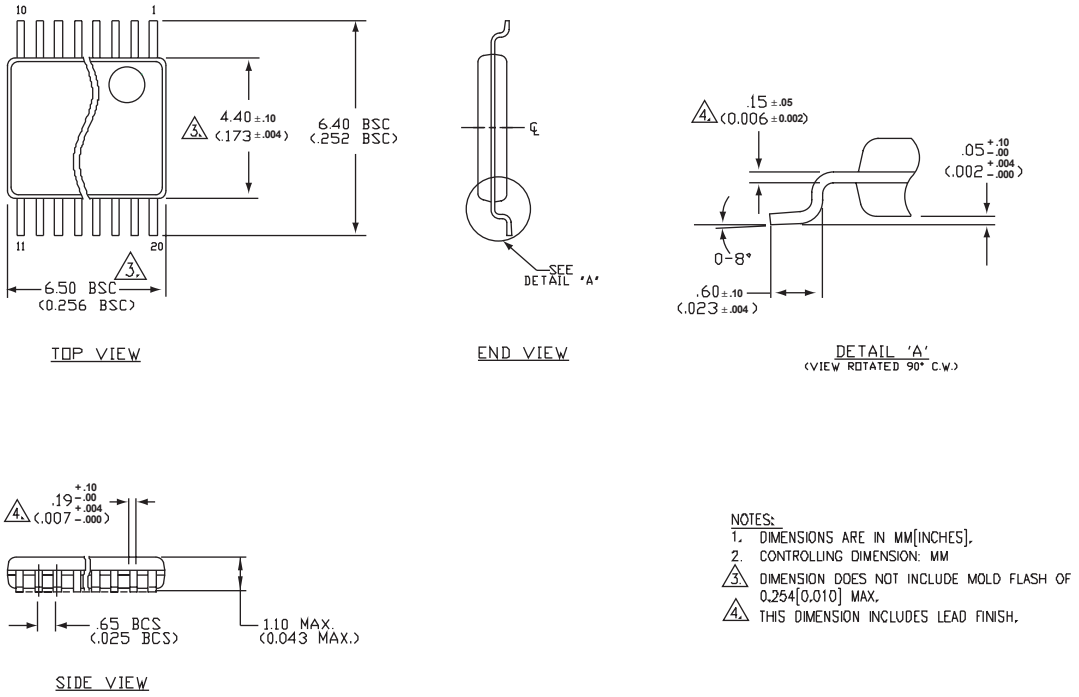
Note 1. Unused output (/Q) must be terminated to balance the output.

Note 2. Micrel's differential I/O logic devices include a V_{BB} reference pin .

Note 3. Connect unused input through 50Ω to V_{BB}. Bypass with a 0.01µF capacitor to V_{CC}, not GND.

Note 4. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

20-PIN TSSOP (K4-20-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 01

Package Notes:

Note 1. Package meets Level 1 moisture sensitivity.

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