3.3V 32-1250Mbps AnyRate® CLOCK AND DATA RECOVERY

- **Industrial temperature range (–40°C to +85°C)**
- **3.3V power supply**
- **Clock and data recovery from 32Mbps up to 1.25Gbps NRZ data stream, clock generation from 32Mbps to 1.25Gbps**
- **Complies with Bellcore, ITU/CCITT and ANSI specifications for applications such as OC-1, OC-3, OC-12, ATM, FDDI, Fibre Channel and Gigabit Ethernet as well as proprietary applications**
- **Two on-chip PLLs: one for clock generation and another for clock recovery**
- **Selectable reference frequencies**
- **Differential PECL high-speed serial I/O**
- **Line receiver input: no external buffering needed**
- **Link fault indication**
- **100k ECL compatible I/O**
- **Available in 32-pin EPAD-TQFP and 28-pin SOIC packages (28-pin SOIC is available, but NOT recommended for new designs.)**

The SY87701L is a complete Clock Recovery and Data Retiming integrated circuit for data rates from 32Mbps up to 1.25Gbps NRZ. The device is ideally suited for SONET/SDH/ATM and Fibre Channel applications and other high-speed data transmission systems.

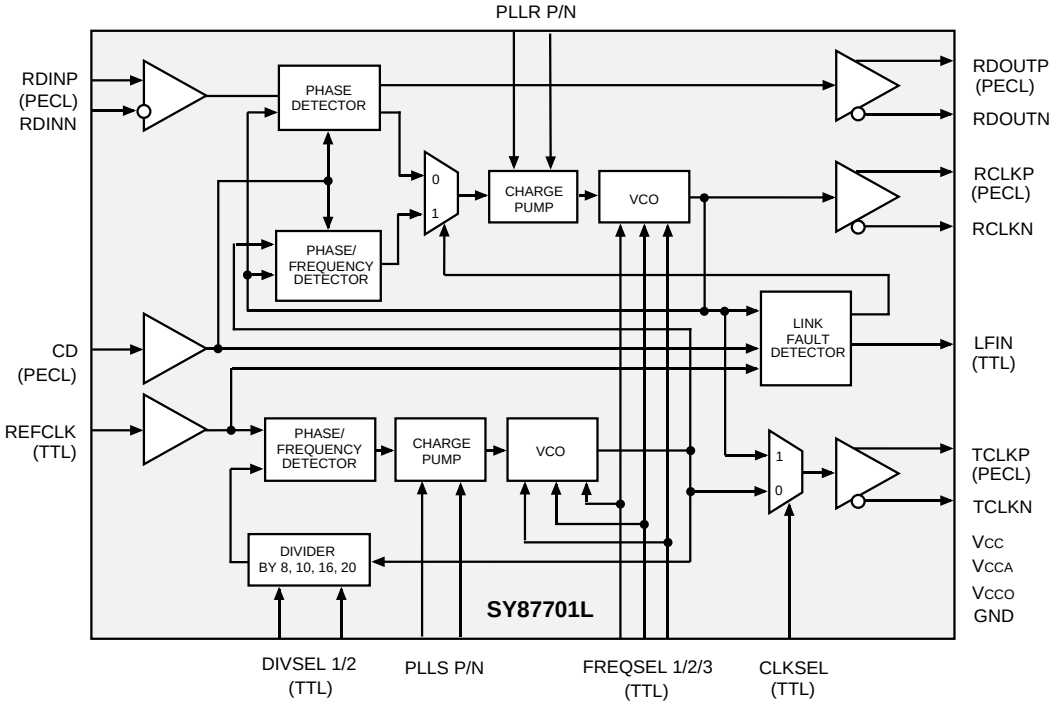
Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate source as reference.

The SY87701L also includes a link fault detection circuit.

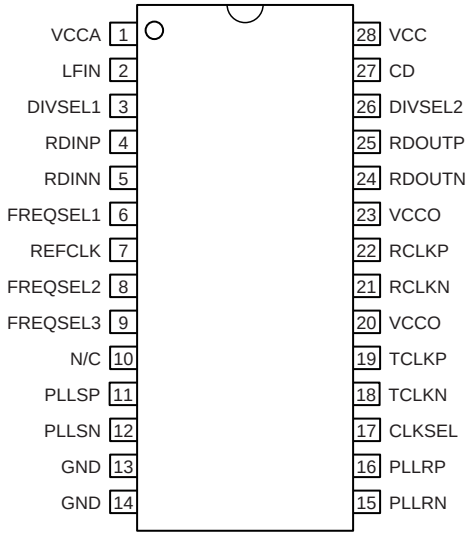
All support documentation can be found on Micrel's web site at www.micrel.com.

SONET/SDH/ATM OC-1, OC-3, OC-12, OC-24

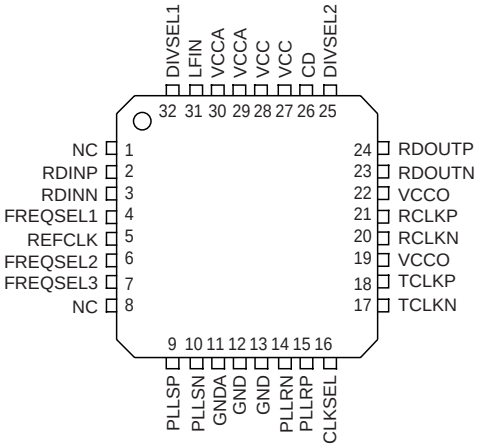
- **Fibre Channel, Escon, SMPTE 259**
- **Gigabit Ethernet/Fast Ethernet**
- **Proprietary architecture up to 1.25Gbps**



AnyRate is a registered trademark of Micrel, Inc.



28-Pin SOIC (Z28-1)



32-Pin EPAD TQFP (H32-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY87701LZI	Z28-1	Industrial	SY87701LZI	Sn-Pb
SY87701LZITR[2]	Z28-1	Industrial	SY87701LZI	Sn-Pb
SY87701LHI	H32-1	Industrial	SY87701LHI	Sn-Pb
SY87701LHITR[2]	H32-1	Industrial	SY87701LHI	Sn-Pb
SY87701LZG[3]	Z28-1	Industrial	SY87701LZG with Pb-Free bar line indicator	NiPdAu Pb-Free
SY87701LZGTR[2, 3]	Z28-1	Industrial	SY87701LZG with Pb-Free bar line indicator	NiPdAu Pb-Free
SY87701LHG	H32-1	Industrial	SY87701LHG with Pb-Free bar line indicator	NiPdAu Pb-Free
SY87701LHGTR[2, 3]	H32-1	Industrial	SY87701LHG with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Number SOIC	Pin Number TQFP	Pin Name	Pin Function
4 5	2 3	RDINP, RDINN	Serial Data Input (Differential PECL): These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of five frequency ranges depending on the state of the FREQSEL pins. See “Frequency Selection” table.
7	5	REFCLK	Reference Clock (TTL Inputs): This input is used as the reference for the internal frequency synthesizer and the “training” frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs.
27	26	CD	Carrier Detect (PECL Input): This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to look onto the clock frequency generated from REFCLK.
6 8 9	4 6 7	FREQSEL1, FREQSEL2, FREQSEL3	Frequency Select (TTL Inputs): These inputs select the output clock frequency range as shown in the “Frequency Selection” table.
3 26	32 25	DIVSEL1, DIVSEL2	Divider Select (TTL Inputs): These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the “Reference Frequency Selection” table.
17	16	CLKSEL	Clock Select (TTL Inputs): This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs.
2	31	LFIN	Link Fault Indicator (TTL Output): This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (1000ppm). LFIN is an asynchronous output.
25 24	24 23	RDOUTP, RDOUTN	Receive Data Output (Differential PECL): These ECL 100k outputs represent the recovered data from the input data stream (RDIN). This recovered data is specified against the rising edge of RCLK.
22 21	21 20	RCLKP, RCLKN	Clock Output (Differential PECL): These ECL 100k outputs represent the recovered clock used to sample the recovered data (RDOUT).
19 18	18 17	TCLKP, TCLKN	Clock Output (Differential PECL): These ECL 100k outputs represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).
11 12	9 10	PLLSP, PLLSN	Clock Synthesis PLL Loop Filter. External loop filter pins for the clock synthesis PLL.
16 15	15 14	PLLRP, PLLRN	Clock Recovery PLL Loop Filter. External loop filter pins for the receiver PLL.
	27, 28,	V_{CC}	Supply Voltage(1)
1	29, 30	V_{CCA}	Analog Supply Voltage(1)
20, 23	19, 22	V_{CCO}	Output Supply Voltage(1)
13, 14	12, 13	GND	Ground
10	1, 8	NC	No Connect

Note:

1. V_{CC}, V_{CCA}, V_{CCO} must be the same value.

Clock Recovery, as shown in the block diagram generates a clock that is at the same frequency as the incoming data bit rate at the Serial Data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the Frequency of the incoming signal varies by greater than approximately 1000ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30μs data stream of continuous 1's or 0's for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL provides jitter tolerance which is better than the specified tolerance in GR-253-CORE.

Lock Detect

The SY87701L contains a link fault indication circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than approximately 1000ppm, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within approximately 1000ppm, the PLL will be declared in lock and the lock detect output will go active.

The SY87701L PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

Input Jitter Tolerance

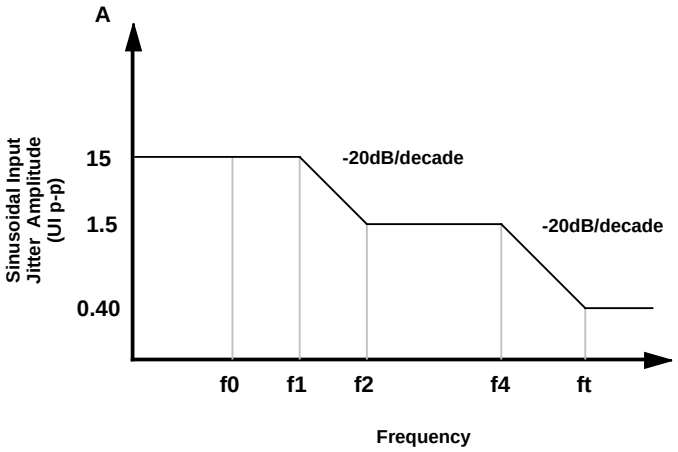
Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1dB optical/electrical power penalty. SONET input jitter tolerance requirement condition is the input jitter amplitude which causes an equivalent of 1dB power penalty.

Jitter Transfer

Jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 2.

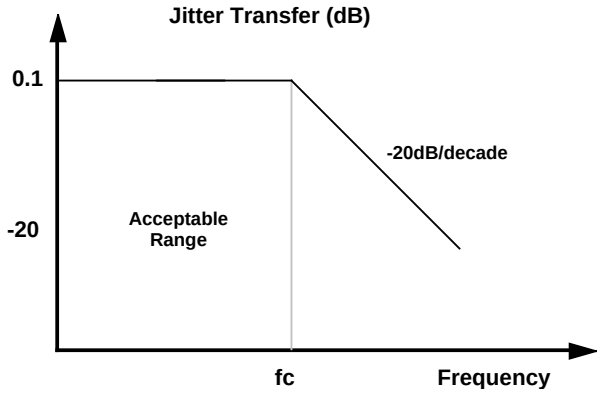
Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed .01 U.I. rms when a serial data input with no jitter is presented to the serial data inputs.



OC/STS-N Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
3	10	30	300	6.5	65
12	10	30	300	25	250

Figure 1. Input Jitter Tolerance

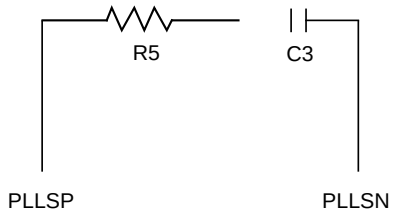


OC/STS-N Level	fc (kHz)	P (dB)
3	130	0.1
12	225	0.1

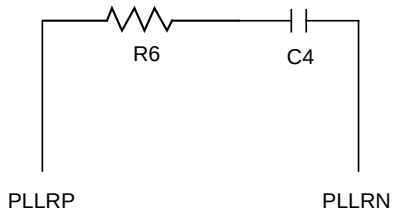
Figure 2. Jitter Transfer

			f_{VCO}/f_{RCLK}	f_{RCLK} Data Rates (Mbps)
0	0	0	1	750 - 1250
0	0	1	2	375 - 625
0	1	0	4	188 - 313
0	1	1	6	125 - 208
1	0	0	8	94 - 157
1	0	1	12	63 - 104
1	1	0	16	47 - 78
1	1	1	24	32 - 52

DIVSEL1	DIVSEL2	f_{RCLK}/f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20



Wide Range
R5 = 350Ω
C3 = 1.0μF (X7R Dielectric)



Wide Range
R6 = 680Ω
C4 = 1.0μF (X7R Dielectric)

Note:
1. Suggested Values. Values may vary for different applications.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.15V to +3.45V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  SOIC (θ_{JA})[4] ..... 80°C/W
  EPAD TQFP (θ_{JA})[5]
    0lfpm airflow ..... 27.6°C/W
    200lfpm airflow ..... 22.6°C/W
    500lfpm airflow ..... 20.7°C/W

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Power Supply Current			170	230	mA

$_{CC}$ = V_{CCO} = V_{CCA} = 3.3V ±5%; T_A = –40°C to +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC} –1.165		V_{CC} –0.880	V
V_{IL}	Input LOW Voltage		V_{CC} –1.810		V_{CC} –1.475	V
V_{OH}	Output HIGH Voltage	50Ω to V_{CC} –2V	V_{CC} –1.075		V_{CC} –0.830	V
V_{OL}	Output LOW Voltage	50Ω to V_{CC} –2V	V_{CC} –1.860		V_{CC} –1.570	V
I_{IL}	Input LOW Current	V_{IN} = V_{IL}(min)	0.5			µA

$_{CC}$ = V_{CCO} = V_{CCA} = 3.3V ±5%; T_A = –40°C to +85°C; unless noted.

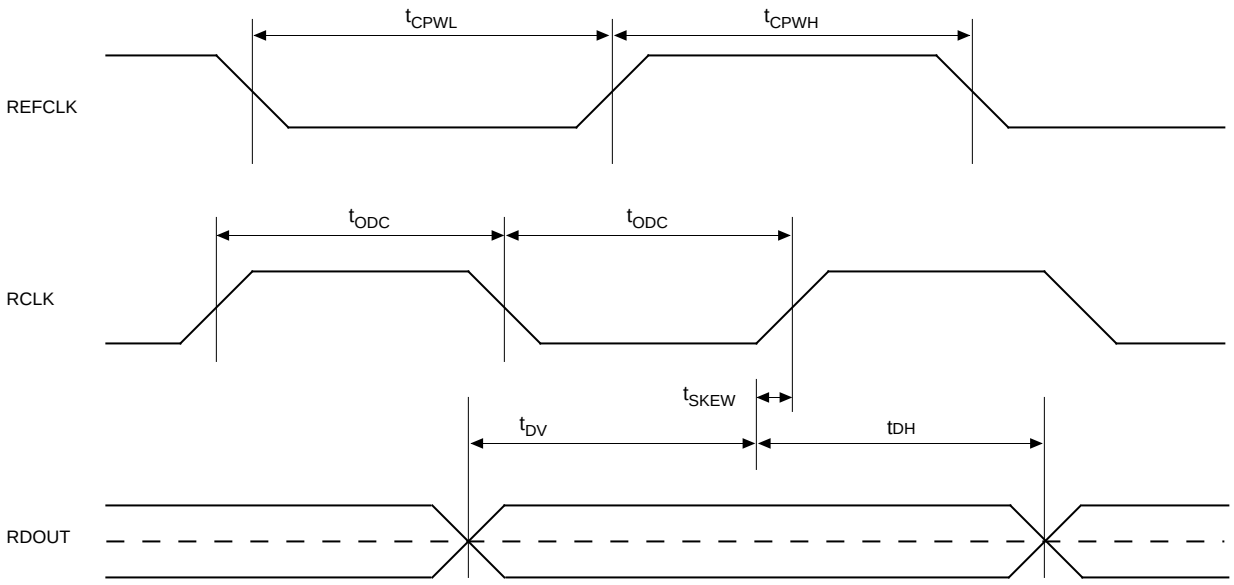
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –0.4mA	2.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA			0.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V, V_{CC} = max. V_{IN} = V_{CC}, V_{CC} = max.	–175		 +100	µA µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V, V_{CC} = max.	–300			µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (maximum 1 sec)	–15		–100	mA

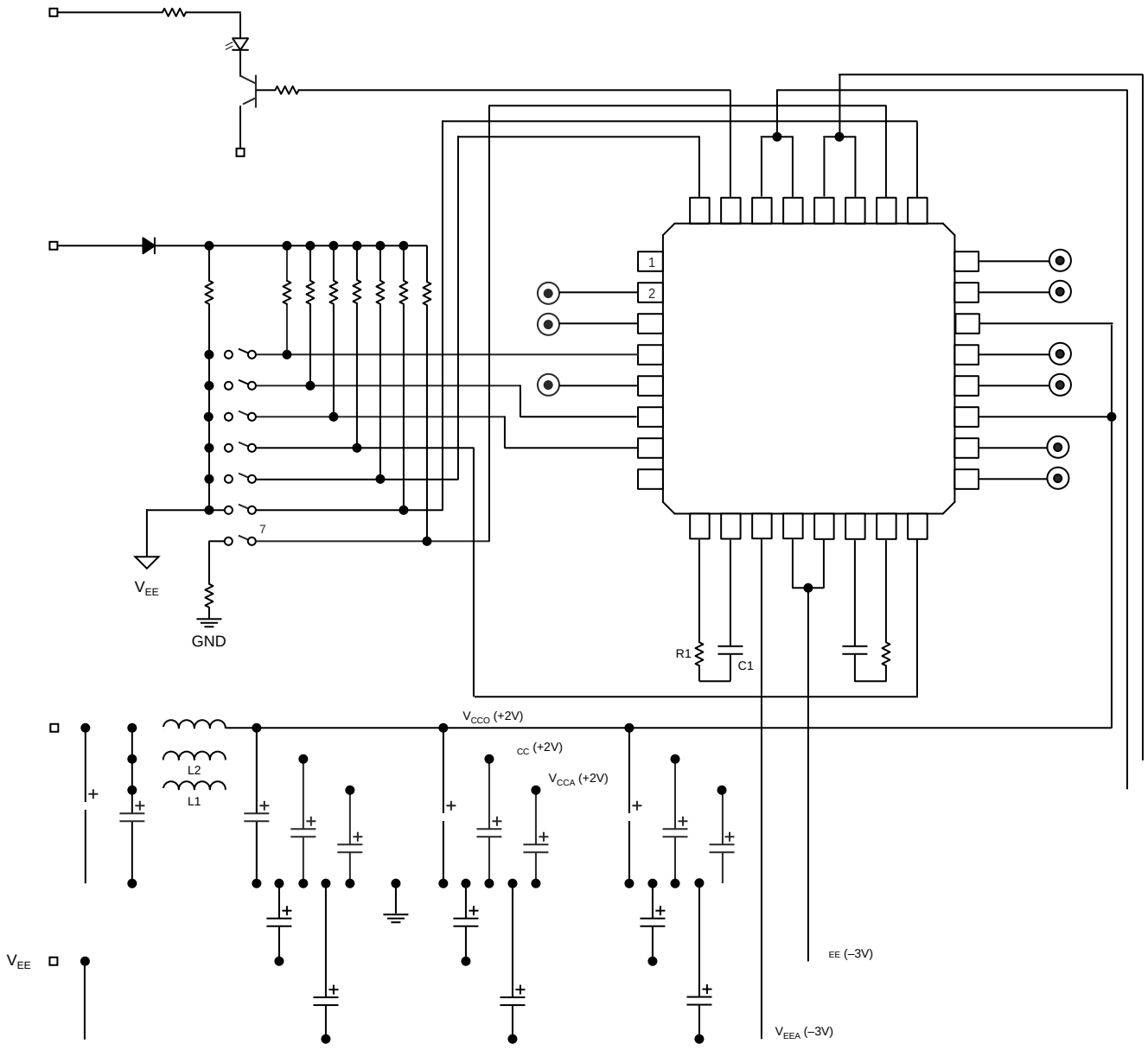
Notes:

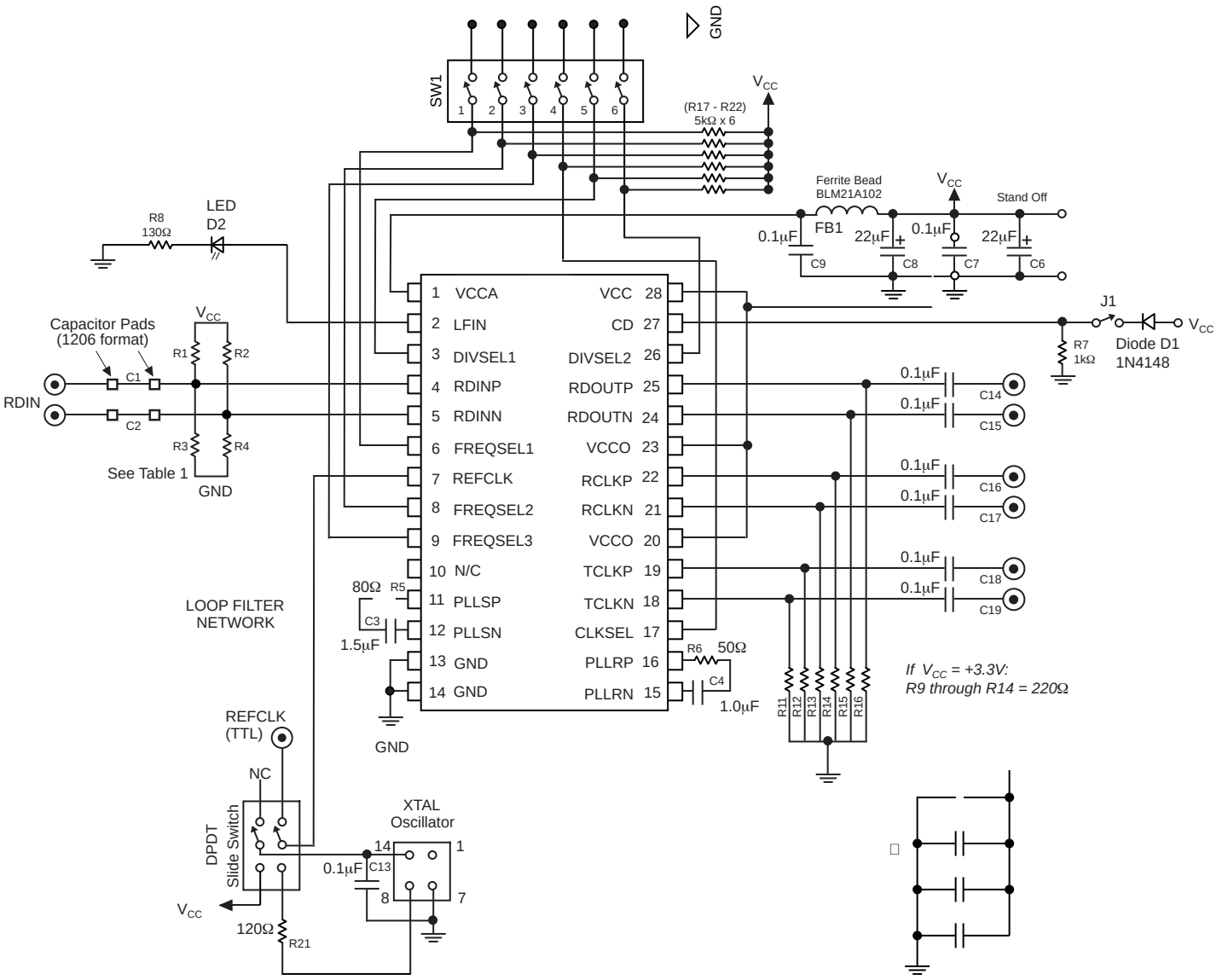
1. Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to “Absolute Maximum Ratings” conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Airflow of 500lfpm recommended for 28-pin SOIC.
4. 28-pin SOIC package is NOT recommended for new designs.
5. Using JEDEC standard test boards with die attach pad soldered to PCB. See www.amkor.com for additional package details.

$_{CC}$ = V_{CCO} = V_{CCA} = 3.3V ±5%; T_A = –40°C to +85°C; unless noted.

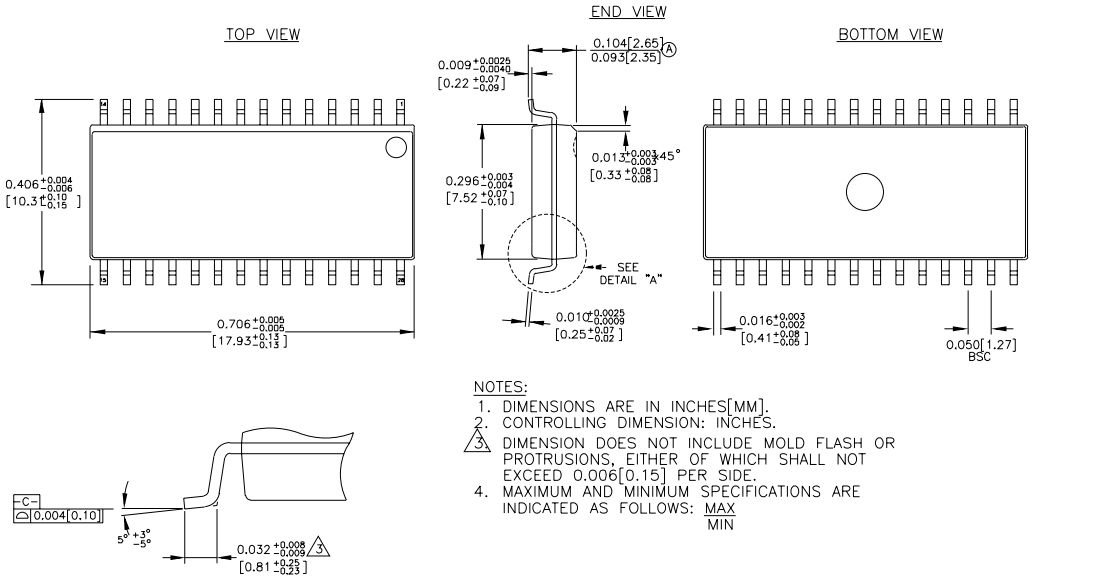
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{VCO}	VCO Center Frequency	f_{REFCLK} × Byte Rate	750		1250	MHz
Δf_{VCO}	VCO Center Frequency Tolerance	Nominal		5		%
t_{ACQ}	Acquisition Lock Time				15	µs
t_{CPWH}	REFCLK Pulse Width HIGH		4			ns
t_{CPWL}	REFCLK Pulse Width LOW		4			ns
t_{ir}	REFCLK Input Rise Time			0.5	2	ns
t_{ODC}	Output Duty Cycle (RCLK/TCLK)		45		55	% of UI
t_r, t_f	ECL Output Rise/Fall Time (20% to 80%)	50Ω to V_{CC} –2V	100		500	ps
t_{SKEW}	Recovered Clock Skew		–200		+200	ps
t_{DV}	Data Valid		$1/(2 \times f_{RCLK}) – 200$			ps
t_{DH}	Data Hold		$1/(2 \times f_{RCLK}) – 200$			ps




1
2
7
V_{EE}
GND
R1
C1
V_{CCO} (+2V)
$_{CC}$ (+2V)
V_{CCA} (+2V)
L2
L1
V_{EE}
$_{EE}$ (–3V)
V_{EEA} (–3V)


GND
SW1
1 2 3 4 5 6
VCC
(R17 - R22)
5kΩ x 6
Ferrite Bead
BLM21A102
FB1
Stand Off
0.1µF
22µF
C9
C8
C7
C6
R8
130Ω
LED
D2
J1
R7
1kΩ
Diode D1
1N4148
Capacitor Pads
(1206 format)
R1
R2
C1
C2
RDIN
R3
R4
See Table 1
GND
1 VCCA
2 LFIN
3 DIVSEL1
4 RDINP
5 RDINN
6 FREQSEL1
7 REFCLK
8 FREQSEL2
9 FREQSEL3
10 N/C
11 PLLSP
12 PLLSN
13 GND
14 GND
VCC 28
CD 27
DIVSEL2 26
RDOUTP 25
RDOUTN 24
VCCO 23
RCLKP 22
RCLKN 21
VCCO 20
TCLKP 19
TCLKN 18
CLKSEL 17
PLLRP 16
PLLRN 15
0.1µF
C14
C15
C16
C17
C18
C19
80Ω R5
C3
1.5µF
LOOP FILTER
NETWORK
R6 50Ω
C4
1.0µF
R11
R12
R13
R14
R15
R16
If VCC = +3.3V:
R9 through R14 = 220Ω
REFCLK
(TTL)
NC
DPDT
Slide Switch
XTAL
Oscillator
14
1
8
7
0.1µF C13
120Ω
R21

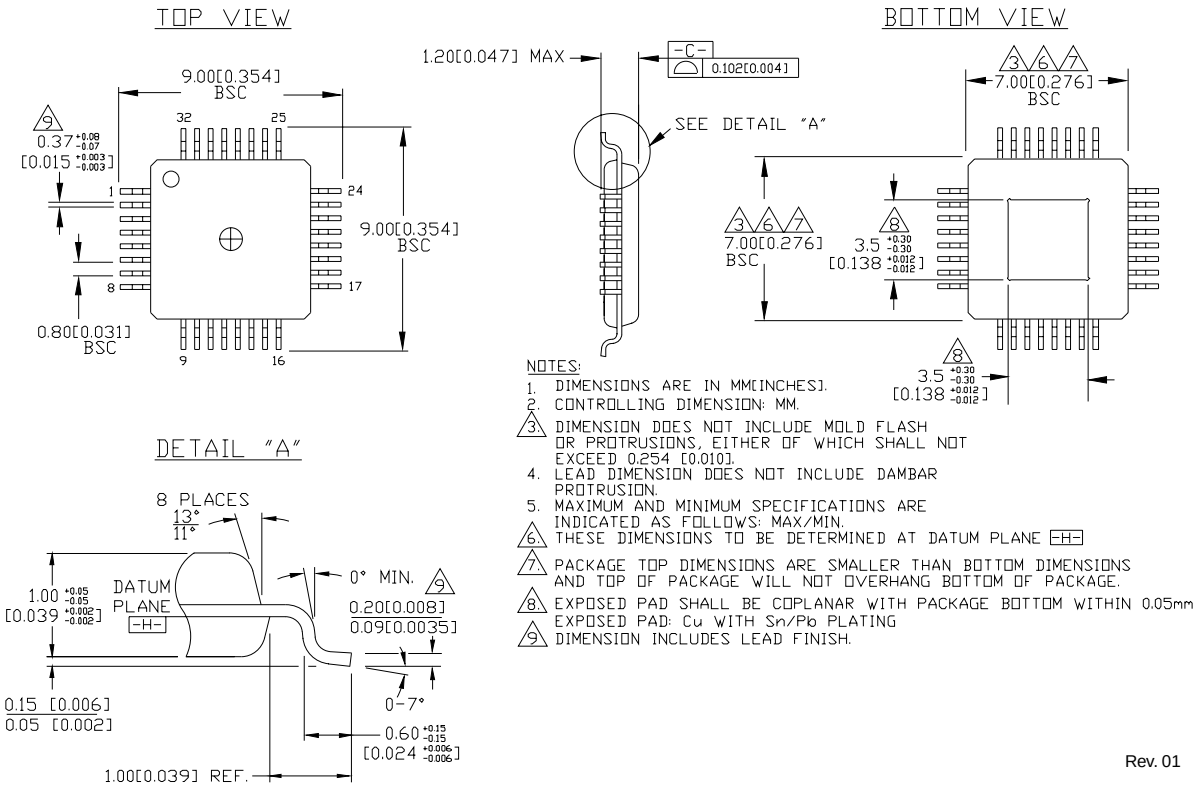
C1, C2	VJ0603Y105JXJAT	Vishay	1.0μF Ceramic Capacitor, Size 0603 X7R Dielectric, Loop Filter, Critical	2
C3, C4	VJ0603Y105JXJAT	Vishay	1.0μF Ceramic Capacitor, Size 0603 X7R Dielectric, Loop Filter, Optional	2
C5	ECS-T1ED226R	Panasonic	22μF Tantalum Electrolytic Capacitor, Size D	1
C6	ECU-V1H104KBW	Panasonic	0.1μF Ceramic Capacitor, Size 1206 X7R Dielectric, Power Supply Decoupling	1
C7, C8, C9, C10	ECS-T1EC685R	Panasonic	6.8μF Tantalum Electrolytic Capacitor, Size C	4
C19	ECJ-3YB1E105K	Panasonic	1.0μF Ceramic Capacitor, Size 1206 X7R Dielectric, VEEA Decoupling	1
C11, C13	ECU-V1H104KBW	Panasonic	0.1μF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCO/VCC Decoupling	1
C15, C17	ECU-V1H104KBW	Panasonic	0.1μF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCA/VEEA Decoupling	1
C20	ECU-V1H104KBW	Panasonic	0.1μF Ceramic Capacitor, Size 1206 X7R Dielectric, VEEA Decoupling	1
C12, C14	ECU-V1H103KBW	Panasonic	0.01μF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCO/VCC Decoupling	1
C16, C18	ECU-V1H103KBW	Panasonic	0.01μF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCA/VEEA Decoupling	1
C21	ECU-V1H103KBW	Panasonic	0.01μF Ceramic Capacitor, Size 1206 X7R Dielectric, VEEA Decoupling	1
D1	1N4148		Diode	1
D2	P300-ND/P301-ND	Panasonic	T-1 3/4 Red LED	1
J1, J2, J3, J4, J5 J6, J7, J8, J9, J10, J11, J12	142-0701-851	Johnson Components	Gold Plated, Jack, SMA, PCB Mount	12
L1, L2, L3	BLM21A102F	Murata	Ferrite Beads, Power Noise Suppression	3
Q1	NTE123A	NTE	2N2222A Buffer/Driver Transistor, NPN	1
R1			350Ω Resistor, 2%, Size 0402 Loop Filter Component, Critical	1
R2			680Ω Resistor, 2%, Size 0402 Loop Filter Component, Critical	1
R3, R4, R5, R6 R7, R8, R9, R10			5kΩ Pull-up Resistors, 2%, Size 1206	8
R11			1kΩ Pull-down Resistor, 2%, Size 1206	1
R12			12kΩ Resistor, 2%, Size 1206	1
R13			130Ω Pull-up Resistor, 2%, Size 1206	1
SW1	206-7	CTS	SPST, Gold Finish, Sealed Dip Switch	1

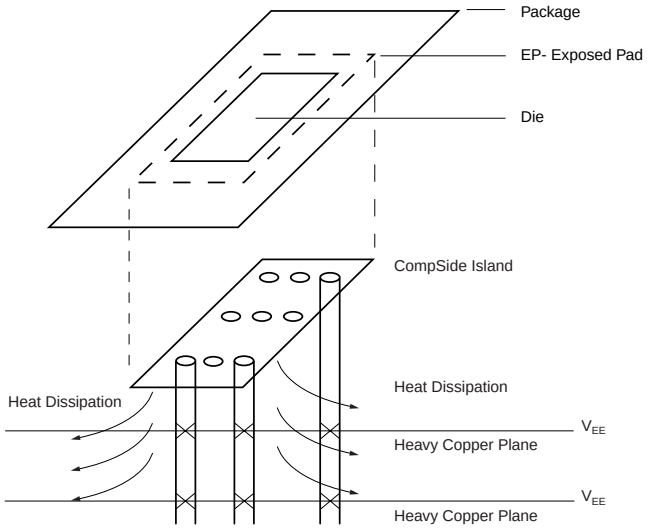


Rev. 02

Note:

The 28 Lead SOIC package is NOT recommended for new designs.





PCB Thermal Consideration for 32-Pin EPAD-TQFP Package

APPENDIX A

Layout and General Suggestions

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques.
2. Signal paths should have, approximately, the same width as the device pads.
3. All differential paths are critical timing paths, where skew should be matched to within ±10ps.
4. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
5. Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
7. Higher speed operation may require use of fundamental-tone (third-overtone typically have more jitter) crystal based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
8. All unused outputs must be terminated. To conserve power, unused PECL outputs can be terminated with a 1kΩ resistor to V_{EE}.

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