TAS2564 7-W Class-D Smart Amp With Integrated 13-V Class-H boost &I/V Sense for Speaker Protection

1 Features

- Key Features
  - 256 Level, 13-V Class-H Boost
  - Speaker Current and Voltage Sense
  - Inter Chip Alignment (ICLA) of gain across devices.
- Output Power
  - 7-W 0.1% THD+N (8 Ω at 3.8 V)
- Power Consumption (1% THD+N, 4.2 V into 8 Ω)
  - 83.5% efficiency at 1 W
  - <1uA HW shutdown VBAT Current
- Power Supplies
  - VBAT: 2.7 V to 5.5 V
  - VDD: 1.65 V to 1.95 V
  - Digital (1.5 V) is internally generated from VDD.
  - IO and Analog supplies are internally shorted to VDD.
- Protections
  - Battery: Advanced Brown Out
  - Clipping: VBAT Tracking Peak Voltage Limiter
  - Transducer: DC Detection and Prevention
  - Device: Thermal and Over Current Protection
- Interfaces and Control
  - I2S/TDM: 8 Channels of 32 bit each up to 96 KSPS
  - I2C: 4 selectable addresses
  - 16 KSPS to 192 KSPS Sample Rates
  - MCLK Free operation
- Performance
  - Speaker/Receiver Mode with Dynamic Noise Control of Idle Channel Noise (ICN)
  - Receiver Mode: 10 µVrms ICN
  - Speaker Mode: 15 µVrms ICN
  - Spread Spectrum Low EMI Mode
  - 110 dB SNR at 1% THD+N(8Ω)

2 Applications

- Mobile phones
- Tablets
- Bluetooth speakers
- Consumer audio devices
- Wireless speakers

3 Description

The TAS2564 is a digital input, Class-D audio amplifier with a 256 level, 13 V Class-H boost. The robust 13 V Class-H boost provides the power needed for peak output while the algorithmically-controlled 256 level boost reduces the average power consumption. The boost is easily configured with PurePath Console GUI.

The Class-D amplifier is capable of delivering 7 W of peak power into an 8 Ω. TAS2564 is 83.5% efficient at 1 W output level. Integrated speaker voltage and current sense provides real time monitoring to keep speakers in the safe operation area.

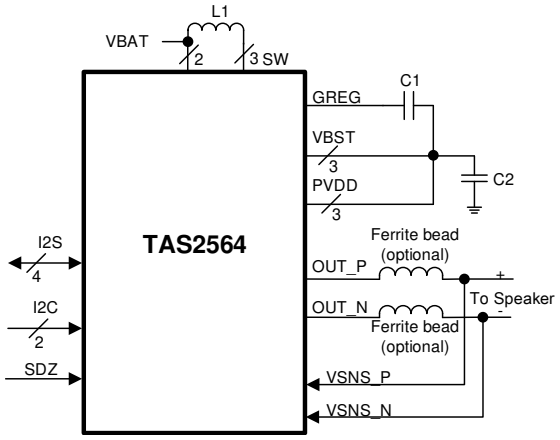
Battery tracking peak voltage limiter with brown-out prevention optimizes amplifier headroom over the entire battery discharge. Up to four devices can share a common bus via I2S/TDM + I 2C interfaces.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS2564	DSBGA	2.63 mm x 2.46 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 I^2C Timing Requirements ... 11
6.7 TDM Port Timing Requirements ... 11
6.8 Typical Characteristics ... 13
7 Parameter Measurement Information ... 17
8 Detailed Description ... 18
8.1 Overview ... 18
8.2 Functional Block Diagram ... 18
8.3 Feature Description ... 18
8.4 Device Functional Modes ... 25
8.5 Register Maps ... 52
9 Application and Implementation ... 97
9.1 Application Information ... 97
9.2 Typical Application ... 97
10 Power Supply Recommendations ... 100
10.1 Power Supplies ... 100
10.2 Power Supply Sequencing ... 100
11 Layout ... 101
11.1 Layout Guidelines ... 101
11.2 Layout Example ... 102
12 Device and Documentation Support ... 106
12.1 Documentation Support ... 106
12.2 Receiving Notification of Documentation Updates ... 106
12.3 Community Resources ... 106
12.4 Trademarks ... 106
12.5 Electrostatic Discharge Caution ... 106
12.6 Glossary ... 106
13 Mechanical, Packaging, and Orderable Information ... 107
13.1 Package Option Addendum ... 111

4 Revision History

Changes from Original (October 2019) to Revision A	Page
• Changed device status to Production Data	1

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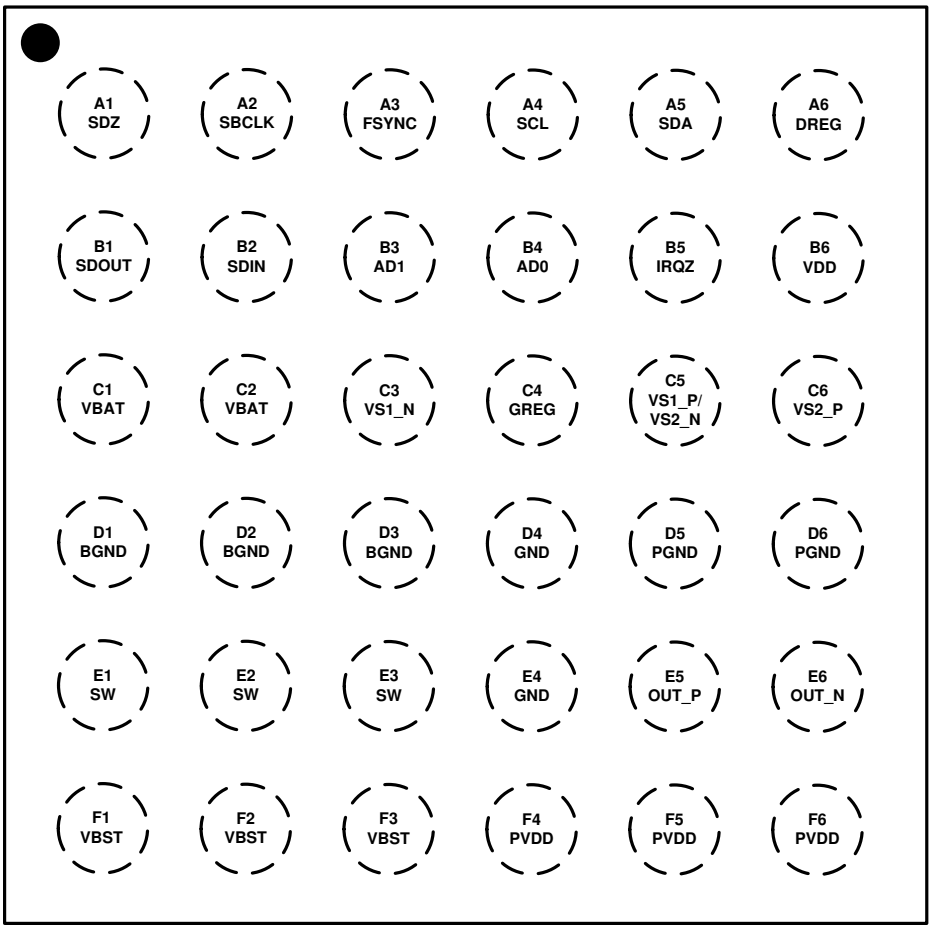
5 Pin Configuration and Functions

YFP Package
36-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
AD0	B4	I	I_2C address pin LSB.
AD1	B3	I	I_2C address pin LSB+1.
BGND	D1	P	Boost ground. Connect to PCB GND plane.
	D2		
	D3		
DREG	A6	P	Digital core voltage regulator output. Bypass to GND with a cap. Do not connect to external load.
FSYNC	A3	IO	I2S word clock or TDM frame sync.
GREG	C4	P	High-side gate CP regulator output. Do not connect to external load.
GND	D4	P	Digital ground. Connect to PCB GDN plane.
	E4		
IRQZ	B5	O	Open drain, active low interrupt pin. Pull up to VDDD with resistor if optional internal pull up is not used.
OUT_N	E6	O	Class-D negative output.
OUT_P	E5	O	Class-D positive output.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PGND	D5	P	Power stage ground. Connect to PCB GND plane.
	D6		
PVDD	F4	P	Power stage supply.
	F5		
	F6		
SBCLK	A2	IO	I2S/TDM serial bit clock.
SCL	A4	I	I^2C Clock Pin. Pull up to VDD with a resistor.
SDA	A5	IO	I^2C Data Pin. Pull up to VDD with a resistor.
SDIN	B2	I	I2S/TDM serial data input.
SDOUT	B1	IO	I2S/TDM serial data output.
SDZ	A1	I	Low = Hardware Shutdown. High= Device Enabled
SW	E1	P	Boost converter switch input.
	E2		
	E3		
VBAT	C1	P	Battery power supply input. Connect to 2.7 V to 5.5 V supply and decouple with a cap.
	C2		
VBST	F1	P	Boost converter output. Do not connect to external load.
	F2		
	F3		
VDD	B6	P	Analog, digital, and IO power supply. Connect to 1.8 V supply and decouple to GND with cap.
VSNS1_N	C3	I	Voltage sense negative input. Connect to Class-D OUT_N output after Ferrite bead filter.
VSNS1_P/VSNS2_N	C5	I	Voltage sense Center input. Connect to Speaker Center Tap.
VSNS2_P	C6	I	Voltage sense positive input. Connect to Class-D OUT_P output after Ferrite bead filter.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Analog / IO Supply Voltage	VDD	–0.3	2	V
Battery Supply Voltage	VBAT	–0.3	6	V
Boost Pin	VBST [2]	-0.3	18.5	V
Power Supply Voltage	PVDD [2]	-0.3	18.5	V
Switching Pin	SW	-0.7	16	V
High Side Regulator Pin	GREG	-0.3	PVDD+6	V
Digital Regular Pin	DREG	-0.3	1.65	V
Input voltage [3]	Digital IOs referenced to VDD supply	–0.3	VDD+0.3	V
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) PVDD can handle 19V transients for less than 10ns
(3) All digital inputs and IOs are failsafe.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 OUT_N / OUT_P / VSNS_N / VSNS_P Pins [1]	±4000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBAT	Supply voltage	2.7	3.6	5.5	V
VDD	Supply voltage	1.65	1.8	1.95	V
PVDD	Supply voltage - external boost mode	VBAT		16	V
V_{IH}	High-level digital input voltage		VDD		V
V_{IL}	Low-level digital input voltage		0		V
R_{SPK}	Minimum speaker impedance	6.4	8		Ω
L_{SPK}	Minimum speaker inductance	10			µH

6.4 Thermal Information

THERMAL METRIC [1]		TAS2564 YFF (WCSP) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25 °C, VBAT = 3.8 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 17.5 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT and OUTPUT						
V_{IH}	High-level digital input logic voltage threshold	All digital pins except SDA and SCL	0.65 × VDD			V
V_{IL}	Low-level digital input logic voltage threshold	All digital pins except SDA and SCL			0.35 × VDD	V
$V_{IH(I2C)}$	High-level digital input logic voltage threshold	SDA and SCL	0.7 × VDD			V
$V_{IL(I2C)}$	Low-level digital input logic voltage threshold	SDA and SCL			0.3 × VDD	V
V_{OH}	High-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I_{OH} = 2 mA.	VDD – 0.45 V			V
V_{OL}	Low-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I_{OL} = –2 mA.			0.45	V
$V_{OL(I2C)}$	Low-level digital output voltage	SDA and SCL; $I_{OL(I2C)}$ = –2 mA.			0.2 × VDD	V
$V_{OL(IRQZ)}$	Low-level digital output voltage for IRQZ open drain Output	IRQZ; $I_{OL(IRQZ)}$ = –2 mA.			0.45	V
I_{IH}	Input logic-high leakage for digital inputs	All digital pins; Input = VDD.	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins; Input = GND.	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pull down resistance for digital input/IO pins when asserted on	SDOUT, SDIN, FSYNC, SBCLK		50		kΩ
AMPLIFIER PERFORMANCE - Internal Boost						
	Output Voltage for Full-scale digital Input	Measured at -6 dB FS input and scaled by 6dB		7.5		Vrms
P_{OUT}	Maximum Continuous Output Power	R_L = 32Ω + 33 µH, THD+N = 0.03 %, f_{in} = 1 kHz		1.75		W
		R_L = 8 Ω + 33 µH, THD+N = 0.03 %, f_{in} = 1 kHz		7		W
	System efficiency at P_{OUT} = 1 W	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		83		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		83.5		%
	System efficiency at P_{OUT} =0.5 W	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		85		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		85.5		%
	System efficiency at 0.1% THD+N power level	R_L = 8 Ω + 33 µH, P_{OUT} = 7W, f_{in} = 1 kHz,		81		%
THD+N	Total harmonic distortion + noise	P_{OUT} = 0.25 W, R_L = 32Ω + 33 µH, f_{in} = 1 kHz		0.01		%
		P_{OUT} = 1 W, R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		0.01		%
V_N	Idle channel noise	A-Weighted, 20 Hz - 20 kHz		14.8		µV
F_{PWM}	Class-D PWM switching frequency	Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 44.1, 88.2, 174.6 kHz		352.8		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 48, 96, 192 kHz		384		kHz
V_{OS}	Output offset voltage		-1.2		1.2	mV
DNR	Dynamic range	A-Weighted, -60 dBFS Method		110		dB
SNR	Signal to noise ratio	A-Weighted, Referenced to 1 % THD+N Output Level		110		dB

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Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.8 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 17.5 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{CP}	Click and pop performance	Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. Measured with APx Plugin.		3.4		mV
	Programmable digital gain range		0		23	dBV
	Programmable digital gain step size			0.5		dB
AV_{ERROR}	Amplifier gain error	P_{OUT} = 1 W		±0.1		dB
	Mute attenuation	Device in Shutdown or Muted in Normal Operation		110		dB
	VBAT power-supply rejection ratio	VBAT = 3.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		108		dB
		VBAT = 3.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		dB
	AVDD power-supply rejection ratio	VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		98		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		93		dB
	Turn on time from release of SW shutdown	No Volume Ramping		1.8		ms
		Volume Ramping		4.5		ms
	Turn off time from assertion of SW shutdown to amp Hi-Z	No Volume Ramping		0.75		ms
		Volume Ramping		12.5		ms
AMPLIFIER PERFORMANCE - Receiver Mode						
	Output Voltage for Full-scale digital Input	Measured at -6 dB FS input and scaled by 6dB		2		Vrms
P_{OUT}	Maximum Continuous Output Power	R_L = 32Ω + 33 µH, THD+N = 0.03 %, f_{in} = 1 kHz		124.4		mW
		R_L = 8 Ω + 33 µH, THD+N = 0.03 %, f_{in} = 1 kHz		0.45		W
	System efficiency at P_{OUT} = 100 mW	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		63.5		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		65.5		%
	System efficiency at P_{OUT} =0.45 W	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		84.5		%
		R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, VBAT = 4.2 V		85		%
THD+N	Total harmonic distortion + noise	P_{OUT} = 1 W, R_L = 8 Ω + 33 µH, f_{in} = 1 kHz		.01		%
V_N	Idle channel noise	A-Weighted, 20 Hz - 20 kHz, DAC Modulator Running		10		µV
F_{PWM}	Class-D PWM switching frequency	Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 44.1, 88.2, 174.6 kHz		352.8		kHz
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 48, 96, 192 kHz		384		kHz
V_{OS}	Output offset voltage		-1		1	mV
DNR	Dynamic range	A-Weighted, -60 dBFS Method		101.2		dB
SNR	Signal to noise ratio	A-Weighted, Referenced to 1 % THD+N Output Level		105.73		dB
K_{CP}	Click and pop performance	Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. Measured with APx Plugin.		3.4		mV
	Programmable digital gain range		0		23	dBV
	Programmable digital gain step size			0.5		dB
AV_{ERROR}	Amplifier gain error	P_{OUT} = 1 W		±0.1		dB
	Mute attenuation	Device in Shutdown or Muted in Normal Operation		113		dB

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.8 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 17.5 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VBAT power-supply rejection ratio	VBAT = 3.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		110		dB
		VBAT = 3.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		95		dB
	AVDD power-supply rejection ratio	VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		102		dB
		VDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		102		dB
	Turn on time from release of SW shutdown	No Volume Ramping		1.8		ms
		Volume Ramping		4.5		ms
	Turn off time from assertion of SW shutdown to amp Hi-Z	No Volume Ramping		0.75		ms
		Volume Ramping		12.5		ms
BOOST CONVERTER						
	Max Output Voltage	0.1A DC load, Average voltage (w/o including ripple)		13		V
	Startup inrush current limit	default setting		1.5		A
	Startup inrush limit time	default setting		0.45		ms
	Switching Frequency	PFM mode		50		kHz
		Current Control Mode		4		MHz
	Minimum Switching Frequency	Current Control Mode		400		KHz
	Inductor Peak Current Limit	default setting		5		A
DIE TEMPERATURE SENSOR						
	Resolution			8		bits
	Die temperature measurement range		-40		150	°C
	Die temperature resolution			0.75		°C
	Die temperature accuracy			±5		°C
VOLTAGE MONITOR						
	Resolution			10		bits
	VBAT measurement range		2		6	V
	VBAT resolution			6		mV
	VBAT accuracy			±25		mV
TDM SERIAL AUDIO PORT						
	PCM Sample Rates & FSYNC Input Frequency		16		192	kHz
	SBCLK Input Frequency	I^2S/TDM Operation	0.512		24.57	MHz
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			1	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			10	ns
	SBCLK Cycles per FSYNC in I^2S and TDM Modes	Values: 64, 96, 128, 192, 256, 384 and 512	64		512	Cycles
PCM PLAYBACK CHARACTERISTICS to fs ≤ 48 kHz						
fs	Sample Rates		16		48	kHz
	Passband LPF Corner			0.454		fs
	Passband Ripple	20 Hz to LPF cutoff	-0.3		0.3	dB
	Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Group Delay	DC to 0.454 fs			8.6	1/fs

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Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.8 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 17.5 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PCM PLAYBACK CHARACTERISTICS fs > 48 kHz						
fs	Sample Rates		88.2		192	kHz
	Passband LPF Corner	fs = 96 kHz		0.42		fs
		fs = 192 kHz		0.21		fs
	Passband Ripple	DC to LPF cutoff	-0.5		0.5	dB
	Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Group Delay	DC to 0.375 fs for 96 kHz			8.6	1/fs
CURRENT SENSE						
DNR	Dynamic range	Un-Weighted, Relative to 0 dBFS		69		dB
THD+N	Total harmonic distortion + noise	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, P_{OUT} = 1 W		-56		dB
	Full-scale input current			3.3		A
	Current-sense accuracy	R_L = 8 Ω + 33 µH, I_{OUT} = 354 mA_{RMS} (P_{OUT} = 1 W @ 1kHz)		±1		%
	Current-sense gain error over temperature	0°C to 70°C, 8 Ω, using a 60Hz -40dB pilot tone		±1		%
	Current-sense gain error over output power	50mW to 0.1 % THD+N level, f_{in} = 1 kHz, 8 Ω, using a 60Hz -40dB pilot tone		±1.5		%
	LPF passband corner	fs = 16 kHz to 48 kHz		0.417		fs
		fs = 96 kHz		0.208		fs
		fs = 192 kHz		0.104		fs
	LPF passband ripple		-0.05		0.05	dB
	LPF stopband attenuation	0.55 fs		60		dB
	LPF group delay	DC to 0.417 fs			5.7	1/fs
VOLTAGE SENSE						
DNR	Dynamic range	Un-Weighted, Relative 0 dBFS		69		dB
THD+N	Total harmonic distortion + noise	R_L = 8 Ω + 33 µH, f_{in} = 1 kHz, P_{OUT} = 1W		-60		dB
	Full-scale input voltage			14		V_{PK}
	Voltage-sense accuracy	R_L = 8 Ω + 33 µH, I_{OUT} = 354 mA_{RMS} (P_{OUT} = 1 W)		±0.5%		
	Voltage-sense gain error over temperature	0°C to 70°C, 8 Ω, using a 60Hz -40dB pilot tone		±0.5%		
	Voltage-sense gain error over output power	50mV to 0.1 % THD+N level, 8 Ω, using a 60Hz -40dB pilot tone		±0.5%		
	LPF passband corner	fs = 16 kHz to 48 kHz		0.417		fs
		fs = 96 kHz		0.208		fs
		fs = 192 kHz		0.104		fs
	LPF passband ripple		-0.05		0.05	dB
	LPF stopband attenuation	0.55 fs		60		dB
	LPF group delay	DC to 0.417 fs			5.7	1/fs
VOLTAGE/CURRENT SENSE RATIO						
	Gain ratio error over output power	10uW to 0.1% THD+N level, fin = 1 kHz, 8Ω, using a 60Hz -40dB pilot tone		±3%		
	Gain ratio error over output power	250uW to 0.1 % THD+N level, fin = 1 kHz, 8Ω, using a 60Hz -40dB pilot tone		±2%		
	Gain ratio error over output power	50mW to 0.1 % THD+N level, fin = 1 kHz, 8Ω, using a 60Hz -40dB pilot tone		±1%		
	Gain ratio drift over temperature	0°C to 70°C		±1%		

Electrical Characteristics (continued)

T_A = 25 °C, VBAT = 3.8 V, (External PVDD = 12 V), VDD = 1.8 V, R_L = 8Ω + 33 µH, f_{in} = 1 kHz, SSM, f_s = 48 kHz, Gain = 17.5 dBV (External PVDD Gain=18 dBV), SDZ = 1, Thermal Foldback Disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V/I phase error			300		ns
TYPICAL CURRENT CONSUMPTION						
	Current consumption in hardware shutdown	SDZ = 0, VBAT		0.1		µA
		SDZ = 0, VDD		1		µA
	Current consumption in software shutdown	All Clocks Stopped, VBAT		0.5		µA
		All Clocks Stopped, VDD		10		µA
	Current consumption in idle channel	Clocking 0s PCM mode, VBAT		2.7		mA
		Clocking 0s PCM mode, VDD		8.9		mA
	Current consumption during active operation with IV sense disabled	f_s = 48 kHz, VBAT		4.6		mA
		f_s = 48 kHz, VDD		8.9		mA
	Current consumption during active operation with IV sense enabled	f_s = 48 kHz, VBAT		4.6		mA
		f_s = 48 kHz, VDD		11.4		mA
PROTECTION CIRCUITRY						
	Thermal shutdown temperature			140		°C
	Thermal shutdown retry			1.5		s
	VBAT undervoltage lockout threshold (UVLO)	UVLO is asserted	2			V
		UVLO is released			2.55	V
	Output short circuit limit	Output to Output, Output to GND, Output to VBST or Output to VBAT Short		4.5		A

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6.6 I²C Timing Requirements

T_A = 25 °C, VDD = 1.8 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Standard-Mode					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0		3.45	µs
$t_{SU;DAT}$	Data set-up time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
C_b	Capacitive load for each bus line			400	pF
Fast-Mode					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	40.6			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	100			ns
t_r	SDA and SCL rise time	20 + 0.1 × Cb		300	ns
t_f	SDA and SCL fall time	20 + 0.1 × Cb		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF
Fast-Mode Plus					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	LOW period of the SCL clock	0.5			µs
t_{HIGH}	HIGH period of the SCL clock	0.26			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0			µs
$t_{SU;DAT}$	Data set-up time	50			ns
t_r	SDA and SCL Rise Time			120	ns
t_f	SDA and SCL Fall Time			120	ns
$t_{SU;STO}$	Set-up time for STOP condition				µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs
C_b	Capacitive load for each bus line			400	pF

6.7 TDM Port Timing Requirements

T_A = 25 °C, VDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

		MIN	NOM	MAX	UNIT
t_H(SBCLK)	SBCLK high period	20			ns
t_L(SBCLK)	SBCLK low period	20			ns
t_{SU}(FSYNC)	FSYNC setup time	8			ns

TDM Port Timing Requirements (continued)

T_A = 25 °C, VDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{HLD}(FSYNC)	FSYNC hold time		8			ns
t_{SU}(FSYNC)	SDIN setup time		8			ns
t_{HLD}(SDIN)	SDIN hold time		8			ns
t_d(DO-SBCLK)	SBCLK to SDOUT delay	50% of FSYNC to 50% of SDOUT			21	ns
t_r(SBCLK)	SBCLK rise time	10% - 90 % Rise Time			8	ns
t_f(SBCLK)	SBCLK fall time	90% - 10 % Fall Time			8	ns

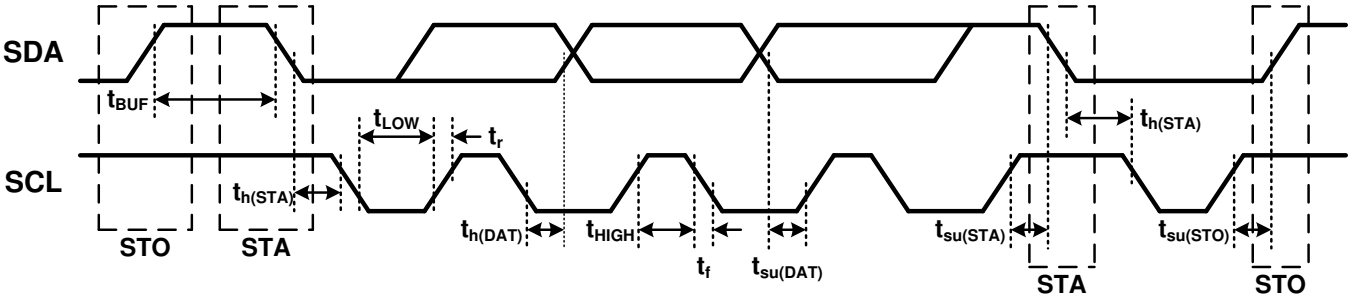

Figure 1. I²C Timing Diagram

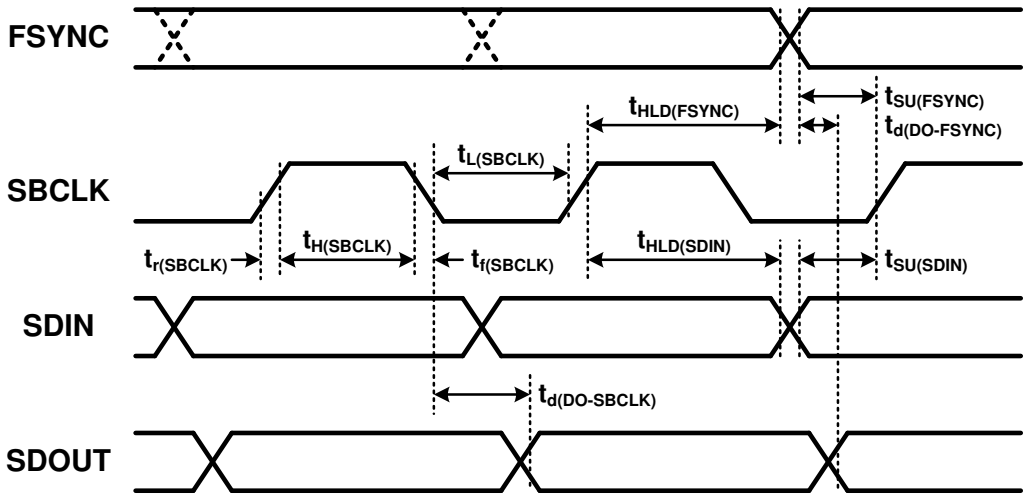

Figure 2. TDM Timing Diagram

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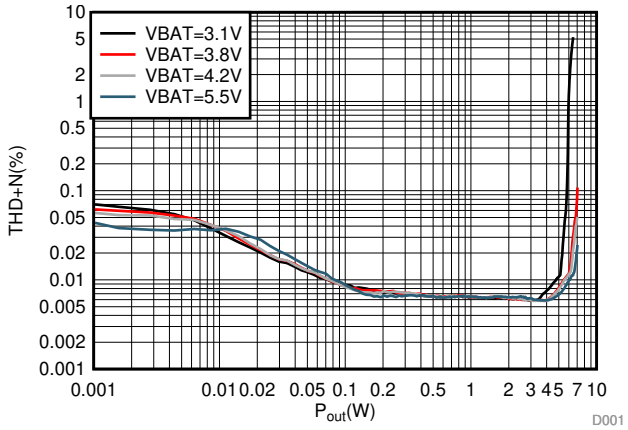
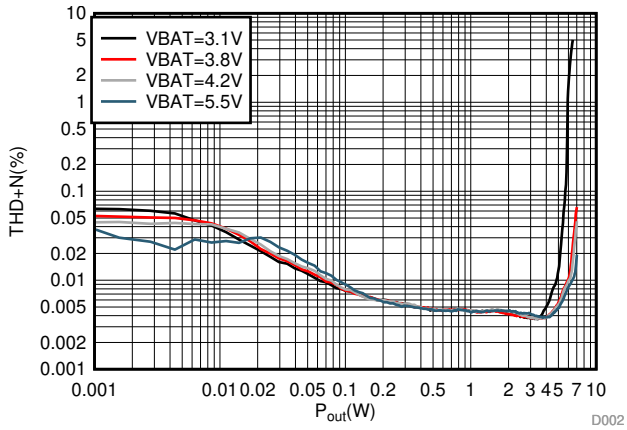
6.8 Typical Characteristics

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



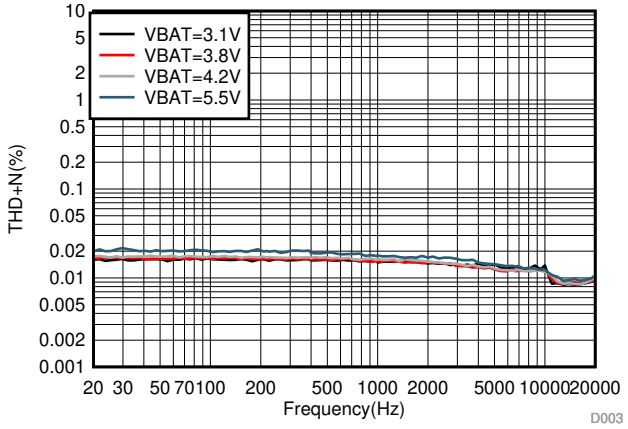
RL = 8 Ω F_{IN} = 1 kHz

Figure 3. THD+N vs Output Power



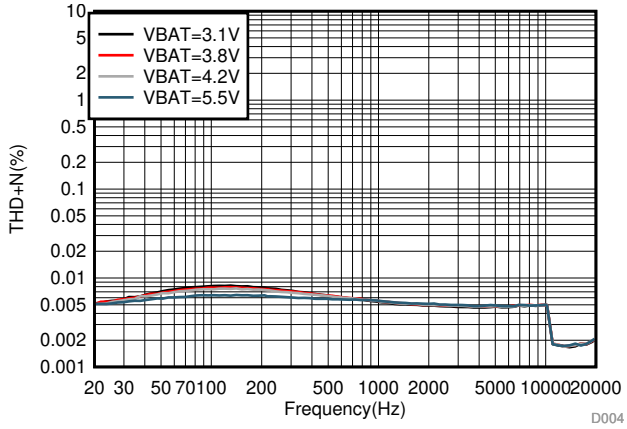
RL = 8 Ω F_{IN} = 6.667 kHz

Figure 4. THD+N vs Output Power



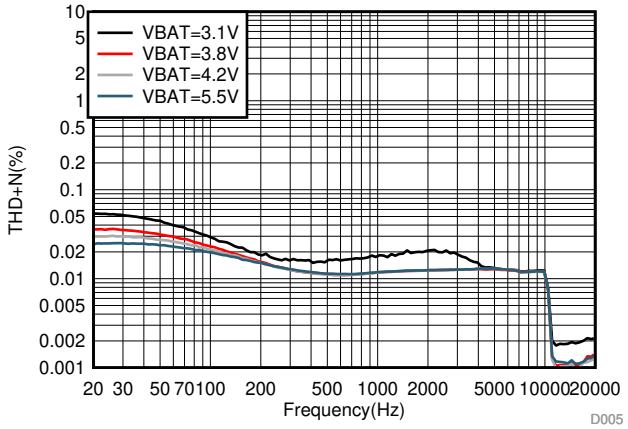
F_{IN} = 20 Hz – 20 kHz P_{OUT} = 0.1 W RL = 8 Ω

Figure 5. THD+N vs Frequency



F_{IN} = 20 Hz – 20 kHz P_{OUT} = 1 W RL = 8 Ω

Figure 6. THD+N vs Frequency



F_{IN} = 20 Hz – 20 kHz P_{OUT} = 5 W RL = 8 Ω + 30 µH

Figure 7. THD+N vs Frequency

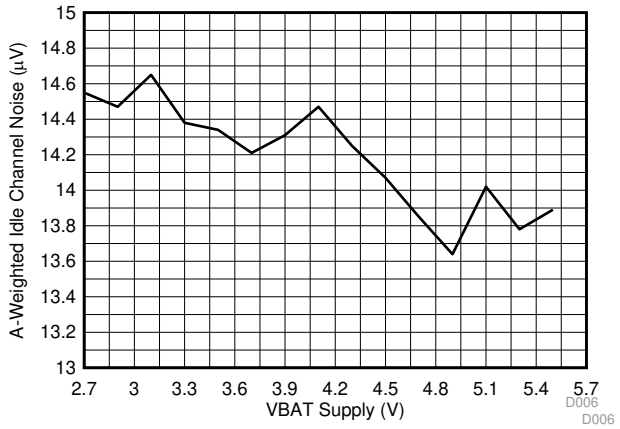


Figure 8. Idle Channel Noise (A-Weighted) vs VBAT

Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.

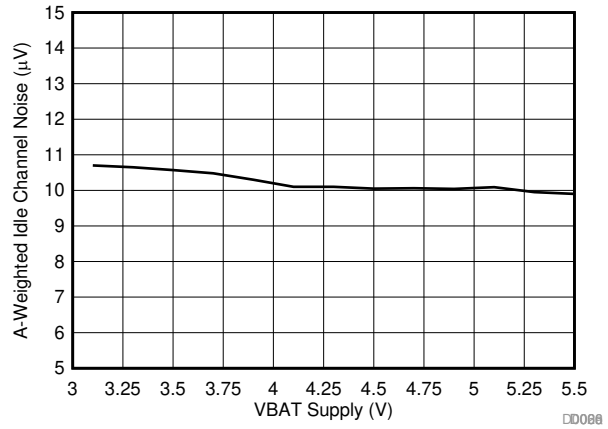
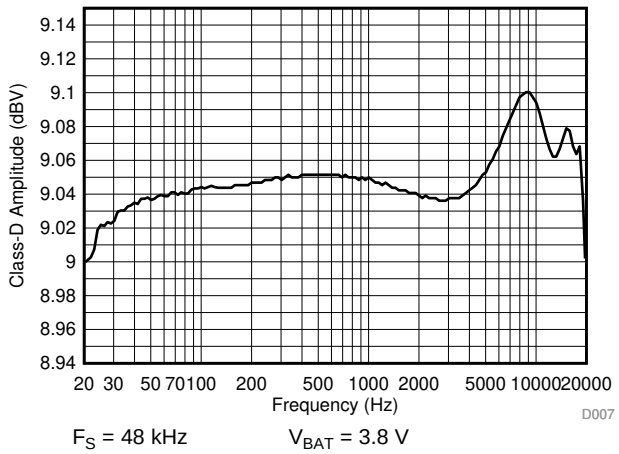
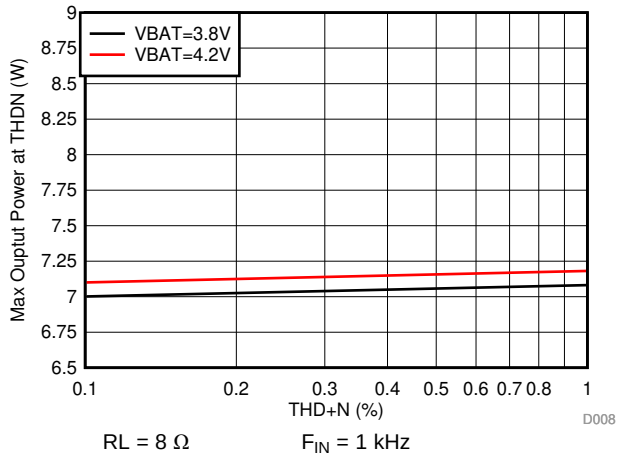


Figure 9. Receiver Idle Channel Noise (A-Weighted) vs VBAT



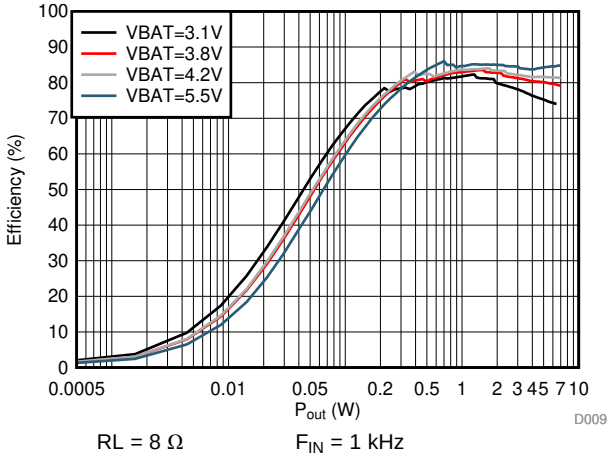
F_S = 48 kHz V_{BAT} = 3.8 V

Figure 10. Amplitude vs Frequency



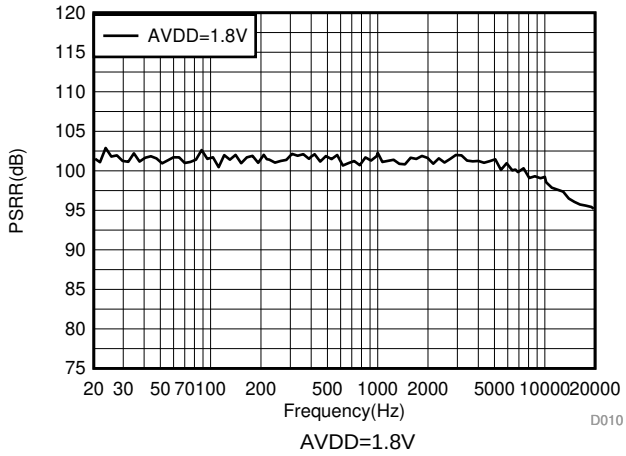
RL = 8 Ω F_{IN} = 1 kHz

Figure 11. Max Output Power vs THD+N



RL = 8 Ω F_{IN} = 1 kHz

Figure 12. Efficiency vs Output Power



AVDD=1.8V

Figure 13. AVDD PSRR vs Frequency

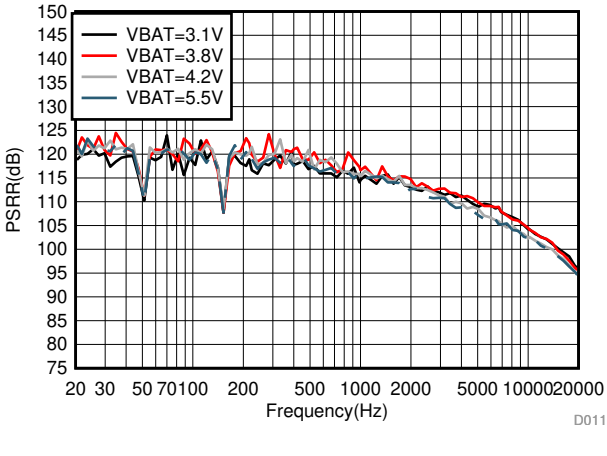


Figure 14. VBAT PSRR vs Frequency

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Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.

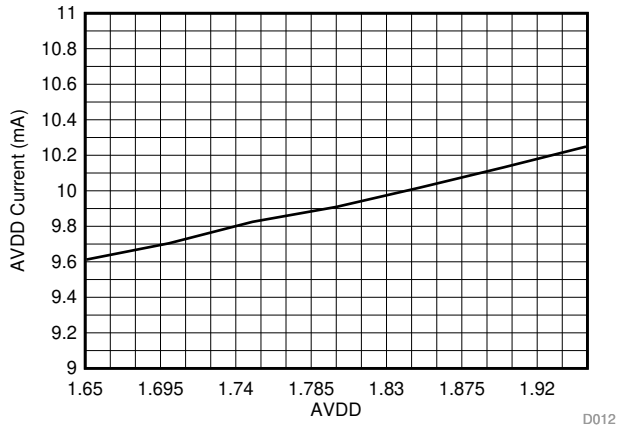


Figure 15. AVDD Idle Current vs AVDD

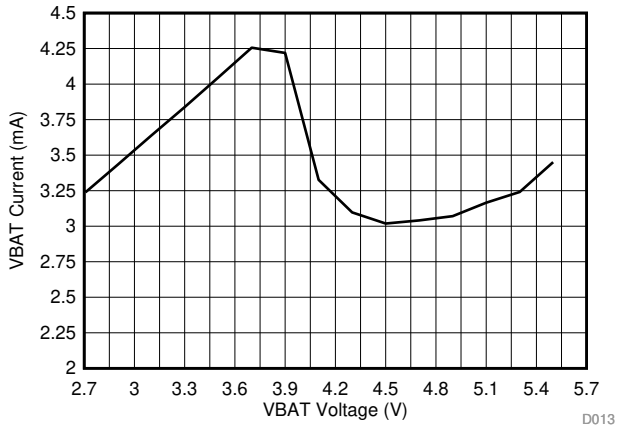
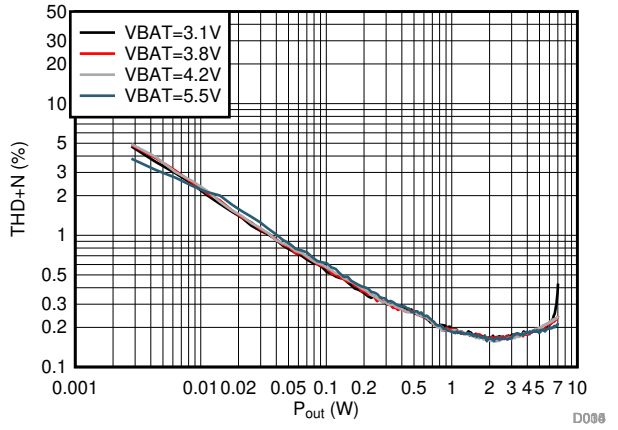
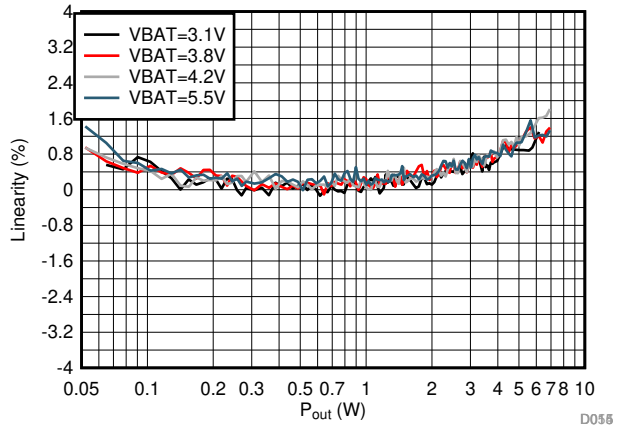


Figure 16. VBAT Idle Current vs VBAT



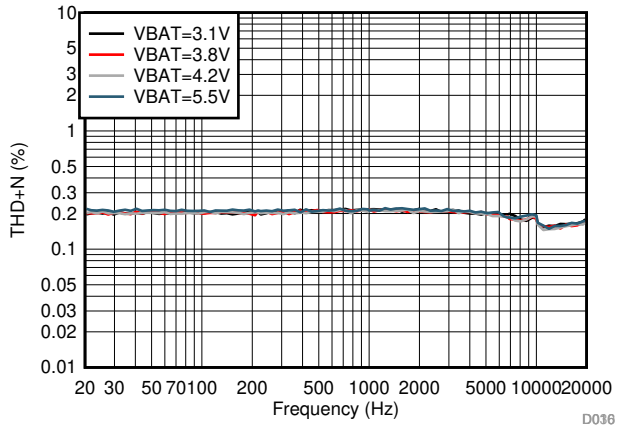
RL = 8 Ω F_{IN} = 1 kHz

Figure 17. I-sense THD+N vs Output Power



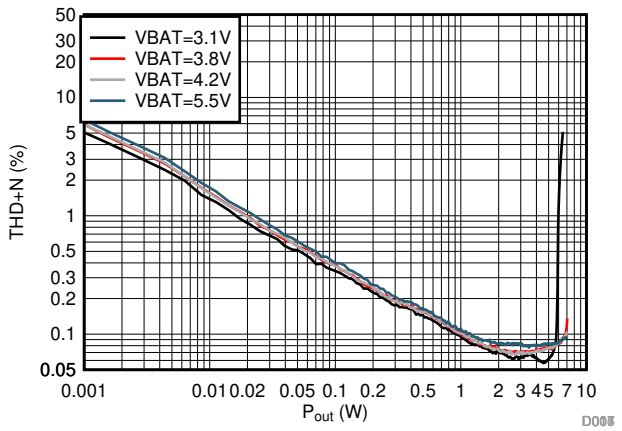
RL = 8 Ω F_{IN} = 1 kHz

Figure 18. I-sense Linearity vs Output Power



RL = 8 Ω F_{IN} = 1 kHz

Figure 19. I-sense THD+N vs Frequency

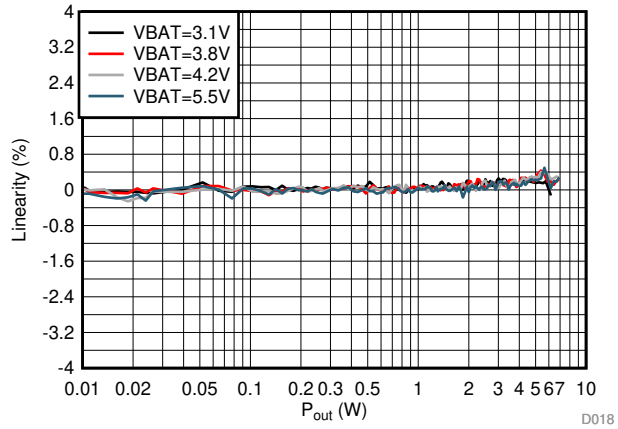


RL = 8 Ω F_{IN} = 1 kHz

Figure 20. V-sense THD+N vs Output Power

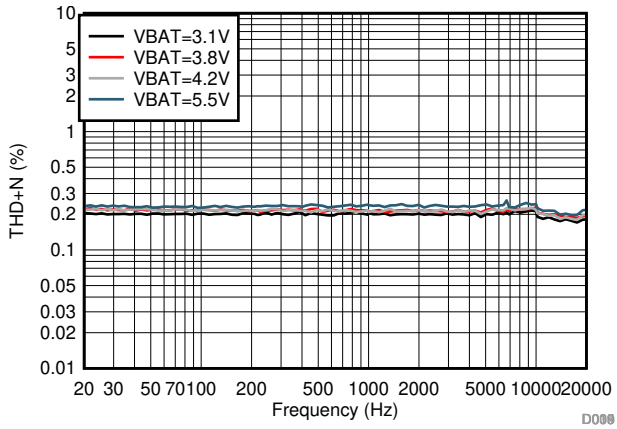
Typical Characteristics (continued)

At T_A = 25°C, f_{SPK_AMP} = 384 kHz, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 µH, unless otherwise noted.



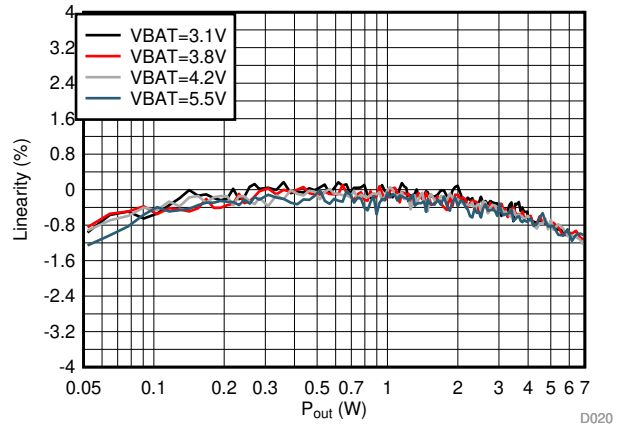
RL = 8 Ω F_{IN} = 1 kHz

Figure 21. V-sense Linearity vs Output Power



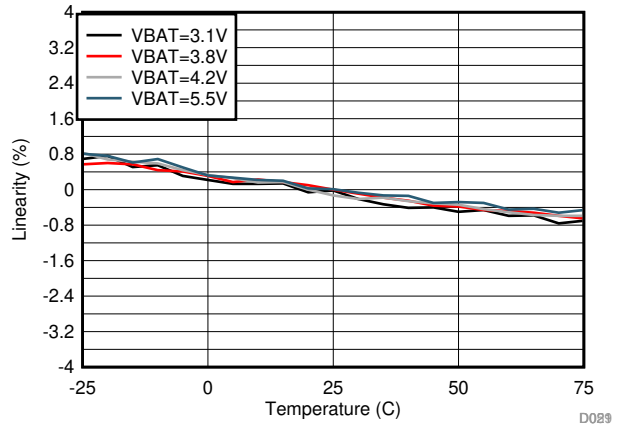
RL = 8 Ω F_{IN} = 1 kHz

Figure 22. V-sense THD+N vs Frequency



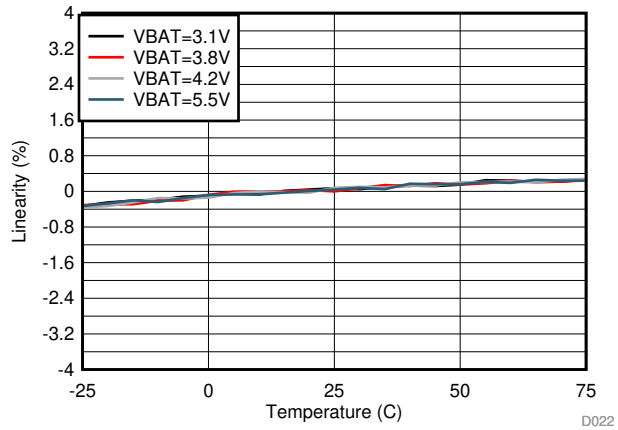
RL = 8 Ω F_{IN} = 1 kHz

Figure 23. V/I-sense Linearity vs Output Power



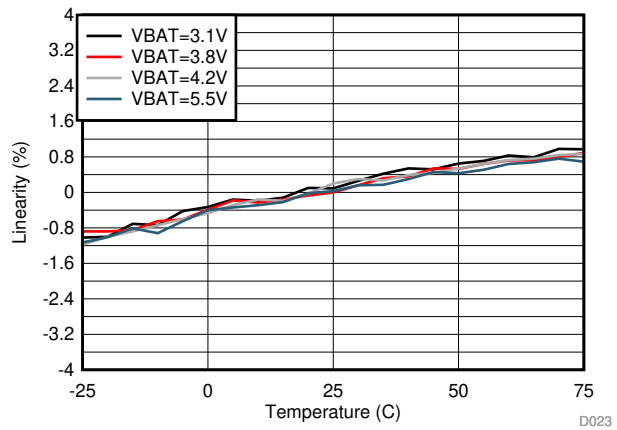
RL = 8Ω P = 1W

Figure 24. I-sense Linearity vs Temperature



RL = 8 Ω F_{IN} = 1 kHz

Figure 25. V-sense Linearity vs Temperature



RL = 8 Ω F_{IN} = 1 kHz

Figure 26. V/I-sense Linearity vs Temperature

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7 Parameter Measurement Information

All typical characteristics for the devices are measured using the Bench EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface is used to allow the I^2S interface to be driven directly into the SYS-2722. Speaker output terminals are connected to the Audio-Precision analyzer analog inputs through a differential-to-single ended (D2S) filter as shown below. The D2S filter contains a 1st order Passive pole at 120 kHz. The D2S filter ensures the TAS2564 high performance class-D amplifier sees a fully differential matched loading at its outputs. This prevents measurement errors due to loading effects of AUX-0025 filter on the class-D outputs.

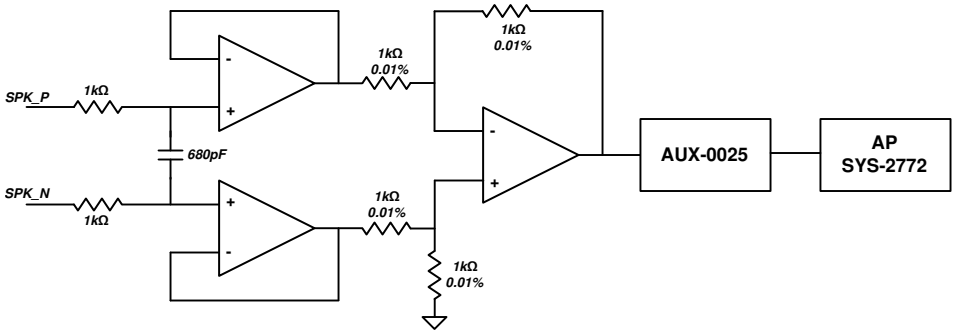


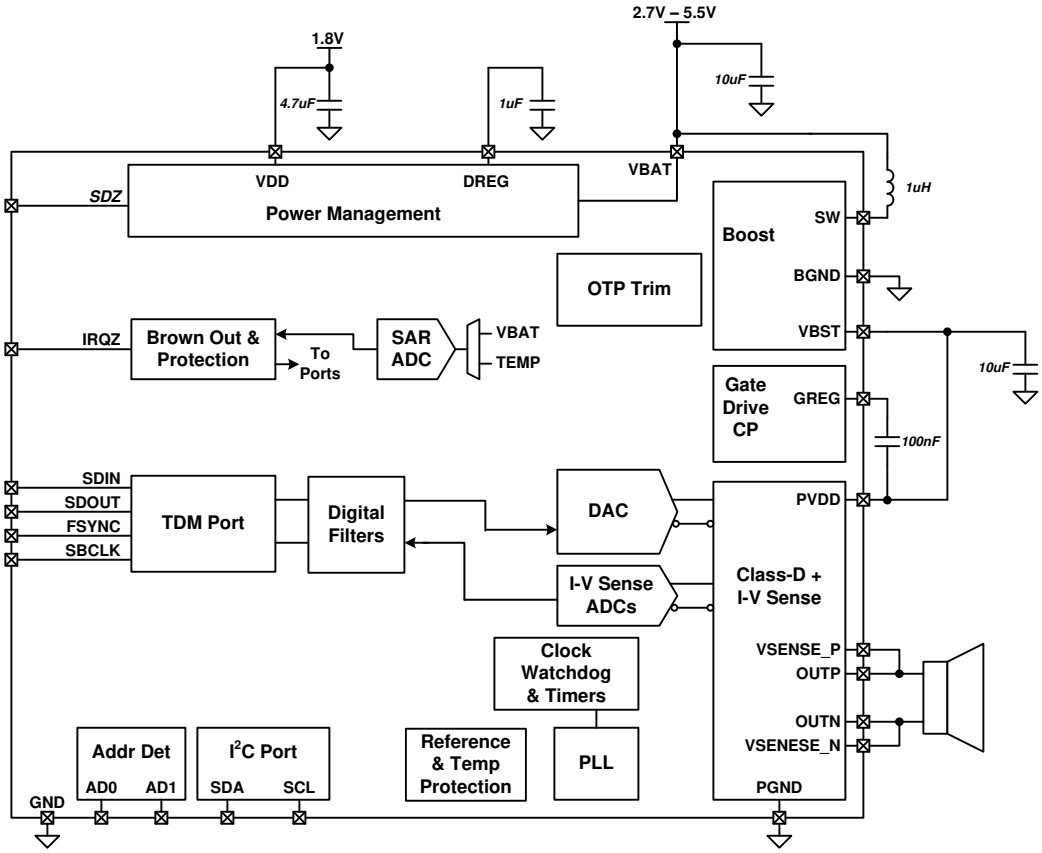
Figure 27. Differential To Single Ended (D2S) Filter

8 Detailed Description

8.1 Overview

The TAS2564 is a mono digital input Class-D amplifier optimized for mobile applications where efficient battery operation and small solution size are crucial. It integrates speaker voltage and current sensing and battery tracking limiting with brown out prevention.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PurePath™ Console 3 Software

The TAS2564 advanced features and device configuration should be performed using PurePath Console 3 (PPC3) software. The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2564 application can be download from with-in PPC3. The PCC3 tool will calculate necessary register coefficients that are described in the following sections. It is the recommended method to configure the device. Once the TAS2564 application calculates and updates the device, the registers values can be read back using the PPC3 tool for final system integration.

8.3.2 Device Mode and Address Selection

The TAS2564 can operate using one of four selectable device addresses. In TDM/I^{2}S Mode, audio input and output are provided via the FSYNC, SBCLK, SDIN and SDOUT pins using formats including I^{2}S, Left Justified and TDM. Configuration and status are provided via the SDA and SCL pins using the I^{2}C protocol. Table 1 below illustrates how to select the device I^{2}C address. I^{2}C slave addresses are shown as 7-bit address format.

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Table 1. I²C Mode Address Selection

I²C SLAVE ADDRESS	AD1 PIN	AD0 PIN
0x48 (global address)	NA	NA
0x4C	GND	GND
0x4D	GND	VDD
0x4E	VDD	GND
0x4F	VDD	VDD

The TAS2564 has a global 7-bit I²C address 0x48. When enabled the device will additionally respond to I²C commands at this address regardless of the AD1 and AD0 pin settings. This is used to speed up device configuration when using multiple TAS2564 devices and programming similar settings across all devices. The I²C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I²C command. The I²C CRC function should be used to ensure each device properly received the I²C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register should be checked on each device using the local address for a proper value. The global I²C address can be disabled using *I2C_GBL_EN* register. The I²C address is detected by sampling the address pins when SDZ pin is released. Additionally, the address may be re-detected by setting *I2C_AD_DET* high after power up and the pins will be resampled.

Table 2. I²C Global Address Enable

I2C_GBL_EN	SETTING
0	Disabled
1	Enabled (default)

Table 3. I²C Global Address Enable

I2C_AD_DET	SETTING
0	normal (default)
1	Re-detect

8.3.3 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. shows a typical sequence.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 2 kΩ and 4.7 kΩ. Do not allow the SDA and SCL voltages to exceed the device supply voltage, VDD. The I²C pins are fault tolerant and will not load the I²C bus when the device is powered down.

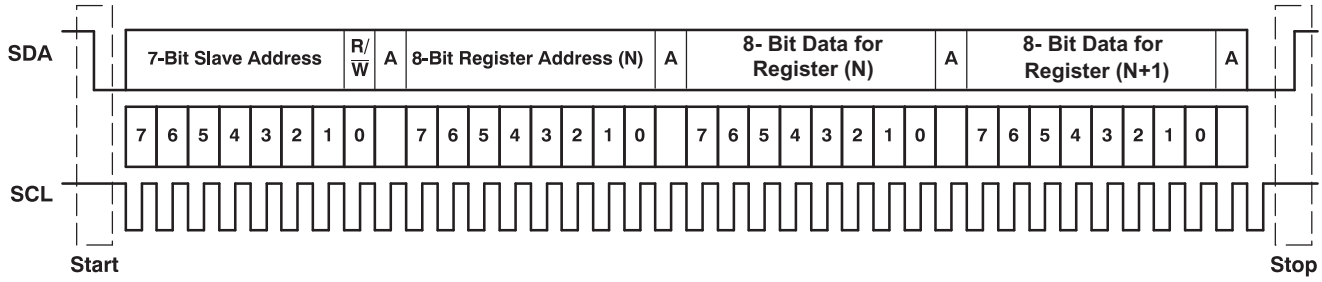

Figure 28. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. Figure 28 shows a generic data transfer sequence.

8.3.4 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2564 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2564 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

8.3.5 Single-Byte Write

As shown in Figure 29, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TAS2564 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

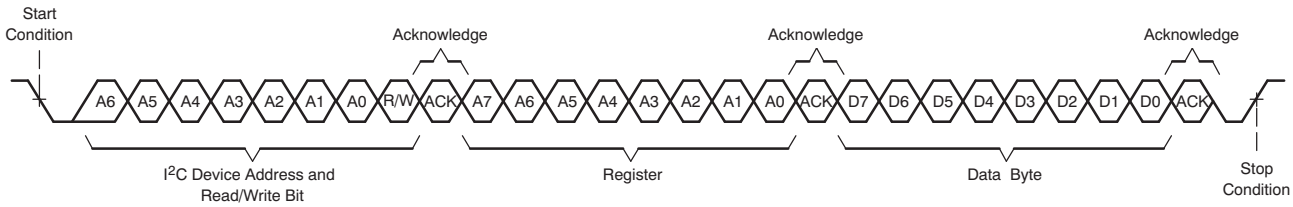

Figure 29. Single-Byte Write Transfer

8.3.6 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2564 as shown in Figure 30. After receiving each data byte, the device responds with an acknowledge bit.

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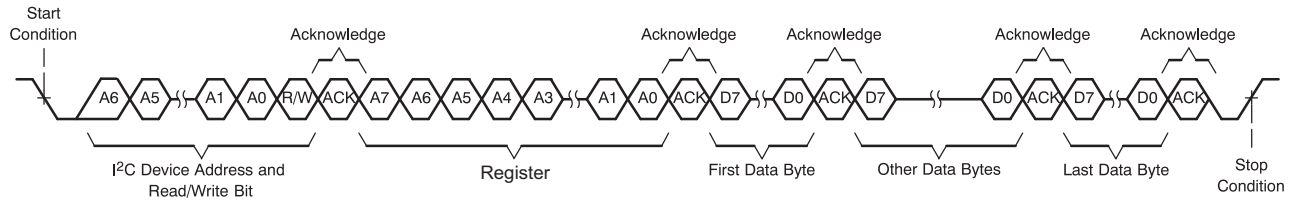

Figure 30. Multi-Byte Write Transfer

8.3.7 Single-Byte Read

As shown in Figure 31, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2564 address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the TAS2564 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2564 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

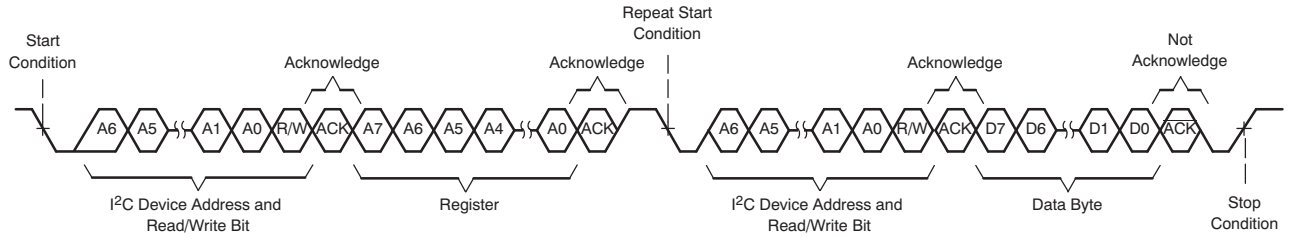

Figure 31. Single-Byte Read Transfer

8.3.8 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2564 to the master device as shown in Figure 32. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

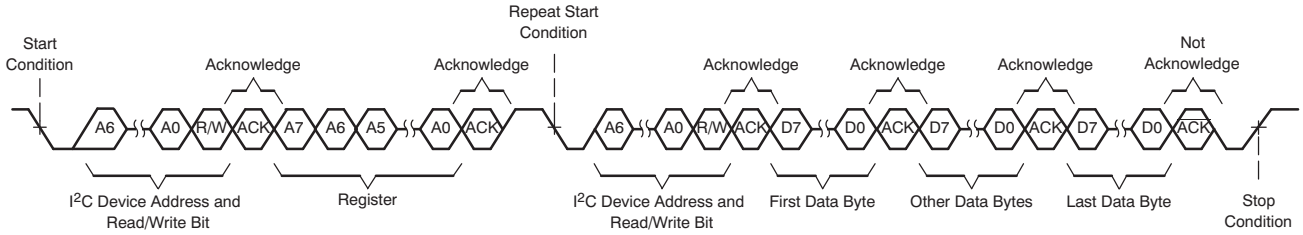

Figure 32. Multi-Byte Read Transfer

8.3.9 Register Organization

Device configuration and coefficients are stored using a page and book scheme. Each page contains 128 bytes and each book contains 256 pages. All device configuration registers are stored in book 0, page 0, which is the default setting at power up (and after a software reset). The book and page can be set by the *BOOK[7:0]* and *PAGE*[7:0] registers respectively.

8.3.10 Operational Modes

8.3.10.1 Hardware Shutdown

The device enters Hardware Shutdown mode if the SDZ pin is asserted low. In Hardware Shutdown mode, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers loose state in this mode and I^2C communication is disabled.

In normal shutdown mode if SDZ is asserted low while audio is playing, the device will ramp down volume on the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into Hardware Shutdown mode. If configured in normal with timeout shutdown mode the device will force a hard shutdown after a timeout of the configurable shutdown timer. Finally the device can be configured for hard shutdown and will not attempt to gracefully stop the audio channel.

Table 4. Shutdown Control

SDZ_MODE[1:0]	SETTING
00	Normal Shutdown with Timer (default)
01	Immediate Shutdown
10	Normal Shutdown
11	Reserved

Table 5. Shutdown Control

SDZ_TIMEOUT[1:0]	SETTING
00	2 ms
01	4 ms
10	6 ms (default)
11	23.8 ms

When SDZ is released, the device will sample the AD0 and AD1 pins and enter the software shutdown mode.

8.3.10.2 Software Shutdown

Software Shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to loose register state. Software Shutdown is enabled by asserting the *MODE[1:0]* register bits to 2'b10. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When deasserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

8.3.10.3 Mute

The TAS2564 will volume ramp down the Class-D amplifier to a mute state by setting the *MODE[1:0]* register bits to 2'b01. During mute the Class-D still switches, but transmits no audio content. If mute is deasserted, the device will volume ramp back to the programmed digital volume setting.

8.3.10.4 Active

In Active Mode the Class-D switches and plays back audio. Speaker voltage and current sensing are operational if enabled. Set the *MODE[1:0]* register bits to 2'b00 to enter active mode.

8.3.10.5 Perform Load Diagnostics

In Load Diagnostics Mode, chip runs diagnostics on load. Speaker voltage and current sensing are operational. Set the *MODE[1:0]* register bits to 2'b11 to enter this mode.

8.3.10.6 Mode Control and Software Reset

The TAS2564 mode can be configured by writing the *MODE[1:0]* bits.

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Table 6. Mode Control

MODE[1:0]	SETTING
00	Active
01	Mute
10	Software Shutdown (default)
11	

A software reset can be accomplished by asserting the *SW_RESET* bit, which is self clearing. This will restore all registers to their default values.

Table 7. Software Reset

SW_RESET	SETTING
0	Don't reset (default)
1	Reset

8.3.11 Faults and Status

During the power-up sequence, the power-on-reset circuit (POR) monitoring the VDD and VBAT pins will hold the device in reset (including all configuration registers) until the supply is valid. The device will not exit hardware shutdown until VDD and VBAT are valid and the SDZ pin is released. Once SDZ is released, the digital core voltage regulator will power up, enabling detection of the operational mode. If VDD dips below the POR threshold, the device will immediately be forced into a reset state.

The device also monitors the VBAT supply and holds the analog core in power down if the supply is below the UVLO threshold. If the TAS2564 is in active operation and a UVLO fault occurs, the analog supplies will immediately power down to protect the device. These faults are latching and require a transition through HW/SW shutdown to clear the fault. The live and latched registers will report UVLO faults.

The device transitions into software shutdown mode if it detects any faults with the TDM clocks such as:

- Invalid SBCLK to FSYNC ratio
- Invalid FSYNC frequency
- Halting of SBCLK or FSYNC clocks

Upon detection of a TDM clock error, the device transitions into software shutdown mode as quickly as possible to limit the possibility of audio artifacts. Once all TDM clock errors are resolved, the device volume ramps back to its previous playback state. During a TDM clock error, the IRQZ pin will assert low if the clock error interrupt mask register bit is set low (*INT_MASK[2]*). The clock fault is also available for readback in the live or latched fault status registers (*INT_LIVE[2]* and *INT_LTCH[2]*). Reading the latched fault status register (*INT_LTCH[7:0]*) clears the register.

The TAS2564 also monitors die temperature and Class-D load current and will enter software shutdown mode if either of these exceed safe values. As with the TDM clock error, the IRQZ pin will assert low for these faults if the appropriate fault interrupt mask register bit is set low (*INT_MASK[0]* for over temp and *INT_MASK[1]* for over current). The fault status can also be monitored in the live and latched fault registers as with the TDM clock error.

Die over temp and Class-D over current errors can either be latching (for example the device will enter software shutdown until a HW/SW shutdown sequence is applied) or they can be configured to automatically retry after a prescribed time. This behavior can be configured in the *OTE_RETRY* and OCE_RETRY register bits (for over temp and over current respectively). Even in latched mode, the Class-D will not attempt to retry after an over temp or over current error until the retry time period (1.5 s) has elapsed. This prevents applying repeated stress to the device in a rapid fashion that could lead to device damage. If the device has been cycled through SW/HW shutdown, the device will only begin to operate after the retry time period.

The status registers (and IRQZ pin if enabled via the status mask register) also indicates limiter behavior including when the limiter is activity, when VBAT is below the inflection point, when maximum attenuation has been applied, when the limiter is in infinite hold and when the limiter has muted the audio.

Interrupts can be queried using the *INT_LIVE[9:0]* and *INT_LTCH[13:0]* registers and correspond to the *INT_MASK[10:0]* Interrupts. The latched registers are cleared by writing the self clearing register *INT_CLR_LTCH* high.

The IRQZ pin is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDDVDD. An internal pull up resistor is provided in the TAS2564 and can be accessed by setting the *IRQZ_PU* register bit high. Figure 33 below highlights the IRQZ pin circuit.

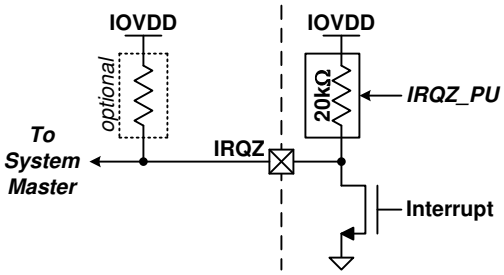

Figure 33. IRQZ Pin

Table 8. Fault Interrupt Mask

INT_MASK[10:0] BIT	INTERRUPT	DEFAULT (1 = Mask)
0	Over Temp Error	0
1	Over Current Error	0
2	TDM Clock Error	1
3	Limiter Active	1
4	Limter Voltage < Inf Point	1
5	Limiter Max Atten	1
6	Limiter Inf Hold	1
7	Limiter Mute	1
8	Brown Out on VBAT Supply	0
9	Brown Out Protection Active	1
10	Brown Out Power Down (Latched Only)	1
11:12	Speaker Open Load (Latched Only)	00
13	Load Diagnostic Complete (Latched Only)	1

Table 9. IRQ Clear Latched

INT_CLR_LTCH	STATE
0	Don't Clear
1	Clear (self clearing)

Table 10. IRQZ Internal Pull Up Enable

IRQZ_PU	STATE
0	Disabled (default)
1	Enabled

Table 11. IRQZ Polarity

IRQZ_POL	STATE
0	Active High
1	Active Low (default)

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Table 12. IRQZ Assert Interrupt Configuration

IRQZ_PIN_CFG[1:0]	VALUE
00	On any unmasked live interrupts
01	On any unmasked latched interrupts (default)
10	For 2-4 ms one time on any unmasked live interrupt event
11	For 2-4 ms every 4 ms on any unmasked latched interrupts

Table 13. Retry after Over Current Event

OCE_RETRY	STATE
0	Disabled (default)
1	Enabled

Table 14. Retry after Over Temperature Event

OTE_RETRY	VALUE
0	Do not retry (default)
1	Retry after 1.5 s

8.3.12 Power Sequencing Requirements

There are no other power sequencing requirements for order of rate of ramping up or down.

8.3.13 Digital Input Pull Downs

Each digital input and IO has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown.

8.4 Device Functional Modes

8.4.1 TDM Port

The TAS2564 provides a flexible TDM serial audio port. The port can be configured to support a variety of formats including stereo I^2S, Left Justified and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including speaker voltage and current sense, VBAT voltage, die temperature and channel gain.

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48 kHz, 8 32-bit time slots at a 88.2/96 kHz sample rate and 4 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. Valid SBCLK to FSYNC ratios are 64, 96, 128, 192, 256, 384 and 512. The device will automatically detect the number of time slots and this does not need to be programmed.

By default, the TAS2564 will automatically detect the PCM playback sample rate. This can be disabled by setting the *AUTO_RATE* register bit high and manually configuring the device.

The *SAMP_RATE* register bits set the PCM audio sample rate when *AUTO_RATE* is enabled. The TAS2564 employs a robust clock fault detection engine that will automatically volume ramp down the playback path if FSYNC does not match the configured sample rate (*AUTO_RATE* enabled) or the ratio of SBCLK to FSYNC is not supported (minimizing any audible artifacts). Once the clocks are detected to be valid in both frequency and ratio, the device will automatically volume ramp the playback path back to the configured volume and resume playback.

When using the auto rate detection the sampling rate and SBCLK to FSYNC ration detected on the TDM bus is reported back on the read-only register *FS_RATE* and *FS_RATIO* respectively.

Device Functional Modes (continued)

While the sampling rate of 192 kHz is supported, it is internally down-sampled to 96 kHz. Therefore audio content greater than 40 kHz should not be applied to prevent aliasing. This additionally effects all processing blocks like BOP and limiter which should use 96 kHz fs when accepting 192 kHz audio. It is recommend to use PurePath™ Console 3 Software to configure the device.

Table 15. PCM Auto Sample Rate Detection

AUTO_RATE	SETTING
0	Enabled (default)
1	Disabled

Table 16. PCM Audio Sample Rates

SAMP_RATE[2:0]	*FS_RATE*(read only)	SAMPLE RATE
000	000	
001	001	14.7kHz / 16kHz
010	010	22.05 kHz / 24 kHz
011	011	29.4 kHz / 32 kHz
100	100	44.1 kHz / 48 kHz (default)
101	101	88.2 kHz / 96 kHz
110	110	176.4 kHz / 192 kHz
111	111	Reserved

Table 17. PCM SBCLK to FSYNC Ratio Rates

FS_RATIO[3:0]	SAMPLE RATE
0x0-0x3	Reserved
0x4	64
0x5	96
0x6	128
0x7	192
0x8	256
0x9	384
0xA	512
0xB-0xE	Reserved
0xF	Error Condition

Figure 34 and Figure 35 below illustrates the receiver frame parameters required to configure the port for playback. A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge (set by the *RX_EDGE* register bit). The *RX_OFFSET* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I^2S format.

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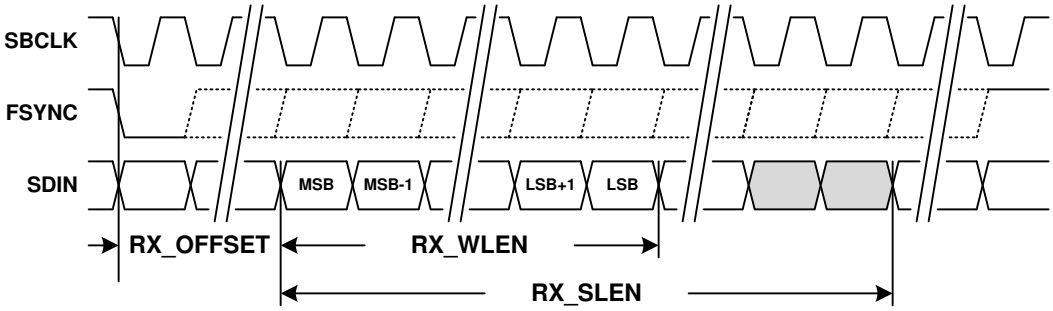

Figure 34. TDM RX Time Slot with Left Justification

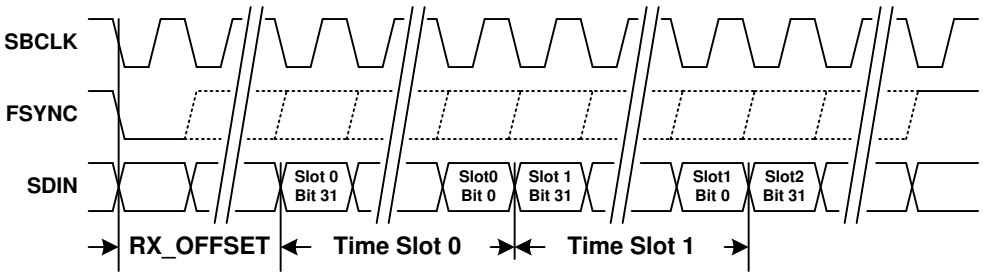

Figure 35. TDM RX Time Slots

Table 18. TDM Start of Frame Polarity

FRAME_START	POLARITY
0	Low to High on FSYNC (1)
1	High to Low on FSYNC (default) (2)

(1) When Low to High is used RX_EDGE and TX_EDGE cannot both simultaneously be set to rising edge.
(2) When High to Low is used RX_EDGE and TX_EDGE cannot both simultaneously be set to falling edge.

Table 19. TDM RX Capture Polarity

RX_EDGE	FSYNC AND SDIN CAPTURE EDGE
0	Rising edge of SBCLK (default)
1	Falling edge of SBCLK

Table 20. TDM RX Start of Frame to Time Slot 0 Offset

RX_OFFSET[4:0]	SBCLK CYCLES
0x00	0
0x01	1 (default)
0x02	2
...	...
0x1E	30
0x1F	31

The *RX_SLEN[1:0]* register bits set the length of the RX time slot. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit. The TAS2564 supports mono and stereo down mix playback ([L+R]/2) via the left time slot, right time slot and time slot configuration register bits (*RX_SLOT_L[3:0]*, *RX_SLOT_R[3:0]* and *RX_SCFG[1:0]* respectively). By default the device will playback mono from the time slot equal to the I^2C base address offset for playback. The *RX_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_L[3:0]* and *RX_SLOT_R[3:0]* register bits.

If time slot selections places reception either partially or fully beyond the frame boundary, the receiver will return a null sample equivalent to a digitally muted sample.

Table 21. TDM RX Time Slot Length

RX_SLEN[1:0]	TIME SLOT LENGTH
00	16-bits
01	24-bits
10	32-bits (default)
11	reserved

Table 22. TDM RX Sample Word Length

RX_WLEN[1:0]	LENGTH
00	16-bits
01	20-bits
10	24-bits (default)
11	32-bits

Table 23. TDM RX Sample Justification

RX_JUSTIFY	JUSTIFICATION
0	Left (default)
1	Right

Table 24. TDM RX Time Slot Select Configuration

RX_SCFG[1:0]	CONFIG ORIGIN
00	Mono with Time Slot equal to I^2C Address Offset (default)
01	Mono Left Channel
10	Mono Right Channel
10	Stereo Down Mix [L+R]/2

Table 25. TDM RX Left Channel Time Slot

RX_SLOT_L[3:0]	TIME SLOT
0x0	0 (default)
0x1	1
...	...
0xE	14
0xF	15

Table 26. TDM RX Right Channel Time Slot

RX_SLOT_R[3:0]	TIME SLOT
0x0	0
0x1	1 (default)

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Table 26. TDM RX Right Channel Time Slot (continued)

RX_SLOT_R[3:0]	TIME SLOT
. . .	...
0xE	14
0xF	15

The TDM port can transmit a number sample streams on the SDOUT pin includingboth speaker voltage sense, speaker current sense, VBAT voltage, die temperature and channel gain. Figure 36 below illustrates the alignment of time slots to the beginning of a frame and how a given sample stream is mapped to time slots. Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin, which can be configured by setting the *TX_EDGE* register bit. The *TX_OFFSET* register defines the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This would typically be programmed to 0 for Left Justified format and 1 for I^2S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit setting. An optional bus keeper will weakly hold the state of SDOUT when all devices driving are Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX_KEEPEN* register bit. The bus-keeper can additionally be configured to be enabled for only 1LSB cycle or always using *TX_KEEPLN* and to drive the full or half cycle of the LSB using *TX_KEEPCY*.

Each sample stream is composed of either one or two 8-bit time slots. Speaker voltage sense and speaker current sense sample streams are 16-bit precision, so they will always utilize two TX time slots. The VBAT voltage stream is 10-bit precision, and can either be transmitted left justified in a 16-bit word (using two time slots) or can be truncated to 8-bits (the top 8 MSBs) and be transmitted in a single time slot. This is configured by setting *VBAT_SLEN* register bit. The Die temperature and gain are both 8-bit precision and are transmitted in a single time slot.

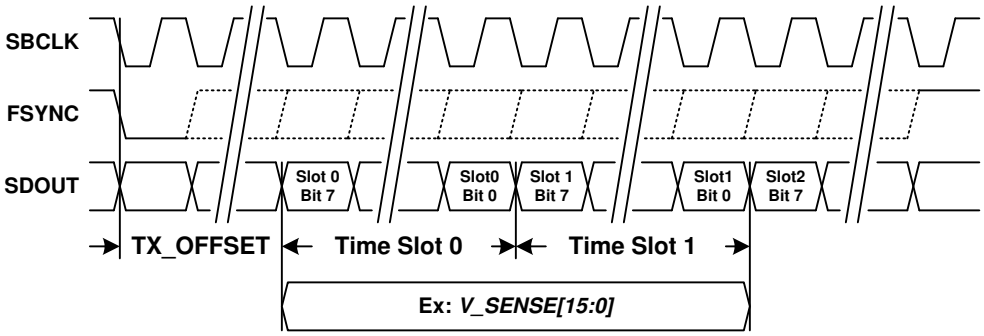

Figure 36. TDM Port TX Diagram

Table 27. TDM TX Transmit Polarity

TX_EDGE	SDOUT TRANSMIT EDGE
0	Rising edge of SBCLK
1	Falling edge of SBCLK (default)

Table 28. TDM TX Start of Frame to Time Slot 0 Offset

TX_OFFSET[2:0]	SBCLK CYCLES
0x0	0
0x1	1 (default)
0x2	2
. . .	...
0x6	6
0x7	7

Table 29. TDM TX Unused Bit Field Fill

TX_FILL	SDOUT UNUSED BIT FIELDS
0	Transmit 0
1	Transmit Hi-Z (default)

Table 30. TDM TX SDOUT Bus Keeper Enable

TX_KEEPEN	SDOUT BUS KEEPER
0	Disable bus keeper
1	Enable bus keeper (default)

Table 31. TDM TX SDOUT Bus Keeper Length

TX_KEEPLN	SDOUT BUS KEEPER ENABLED FOR
0	1 LSB cycle (default)
1	Always

Table 32. TDM TX SDOUT Bus Keeper LSB Cycle

TX_KEEPCY	SDOUT BUS KEEPER DRIVEN
0	full-cycle (default)
1	half-cycle

The time slot register for each sample stream defines where the MSB transmission begins. For instance, if *VSNS_SLOT* is set to 2, the upper 8 MSBs will be transmitted in time slot 2 and the lower 8 LSBs will be transmitted in time slot 3. Each sample stream can be individually enabled or disabled. This is useful to manage limited TDM bandwidth since it may not be necessary to transmit all streams for all devices on the bus.

It is important to ensure that time slot assignments for actively transmitted sample streams do not conflict. For instance, if *VSNS_SLOT* is set to 2 and *ISNS_SLOT* is set to 3, the lower 8 LSBs of voltage sense will conflict with the upper 8 MSBs of current sense. This will produce unpredictable transmission results in the conflicting bit slots (for example the priority is not defined).

The current and voltage values are transmitted at the full 16-bit measured values by default. The *IVMON_LEN* register can be used to transmit only the 8 MSB bits in one slot or 12 MSB bits values across multiple slots. The special 12-bit mode is used when only 24-bit I2S/TDM data can be processed by the host processor. The device should be configured with the voltage-sense slot and current-sense slot off by 1 slot and will consume 3 consecutive 8-bit slots. In this mode the device will transmit the first 12 MSB bits followed by the second 12 MSB bits specified by the preceding slot.

If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

It is recommended to keep the following slot ordering:

ISNS_SLOT<VSNS_SLOT<VBAT_SLOT<TEMP_SLOT<GAIN_SLOT<BIL_ILIM_SLOT.

Table 33. TDM Voltage/Current Length

IVMON_LEN[1:0]	LENGTH BITS
00	16 bits (default)
01	12 bits
10	8 bits
11	Reserved

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Table 34. TDM Voltage Sense Time Slot

VSNS_SLOT[5:0]	SLOT
0x00	0
0x01	1
0x02	2 (default)
...	...
0x3E	62
0x3F	63

Table 35. TDM Voltage Sense Transmit Enable

VSNS_TX	STATE
0	Disabled (default)
1	Enabled

Table 36. TDM Current Sense Time Slot

ISNS_SLOT[5:0]	SLOT
0x00	0 (default)
0x01	1
0x02	2
...	...
0x3E	62
0x3F	63

Table 37. TDM Current Sense Transmit Enable

ISNS_TX	STATE
0	Disabled (default)
1	Enabled

Table 38. TDM VBAT Time Slot

VBAT_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x04	4 (default)
...	...
0x3E	62
0x3F	63

Table 39. TDM VBAT Time Slot Length

VBAT_SLEN	SLOT LENGTH
0	Truncate to 8-bits (default)
1	Left justify to 16-bits

Table 40. TDM VBAT Transmit Enable

VBAT_TX	STATE
0	Disabled (default)
1	Enabled

Table 41. TDM Temp Sensor Time Slot

TEMP_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x05	5 (default)
...	...
0x3E	62
0x3F	63

Table 42. TDM Temp Sensor Transmit Enable

TEMP_TX	STATE
0	Disabled (default)
1	Enabled

The following sample streams are part of the Inter Chip Limiter Alignment system. These data streams can be routed over the audio TDM bus.

Table 43. TDM Limiter Gain Reduction Time Slot

GAIN_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x06	6 (default)
...	...
0x3E	62
0x3F	63

Table 44. TDM Limiter Gain Reduction Transmit Enable

GAIN_TX	STATE
0	Disabled (default)
1	Enabled

Table 45. TDM Boost Sync Time Slot

BST_SLOT[5:0]	SLOT
0x00	0
0x01	1
...	...
0x07	7 (default)
...	...
0x3E	62
0x3F	63

Table 46. TDM Boost Sync Enable

BST_TX	STATE
0	Disabled (default)
1	Enabled

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8.4.2 Playback Signal Path

8.4.2.1 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The TAS2564 employs a high-pass filter (HPF) to prevent this from occurring for the PCM playback path. The HPF can be disabled using register HPF_EN. The HPF Bi-Quad filter coefficients can be changed from the default 2 Hz using the *HPFC_N0*, *HPFC_N1*, *HPFC_D1* registers using the equation [N, D] = butter(1, fc/(fs/2), 'high'); round(N(0)*2^31);. These coefficients should be calculated and set using PurePath™ Console 3 Software.

Table 47. HPF Enable

HPF_EN	STATE
0	Enabled (default)
1	Disabled

8.4.2.2 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's output level and digital volume control (DVC).

Amplifier output level settings are presented in dBV (dB relative to 1 V_{rms}) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only. below shows gain settings that can be programmed via the *AMP_LEVEL* register.

Table 48. Amplifier Output Level Settings

AMP_LEVEL[4:0]	dBV	V_{PEAK} (V)
0x00	9.7	4.32
0x01	10.2	4.58
0x02	10.7	4.85
...	...	...
0x10	17.7	10.85
...	...	...
0x1B	23.2	20.44
0x1C	23.7	21.65
0x1D-0x1F	Reserved	Reserved

Equation 1 calculates the amplifiers output voltage.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \ \text{dBV} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A_{dvc} is the digital volume control setting, 0 dB to -100 dB in 0.5 dB steps
- A_{AMP} is the amplifier output level setting in dBV

Settings greater than 0xC8 are interpreted as mute. When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC_RAMP* register bits. If *DVC_RAMP* is set to 0x0000 0000, volume ramping is disabled. This can be used to speed up startup, shutdown and digital volume changes when volume ramping is handled by the system master.

The digital voltage control registers *DVC_PCM* represent the volume in a 2.X format. To calculate the value to write to these 4 registers apply the following formula to the desired dB DVC_PCM = round(10^(dB/20)*2^30).

A volume ramp rate can be set using *DVC_RAMP* and represents a rate in 1.X format. To calculate the value to write to these 4 registers apply the following formula DVC_RAMP = round((1-exp(-1/(0.2*fs*time in seconds)))*2^31).

Table 49. PCM Digital Volume Control

DVC_PCM[31:0]	VOLUME (dB)
0x0000 0D43 (MIN)	-110
...	...
0x4000 0000	0 (default)
...	...
0x5092 BEE4 (MAX)	2

Table 50. Digital Volume Ramp Rate

DVC_RAMP[31:0]	RAMP RATE @ 48kHz (s)
0x0000 0D43	0
...	
0x7FFC 963B	1 s

8.4.2.3 Auto-Mute During Idle Channel Mode

Device will stop playing audio if the input audio level drops below the programmable threshold for a programmable timer window. If this behavior is not preferred, threshold level can be kept at very low levels.

8.4.2.4 Auto-Start/Stop on Audio Clocks

The TAS2564 can enter low power software shutdown when the TDM clocks are stopped instead of going into clock error. The device will resume operation when the clocks resume.

8.4.2.5 Supply Tracking Limiters with Brown Out Prevention

The TAS2564 monitors battery voltage (VBAT) and along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiters threshold can be configured to track the monitored voltage below a programmable inflection point with a programmable slope. A minimum threshold sets the limit of threshold reduction from the voltage tracking. Configurable attack rate, hold time and release rate are provided to shape the dynamic response of each limiter. If the ICLA is enabled the actual attenuation is based on the ICLA configuration using the calculated attenuation value of all devices on the selected ICLA bus.

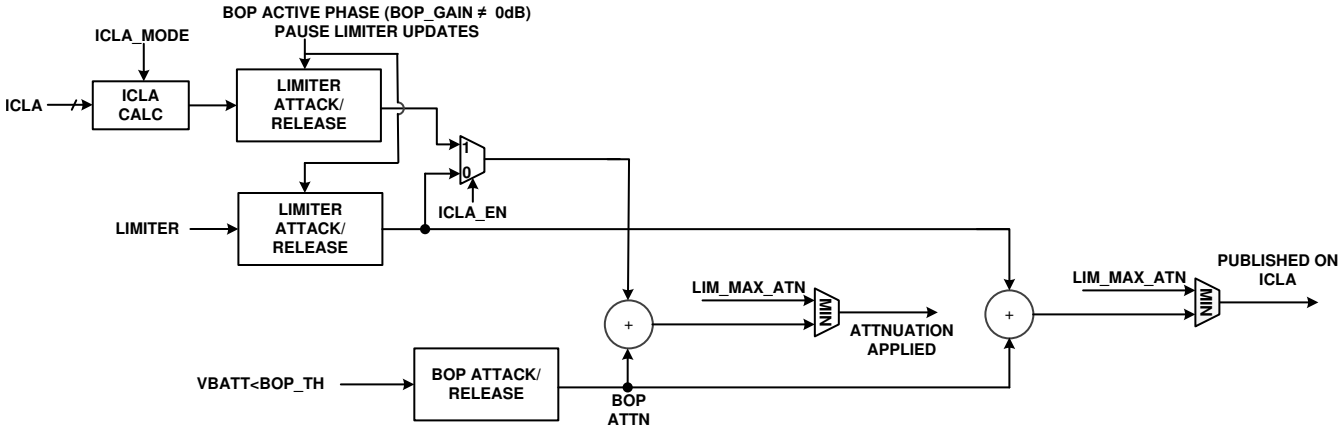

Figure 37. Limiter and Brown Out Prevention Interaction Diagram

A Brown Out Prevention (BOP) feature provides a priority input to provide a fast response to transient dips in the battery supply (VBAT) which at end of charge conditions that can cause system level brown out. When the selected supply dips below the brown-out threshold the BOP will begin reducing gain at a configurable attack rate. When the VBAT supply rises above the brownout threshold, the BOP will begin to release after the programmed hold time. During a BOP event the limiter updates will be paused. This is to prevent a limiter from releasing during a BOP event. The VBAT limiter is enabled by setting the *LIMB_EN* bit high.

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Table 51. VBAT Tracking Limiter Enable

LIMB_EN	VALUE
0	Disabled (default)
1	Enabled

The limiter has a configurable attack rate, hold time and release rate, which are available via the *LIMB_ATK_RT[2:0]*, *LIMB_HLD_TM[2:0]*, *LIMB_RLS_RT[2:0]* register bits. The limiter attack and release step sizes can be set by configuring the *LIMB_ATK_ST[1:0]* and *LIMB_RLS_ST[1:0]* register bits. The rates are based on the number of audio samples and actual time values can be calculated by multiplying by 1/fs. For example the attack rate of 4 samples at 48 ksps would be approximately 83 µs.

Table 52. Limiter Attack Rate

LIMB_ATK_RT[2:0]	ATTACK RATE (samples/step)	ATTACK RATE @ 48 ksps (~µs)
0x0	1	20
0x1	2 (default)	42
0x2	4	83
0x3	8	167
0x4	16	333
0x5	32	666
0x6	64	1300
0x7	128	2700

Table 53. Limiter Hold Time

LIMB_HLD_TM[2:0]	HOLD TIME (samples/step)	HOLD TIME @ 48ksps (ms)
0x0	0	0
0x1	1920	40
0x2	4800	100
0x3	9600	200
0x4	19200	400
0x5	48000	1000
0x6	96000 (default)	2000
0x7	192000	4000

Table 54. Limiter Release Rate

LIMB_RLS_RT[2:0]	Release Rate (samples/step)	RELEASE RATE @ 48 ksps (ms)
0x0	10	0.2
0x1	20	0.4
0x2	40	0.8
0x3	80	1.7
0x4	160	3.3
0x5	320	6.7
0x6	640 (default)	13.3
0x7	1280	26.7

Table 55. Limiter Attack Step Size

LIMB_ATK_ST[1:0]	STEP SIZE (dB)
00	0.25
01	0.5 (default)

Table 55. Limiter Attack Step Size (continued)

LIMB_ATK_ST[1:0]	STEP SIZE (dB)
10	1
11	2

Table 56. Limiter Release Step Size

LIMB_RLS_ST[1:0]	STEP SIZE (dB)
00	0.25
01	0.5 (default)
10	1
11	2

A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM_MAX_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiters have reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

The limiter max attenuation *LIM_MAX_ATN* represent the limit in a 1.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired dB using equation *LIMB_MAX_ATN* = round(10^(-dB/20)*2^31).

Table 57. Limiter Max Attenuation

LIM_MAX_ATN[31:0]	ATTENUATION (dB)
0x7214 82C0	-1
...	...
0x2D6A 866F	-9 (default)
...	...
0x1326 DD71	-16.5

The limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. Figure 38 below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM_TH_MAX*. Set the limiter inflection point using *LIM_INF_PT* below the minimum allowable supply setting. The limiter minimum threshold register *LIM_TH_MIN* does not impact limiter behavior in this use case.

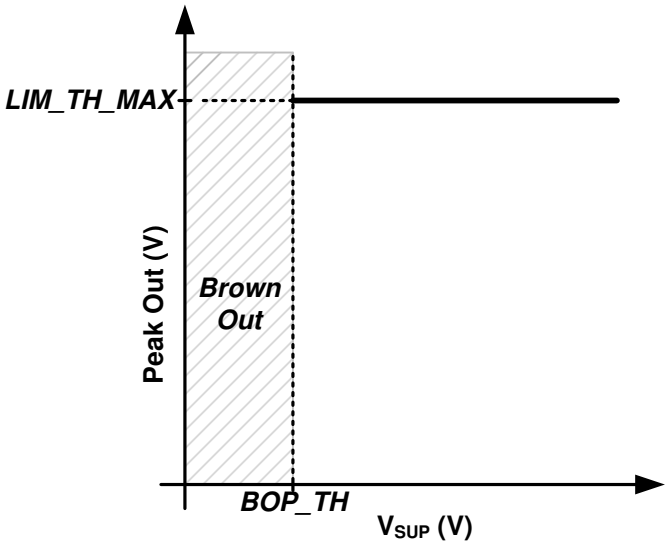

Figure 38. Limiter with Fixed Threshold

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The VBAT limiter threshold max *LIMB_TH_MAX* and min *LIMB_TH_MIN* registers represent the limit in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired threshold voltage using the equation *LIMB_TH_MAX* or *LIMB_TH_MIN* = round(Volts*2^27).

Table 58. VBAT Limiter Maximum Threshold

LIMB_TH_MAX[31:0]	THRESHOLD (V)
0x1400 0000	2.5
. . .	...
0x4800 0000	9 (default)
. . .	...
0x7C00 0000	15.5

Table 59. VBAT Limiter Minimum Threshold

LIMB_TH_MIN[31:0]	THRESHOLD (V)
0x1400 0000	2.5
. . .	...
0x2000 0000	4 (default)
. . .	...
0x7C00 0000	15.5

The VBAT limiter inflection point *LIMB_INF_PT* represent the limit in a 4.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired infection voltage using the equation *LIMB_INF_PT* = round(Volts*2^28).

Table 60. VBAT Limiter Inflection Point

LIMB_INF_PT[31:0]	THRESHOLD (V)
0x2000 0000	2
. . .	...
0x34CC CCCD	3.3 (default)
. . .	...
0x3000 0000	6

Figure 39 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM_TH_MAX* register to the desired threshold and *LIM_INF_PT* register to the desired inflection point where the limiter will begin reducing the threshold with the selected supply. The *LIMP_SLOPE[1:0] and LIMB_SLOPE[1:0]* register bits can be used to change the slope of the limiter tracking the respective PVDD and VBAT supply.The *LIMB_SLOPE[1:0]* register bits can be used to change the slope of the limiter tracking the VBAT supply. The default value of 1 V/V will reduce the threshold 1 V for every 1 V of drop in the supply voltage. More aggressive tracking slopes can be programmed if desired. Program the *LIM_TH_MIN* below the minimum the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

The VBAT limiter tracking slope *LIMB_SLOPE[31:0]* represent the limit in a 4.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired infection voltage using equation *LIMB_SLOPE* = round(slope(V/V)*2^28).

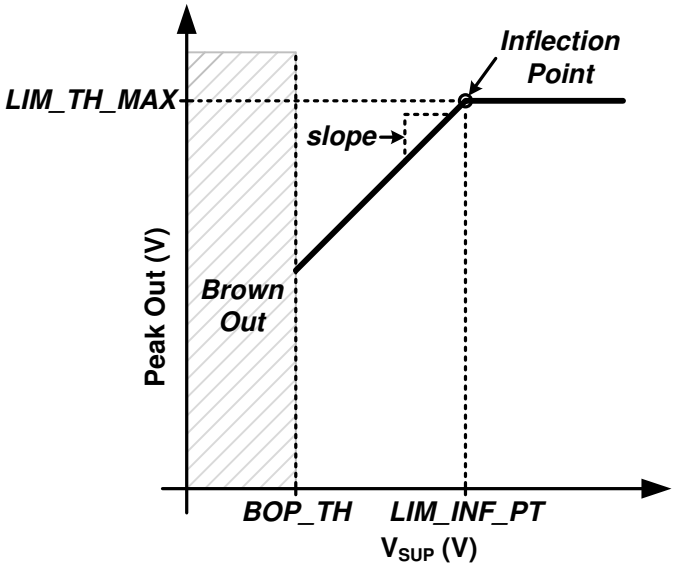

Figure 39. Limiter with Inflection Point

Table 61. Limiter VBAT Tracking Slope

LIMB_SLOPE[31:0]	SLOPE (V/V)
0x1000 0000	1 (default)
. . .	...
0x4000 0000	4

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the *LIM_TH_MIN* register to the desired minimum threshold. This is shown in Figure 40 below.

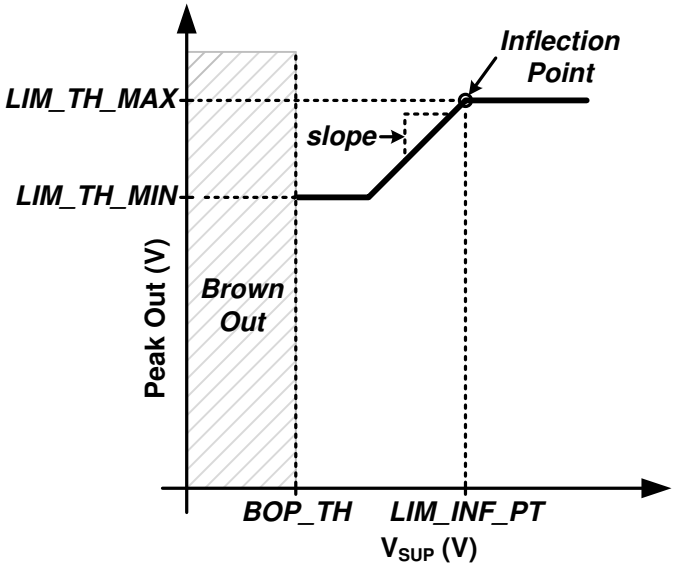

Figure 40. Limiter with Inflection Point and Minimum Threshold

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The TAS2564 also employs a Brown Out Prevention (BOP) feature that serves as a low latency priority input to the limiter engine that begins attacking the VBAT supply dipping below the programmed BOP threshold. This feature can be enabled by setting the *BOP_EN* register bit high. It should be noted that the BOP feature is independent of the limiter and will function if enabled, even if the limiter is disabled. The BOP threshold is configured by setting the threshold with register bits *BOP_TH*.

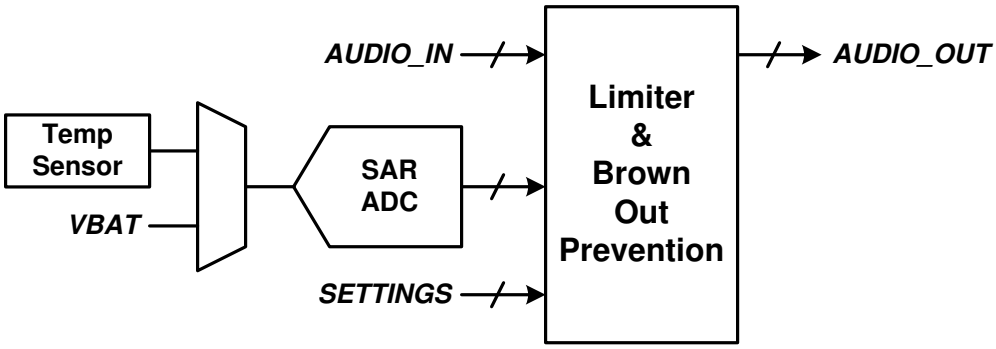

Figure 41. Limiter Block Diagram

Table 62. Brown Out Prevention Enable

BOP_EN	VALUE
0	Disabled
1	Enabled (default)

The Brownout prevention threshold *BOP_TH* represent a threshold in a 4.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired brownout threshold using equation *BOP_TH* = round(Volts*2^28).

Table 63. Brown Out Prevention Threshold

BOP_TH[31:0]	VBAT THRESHOLD (V)
0x0000 000 - 0x1FFF FFFF	Reserved
0x2000 0000	2.5
...	...
0x2E66 6666	2.9 (default)
...	...
0x2000 0000	4
0x2000 0001 - 0xFFFF FFFF	Reserved

The BOP feature has a separate attack rate *BOP_ATK_RT*, attack step size *BOP_ATK_ST* and hold time *BOP_HLD_TM* from the battery tracking limiter. The BOP feature uses the *LIMB_RLS_RT* register setting to release after a brown out event. The rates are based on the number of audio samples and actual time values can be calculated by multiplying by 1/fs. For example the attack rate of 4 samples at 48 ksps would be approximately 83 µs.

Table 64. Brown Out Prevention Attack Rate

BOP_ATK_RT[2:0]	ATTACK RATE (samples/step)	ATTACK RATE @ 48 ksps (~µs)
0x0	1	20
0x1	2	42
0x2	4	83
0x3	8	167
0x4	16	333
0x5	32	666

Table 64. Brown Out Prevention Attack Rate (continued)

BOP_ATK_RT[2:0]	ATTACK RATE (samples/step)	ATTACK RATE @ 48 ksps (~µs)
0x6	64	1300
0x7	128	2700

Table 65. Brown Out Prevention Attack Step Size

BOP_ATK_ST[1:0]	STEP SIZE (dB)
00	0.5
01	1 (default)
10	1.5
11	2

Table 66. Brown Out Prevention Hold Time

BOP_HLD_TM[2:0]	HOLD TIME (ms)
0x0	0
0x1	10
0x2	25
0x3	50
0x4	100
0x5	250
0x6	500 (default)
0x7	1000

The TAS2564 can also shutdown the device when a brown out event occurs if the *BOP_MUTE* register bit is set high. For the device to continue playing audio again, the device must transition through a SW/HW shutdown state. Setting the *BOP_INF_HLD* high will cause the limiter to stay in the hold state (for example never release) after a cleared brown out event until either the device transitions through a mute or SW/HW shutdown state or the register bit *BOP_HLD_CLR* is written to a high value (which will cause the device to exit the hold state and begin releasing). This bit is self clearing and will always readback low. Figure 42 below illustrates the entering and exiting from a brown out event.

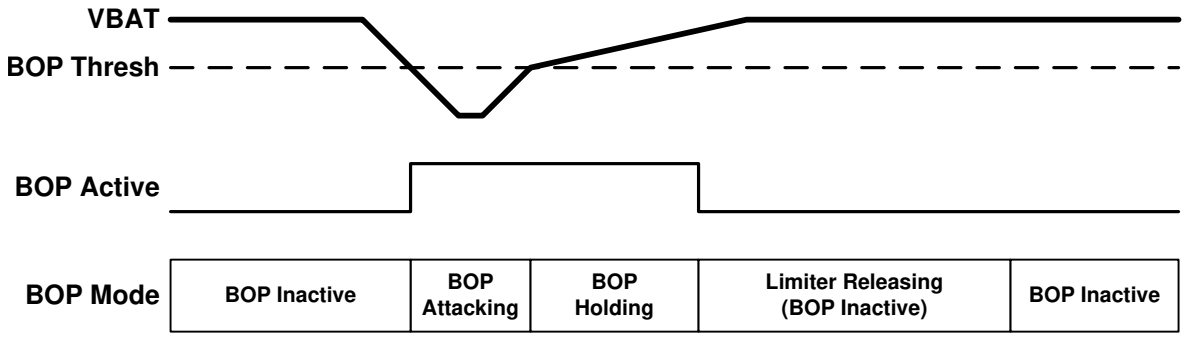

Figure 42. Brown Out Prevention Event

Table 67. Shutdown on Brown Out Event

BOP_MUTE	VALUE
0	Don't Shutdown (default)
1	Mute then shutdown

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Table 68. Infinite Hold on Brown Out Event

BOP_INF_HLD	VALUE
0	Use *BOP_HLD_TM* after Brown Out event (default)
1	Do not release until *BOP_HLD_CLR* is asserted high

If the TAS2564 is configured to hold the brownout event until cleared the attenuation will remain until *BOP_HLD_CLR* register clear is performed. This should be performed by setting the *BOP_HLR_CLR* bit high, reading the register and then setting the *BOP_HLD_CLR* back to low.

Table 69. BOP Infinite Hold Clear

BOP_HLD_CLR	VALUE
0	Don't clear (default)
1	Clear event

A hard brownout level can be set to shutdown the TAS2564 if the BOP cannot mitigate the drop in battery voltage VBAT. This will shutdown the device and should not be used if the *BOP_MUTE* is enable. The brownout shutdown will only function if brownout engine is enabled using *BOP_EN*.

Table 70. Brown Out Shutdown Enable

BOSD_EN	VALUE
0	Disabled (default)
1	Enabled

The Brownout prevention shutdown threshold *BOSD_TH* represent a threshold in a 5.X format. To calculate the value to write to the 4 registers by apply the following formula to the desired brownout threshold using equation *BOSD_TH* = round(Volts*2^27).

Table 71. Brown Out Shutdown Threshold

BOSD_TH[31:0]	VBAT THRESHOLD (V)
0x2000 0000	2.5
. . .	...
0x2B33 3333	2.7 (default)
. . .	...
0x3FFF FFFF	3.99

8.4.2.6 Inter Chip Limiter Alignment

8.4.2.6.1 TDM Mode

The TAS2564 supports alignment of limiter (including brown out prevention) dynamics across devices that share the same TDM bus. This ensures consistent gain between channels during limiting or brown out events since these dynamics are dependent on audio content, which can vary across channels. Each device can be configured to align to a specified number of other devices, which allows creation of groupings of devices that align only to each other. All devices in the same group must use the same setting.

Limiter activity is communicated via the limiter gain reduction parameter that can be optionally transmitted by each device on SDOUT in an 8-bit time slot. Gain reduction should be transmitted in adjacent time slots for all devices that are to be aligned beginning with the first slot that is specified by the *ICLA_SLOT* register. The order of the devices is not important as long as they are adjacent. The time slot for limiter gain reduction is configured by the *GAIN_SLOT* register and enabled by the *GAIN_TX* register bit.

The *ICLA_SEN* register specify which time slots should be listened to for gain alignment. This allows any number of devices between two and eight to be grouped together. At least two of these bits should be enabled for alignment to take place. The *ICLA_USE_MAX* register bit determines whether alignment is based on the maximum or minimum gain reduction value from the group of enabled devices. If the BIL_ICLA_EN is enabled the # of slots will be double what is selected. For example if time-slot 0,1, and 2 are used for gain alignment. Then time-slots 3, 4, and 5 will be used for brownout-current alignment.

To enable the inter chip limiter alignment feature, the *ICLA_GAIN_EN* register bit should be asserted high and all devices should be configured with identical limiter and brown out prevention settings. Limiter gain reduction transmission should be enabled on all devices as described above.

Table 72. Inter Chip Limiter Alignment

ICLA_GAIN_EN	VALUE
0	Disabled (default)
1	Enabled

Table 73. ICLA Gain Alignment Configuration

ICLA_MODE	VALUE
00	Use the maximum gain reduction of the ICLA group (default)
01	Use the minimum gain reduction of the ICLA group
10-11	Reserved

Table 74. Inter Chip Limiter Gain Alignment Starting Time Slot

ICLA_GAIN_SLOT[5:0]	STARTING TIME SLOT
0x00	Time Slot 0
0x01	Time Slot 1
0x02	Time Slot 2
...	...
0x3F	Time Slot 63

Table 75. Inter Chip Limiter Alignment Time Slots Enable

REGISTER BIT	DESCRIPTION	BIT VALUE	STATE
ICLA_GAIN_SEN[0]	Time Slot = *ICLA_GAIN_SLOT*. When enabled, the limiter will include this time slot in the alignment group.	0	Disabled (default)
		1	Enabled
ICLA_GAIN_SEN[[1]	Time Slot = *ICLA_GAIN_SLOT* + 1. When enabled, the limiter will include this time slot in the alignment group.	0	Disabled (default)
		1	Enabled
ICLA_GAIN_SEN[[2]	Time Slot = *ICLA_GAIN_SLOT* + 2. When enabled, the limiter will include this time slot in the alignment group.	0	Disabled (default)
		1	Enabled
ICLA_GAIN_SEN[3]	Time Slot = *ICLA_GAIN_SLOT* + 3. When enabled, the limiter will include this time slot in the alignment group.	0	Disabled (default)
		1	Enabled

8.4.2.7 Class-D Settings

The TAS2564 Class-D amplifier supports spread spectrum PWM modulation, which can be enabled by setting the *AMP_SS* register bit high. This can help reduce EMI in some systems.

Table 76. Low EMI Spread Spectrum Mode

AMP_SS	SPREAD SPECTRUM
0	Disabled
1	Enabled (default)

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By default the Class-D amplifier's switching frequency is based on the device's trimmed internal oscillator. To synchronize switching to the audio sample rate, set the *CLASSD_SYNC* register bit high. When the Class-D is synchronized to the audio sample rate, the *RATE_RAMP* register bit must be set based whether the audio sample rate is based on a 44.1 kHz or 48 kHz frequency. For 44.1, 88.2 and 176.4 kHz, set this bit high. for 48, 96 and 192 kHz, set this bit low. This ensures that the internal ramp generator has the appropriate slope.

Table 77. Class-D Synchronization Mode

CLASSD_SYNC	SYNCHRONIZATION MODE
0	Not synchronized to audio clocks (default)
1	Synchronized to audio clocks

Table 78. Sample Rate for Class-D Synchronized Mode

RAMP_RATE	PLAYBACK SAMPLE RATE
0	multiples of 48 kHz(default)
1	multiples of 44.1 kHz

TAS2564 also supports low noise receiver mode which can be enabled by *ICN_MODE*. In this mode, device gain should be limited to 6dBV. It is recommended to use the device in internal Boost configuration to achieve best noise performance in receiver mode

Table 79. Receiver Mode

ICN_MODE	MODE
0	Speaker Mode (default)
1	Receiver Mode

8.4.3 SAR ADC

A 10-bit SAR ADC monitors VBAT voltage *VBAT_CNV* and die temperature *TMP_CNV*. VBAT voltage conversions are also used by the limiter and brown out prevention features.

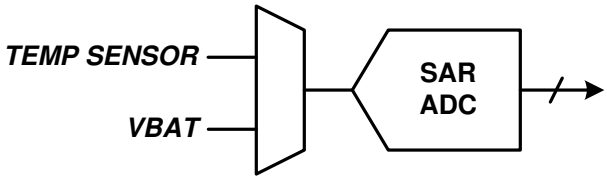

Figure 43. SAR Block Diagram

Actual VBAT voltage is calculated by dividing the *VBAT_CNV* register by 64. Actual die temperature is calculated by subtracting 93 from *TMP_CNV* register. The battery voltage VBAT can be filtered using *VBAT_FLT* register but will increase the latency. The *VBAT_CNV* registers should be read *VBAT_MSB* followed by *VBAT_LSB*.

Table 80. VBAT Filtering

VBAT_FLT[0]	FILTER POLE
0	100 kHz (default)
1	Bypass

Table 81. ADC VBAT Voltage Conversion

VBAT_CNV[9:0]	VBAT VOLTAGE (V)
0x000	0 V
0x001	0.0156 V
...	...
0x100	4.0 V

Table 81. ADC VBAT Voltage Conversion (continued)

VBAT_CNV[9:0]	VBAT VOLTAGE (V)
. . .	...
0x17F	5.9844 V
0x180	6.0 V

Table 82. ADC Die Temperature Conversion

TMP_CNV[7:0]	DIE TEMPERATURE (°C)
0x00	-93 °C
0x01	-92 °C
. . .	...
0x76	25 °C
. . .	...
0xFE	161 °C
0xFF	162 °C

8.4.4 Boost

The TAS2564 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required it is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using Table 83.

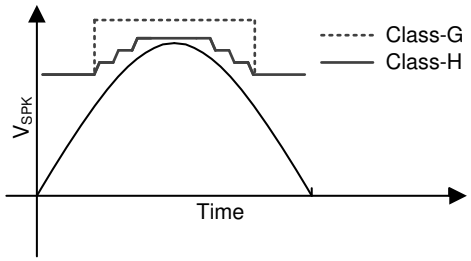

Figure 44. Boost Mode Signal Tracking Example

Table 83. Boost Mode

BST_MODE[1:0]	BOOST MODE
00	Class-H - High efficiency (default)
01	Class-G - Low in-rush
10	Always On
11	Always Off - Pass-through

The boost can be enabled and disabled using *BST_EN* register. When driving the Class-D amplifier using an external supply through the PVDD pin, the boost should be disabled and the VBST pin can be left floating. Do not drive an external voltage on the VBST pin. When suppling and external PVDD voltage the VBAT voltage must also be supplied to the device. While VBAT supply must be present it will not carry current to the speaker load.

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Table 84. Boost Enable

BST_EN	BOOST IS
0	Disabled
1	Enabled (default)

Table 85. Active Mode PFM Lower Frequency Limit

BST_PFML[1:0]	LOWER LIMIT (Hz)
00	No lower limit
01	25 kHz
10	50 kHz (default)
11	100 kHz

The boost has a soft-start to limit in-rush current during the initial charge. The current limit and soft-start timer are configurable to adjust to system component selection.

Table 86. Soft-Start Current Limit

BST_SSL[1:0]	CURRENT LIMIT (A)
00	Disabled - Boost Normal Limit
01	1.2 A(default)
10	1.83 A
11	2.44 A

The boost inductor and decoupling capacitor range needs to be specified using *BST_IR* and *BST_LR* registers. These setting optimize the boost to ensure current limit accuracy and avoid clipping in class-H operation.

Table 87. Boost Inductor Range

BST_IR[1:0]	INDUCTANCE (H)
00	< 0.6 µH
01	0.6 µH-1.3 µH (default)
10	1.3 µH - 2.5 µH
11	Reserved

Table 88. Boost Load Regulation

BST_LR	VALUE
00	4.4A/V; load regulation = 0.9 V
01	3.67 A/V; load regulation = 1.1 V
10	2.93 A/V; load regulation = 1.37 V
11	1.95A/V; load regulation=2.06V

The maximum boost voltage regulation is set by BST_VREG. When operating in class-G mode the boost when needed will be at this voltage. In class-H mode of operation the boost voltage is automatically selected based on the audio signal but, will not exceed this set value.

Table 89. Boost Max Regulation Voltage

BST_VREG[4:0]	BOOST VOLTAGE (V)
0x00-0x06	Reserved
0x7	6 V
0x8	6.5 V
. . .	...
0x13	12 V
0x14	12.5 V (default)
0x15	13 V

Table 89. Boost Max Regulation Voltage (continued)

BST_VREG[4:0]	BOOST VOLTAGE (V)
0x16-0X1F	Reserved

The peak current limits the boost current drawn from the VBAT supply. This setting allows flexibility in the inductor selection for various saturation currents. The current limit can be adjust in 45 mA steps with register BST_ILIM[5:0]. The peak current limit setting is the maximum and may be temporarily reduced if the and ICLA current limit is active.

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Table 90. Peak Current Limit

BST_ILIM[5:0]	CURRENT (A)
0x00	1.206 A
0x01	1.273 A
0x02	1.340 A
. . .	...
0x39	5.025 A (default)
. . .	...
0x3F	5.427A

8.4.5 IV Sense

The TAS2564 provides speaker voltage and current sense for real time monitoring of loudspeaker behavior. The VSNS_P and VSNS_N pins should be connected after any ferrite bead filter (or directly to the OUT_P and OUT_N connections if no EMI filter is used). The V-Sense connections eliminate IR drop error due to packaging, PCB interconnect or ferrite bead filter resistance. It should be noted that any interconnect resistance after the V-Sense terminals will not be corrected for, so it is advised to connect the sense connections as close to the load as possible.

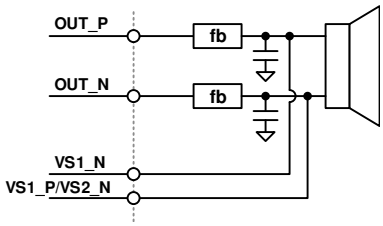

Figure 45. V-Sense Connections

TAS2564 also supports Dual V-Sense Channel. Second V-Sense Channel can be used with dual voice coil speakers. Similar to Conventional Speakers, two of the connections driven by speaker, should be connected after any ferrite bead and as close to load as possible. Center tap can be tapped directly from center terminal of speaker available for dual voice coils.

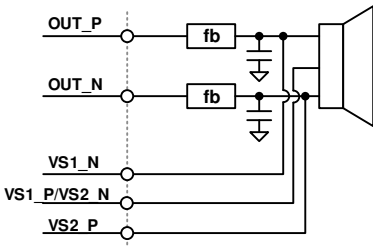

Figure 46. Dual V-Sense Connections

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I-Sense and V-Sense can be powered down by asserting the *ISNS_PD*, *VSNS_PD* and *VSNS2_PD* register bits. When powered down, the device will return null samples for the powered down block. The IV-sense is High Passed Filtered and the Bi-Quad filter coefficients can be changed from the default 2 Hz using the *IVHPF_N0*, *IVHPF_N1*, *IVHPF_D1* registers using the equations [N, D] = butter(1, fc/(fs/2), 'high'); round(N(0)*2^31);. These coefficients can be calculated and set using PurePath™ Console 3 Software.

Table 91. I-Sense Power Down

ISNS_PD	SETTING
0	I-Sense is active
1	I-Sense is powered down (default)

Table 92. V-Sense Power Down

VSNS_PD	SETTING
0	V-Sense is active
1	V-Sense is powered down (default)

Table 93. V-Sense2 Power Down

VSNS2_PD	SETTING
0	V-Sense 2 is active
1	V-Sense 2 is powered down (default)

8.4.6 DC Detect

TAS2564 supports DC Playback, detection and protection against High DC playback. To enable DC Playback, High Pass Filter in Playback path needs to be disabled by setting *HPF_DIS*. Device also offers protection against potentially damaging DC Voltages across speaker load if the DC Playback is enabled. DC playback higher than threshold set by *DC_DET_TH* for time greater than *DC_DET_TM*, TAS2564 will detect DC and shutdown the device. Device shutdown on high DC detection can be disabled by*DC_DET_PD*. DC detection feature itself can be disabled by *DC_DET_EN*. It is recommended to use PurePath™ Console 3 Software to configure the DC Detection and Protection feature as the software will perform the necessary math for each register.

Table 94. DC Detection Enable

DC_DET_EN	Setting
0	DC Detection is disabled(default)
1	DC Detection is enabled

Table 95. HPF Disable

HPF_DIS	SETTING
0	HPF is enabled(default)
1	HPF is disabled.

Table 96. DC Detection Timer

DC_DET_TM	Delay
00	20 ms
01	50 ms(default)
10	75 ms
11	100 ms

Table 97. Shutdown on DC Detection

DC_DET_PD	SETTING
0	No Powerdown on High DC detection (default)
1	Device powerdown on High DC detection

It is worth noting that DC Detection inside the device is implemented with a Low Pass Filter which will cause low frequencies to cause some measurement errors in DC. DC detection filter offers 25 dB attenuation at 20 Hz and greater than 40dB attenuation for frequencies greater than 40 Hz. DC Detection Threshold should be selected while taking care of these constraints.

8.4.7 Load Diagnostics

The TAS2564 can check the speaker terminal for an open or short. This can be used to determine if a problem exists with the speaker or trace to the speaker. The entire operation is performed by the TAS2564 and results reported using the IRQZ pin or read over I^2C bus on completion. The load diagnostics can be performed using external audio clock or the internal oscillator.

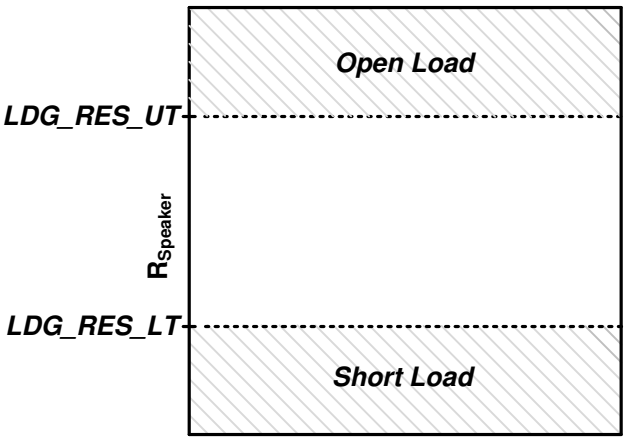

Figure 47. Load Diagnostics

The speaker open and short thresholds are configured using the respective *LDG_RES_UT* and *LDG_RES_LT* registers using equation round (Ω/7*2^22). The load diagnostic mode can be run in two ways. First if the device is in Software Shutdown the load diagnostic mode can be run but setting LDG_MODE high. The diagnostic will be run and the device will return to Software Shutdown. The load diagnostics can also be run before transitioning to Active. This is done by setting the MODE register to . If the load is within the specified range the device will transition to Active otherwise it will transition to Software Shutdown. When the load diagnostics is run it will play a 22 kHz at -35 dBFS for 100 ms and measure the resistance of the speaker trace. The result is averaged over the time specified by the IVSNS_AVG register. The measured speaker impedance can be read from *LDS_RES_VAL1* using the equations Impedance = 7*(LD_RES_VAL1)/2^22) Ω.

Table 98. IV-Sense Averaging

IVSNS_AVG[1:0]	SETTING
00	5 ms (default)
01	10 ms
10	50 ms
11	100 ms

Table 99. Load Diagnostic Mode

LDG_MODE	SETTING
0	Load Diagnostic Not Running (default)
1	Run Load Diagnostic

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Table 100. Load Diagnostic Clock Source

LDG_CLK	SETTING
0	External TDM
1	Internal Oscillator (default)

8.4.8 Clocks and PLL

In TMD/I^{2}C Mode, the device operates from SBCLK. Table 101 and Table 102 below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio (for 44.1 kHz and 48 kHz family frequencies respectively.

If the sample rate is properly configured via the *SAMP_RATE[1:0]* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts. After the clock error is detected the device will enter a low power halt mode after *CLK_HALT_TIMER* if *CLK_HALT_EN* is enabled. Additionally the device can automatically power up and down on valid clock signals if *CLK_ERR_PWR_EN* is set. The device sampling rate should not be changed while this feature is enabled. Additionally, the *CLK_HALT_EN* should be set when *CLK_ERR_PWR_EN* is set for this feature to work properly.

Table 101. Supported SBCLK Frequencies (48 kHz based sample rates)

SAMPLE RATE (kHz)	SBCLK TO FSYNC RATIO						
	64	96	128	192	256	384	512
16 kHz	1.024 MHz	1.536 MHz	2.048 MHz	3.072 MHz	4.096 MHz	6.144 MHz	8.192 MHz
32 kHz	2.048 MHz	3.072 MHz	4.0960 MHz	6.144 MHz	8.192 MHz	12.288 MHz	16.384 MHz
48 kHz	3.072 MHz	4.608 MHz	6.144 MHz	9.216 MHz	12.288 MHz	18.432 MHz	24.576 MHz
96 kHz	6.144 MHz	9.216 MHz	12.288 MHz	18.432 MHz	24.576 MHz	-	-

Table 102. Supported SBCLK Frequencies (44.1 kHz based sample rates)

SAMPLE RATE (kHz)	SBCLK TO FSYNC RATIO						
	64	96	128	192	256	384	512
14.7 kHz	940.8 kHz	1.4112 MHz	1.8816 MHz	2.8224 MHz	3.7632 MHz	5.6448 MHz	7.5264 MHz
29.4 kHz	1.8816 MHz	2.8224 MHz	3.7632 MHz	5.6448 MHz	7.5264 MHz	11.2896 MHz	15.0528 MHz
44.1 kHz	2.8224 MHz	4.2336 MHz	5.6448 MHz	8.4672 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz
88.2 kHz	5.6448 MHz	8.4672 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	-	-

Table 103. Clock Power Up/Down on Valid ASI Clocks

CLK_ERR_PWR_EN	SETTING
0	Disabled (default)
1	Enabled

Table 104. Clock Halt(Sleep) After Errors Longer Than Halt Timer

CLK_HALT_EN	SETTING
0	Enabled (default)
1	Disabled

Table 105. Clock Halt Timer

CLK_HALT_TIMER[2:0]	SETTING
000	1 ms
001	3.27 ms
010	26.21 ms
011	52.42 ms (default)
100	104.85 ms

Table 105. Clock Halt Timer (continued)

CLK_HALT_TIMER[2:0]	SETTING
101	209.71 ms
110	419.43 ms
111	838.86 ms

8.4.9 Thermal Foldback

The TAS2564 monitors the die temperature and can automatically limit the audio signal when the die temperature reaches a set threshold. It is recommended to use PurePath™ Console 3 Software to configure the thermal foldback as the software will perform the necessary math for each register.

Thermal foldback can be disabled using *TF_EN*. If the die temperature reaches *TF_TEMP_TH* this feature will begin to attenuate the audio signal to prevent the device from shutting down due to over-temperature. It will attenuate the audio signal by TF_LIMS db per degree of temperature over TF_TEMP_TH. The thermal foldback with attack at a fixed rate of 0.25 dB per sample. A maximum attenuation of TF_MAX_ATTN can be specified. However if the device continue to heat up eventually the device over-temperature will be triggered. The attenuation will be held for *TF_HOLD_CNT* samples before the attenuation will begin releasing.

Table 106. Thermal Foldback Enable

TF_EN	SETTING
0	Disabled
1	Enabled (default)

Table 107. Thermal Foldback Registers

REGISTER	DESCRIPTION	CALCULATION
TF_LIMS	Thermal foldback limiter slope (in db/°C)	round(10^(-slope / 20)*2^31)
TF_HOLD_CNT	Thermal foldback hold count (samples)	round(seconds * 1000)
TF_REL_RATE	Thermal foldback limiter release rate (db/samples)	round(10^(dB per sample / 20)*2^30)
TF_TEMP_TH	Thermal foldback limiter temperature threshold (°C)	round(°C * 2^23)
TF_MAX_ATTN	Thermal foldback max gain reduction (dB)	round(10^(max attn dB/20)*2^31)

8.4.10 Internal Tone Generator

The TAS2564 has two internal tone generators that can be used for pilot tone, ultrasonic tone, or diagnostic purposes. It is recommended to use PurePath™ Console 3 Software to configure the tone generators as the software will perform the necessary math for each register.

The frequency and amplitude or each generator can be set independently. Each tone generator is enabled using TGx_EN and will soft-ramp to the level set by registers TGx_AMP if corresponding register TGx_SR is set. The frequency using registers TGx_FREQ and amplitude using registers TGx_AMP. These amplitude and frequency should be set only when the tone generator is disabled. Additionally the first tone-generator can be configured to enable and disable the tone using a pin selected by TG1_PINEN pin. When enabled the pin will be logically ORed with the TG1_EN register to play the tone. This can be used for audible diagnostic tones or other alerting functions.

When the tone generator is configured to operate in pin-triggered mode, the sampling rate used in the TG1 equations should be 96 kHz. The range of frequencies that can be generated in this mode is 20 Hz to 38 kHz. For ASI bus sample rates of 192 kHz the tone generator 1 and 2 will run only at 96 kHz and this sampling rate should be used in the calculation. When not in pin trigger TG1 can generate tones up to fs/2.

The max frequency for tone generator 2 is based on the sampling rate and shown in Table 114.

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Table 108. Tone Generator Clock Source

TG_CLK	SETTING
0	External TDM (default)
1	Internal Oscillator

Table 109. Tone Generator 1 Enable

TG1_EN	TONE GENERATOR OUTPUT
00	disabled / pin trigger (default)
01	enabled - play tone always
10	audio level enabled
11	reserved

Table 110. Tone Generator 1 Pin Enable

TG1_PINEN[1:0]	TONE GENERATOR OUTPUT
00	disabled (default)
01	SDIN pin
10	MCLK pin
11	AD1 pin

Table 111. Tone Generator 1 Soft-Ramp

TG1_SR	SOFT RAMPUP
0	disabled
1	enabled (default)

The pilot tone frequency and amplitude can be programmed using the following register. The equations are used to calculate the register settings for a given gain, frequency, and audio sampling rate.

fc = frequency of the tone

fs = sampling rate

TG1_FREQ1[1-4] = 2 * cos(2 * pi * fc / fs)

TG1_FREQ2[1-4] = sin(2 * pi * fc / fs)

TG1_FREQ3[1-4] = (lcm(fs,fc) / fc) - 1

TG1_AMP = 10 ^ (dB/20)

Equations for tone generator 2 are

TG2_FREQ1[1-4] = 2 * cos(2 * pi * fc / (n*fs))
TG2_FREQ2[1-4] = sin(2 * pi * fc / (n*fs))
TG2_FREQ3[1-4] = (lcm(n*fs,fc) / fc) - n
TG2_AMP = (10 ^ (dB/20)) / 4

Table 112. Tone Generator Defaults

REGISTER	DEFAULT VALUE	DEFAULT REGISTERVALUE
TG1_FREQ1[1-4]	0	0x0000 0000
TG1_FREQ2[1-4]	0	0x0000 0000
TG1_FREQ3[1-4]	0	0x0000 0000
TG1_AMP	-40 dBFS	0x0147 AE14
TG2_FREQ1[1-4]	0	0x0000 0000
TG2_FREQ2[1-4]	0	0x0000 0000
TG2_FREQ3[1-4]	0	0x0000 0000

Table 112. Tone Generator Defaults (continued)

REGISTER	DEFAULT VALUE	DEFAULT REGISTERVALUE
TG2_AMP	-12 dBFS	0x2026 F310

Table 113. Tone Generator 2 Enable

TG2_EN	TONE GENERATOR OUTPUT
0	disabled (default)
1	enabled - play tone

Table 114. Tone Generator 2 n Value and Range

fs	n	MAX TONE FREQUENCY
96 kHz	1	< fs /2
48 kHz, 32 kHz	2	< fs
24 kHz	4	< 2*fs
16 kHz, 8 kHz	8	< 4 * fs

Table 115. Tone Generator 2 Soft-Ramp

TG2_SR	SOFT RAMPUP
0	disabled
1	enabled (default)

8.5 Register Maps

8.5.1 Register Summary Table Page=0x00

Addr	Register	Description	Section
0x00	PAGE0	Device Page	PAGE0 (page=0x00 address=0x00) [reset=0h]
0x01	SW_RESET	Software Reset	SW_RESET (page=0x00 address=0x01) [reset=1h]
0x02	PWR_CTL	Power Control	PWR_CTL (page=0x00 address=0x02) [reset=8Eh]
0x03	PB_CFG1	Playback Configuration 1	PB_CFG1 (page=0x00 address=0x03) [reset=20h]
0x04	MISC_CFG1	Misc Configuration 1	MISC_CFG1 (page=0x00 address=0x04) [reset=C6h]
0x05	MISC_CFG2	Misc Configuration 2	MISC_CFG2 (page=0x00 address=0x05) [reset=22h]
0x06	TDM_CFG0	TDM Configuration 0	TDM_CFG0 (page=0x00 address=0x06) [reset=9h]
0x07	TDM_CFG1	TDM Configuration 1	TDM_CFG1 (page=0x00 address=0x07) [reset=2h]
0x08	TDM_CFG2	TDM Configuration 2	TDM_CFG2 (page=0x00 address=0x08) [reset=Ah]
0x09	TDM_CFG3	TDM Configuration 3	TDM_CFG3 (page=0x00 address=0x09) [reset=10h]
0x0A	TDM_CFG4	TDM Configuration 4	TDM_CFG4 (page=0x00 address=0x0A) [reset=13h]
0x0B	TDM_CFG5	TDM Configuration 5	TDM_CFG5 (page=0x00 address=0x0B) [reset=2h]
0x0C	TDM_CFG6	TDM Configuration 6	TDM_CFG6 (page=0x00 address=0x0C) [reset=0h]
0x0D	TDM_CFG7	TDM Configuration 7	TDM_CFG7 (page=0x00 address=0x0D) [reset=4h]
0x0E	TDM_CFG8	TDM Configuration 8	TDM_CFG8 (page=0x00 address=0x0E) [reset=5h]
0x0F	TDM_CFG9	TDM Configuration 9	TDM_CFG9 (page=0x00 address=0x0F) [reset=6h]
0x10	TDM_CFG10	TDM Configuration 10	TDM_CFG10 (page=0x00 address=0x10) [reset=7h]
0x11	TDM_DET	TDM Clock detection monitor	TDM_DET (page=0x00 address=0x11) [reset=7Fh]
0x12	LIM_CFG_0	Limiter Configuration 0	LIM_CFG_0 (page=0x00 address=0x12) [reset=12h]
0x13	LIM_CFG_1	Limiter Configuration 1	LIM_CFG_1 (page=0x00 address=0x13) [reset=76h]
0x14	BOP_CFG_0	Brown Out Prevention 0	BOP_CFG_0 (page=0x00 address=0x14) [reset=1h]
0x15	BOP_CFG_1	Brown Out Prevention 1	BOP_CFG_1 (page=0x00 address=0x15) [reset=2Eh]
0x18	GAIN_ICLA_CFG0	Inter Chip Limiter Alignment 0	GAIN_ICLA_CFG0 (page=0x00 address=0x18) [reset=Ch]
0x19	ICLA_CFG1	Inter Chip Limiter Alignment 1	ICLA_CFG1 (page=0x00 address=0x19) [reset=0h]

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Register Maps (continued)

0x1A	INT_MASK0	Interrupt Mask 0	INT_MASK0 (page=0x00 address=0x1A) [reset=FCh]
0x1B	INT_MASK1	Interrupt Mask 1	INT_MASK1 (page=0x00 address=0x1B) [reset=A6h]
0x1E	INT_MASK6	Interrupt Mask 6- Interrupt masks.	INT_MASK6 (page=0x00 address=0x1E) [reset=80h]
0x24	INT_LTCH0	Latched Interrupt Readback 0	INT_LTCH0 (page=0x00 address=0x24) [reset=0h]
0x25	INT_LTCH1	Latched Interrupt Readback 1	INT_LTCH1 (page=0x00 address=0x25) [reset=0h]
0x28	INT_LTCH6	Latched Interrupt Readback 6	INT_LTCH6 (page=0x00 address=0x28) [reset=0h]
0x2A	VBAT_MSB	SAR ADC Conversion 0	VBAT_MSB (page=0x00 address=0x2A) [reset=0h]
0x2B	VBAT_LSB	SAR ADC Conversion 1	VBAT_LSB (page=0x00 address=0x2B) [reset=0h]
0x2C	TEMP	SAR ADC Conversion 2	TEMP (page=0x00 address=0x2C) [reset=0h]
0x30	INT_CLK	Interrupt and Clock Error	INT_CLK (page=0x00 address=0x30) [reset=19h]
0x31	DIN_PD	Digital Input Pin Pull Down	DIN_PD (page=0x00 address=0x31) [reset=40h]
0x32	MISC_CFG3	Misc Configuration 3	MISC_CFG3 (page=0x00 address=0x32) [reset=80h]
0x33	BOOST_CFG1	Boost Configure 1	BOOST_CFG1 (page=0x00 address=0x33) [reset=34h]
0x34	BOOST_CFG2	Boost Configure 2	BOOST_CFG2 (page=0x00 address=0x34) [reset=40h]
0x35	BOOST_CFG3	Boost Configure 3	BOOST_CFG3 (page=0x00 address=0x35) [reset=78h]
0x3D	MISC_CFG4	Misc Configuration 4	MISC_CFG4 (page=0x00 address=0x3D) [reset=8h]
0x3F	TG_CFG0	Tone Generator	TG_CFG0 (page=0x00 address=0x3F) [reset=0h]
0x40	BOOST_CFG4	Boost Configure 4	BOOST_CFG4 (page=0x00 address=0x40) [reset=79h]
0x41	TDM_CFG11	TDM Configuration 11	TDM_CFG11 (page=0x00 address=0x41) [reset=48h]
0x42	IO_DRV1	PAD drain strength control 1	IO_DRV1 (page=0x00 address=0x42) [reset=0h]
0x43	IO_DRV2	PAD drain strength control 2	IO_DRV2 (page=0x00 address=0x43) [reset=0h]
0x44	IO_DRV3	PAD drain strength control 3	IO_DRV3 (page=0x00 address=0x44) [reset=0h]
0x48	MISC_CFG5	Boost and Class-D Settings	MISC_CFG5 (page=0x00 address=0x48) [reset=A0h]
0x7D	REV_ID	Revision and PG ID	REV_ID (page=0x00 address=0x7D) [reset=0h]
0x7E	I2C_CKSUM	I2C Checksum	I2C_CKSUM (page=0x00 address=0x7E) [reset=0h]
0x7F	BOOK	Device Book	BOOK (page=0x00 address=0x7F) [reset=0h]

8.5.2 Register Summary Table Page=0x01

Addr	Register	Description	Section
0x00	PAGE1	Device Page	PAGE1 (page=0x01 address=0x00) [reset=0h]
0x08	TF_CFG	Thermal Folder Configure	TF_CFG (page=0x01 address=0x08) [reset=0h]
0x24	LDG_CFG2	Load Diagnostic 1	LDG_CFG2 (page=0x01 address=0x24) [reset=0h]

8.5.3 Register Summary Table Page=0x02

Addr	Register	Description	Section
0x00	PAGE2	Device Page	PAGE2 (page=0x02 address=0x00) [reset=0h]
0x0C	DVC_CFG1	Digital Volume Control 1	DVC_CFG1 (page=0x02 address=0x0C) [reset=40h]
0x0D	DVC_CFG2	Digital Volume Control 2	DVC_CFG2 (page=0x02 address=0x0D) [reset=0h]
0x0E	DVC_CFG3	Digital Volume Control 3	DVC_CFG3 (page=0x02 address=0x0E) [reset=0h]
0x0F	DVC_CFG4	Digital Volume Control 4	DVC_CFG4 (page=0x02 address=0x0F) [reset=0h]
0x10	DVC_CFG5	Digital Volume Control 5	DVC_CFG5 (page=0x02 address=0x10) [reset=3h]
0x11	DVC_CFG6	Digital Volume Control 6	DVC_CFG6 (page=0x02 address=0x11) [reset=4Ah]
0x12	DVC_CFG7	Digital Volume Control 7	DVC_CFG7 (page=0x02 address=0x12) [reset=51h]
0x13	DVC_CFG8	Digital Volume Control 8	DVC_CFG8 (page=0x02 address=0x13) [reset=6Ch]
0x14	LIM_CFG1	Limiter Configuration 1	LIM_CFG1 (page=0x02 address=0x14) [reset=2Dh]
0x15	LIM_CFG2	Limiter Configuration 2- Sets limiter max attenuation	LIM_CFG2 (page=0x02 address=0x15) [reset=6Ah]
0x16	LIM_CFG3	Limiter Configuration 3- Sets limiter max attenuation	LIM_CFG3 (page=0x02 address=0x16) [reset=86h]
0x17	LIM_CFG4	Limiter Configuration 4- Sets limiter max attenuation	LIM_CFG4 (page=0x02 address=0x17) [reset=6Fh]
0x18	LIM_CFG5	Limiter Configuration 5	LIM_CFG5 (page=0x02 address=0x18) [reset=56h]

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0x19	LIM_CFG6	Limiter Configuration 6	LIM_CFG6 (page=0x02 address=0x19) [reset=B7h]
0x1A	LIM_CFG7	Limiter Configuration 7	LIM_CFG7 (page=0x02 address=0x1A) [reset=96h]
0x1B	LIM_CFG8	Limiter Configuration 8	LIM_CFG8 (page=0x02 address=0x1B) [reset=FFh]
0x1C	LIM_CFG9	Limiter Configuration 9	LIM_CFG9 (page=0x02 address=0x1C) [reset=16h]
0x1D	LIM_CFG10	Limiter Configuration 10	LIM_CFG10 (page=0x02 address=0x1D) [reset=66h]
0x1E	LIM_CFG11	Limiter Configuration 11	LIM_CFG11 (page=0x02 address=0x1E) [reset=66h]
0x1F	LIM_CFG12	Limiter Configuration 12	LIM_CFG12 (page=0x02 address=0x1F) [reset=66h]
0x20	LIM_CFG13	Limiter Configuration 13	LIM_CFG13 (page=0x02 address=0x20) [reset=34h]
0x21	LIM_CFG14	Limiter Configuration 14	LIM_CFG14 (page=0x02 address=0x21) [reset=CCh]
0x22	LIM_CFG15	Limiter Configuration 15	LIM_CFG15 (page=0x02 address=0x22) [reset=CCh]
0x23	LIM_CFG16	Limiter Configuration 16	LIM_CFG16 (page=0x02 address=0x23) [reset=CDh]
0x24	LIM_CFG17	Limiter Configuration 1	LIM_CFG17 (page=0x02 address=0x24) [reset=10h]
0x25	LIM_CFG18	Limiter Configuration 2	LIM_CFG18 (page=0x02 address=0x25) [reset=0h]
0x26	LIM_CFG19	Limiter Configuration 3	LIM_CFG19 (page=0x02 address=0x26) [reset=0h]
0x27	LIM_CFG20	Limiter Configuration 4	LIM_CFG20 (page=0x02 address=0x27) [reset=0h]
0x28	BOP_CFG1	Brown Out Prevention 1	BOP_CFG1 (page=0x02 address=0x28) [reset=2Eh]
0x29	BOP_CFG2	Brown Out Prevention 2	BOP_CFG2 (page=0x02 address=0x29) [reset=66h]
0x2A	BOP_CFG3	Brown Out Prevention 3	BOP_CFG3 (page=0x02 address=0x2A) [reset=66h]
0x2B	BOP_CFG4	Brown Out Prevention 4	BOP_CFG4 (page=0x02 address=0x2B) [reset=66h]
0x2C	BOP_CFG5	Brown Out Prevention 5	BOP_CFG5 (page=0x02 address=0x2C) [reset=2Bh]
0x2D	BOP_CFG6	Brown Out Prevention 6	BOP_CFG6 (page=0x02 address=0x2D) [reset=33h]
0x2E	BOP_CFG7	Brown Out Prevention 7	BOP_CFG7 (page=0x02 address=0x2E) [reset=33h]
0x2F	BOP_CFG8	Brown Out Prevention 8	BOP_CFG8 (page=0x02 address=0x2F) [reset=33h]
0x30	HPFC_CFG1	HPF Coefficient 1	HPFC_CFG1 (page=0x02 address=0x30) [reset=7Fh]
0x31	HPFC_CFG2	HPF Coefficient 2	HPFC_CFG2 (page=0x02 address=0x31) [reset=FBh]
0x32	HPFC_CFG3	HPF Coefficient 3	HPFC_CFG3 (page=0x02 address=0x32) [reset=B6h]
0x33	HPFC_CFG4	HPF Coefficient 4	HPFC_CFG4 (page=0x02 address=0x33) [reset=14h]
0x34	HPFC_CFG5	HPF Coefficient 5	HPFC_CFG5 (page=0x02 address=0x34) [reset=80h]
0x35	HPFC_CFG6	HPF Coefficient 6	HPFC_CFG6 (page=0x02 address=0x35) [reset=4h]
0x36	HPFC_CFG7	HPF Coefficient 7	HPFC_CFG7 (page=0x02 address=0x36) [reset=49h]
0x37	HPFC_CFG8	HPF Coefficient 8	HPFC_CFG8 (page=0x02 address=0x37) [reset=ECh]
0x38	HPFC_CFG9	HPF Coefficient 9	HPFC_CFG9 (page=0x02 address=0x38) [reset=7Fh]
0x39	HPFC_CFG10	HPF Coefficient 10	HPFC_CFG10 (page=0x02 address=0x39) [reset=7Fh]
0x3A	HPFC_CFG11	HPF Coefficient 11	HPFC_CFG11 (page=0x02 address=0x3A) [reset=6Ch]
0x3B	HPFC_CFG12	HPF Coefficient 12	HPFC_CFG12 (page=0x02 address=0x3B) [reset=28h]
0x3C	TG_CFG1	Tone Generator 1 Freq Calc 1	TG_CFG1 (page=0x02 address=0x3C) [reset=3Fh]
0x3D	TG_CFG2	Tone Generator 1 Freq Calc 1	TG_CFG2 (page=0x02 address=0x3D) [reset=FFh]
0x3E	TG_CFG3	Tone Generator 1 Freq Calc 1	TG_CFG3 (page=0x02 address=0x3E) [reset=7Ah]
0x3F	TG_CFG4	Tone Generator 1 Freq Calc 1	TG_CFG4 (page=0x02 address=0x3F) [reset=E3h]
0x40	TG_CFG5	Tone Generator 1 Freq Calc 2	TG_CFG5 (page=0x02 address=0x40) [reset=1h]
0x41	TG_CFG6	Tone Generator 1 Freq Calc 2	TG_CFG6 (page=0x02 address=0x41) [reset=1h]
0x42	TG_CFG7	Tone Generator 1 Freq Calc 2	TG_CFG7 (page=0x02 address=0x42) [reset=5Bh]
0x43	TG_CFG8	Tone Generator 1 Freq Calc 2	TG_CFG8 (page=0x02 address=0x43) [reset=4Ch]
0x44	TG_CFG9	Tone Generator 1 Freq Calc 3	TG_CFG9 (page=0x02 address=0x44) [reset=0h]
0x45	TG_CFG10	Tone Generator 1 Freq Calc 3	TG_CFG10 (page=0x02 address=0x45) [reset=0h]
0x46	TG_CFG11	Tone Generator 1 Freq Calc 3	TG_CFG11 (page=0x02 address=0x46) [reset=3h]
0x47	TG_CFG12	Tone Generator 1 Freq Calc 3	TG_CFG12 (page=0x02 address=0x47) [reset=1Fh]
0x48	TG_CFG13	Tone Generator 1 Amplitude Calc	TG_CFG13 (page=0x02 address=0x48) [reset=2h]
0x49	TG_CFG14	Tone Generator 1 Amplitude Calc	TG_CFG14 (page=0x02 address=0x49) [reset=46h]
0x4A	TG_CFG15	Tone Generator 1 Amplitude Calc	TG_CFG15 (page=0x02 address=0x4A) [reset=B4h]
0x4B	TG_CFG16	Tone Generator 1 Amplitude Calc	TG_CFG16 (page=0x02 address=0x4B) [reset=E4h]
0x5C	LD_CFG0	Load Diagnostics Resistance Upper Threshold	LD_CFG0 (page=0x02 address=0x5C) [reset=2h]
0x5D	LD_CFG1	Load Diagnostics Resistance Upper Threshold	LD_CFG1 (page=0x02 address=0x5D) [reset=80h]
0x5E	LD_CFG2	Load Diagnostics Resistance Upper Threshold	LD_CFG2 (page=0x02 address=0x5E) [reset=0h]

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0x5F	LD_CFG3	Load Diagnostics Resistance Upper Threshold	LD_CFG3 (page=0x02 address=0x5F) [reset=0h]
0x60	LD_CFG4	Load Diagnostics Resistance Lower Threshold	LD_CFG4 (page=0x02 address=0x60) [reset=0h]
0x61	LD_CFG5	Load Diagnostics Resistance Lower Threshold	LD_CFG5 (page=0x02 address=0x61) [reset=19h]
0x62	LD_CFG6	Load Diagnostics Resistance Lower Threshold	LD_CFG6 (page=0x02 address=0x62) [reset=99h]
0x63	LD_CFG7	Load Diagnostics Resistance Lower Threshold	LD_CFG7 (page=0x02 address=0x63) [reset=9Ah]
0x64	IDC_CFG0	Idle channel detection threshold	IDC_CFG0 (page=0x02 address=0x64) [reset=0h]
0x65	IDC_CFG1	Idle channel detection threshold	IDC_CFG1 (page=0x02 address=0x65) [reset=20h]
0x66	IDC_CFG2	Idle channel detection threshold	IDC_CFG2 (page=0x02 address=0x66) [reset=C4h]
0x67	IDC_CFG3	Idle channel detection threshold	IDC_CFG3 (page=0x02 address=0x67) [reset=9Ch]
0x68	IDC_CFG4	MID Power Threshold	IDC_CFG4 (page=0x02 address=0x68) [reset=2h]
0x69	IDC_CFG5	MID Power Threshold	IDC_CFG5 (page=0x02 address=0x69) [reset=46h]
0x6A	IDC_CFG6	MID Power Threshold	IDC_CFG6 (page=0x02 address=0x6A) [reset=B4h]
0x6B	IDC_CFG7	MID Power Threshold	IDC_CFG7 (page=0x02 address=0x6B) [reset=E4h]
0x6C	IDC_CFG8	Hystersis for idle channel detection	IDC_CFG8 (page=0x02 address=0x6C) [reset=0h]
0x6D	IDC_CFG9	Hystersis for idle channel detection	IDC_CFG9 (page=0x02 address=0x6D) [reset=0h]
0x6E	IDC_CFG10	Hystersis for idle channel detection	IDC_CFG10 (page=0x02 address=0x6E) [reset=12h]
0x6F	IDC_CFG11	Hystersis for idle channel detection	IDC_CFG11 (page=0x02 address=0x6F) [reset=C0h]
0x70	IVHPFC_CFG1	IVSENSE HPF N0 coefficient	IVHPFC_CFG1 (page=0x02 address=0x70) [reset=7Fh]
0x71	IVHPFC_CFG2	IVSENSE HPF N0 coefficient	IVHPFC_CFG2 (page=0x02 address=0x71) [reset=FBh]
0x72	IVHPFC_CFG3	IVSENSE HPF N0 coefficient	IVHPFC_CFG3 (page=0x02 address=0x72) [reset=B6h]
0x73	IVHPFC_CFG4	IVSENSE HPF N0 coefficient	IVHPFC_CFG4 (page=0x02 address=0x73) [reset=14h]
0x74	IVHPFC_CFG5	IVSENSE HPF N1 coefficient	IVHPFC_CFG5 (page=0x02 address=0x74) [reset=80h]
0x75	IVHPFC_CFG6	IVSENSE HPF N1 coefficient	IVHPFC_CFG6 (page=0x02 address=0x75) [reset=4h]
0x76	IVHPFC_CFG7	IVSENSE HPF N1 coefficient	IVHPFC_CFG7 (page=0x02 address=0x76) [reset=49h]
0x77	IVHPFC_CFG8	IVSENSE HPF N1 coefficient	IVHPFC_CFG8 (page=0x02 address=0x77) [reset=ECh]
0x78	IVHPFC_CFG9	IVSENSE HPF D1 coefficient	IVHPFC_CFG9 (page=0x02 address=0x78) [reset=7Fh]
0x79	IVHPFC_CFG10	IVSENSE HPF D1 coefficient	IVHPFC_CFG10 (page=0x02 address=0x79) [reset=F7h]
0x7A	IVHPFC_CFG11	IVSENSE HPF D1 coefficient	IVHPFC_CFG11 (page=0x02 address=0x7A) [reset=6Ch]
0x7B	IVHPFC_CFG12	IVSENSE HPF D1 coefficient	IVHPFC_CFG12 (page=0x02 address=0x7B) [reset=28h]
0x7C	TF_CFG_1	Thermal foldback limiter slope (in db/C)	TF_CFG_1 (page=0x02 address=0x7C) [reset=72h]
0x7D	TF_CFG_2	Thermal foldback limiter slope (in db/C)	TF_CFG_2 (page=0x02 address=0x7D) [reset=14h]
0x7E	TF_CFG_3	Thermal foldback limiter slope (in db/C)	TF_CFG_3 (page=0x02 address=0x7E) [reset=82h]
0x7F	TF_CFG_4	Thermal foldback limiter slope (in db/C)	TF_CFG_4 (page=0x02 address=0x7F) [reset=C0h]

8.5.4 Register Summary Table Page=0x03

Addr	Register	Description	Section
0x00	PAGE3	Device Page	PAGE3 (page=0x03 address=0x00) [reset=0h]
0x1C	DC_DET_THR1	DC detection threshold 1	DC_DET_THR1 (page=0x03 address=0x1C) [reset=18h]
0x1D	DC_DET_THR2	DC detection threshold 2	DC_DET_THR2 (page=0x03 address=0x1D) [reset=2Ah]
0x1E	DC_DET_THR3	DC detection threshold 3	DC_DET_THR3 (page=0x03 address=0x1E) [reset=FFh]
0x1F	DC_DET_THR4	DC detection threshold 4	DC_DET_THR4 (page=0x03 address=0x1F) [reset=53h]
0x20	DC_DET_HYST1	DC detection hysteresis time 1	DC_DET_HYST1 (page=0x03 address=0x20) [reset=0h]
0x21	DC_DET_HYST2	DC detection hysteresis time 2	DC_DET_HYST2 (page=0x03 address=0x21) [reset=0h]
0x22	DC_DET_HYST3	DC detection hysteresis time 3	DC_DET_HYST3 (page=0x03 address=0x22) [reset=27h]
0x23	DC_DET_HYST4	DC detection hysteresis time 4	DC_DET_HYST4 (page=0x03 address=0x23) [reset=10h]
0x24	CLS_H_CFG1	ClassH	CLS_H_CFG1 (page=0x03 address=0x24) [reset=Ah]
0x25	CLS_H_CFG2	ClassH	CLS_H_CFG2 (page=0x03 address=0x25) [reset=3Bh]
0x26	CLS_H_CFG3	ClassH	CLS_H_CFG3 (page=0x03 address=0x26) [reset=C7h]
0x27	CLS_H_CFG4	ClassH	CLS_H_CFG4 (page=0x03 address=0x27) [reset=DCh]
0x28	CLS_H_CFG5	ClassH	CLS_H_CFG5 (page=0x03 address=0x28) [reset=0h]
0x29	CLS_H_CFG6	ClassH	CLS_H_CFG6 (page=0x03 address=0x29) [reset=0h]
0x2A	CLS_H_CFG7	ClassH	CLS_H_CFG7 (page=0x03 address=0x2A) [reset=0h]
0x2B	CLS_H_CFG8	ClassH	CLS_H_CFG8 (page=0x03 address=0x2B) [reset=0h]

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0x74	CLS_H_CFG9	ClassH Minimum boost level in Voltage	CLS_H_CFG9 (page=0x03 address=0x74) [reset=0h]
0x75	CLS_H_CFG10	ClassH Minimum boost level in Voltage	CLS_H_CFG10 (page=0x03 address=0x75) [reset=0h]
0x76	CLS_H_CFG11	ClassH Minimum boost level in Voltage	CLS_H_CFG11 (page=0x03 address=0x76) [reset=2h]
0x77	CLS_H_CFG12	ClassH Minimum boost level in Voltage	CLS_H_CFG12 (page=0x03 address=0x77) [reset=0h]

8.5.5 Register Summary Table Page=0x04

Addr	Register	Description	Section
0x00	PAGE4	Device Page	PAGE4 (page=0x04 address=0x00) [reset=0h]
0x18	LD_CFG8	Load Resistance Value after load diagnostics is completed	LD_CFG8 (page=0x04 address=0x18) [reset=0h]
0x19	LD_CFG9	Load Resistance Value after load diagnostics is completed	LD_CFG9 (page=0x04 address=0x19) [reset=0h]
0x1A	LD_CFG10	Load Resistance Value after load diagnostics is completed	LD_CFG10 (page=0x04 address=0x1A) [reset=0h]
0x1B	LD_CFG11	Load Resistance Value after load diagnostics is completed	LD_CFG11 (page=0x04 address=0x1B) [reset=0h]
0x58	TF_CFG4	Thermal foldback hold count (samples)	TF_CFG4 (page=0x04 address=0x58) [reset=0h]
0x59	TF_CFG5	Thermal foldback hold count (samples)	TF_CFG5 (page=0x04 address=0x59) [reset=0h]
0x5A	TF_CFG6	Thermal foldback hold count (samples)	TF_CFG6 (page=0x04 address=0x5A) [reset=0h]
0x5B	TF_CFG7	Thermal foldback hold count (samples)	TF_CFG7 (page=0x04 address=0x5B) [reset=64h]
0x5C	TF_CFG8	Thermal foldback limiter release rate (db/samples)	TF_CFG8 (page=0x04 address=0x5C) [reset=40h]
0x5D	TF_CFG9	Thermal foldback limiter release rate (db/samples)	TF_CFG9 (page=0x04 address=0x5D) [reset=BDh]
0x5E	TF_CFG10	Thermal foldback limiter release rate (db/samples)	TF_CFG10 (page=0x04 address=0x5E) [reset=B7h]
0x5F	TF_CFG11	Thermal foldback limiter release rate (db/samples)	TF_CFG11 (page=0x04 address=0x5F) [reset=B0h]
0x60	TF_CFG12	Thermal foldback limiter temperature threshold	TF_CFG12 (page=0x04 address=0x60) [reset=39h]
0x61	TF_CFG13	Thermal foldback limiter temperature threshold	TF_CFG13 (page=0x04 address=0x61) [reset=82h]
0x62	TF_CFG14	Thermal foldback limiter temperature threshold	TF_CFG14 (page=0x04 address=0x62) [reset=60h]
0x63	TF_CFG16	Thermal foldback limiter temperature threshold	TF_CFG16 (page=0x04 address=0x63) [reset=7Fh]
0x64	TF_CFG17	Thermal foldback max gain reduction (dB)	TF_CFG17 (page=0x04 address=0x64) [reset=2Dh]
0x65	TF_CFG18	Thermal foldback max gain reduction (dB)	TF_CFG18 (page=0x04 address=0x65) [reset=6Ah]
0x66	TF_CFG19	Thermal foldback max gain reduction (dB)	TF_CFG19 (page=0x04 address=0x66) [reset=86h]
0x67	TF_CFG20	Thermal foldback max gain reduction (dB)	TF_CFG20 (page=0x04 address=0x67) [reset=6Fh]
0x6C	DVC_SR1	Volume Control slew rate for 16kHz fs	DVC_SR1 (page=0x04 address=0x6C) [reset=2h]
0x6D	DVC_SR2	Volume Control slew rate for 16kHz fs	DVC_SR2 (page=0x04 address=0x6D) [reset=79h]
0x6E	DVC_SR3	Volume Control slew rate for 16kHz fs	DVC_SR3 (page=0x04 address=0x6E) [reset=CAh]
0x6F	DVC_SR4	Volume Control slew rate for 16kHz fs	DVC_SR4 (page=0x04 address=0x6F) [reset=5Eh]
0x70	CD_CFG1	Class D gain	CD_CFG1 (page=0x04 address=0x70) [reset=56h]
0x71	CD_CFG2	Class D gain	CD_CFG2 (page=0x04 address=0x71) [reset=B7h]
0x72	CD_CFG3	Class D gain	CD_CFG3 (page=0x04 address=0x72) [reset=96h]
0x73	CD_CFG4	Class D gain	CD_CFG4 (page=0x04 address=0x73) [reset=FFh]

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8.5.6 PAGE0 (page=0x00 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

Table 116. Device Page Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.5.7 SW_RESET (page=0x00 address=0x01) [reset=1h]

Asserting Software Reset will place all register values in their default POR (Power on Reset) state.

Table 117. Software Reset Field Descriptions

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0h	Reserved
0	SW_RESET	RW	1h	Software reset. Bit is self clearing. 0b = Don't reset 1b = Reset

8.5.8 PWR_CTL (page=0x00 address=0x02) [reset=8Eh]

Sets device's mode of operation and power down of IV sense blocks.

Table 118. Power Control Field Descriptions

Bit	Field	Type	Reset	Description
7	VSNS2_PD	RW	1h	Voltage sense power down. 0b = voltage sense is active 1b = Voltage sense is powered down
6	LDG_MODE	RW	0h	Load Diagnostic is 0b = Not Running 1b = Running (self clearing)
5	Reserved	RW	0h	Reserved
4	Reserved	RW	0h	Reserved
3	ISNS_PD	RW	1h	Current sense power down. 0b = Current sense active 1b = Current sense is powered down
2	VSNS_PD	RW	1h	Voltage sense power down. 0b = voltage sense is active 1b = Voltage sense is powered down
1-0	MODE[1:0]	RW	2h	Device operational mode. 00b = Active 01b = Mute 10b = Software Shutdown 11b = Load Diagnostics

8.5.9 PB_CFG1 (page=0x00 address=0x03) [reset=20h]

Sets playback high pass filter corner (PCM playback only).

Table 119. Playback Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_SPKR_mode	RW	0h	Register write option for the device to go into Low Noise mode 0b = SPKR Mode [Normal Mode, 17.5 dB] 1b = RX Mode [Low Noise Mode, 5.8 dB]

Table 119. Playback Configuration 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	HPF_EN	RW	0h	Disable DC Blocker 0b = Enabled 1b = Disabled
5-1	AMP_LEVEL[4:0]	RW	10h	1Dh-1Fh - Reserved 01h = 10.0 dBV (4.58 Vpk) 02h = 10.5 dBV (4.85 Vpk) 03h = 11.0 dBV (5.13 Vpk) 04h = 11.5 dBV (5.44 Vpk) 05h = 12.0 dBV (5.76 Vpk) 06h = 12.5 dBV (6.1 Vpk) 07h = 13.0 dBV (6.46 Vpk) 08h = 13.5 dBV (6.85 Vpk) 09h = 14.0 dBV (7.25 Vpk) 0Ah = 14.5 dBV (7.68 Vpk) 0Bh = 15.0 dBV (8.14 Vpk) 0Ch = 15.5 dBV (8.62 Vpk) 0Dh = 16.0 dBV (9.13 Vpk) 0Eh = 16.5 dBV (9.67 Vpk) 0Fh = 17.0 dBV (10.25 Vpk) 10h = 17.5 dBV (10.85 Vpk) 11h = 18.0 dBV (11.5 Vpk) 12h = 18.5 dBV (12.18 Vpk) 13h = 19.0 dBV (12.9 Vpk) 14h = 19.5 dBV (13.66 Vpk) 15h = 20.0 dBV (14.47 Vpk) 16h = 20.5 dBV (15.33 Vpk) 17h = 21.0 dBV (16.24 Vpk) 18h = 21.5 dBV (17.2 Vpk) 19h = 22.0 dBV (18.22 Vpk) 1Ah = 22.5 dBV (19.3 Vpk) 1Bh = 23.0 dBV (20.44 Vpk) 1Ch = 23.5 dBV (21.65 Vpk) 1Dh-1Fh - Reserved
0	Reserved	RW	0h	Reserved

8.5.10 MISC_CFG1 (page=0x00 address=0x04) [reset=C6h]

Sets OTE/OCE retry, IRQZ pull up, and amp spread spectrum.

Table 120. Misc Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	1h	Reserved
6	Reserved	RW	1h	Reserved
5	OCE_RETRY	RW	0h	Retry after over current event. 0b = Do not retry 1b = Retry after 1.5 s
4	OTE_RETRY	RW	0h	Retry after over temperature event. 0b = Do not retry 1b = Retry after 1.5 s
3	IRQZ_PU	RW	0h	IRQZ internal pull up enable. 0b = Disabled 1b = Enabled
2	AMP_SS	RW	1h	Low EMI spread spectrum enable. 0b = Disabled 1b = Enabled
1-0	Reserved	RW	2h	Reserved

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8.5.11 MISC_CFG2 (page=0x00 address=0x05) [reset=22h]

Set shutdown, VBAT filter, and I2C options.

Table 121. Misc Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SDZ_MODE[1:0]	RW	0h	SDZ Mode configuration. 00b = Initiates normal shutdown; force shutdown after timeout 01b = Immediate force shutdown 10b = Normal shutdown only 11b = Reserved
5-4	SDZ_TIMEOUT[1:0]	RW	2h	SDZ Timeout value 00b = 2 ms 01b = 4 ms 10b = 6 ms 11b = 23.8 ms
3	Reserved	RW	0h	Reserved
2	VBAT_FLT	RW	0h	VBAT filter into SAR ADC. 0b = 100kHz cut off 1b = Bypass
1	I2C_GBL_EN	RW	1h	I2C global address is 0b = Disabled 1b = Enabled
0	I2C_AD_DET	RW	0h	Re-detect I2C slave address (self clearing bit). 0b = normal 1b = Re-detect address

8.5.12 TDM_CFG0 (page=0x00 address=0x06) [reset=9h]

Sets the TDM frame start, TDM sample rate, TDM auto rate detection and whether rate is based on 44.1 kHz or 48 kHz frequency.

Table 122. TDM Configuration 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CLASSD_SYNC	RW	0h	Class-D synchronization mode. 0b = Not synchronized to audio clocks 1b = Synchronized to audio clocks
5	RAMP_RATE	RW	0h	Sample rate based on 44.1kHz or 48kHz when CLASSD_SYNC=1. 0b = 48kHz 1b = 44.1kHz
4	AUTO_RATE	RW	0h	Auto detection of TDM sample rate. 0b = Enabled 1b = Disabled
3-1	SAMP_RATE[2:0]	RW	4h	Sample rate of the TDM bus. 000b = Reserved 001b = 14.7/16 kHz 010b = 22.05/24 kHz 011b = 29.4/32 kHz 100b = 44.1/48 kHz 101b = 88.2/96 kHz 110b = 176.4/192 kHz 111b = Reserved
0	FRAME_START	RW	1h	TDM frame start polarity. 0b = Low to High on FSYNC 1b = High to Low on FSYNC

8.5.13 TDM_CFG1 (page=0x00 address=0x07) [reset=2h]

Sets TDM RX justification, offset and capture edge.

Table 123. TDM Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	RX_JUSTIFY	RW	0h	TDM RX sample justification within the time slot. 0b = Left 1b = Right
5-1	RX_OFFSET[4:0]	RW	1h	TDM RX start of frame to time slot 0 offset (SBCLK cycles).
0	RX_EDGE	RW	0h	TDM RX capture clock polarity. 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK

8.5.14 TDM_CFG2 (page=0x00 address=0x08) [reset=Ah]

Sets TDM RX time slot select, word length and time slot length.

Table 124. TDM Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	IVMON_LEN[1:0]	RW	0h	Sets the current and voltage data to length of 00b = 16 bits 01b = 12 bits 10b = 8 bits 11b = Reserved
5-4	RX_SCFG[1:0]	RW	0h	TDM RX time slot select config. 00b = Mono with time slot equal to I2C address offset 01b = Mono left channel 10b = Mono right channel 11b = Stereo downmix (L+R)/2
3-2	RX_WLEN[1:0]	RW	2h	TDM RX word length. 00b = 16-bits 01b = 20-bits 10b = 24-bits 11b = 32-bits
1-0	RX_SLEN[1:0]	RW	2h	TDM RX time slot length. 00b = 16-bits 01b = 24-bits 10b = 32-bits 11b = Reserved

8.5.15 TDM_CFG3 (page=0x00 address=0x09) [reset=10h]

Sets TDM RX left and right time slots.

Table 125. TDM Configuration 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RX_SLOT_R[3:0]	RW	1h	TDM RX Right Channel Time Slot.
3-0	RX_SLOT_L[3:0]	RW	0h	TDM RX Left Channel Time Slot.

8.5.16 TDM_CFG4 (page=0x00 address=0x0A) [reset=13h]

Sets TDM TX bus keeper, fill, offset and transmit edge.

Table 126. TDM Configuration 4 Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_KEEPCY	RW	0h	TDM TX SDOUT LSB data will be driven for 0b = full-cycle 1b = half-cycle

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Table 126. TDM Configuration 4 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TX_KEEPLN	RW	0h	TDM TX SDOUT will hold the bus for the following when TX_KEEPEN is enabled 0b = 1 LSB cycle 1b = always
5	TX_KEEPEN	RW	0h	TDM TX SDOUT bus keeper enable. 0b = Disable bus keeper 1b = Enable bus keeper
4	TX_FILL	RW	1h	TDM TX SDOUT unused bitfield fill. 0b = Transmit 0 1b = Transmit Hi-Z
3-1	TX_OFFSET[2:0]	RW	1h	TDM TX start of frame to time slot 0 offset.
0	TX_EDGE	RW	1h	TDM TX launch clock polarity. 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK

8.5.17 TDM_CFG5 (page=0x00 address=0x0B) [reset=2h]

Sets TDM TX V-Sense time slot and enable.

Table 127. TDM Configuration 5 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	VSNS_TX	RW	0h	TDM TX voltage sense transmit enable. 0b = Disabled 1b = Enabled
5-0	VSNS_SLOT[5:0]	RW	2h	TDM TX voltage sense time slot.

8.5.18 TDM_CFG6 (page=0x00 address=0x0C) [reset=0h]

Sets TDM TX I-Sense time slot and enable.

Table 128. TDM Configuration 6 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	ISNS_TX	RW	0h	TDM TX current sense transmit enable. 0b = Disabled 1b = Enabled
5-0	ISNS_SLOT[5:0]	RW	0h	TDM TX current sense time slot.

8.5.19 TDM_CFG7 (page=0x00 address=0x0D) [reset=4h]

Sets TDM TX VBAT time slot and enable.

Table 129. TDM Configuration 7 Field Descriptions

Bit	Field	Type	Reset	Description
7	VBAT_SLEN	RW	0h	TDM TX VBAT time slot length. 0b = Truncate to 8-bits 1b = Left justify to 16-bits
6	VBAT_TX	RW	0h	TDM TX VBAT transmit enable. 0b = Disabled 1b = Enabled
5-0	VBAT_SLOT[5:0]	RW	4h	TDM TX VBAT time slot.

8.5.20 TDM_CFG8 (page=0x00 address=0x0E) [reset=5h]

Sets TDM TX temp time slot and enable.

Table 130. TDM Configuration 8 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	TEMP_TX	RW	0h	TDM TX temp sensor transmit enable. 0b = Disabled 1b = Enabled
5-0	TEMP_SLOT[5:0]	RW	5h	TDM TX temp sensor time slot.

8.5.21 TDM_CFG9 (page=0x00 address=0x0F) [reset=6h]

Sets ICLA bus, TDM TX limiter gain reduction time slot and enable.

Table 131. TDM Configuration 9 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	GAIN_TX	RW	0h	TDM TX limiter gain reduction transmit enable. 0b = Disabled 1b = Enabled
5-0	GAIN_SLOT[5:0]	RW	6h	TDM TX limiter gain reduction time slot.

8.5.22 TDM_CFG10 (page=0x00 address=0x10) [reset=7h]

Sets boost current limiter slot and enable

Table 132. TDM Configuration 10 Field Descriptions

Bit	Field	Type	Reset	Description
7	BST_TX	RW	0h	TDM TX boost current limiter enable. 0b = Disabled 1b = Enabled
6	BST_SYNC_TX	RW	0h	TDM TX boost clock sync enable. 0b = Disabled 1b = Enabled
5-0	BST_SLOT[5:0]	RW	7h	TDM TX boost sync and current limit time slot.

8.5.23 TDM_DET (page=0x00 address=0x11) [reset=7Fh]

Readback of internal auto-rate detection.

Table 133. TDM Clock detection monitor Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6-3	FS_RATIO[3:0]	R	Fh	Detected SBCLK to FSYNC ratio. 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 0Bh-0Eh = Reserved 0F = Invalid ratio

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Table 133. TDM Clock detection monitor Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	FS_RATE[2:0]	R	7h	Detected sample rate of TDM bus. 000b = Reserved 001b = 14.7/16 KHz 010b = 22.05/24 KHz 011b = 29.4/32 KHz 100b = 44.1/48 KHz 101b = 88.2/96 kHz 110b = 176.4/192 kHz 111b = Error condition

8.5.24 LIM_CFG_0 (page=0x00 address=0x12) [reset=12h]

Sets Limiter attack step size, attack rate and enable.

Table 134. Limiter Configuration 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	VBAT_LIM_TH_SELECTION	RW	0h	Select source of threshold for VBAT based limiting 0b = User configured Thresholds 1b = PVDD based thresholds
5-4	LIMB_ATK_ST[1:0]	RW	1h	VBAT Limiter/ICLA attack step size. 00b = 0.25 dB 01b = 0.5 dB 10b = 1 dB 11b = 2 dB
3-1	LIMB_ATK_RT[2:0]	RW	1h	VBAT Limiter/ICLA attack rate. 000b = 1 step in 1 sample 001b = 1 step in 2 samples 010b = 1 step in 4 samples 011b = 1 step in 8 samples 100b = 1 step in 16 samples 101b = 1 step in 32 samples 110b = 1 step in 64 samples 111b = 1 step in 128 samples
0	LIMB_EN	RW	0h	Limiter enable. 0b = Disabled 1b = Enabled

8.5.25 LIM_CFG_1 (page=0x00 address=0x13) [reset=76h]

Sets VBAT limiter release step size, release rate and hold time.

Table 135. Limiter Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIMB_RLS_ST[1:0]	RW	1h	VBAT Limiter/BOP/ICLA release step size. 00b = 0.25 dB 01b = 0.5 dB 10b = 1 dB 11b = 2 dB
5-3	LIMB_RLS_RT[2:0]	RW	6h	VBAT Limiter/BOP/ICLA release rate. 000b = 1 step in 10 samples 001b = 1 step in 20 samples 010b = 1 step in 40 samples 011b = 1 step in 80 samples 100b = 1 step in 160 samples 101b = 1 step in 320 samples 110b = 1 step in 640 samples 111b = 1 step in 1280 samples

Table 135. Limiter Configuration 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	LIMB_HLD_TM[2:0]	RW	6h	VBAT Limiter hold time in samples. 000b = 0 samples 001b = 1920 samples 010b = 4800 samples 011b = 9600 samples 100b = 19200 samples 101b = 48000 samples 110b = 96000 samples 111b = 192000 samples

8.5.26 BOP_CFG_0 (page=0x00 address=0x14) [reset=1h]

Sets BOP infinite hold clear, infinite hold enable, mute on brown out and enable.

Table 136. Brown Out Prevention 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved
4	BOSD_EN	RW	0h	Brown out prevention shutdown enable. 0b = Disabled 1b = Enabled
3	BOP_HLD_CLR	RW	0h	BOP infinite hold clear (self clearing). 0b = Don't clear 1b = Clear
2	BOP_INF_HLD	RW	0h	Infinite hold on brown out event. 0b = Use BOP_HLD_TM after brown out event 1b = Don't release until BOP_HLD_CLR is asserted high
1	BOP_MUTE	RW	0h	Mute on brown out event. 0b = Don't mute 1b = Mute followed by device shutdown
0	BOP_EN	RW	1h	Brown out prevention enable. 0b = Disabled 1b = Enabled

8.5.27 BOP_CFG_1 (page=0x00 address=0x15) [reset=2Eh]

BOP attack rate, attack step size and hold time.

Table 137. Brown Out Prevention 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT[2:0]	RW	1h	Brown out prevention attack rate. 000b = 1 step in 1 sample 001b = 1 step in 2 samples 010b = 1 step in 4 samples 011b = 1 step in 8 samples 100b = 1 step in 16 samples 101b = 1 step in 32 samples 110b = 1 step in 64 samples 111b = 1 step in 128 samples
4-3	BOP_ATK_ST[1:0]	RW	1h	Brown out prevention attack step size. 00b = 0.5 dB 01b = 1 dB 10b = 1.5 dB 11b = 2 dB

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Table 137. Brown Out Prevention 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BOP_HLD_TM[2:0]	RW	6h	Brown out prevention hold time. 000b = 0 samples 001b = 1920 samples 010b = 4800 samples 011b = 9600 samples 100b = 19200 samples 101b = 48000 samples 110b = 96000 samples 111b = 192000 samples

8.5.28 GAIN_ICLA_CFG0 (page=0x00 address=0x18) [reset=Ch]

ICLA starting time slot and enable.

Table 138. Inter Chip Limiter Alignment 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6-1	ICLA_GAIN_SLOT[5:0]	RW	6h	Inter chip limiter alignment gain starting time slot.
0	ICLA_GAIN_EN	RW	0h	Inter chip limiter alignment gain enable. 0b = Disabled 1b = Enabled

8.5.29 ICLA_CFG1 (page=0x00 address=0x19) [reset=0h]

ICLA time slot enables.

Table 139. Inter Chip Limiter Alignment 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	ICLA_GAIN_SEN[3]	RW	0h	Time slot equals ICLA_GAIN_SLOT[5:0]+3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
6	ICLA_GAIN_SEN[2]	RW	0h	Time slot equals ICLA_GAIN_SLOT[5:0]+2. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
5	ICLA_GAIN_SEN[1]	RW	0h	Time slot equals ICLA_GAIN_SLOT[5:0]+1. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
4	ICLA_GAIN_SEN[0]	RW	0h	Time slot equals ICLA_GAIN_SLOT[5:0]+0. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
3	Reserved	RW	0h	Reserved
2	Reserved	RW	0h	Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	RW	0h	Reserved

8.5.30 INT_MASK0 (page=0x00 address=0x1A) [reset=FCh]

Interrupt masks.

Table 140. Interrupt Mask 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK[7]	RW	1h	Limiter mute mask. 0b = Don't Mask 1b = Mask

Table 140. Interrupt Mask 0 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT_MASK[6]	RW	1h	Limiter infinite hold mask. 0b = Don't Mask 1b = Mask
5	INT_MASK[5]	RW	1h	Limiter max attenuation mask. 0b = Don't Mask 1b = Mask
4	INT_MASK[4]	RW	1h	VBAT below limiter inflection point mask. 0b = Don't Mask 1b = Mask
3	INT_MASK[3]	RW	1h	Limiter active mask. 0b = Don't Mask 1b = Mask
2	INT_MASK[2]	RW	1h	TDM clock error mask. 0b = Don't Mask 1b = Mask
1	INT_MASK[1]	RW	0h	Over current error mask. 0b = Don't Mask 1b = Mask
0	INT_MASK[0]	RW	0h	Over temp error mask. 0b = Don't Mask 1b = Mask

8.5.31 INT_MASK1 (page=0x00 address=0x1B) [reset=A6h]

Interrupt masks.

Table 141. Interrupt Mask 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	RW	1h	Reserved
6	Reserved	RW	0h	Reserved
5	INT_MASK[13]	RW	1h	Load Diagnostic Completion Mask 0b = Don't Mask 1b = Masked
4-3	INT_MASK[12_11]	RW	0h	Speaker open load mask 00b = Don't Mask 01b = Mask open Load detection 10b = Mask Short Load detection 11b = Mask both Open,Short Load detection
2	INT_MASK[10]	RW	1h	Brownout device power down start mask 0b = Don't Mask 1b = Mask
1	INT_MASK[9]	RW	1h	Brownout Protection Active mask 0b = Don't Mask 1b = Mask
0	INT_MASK[8]	RW	0h	VBAT Brown out detected mask 0b = Don't Mask 1b = Mask

8.5.32 INT_MASK6 (page=0x00 address=0x1E) [reset=80h]

Interrupt Mask 6- Interrupt masks.

Table 142. Interrupt Mask 6- Interrupt masks. Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK6[7]	RW	1h	DSP DC detect flag mask 0b = Don't Mask 1b = Mask
6	Reserved	R	0h	Reserved

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Table 142. Interrupt Mask 6- Interrupt masks. Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Reserved	R	0h	Reserved
4	Reserved	R	0h	Reserved
3	Reserved	R	0h	Reserved
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

8.5.33 INT_LTCH0 (page=0x00 address=0x24) [reset=0h]

Latched interrupt readback.

Table 143. Latched Interrupt Readback 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0[7]	R	0h	Interrupt due to limiter mute. 0b = No interrupt 1b = Interrupt
6	INT_LTCH0[6]	R	0h	Interrupt due to limiter infinite hold. 0b = No interrupt 1b = Interrupt
5	INT_LTCH0[5]	R	0h	Interrupt due to limiter max attenuation. 0b = No interrupt 1b = Interrupt
4	INT_LTCH0[4]	R	0h	Interrupt due to VBAT below limiter inflection point. 0b = No interrupt 1b = Interrupt
3	INT_LTCH0[3]	R	0h	Interrupt due to limiter active 0b = No interrupt 1b = Interrupt
2	INT_LTCH0[2]	R	0h	Interrupt due to TDM clock error 0b = No interrupt 1b = Interrupt
1	INT_LTCH0[1]	R	0h	Interrupt due to over current error 0b = No interrupt 1b = Interrupt
0	INT_LTCH0[0]	R	0h	Interrupt due to over temp error 0b = No interrupt 1b = Interrupt

8.5.34 INT_LTCH1 (page=0x00 address=0x25) [reset=0h]

Latched interrupt readback.

Table 144. Latched Interrupt Readback 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	Reserved	R	0h	Reserved
5	INT_LTCH1[5]	R	0h	Interrupt due to load diagnostic completion. 0b = Not completed 1b = Completed
4-3	INT_LTCH1[4_3]	R	0h	Interrupt due to Load Diagnostic Mode Fault Status. 00b = Normal Load 01b = Open Load Detected 10b = Short Load Detected 11b = Reserved
2	INT_LTCH1[2]	R	0h	Interrupt due to Brownout Protection Triggered shutdown. 0b = No interrupt 1b = Interrupt

Table 144. Latched Interrupt Readback 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_LTCH1[1]	R	0h	Interrupt due to Brownout Protection Active flag. 0b = No interrupt 1b = Interrupt
0	INT_LTCH1[0]	R	0h	Interrupt due to VBAT brown out detected flag. 0b = No interrupt 1b = Interrupt

8.5.35 INT_LTCH6 (page=0x00 address=0x28) [reset=0h]

Latched interrupt readback.

Table 145. Latched Interrupt Readback 6 Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH6[7]	R	0h	Interrupt due to DSP DC detect flag 0b = No interrupt 1b = Interrupt
6	Reserved	R	0h	Reserved
5	Reserved	R	0h	Reserved
4	Reserved	R	0h	Reserved
3	Reserved	R	0h	Reserved
2	Reserved	R	0h	Reserved
1	Reserved	R	0h	Reserved
0	Reserved	R	0h	Reserved

8.5.36 VBAT_MSB (page=0x00 address=0x2A) [reset=0h]

MSBs of SAR ADC VBAT conversion.

Table 146. SAR ADC Conversion 0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VBAT_CNV_MEMRD[9:2]	R	0h	Returns SAR ADC VBAT conversion MSBs.

8.5.37 VBAT_LSB (page=0x00 address=0x2B) [reset=0h]

LSBs of SAR ADC VBAT conversion.

Table 147. SAR ADC Conversion 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VBAT_CNV_MEMRD[1:0]	R	0h	Returns SAR ADC VBAT conversion LSBs.
5-0	Reserved	R	0h	Reserved

8.5.38 TEMP (page=0x00 address=0x2C) [reset=0h]

SARD ADC Temp conversion.

Table 148. SAR ADC Conversion 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TMP_CNV_MEMRD[7:0]	R	0h	Returns SAR ADC temp sensor conversion.

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8.5.39 INT_CLK (page=0x00 address=0x30) [reset=19h]

Sets ASI clock error handeling and interrupt configuration.

Table 149. Interrupt and Clock Error Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_ERR_PWR_EN	RW	0h	Power up/down based on valid ASI clocks is 0b = Disable 1b = Enabled
6	CLK_HALT_EN	RW	0h	Put device to sleep(halt) after clock error lasts longer than CLK_HALT_TIMER is 0b = Enable 1b = Disable
5-3	CLK_HALT_TIMER[2:0]	RW	3h	If CLK_HALT_EN device will goto sleep after 000b = 1 ms 001b = 3.27 ms 010b = 26.21ms 011b = 52.42ms 100b = 104.85ms 101b = 209.71ms 110b = 419.43ms 111b = 838.86ms
2	INT_CLR_LTCH	RW	0h	Clear INT_LTCH registers 0b = Don't clear 1b = Clear (self clearing bit)
1-0	IRQZ_PIN_CFG[1:0]	RW	1h	IRQZ interrupt configuration. IRQZ will assert 00b = on any unmasked live interrupts 01b = on any unmasked latched interrupts 10b = for 2-4ms one time on any unmasked live interrupt event 11b = for 2-4ms every 4ms on any unmasked latched interrupts

8.5.40 DIN_PD (page=0x00 address=0x31) [reset=40h]

Sets enables of input pin weak pull down.

Table 150. Digital Input Pin Pull Down Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	Reserved	RW	1h	Reserved
5	DIN_PD[5]	RW	0h	Weak pull down for AD1. 0b = Disabled 1b = Enabled
4	DIN_PD[4]	RW	0h	Weak pull down for AD0. 0b = Disabled 1b = Enabled
3	DIN_PD[3]	RW	0h	Weak pull down for SDOUT. 0b = Disabled 1b = Enabled
2	DIN_PD[2]	RW	0h	Weak pull down for SDIN. 0b = Disabled 1b = Enabled
1	DIN_PD[1]	RW	0h	Weak pull down for FSYNC. 0b = Disabled 1b = Enabled
0	DIN_PD[0]	RW	0h	Weak pull down for SBCLK. 0b = Disabled 1b = Enabled

8.5.41 MISC_CFG3 (page=0x00 address=0x32) [reset=80h]

Set IRQZ pin active state

Table 151. Misc Configuration 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	IRQZ_POL	RW	1h	IRQZ pin polarity for interrupt. 0b = Active high (IRQ) 1b = Active low (IRQZ)
6-4	Reserved	RW	0h	Reserved
3-2	Reserved	R	0h	Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.5.42 BOOST_CFG1 (page=0x00 address=0x33) [reset=34h]

Boost Configure 1

Table 152. Boost Configure 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	BST_MODE	RW	0h	Boost Mode
6	BST_MODE	RW	0h	Boost Mode 00b = Class-H 01b = Class-G 10b = Always ON 11b = Always OFF(Passthrough)
5	BST_EN	RW	1h	Boost enable 0b = Disabled 1b = Enabled
4-3	Reserved	RW	2h	Reserved
2-1	BST_PFML[1:0]	RW	2h	Boost active mode PFM lower limit 00b = No lower limit 01b = 25 kHz 10b = 50 kHz 11b = 100 kHz
0	Reserved	RW	0h	Reserved

8.5.43 BOOST_CFG2 (page=0x00 address=0x34) [reset=40h]

Boost Configure 2

Table 153. Boost Configure 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BST_IR[1:0]	RW	1h	Boost inductor range 00b = less than 0.6 uH 01b = 0.6 uH to 1.3 uH 10b = 1.3 uH to 2.5 uH 11b = Reserved
5	Reserved	RW	0h	Reserved
4	Reserved	RW	0h	Reserved
3-0	Reserved	R	0h	Reserved

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8.5.44 BOOST_CFG3 (page=0x00 address=0x35) [reset=78h]

Boost Configure 3

Table 154. Boost Configure 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	7h	Reserved
3-2	BST_LR[1:0]	RW	2h	Slope of boost load regulation 00b = 4.4 A/V, load regulation = 0.914 V 01b = 3.67 A/V, load regulation = 1.095 V 10b = 2.93 A/V, load regulation = 1.37 V 11b = 1.95 A/V, load regulation = 2.056 V
1	Reserved	RW	0h	Reserved
0	Reserved	R	0h	Reserved

8.5.45 MISC_CFG4 (page=0x00 address=0x3D) [reset=8h]

Tone gen clocking, load diagnostic clocking, VI averaging.

Table 155. Misc Configuration 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	Clock source for tone generator beep mode 0b = External TDM 1b = Internal Oscillator
3	LDG_CLK	RW	0h	Clock source for load diagnostic 0b = External TDM 1b = Internal Oscillator
2-1	IVSNS_AVG[1:0]	RW	1h	Duration of Averaging done by the firmware on V/I data 00b = 5ms 01b = 10ms 10b = 50ms 11b = 100ms
0	Reserved	RW	0h	Reserved

8.5.46 TG_CFG0 (page=0x00 address=0x3F) [reset=0h]

Tone Generator

Table 156. Tone Generator Field Descriptions

Bit	Field	Type	Reset	Description
7-6	TG1_EN[1:0]	RW	0h	Tone Generator 1 is 00b = Disabled or pin triggered 01b = Enabled - play tone 10b = audio level enabled 11b = Reserved
5-4	TG1_PINEN[1:0]	RW	0h	Tone pin trigger 00b = Disabled 01b = SDIN 10b = Reserved 11b = AD1
3	TG2_EN	RW	0h	Tone Generator 2 is 0b = Disabled 1b = Enabled
2-0	Reserved	R	0h	Reserved

8.5.47 BOOST_CFG4 (page=0x00 address=0x40) [reset=79h]

Boost Configure 4

Table 157. Boost Configure 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BST_SSL[1:0]	RW	1h	Boost Soft Start Current Limit 00b = Disabled- no limit 01b = 1.2A 10b = 1.83A 11b = 2.44A
5-0	BST_ILIM[5:0]	RW	39h	Boost peak current limit 00h = 1.206 A 01h = 1.273 A 02h = 1.340 A ... 0x3Dh = 5.293 A 0x3Eh = 5.36 A 0x3Fh = 5.427A

8.5.48 TDM_CFG11 (page=0x00 address=0x41) [reset=48h]

Sets VSNS2 slot, enable and slot width

Table 158. TDM Configuration 11 Field Descriptions

Bit	Field	Type	Reset	Description
7	vsns2_tx	RW	0h	TDM TX VSNS2 transmit enable. 0b = Disabled 1b = Enabled
6	vsns2_slen	RW	1h	TDM TX VSNS2 time slot length. 0b = Truncate to 8-bits 1b = Left justify to 16-bits
5-0	vsns2_slot[5:0]	RW	8h	TDM TX VSNS2 time slot.

8.5.49 IO_DRV1 (page=0x00 address=0x42) [reset=0h]

PAD drain strength control 1

Table 159. PAD drain strength control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	bclk_ds[7:0]	RW	0h	Drain strength control register for AD1 pad 2b00 = 2mA drive setting 2b01 = 4mA drive setting 2b10 = 6mA drive setting 2b11 = 8mA drive setting

8.5.50 IO_DRV2 (page=0x00 address=0x43) [reset=0h]

PAD drain strength control 2

Table 160. PAD drain strength control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	dout_ds[7:0]	RW	0h	Drain strength control register for SDZ pad 2b00 = 2mA drive setting 2b01 = 4mA drive setting 2b10 = 6mA drive setting 2b11 = 8mA drive setting

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8.5.51 IO_DRV3 (page=0x00 address=0x44) [reset=0h]

PAD drain strength control 3

Table 161. PAD drain strength control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	sda_ds[7:0]	RW	0h	Reserved

8.5.52 MISC_CFG5 (page=0x00 address=0x48) [reset=A0h]

Boost and Class-D Settings

Table 162. Boost and Class-D Settings Field Descriptions

Bit	Field	Type	Reset	Description
7-3	BST_VREG[4:0]	RW	14h	Boost Maximum Voltage (Default 12.5V) 00000b - 00110 = RESERVED 00111b = 6V 01000b = 6.5V 01001b = 7V ..... 10110b = 13.5V 10111b - 11111b = RESERVED
2	Reserved	RW	0h	Reserved
1	Reserved	RW	0h	Reserved
0	Reserved	RW	0h	Reserved

8.5.53 REV_ID (page=0x00 address=0x7D) [reset=0h]

Returns REV and PG ID.

Table 163. Revision and PG ID Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID[3:0]	R	0h	Returns the revision ID.
3-0	PG_ID[3:0]	R	0h	Returns the PG ID.

8.5.54 I2C_CKSUM (page=0x00 address=0x7E) [reset=0h]

Returns I2C checksum.

Table 164. I2C Checksum Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	RW	0h	Returns I2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages.

8.5.55 BOOK (page=0x00 address=0x7F) [reset=0h]

Device's memory map is divided into pages and books. This register sets the book.

Table 165. Device Book Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOOK[7:0]	RW	0h	Sets the device book. 00h = Book 0 01h = Book 1 ... FFh = Book 255

8.5.56 PAGE1 (page=0x01 address=0x00) [reset=0h]

Device Page

Table 166. Device Page Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.5.57 TF_CFG (page=0x01 address=0x08) [reset=0h]

Set the enable for thermal foldback

Table 167. Thermal Folder Configure Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	TF_EN	RW	0h	Thermal Foldback is 0 = Disabled 1 = Enabled
5-0	Reserved	RW	0h	Reserved

8.5.58 LDG_CFG2 (page=0x01 address=0x24) [reset=0h]

Set number of iternations

Table 168. Load Diagnostic 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	Reserved
3-0	LDG_ITRC[3:0]	RW	0h	Iterations of Load diagnostic mode 0000b = One time 0001b = Two times 0010b = Three times ... 1111b = Sixteen times

8.5.59 PAGE2 (page=0x02 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

Table 169. Device Page Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.5.60 DVC_CFG1 (page=0x02 address=0x0C) [reset=40h]

Sets playback volume for PCM playback path.

Table 170. Digital Volume Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_PCM[31:24]	RW	40h	round(10^(volume in dB/20)*2^30)

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8.5.61 DVC_CFG2 (page=0x02 address=0x0D) [reset=0h]

Sets playback volume for PCM playback path.

Table 171. Digital Volume Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_PCM[23:16]	RW	0h	round(10^(volume in dB/20)*2^30)

8.5.62 DVC_CFG3 (page=0x02 address=0x0E) [reset=0h]

Sets playback volume for PCM playback path.

Table 172. Digital Volume Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_PCM[15:8]	RW	0h	round(10^(volume in dB/20)*2^30)

8.5.63 DVC_CFG4 (page=0x02 address=0x0F) [reset=0h]

Sets playback volume for PCM playback path.

Table 173. Digital Volume Control 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_PCM[7:0]	RW	0h	round(10^(volume in dB/20)*2^30)

8.5.64 DVC_CFG5 (page=0x02 address=0x10) [reset=3h]

Sets ramp rate for volume control

Table 174. Digital Volume Control 5 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_RAMP[31:24]	RW	3h	round((1-exp(-1/(0.2*fs*time in seconds)))*2^31)

8.5.65 DVC_CFG6 (page=0x02 address=0x11) [reset=4Ah]

Sets ramp rate for volume control

Table 175. Digital Volume Control 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_RAMP[23:16]	RW	4Ah	round((1-exp(-1/(0.2*fs*time in seconds)))*2^31)

8.5.66 DVC_CFG7 (page=0x02 address=0x12) [reset=51h]

Sets ramp rate for volume control

Table 176. Digital Volume Control 7 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_RAMP[15:8]	RW	51h	round((1-exp(-1/(0.2*fs*time in seconds)))*2^31)

8.5.67 DVC_CFG8 (page=0x02 address=0x13) [reset=6Ch]

Sets ramp rate for volume control

Table 177. Digital Volume Control 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_RAMP[7:0]	RW	6Ch	round((1-exp(-1/(0.2*fs*time in seconds)))*2^31)

8.5.68 LIM_CFG1 (page=0x02 address=0x14) [reset=2Dh]

Sets limiter max attenuation

Table 178. Limiter Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIM_MAX_ATN[31:24]	RW	2Dh	round(10^(max attn dB/20)*2^31)

8.5.69 LIM_CFG2 (page=0x02 address=0x15) [reset=6Ah]

Limiter Configuration 2- Sets limiter max attenuation

Table 179. Limiter Configuration 2- Sets limiter max attenuation Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIM_MAX_ATN[23:16]	RW	6Ah	round(10^(max attn dB/20)*2^31)

8.5.70 LIM_CFG3 (page=0x02 address=0x16) [reset=86h]

Limiter Configuration 3- Sets limiter max attenuation

Table 180. Limiter Configuration 3- Sets limiter max attenuation Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIM_MAX_ATN[15:8]	RW	86h	round(10^(max attn dB/20)*2^31)

8.5.71 LIM_CFG4 (page=0x02 address=0x17) [reset=6Fh]

Limiter Configuration 4- Sets limiter max attenuation

Table 181. Limiter Configuration 4- Sets limiter max attenuation Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIM_MAX_ATN[7:0]	RW	6Fh	round(10^(max attn dB/20)*2^31)

8.5.72 LIM_CFG5 (page=0x02 address=0x18) [reset=56h]

Sets VBAT Limiter max threshold.

Table 182. Limiter Configuration 5 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MAX[31:24]	RW	56h	round(lim max peak voltage*2^27)

8.5.73 LIM_CFG6 (page=0x02 address=0x19) [reset=B7h]

Sets VBAT Limiter max threshold.

Table 183. Limiter Configuration 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MAX[23:16]	RW	B7h	round(lim max peak voltage*2^27)

8.5.74 LIM_CFG7 (page=0x02 address=0x1A) [reset=96h]

Sets VBAT Limiter max threshold.

Table 184. Limiter Configuration 7 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MAX[15:8]	RW	96h	round(lim max peak voltage*2^27)

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8.5.75 LIM_CFG8 (page=0x02 address=0x1B) [reset=FFh]

Sets VBAT Limiter max threshold.

Table 185. Limiter Configuration 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MAX[7:0]	RW	FFh	round(lim max peak voltage*2^27)

8.5.76 LIM_CFG9 (page=0x02 address=0x1C) [reset=16h]

Sets VBAT limiter min threshold.

Table 186. Limiter Configuration 9 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MIN[31:24]	RW	16h	round(lim min peak voltage*2^27)

8.5.77 LIM_CFG10 (page=0x02 address=0x1D) [reset=66h]

Sets VBAT limiter min threshold.

Table 187. Limiter Configuration 10 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MIN[23:16]	RW	66h	round(lim min peak voltage*2^27)

8.5.78 LIM_CFG11 (page=0x02 address=0x1E) [reset=66h]

Sets VBAT limiter min threshold.

Table 188. Limiter Configuration 11 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MIN[15:8]	RW	66h	round(lim min peak voltage*2^27)

8.5.79 LIM_CFG12 (page=0x02 address=0x1F) [reset=66h]

Sets VBAT limiter min threshold.

Table 189. Limiter Configuration 12 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_TH_MIN[7:0]	RW	66h	round(lim min peak voltage*2^27)

8.5.80 LIM_CFG13 (page=0x02 address=0x20) [reset=34h]

Sets VBAT limiter inflection point.

Table 190. Limiter Configuration 13 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_INF_PT[31:24]	RW	34h	round(Vbat at inflection point*2^28)

8.5.81 LIM_CFG14 (page=0x02 address=0x21) [reset=CCh]

Sets VBAT limiter inflection point.

Table 191. Limiter Configuration 14 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_INF_PT[23:16]	RW	CCh	round(Vbat at inflection point*2^28)

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8.5.82 LIM_CFG15 (page=0x02 address=0x22) [reset=CCh]

Sets VBAT limiter inflection point.

Table 192. Limiter Configuration 15 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_INF_PT[15:8]	RW	CCh	round(Vbat at inflection point*2^28)

8.5.83 LIM_CFG16 (page=0x02 address=0x23) [reset=CDh]

Sets VBAT limiter inflection point.

Table 193. Limiter Configuration 16 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_INF_PT[7:0]	RW	CDh	round(Vbat at inflection point*2^28)

8.5.84 LIM_CFG17 (page=0x02 address=0x24) [reset=10h]

Sets VBAT limiter slope

Table 194. Limiter Configuration 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_SLOPE[31:24]	RW	10h	round(slope*2^28)

8.5.85 LIM_CFG18 (page=0x02 address=0x25) [reset=0h]

Sets VBAT limiter slope

Table 195. Limiter Configuration 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_SLOPE[23:16]	RW	0h	round(slope*2^28)

8.5.86 LIM_CFG19 (page=0x02 address=0x26) [reset=0h]

Sets VBAT limiter slope

Table 196. Limiter Configuration 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_SLOPE[15:8]	RW	0h	round(slope*2^28)

8.5.87 LIM_CFG20 (page=0x02 address=0x27) [reset=0h]

Sets VBAT limiter slope

Table 197. Limiter Configuration 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LIMB_SLOPE[7:0]	RW	0h	round(slope*2^28)

8.5.88 BOP_CFG1 (page=0x02 address=0x28) [reset=2Eh]

BOP threshold.

Table 198. Brown Out Prevention 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOP_TH[31:24]	RW	2Eh	round(Vbat BOP threshold*2^28)

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8.5.89 BOP_CFG2 (page=0x02 address=0x29) [reset=66h]

BOP threshold.

Table 199. Brown Out Prevention 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOP_TH[23:16]	RW	66h	round(Vbat BOP threshold*2^28)

8.5.90 BOP_CFG3 (page=0x02 address=0x2A) [reset=66h]

BOP threshold.

Table 200. Brown Out Prevention 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOP_TH[15:8]	RW	66h	round(Vbat BOP threshold*2^28)

8.5.91 BOP_CFG4 (page=0x02 address=0x2B) [reset=66h]

BOP threshold.

Table 201. Brown Out Prevention 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOP_TH[7:0]	RW	66h	round(Vbat BOP threshold*2^28)

8.5.92 BOP_CFG5 (page=0x02 address=0x2C) [reset=2Bh]

BOSD threshold.

Table 202. Brown Out Prevention 5 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOSD_TH[31:24]	RW	2Bh	round(Vbat BOSD threshold*2^28)

8.5.93 BOP_CFG6 (page=0x02 address=0x2D) [reset=33h]

BOSD threshold.

Table 203. Brown Out Prevention 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOSD_TH[23:16]	RW	33h	round(Vbat BOSD threshold*2^28)

8.5.94 BOP_CFG7 (page=0x02 address=0x2E) [reset=33h]

BOSD threshold.

Table 204. Brown Out Prevention 7 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOSD_TH[15:8]	RW	33h	round(Vbat BOSD threshold*2^28)

8.5.95 BOP_CFG8 (page=0x02 address=0x2F) [reset=33h]

BOSD threshold.

Table 205. Brown Out Prevention 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOSD_TH[7:0]	RW	33h	round(Vbat BOSD threshold*2^28)

8.5.96 HPFC_CFG1 (page=0x02 address=0x30) [reset=7Fh]

HPF Biquad coefficients

Table 206. HPF Coefficient 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N0[31:24]	RW	7Fh	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.97 HPFC_CFG2 (page=0x02 address=0x31) [reset=FBh]

HPF Biquad coefficients

Table 207. HPF Coefficient 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N0[23:16]	RW	FBh	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.98 HPFC_CFG3 (page=0x02 address=0x32) [reset=B6h]

HPF Biquad coefficients

Table 208. HPF Coefficient 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N0[15:8]	RW	B6h	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.99 HPFC_CFG4 (page=0x02 address=0x33) [reset=14h]

HPF Biquad coefficients

Table 209. HPF Coefficient 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N0[7:0]	RW	14h	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.100 HPFC_CFG5 (page=0x02 address=0x34) [reset=80h]

HPF Biquad coefficients

Table 210. HPF Coefficient 5 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N1[31:24]	RW	80h	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.101 HPFC_CFG6 (page=0x02 address=0x35) [reset=4h]

HPF Biquad coefficients

Table 211. HPF Coefficient 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N1[23:16]	RW	4h	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.102 HPFC_CFG7 (page=0x02 address=0x36) [reset=49h]

HPF Biquad coefficients

Table 212. HPF Coefficient 7 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N1[15:8]	RW	49h	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

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8.5.103 HPFC_CFG8 (page=0x02 address=0x37) [reset=ECh]

HPF Biquad coefficients

Table 213. HPF Coefficient 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_N1[7:0]	RW	ECh	[N, D] = butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.104 HPFC_CFG9 (page=0x02 address=0x38) [reset=7Fh]

HPF Biquad coefficients

Table 214. HPF Coefficient 9 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_D1[31:24]	RW	7Fh	[N, D] = butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.105 HPFC_CFG10 (page=0x02 address=0x39) [reset=7Fh]

HPF Biquad coefficients

Table 215. HPF Coefficient 10 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_D1[23:16]	RW	7Fh	[N, D] = butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.106 HPFC_CFG11 (page=0x02 address=0x3A) [reset=6Ch]

HPF Biquad coefficients

Table 216. HPF Coefficient 11 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_D1[15:8]	RW	6Ch	[N, D] = butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.107 HPFC_CFG12 (page=0x02 address=0x3B) [reset=28h]

HPF Biquad coefficients

Table 217. HPF Coefficient 12 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HPF_COEFF_D1[7:0]	RW	28h	[N, D] = butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.108 TG_CFG1 (page=0x02 address=0x3C) [reset=3Fh]

Tone Generator 1 Freq Calc 1

Table 218. Tone Generator 1 Freq Calc 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ1[31:24]	RW	3Fh	round((2*cos(2*pi*f_tone/fs))*2^29)

8.5.109 TG_CFG2 (page=0x02 address=0x3D) [reset=FFh]

Tone Generator 1 Freq Calc 1

Table 219. Tone Generator 1 Freq Calc 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ1[23:16]	RW	FFh	round((2*cos(2*pi*f_tone/fs))*2^29)

8.5.110 TG_CFG3 (page=0x02 address=0x3E) [reset=7Ah]

Tone Generator 1 Freq Calc 1

Table 220. Tone Generator 1 Freq Calc 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ1[15:8]	RW	7Ah	round((2*cos(2*pi*f_tone/fs))*2^29)

8.5.111 TG_CFG4 (page=0x02 address=0x3F) [reset=E3h]

Tone Generator 1 Freq Calc 1

Table 221. Tone Generator 1 Freq Calc 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ1[7:0]	RW	E3h	round((2*cos(2*pi*f_tone/fs))*2^29)

8.5.112 TG_CFG5 (page=0x02 address=0x40) [reset=1h]

Tone Generator 1 Freq Calc 2

Table 222. Tone Generator 1 Freq Calc 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ2[31:24]	RW	1h	round((sin(2*pi*f_tone/fs))*2^31)

8.5.113 TG_CFG6 (page=0x02 address=0x41) [reset=1h]

Tone Generator 1 Freq Calc 2

Table 223. Tone Generator 1 Freq Calc 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ2[23:16]	RW	1h	round((sin(2*pi*f_tone/fs))*2^31)

8.5.114 TG_CFG7 (page=0x02 address=0x42) [reset=5Bh]

Tone Generator 1 Freq Calc 2

Table 224. Tone Generator 1 Freq Calc 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ2[15:8]	RW	5Bh	round((sin(2*pi*f_tone/fs))*2^31)

8.5.115 TG_CFG8 (page=0x02 address=0x43) [reset=4Ch]

Tone Generator 1 Freq Calc 2

Table 225. Tone Generator 1 Freq Calc 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ2[7:0]	RW	4Ch	round((sin(2*pi*f_tone/fs))*2^31)

8.5.116 TG_CFG9 (page=0x02 address=0x44) [reset=0h]

Tone Generator 1 Freq Calc 3

Table 226. Tone Generator 1 Freq Calc 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ3[31:24]	RW	0h	(LCM(fs,f_tone)/f_tone) - 1

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8.5.117 TG_CFG10 (page=0x02 address=0x45) [reset=0h]

Tone Generator 1 Freq Calc 3

Table 227. Tone Generator 1 Freq Calc 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ3[23:16]	RW	0h	(LCM(fs,f_tone)/f_tone) - 1

8.5.118 TG_CFG11 (page=0x02 address=0x46) [reset=3h]

Tone Generator 1 Freq Calc 3

Table 228. Tone Generator 1 Freq Calc 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ3[15:8]	RW	3h	(LCM(fs,f_tone)/f_tone) - 1

8.5.119 TG_CFG12 (page=0x02 address=0x47) [reset=1Fh]

Tone Generator 1 Freq Calc 3

Table 229. Tone Generator 1 Freq Calc 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_FREQ3[7:0]	RW	1Fh	(LCM(fs,f_tone)/f_tone) - 1

8.5.120 TG_CFG13 (page=0x02 address=0x48) [reset=2h]

Tone Generator 1 Amplitude Calc

Table 230. Tone Generator 1 Amplitude Calc Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_AMP[31:24]	RW	2h	round(10^(tone amplitude dB/20)*2^31)

8.5.121 TG_CFG14 (page=0x02 address=0x49) [reset=46h]

Tone Generator 1 Amplitude Calc

Table 231. Tone Generator 1 Amplitude Calc Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_AMP[23:16]	RW	46h	round(10^(tone amplitude dB/20)*2^31)

8.5.122 TG_CFG15 (page=0x02 address=0x4A) [reset=B4h]

Tone Generator 1 Amplitude Calc

Table 232. Tone Generator 1 Amplitude Calc Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_AMP[15:8]	RW	B4h	round(10^(tone amplitude dB/20)*2^31)

8.5.123 TG_CFG16 (page=0x02 address=0x4B) [reset=E4h]

Tone Generator 1 Amplitude Calc

Table 233. Tone Generator 1 Amplitude Calc Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TG1_AMP[7:0]	RW	E4h	round(10^(tone amplitude dB/20)*2^31)

8.5.124 LD_CFG0 (page=0x02 address=0x5C) [reset=2h]

Load Diagnostics Resistance Upper Threshold

Table 234. Load Diagnostics Resistance Upper Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[31:24]	RW	2h	round((ohm/4.2424)*2^22)

8.5.125 LD_CFG1 (page=0x02 address=0x5D) [reset=80h]

Load Diagnostics Resistance Upper Threshold

Table 235. Load Diagnostics Resistance Upper Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[23:16]	RW	80h	round((ohm/4.2424)*2^22)

8.5.126 LD_CFG2 (page=0x02 address=0x5E) [reset=0h]

Load Diagnostics Resistance Upper Threshold

Table 236. Load Diagnostics Resistance Upper Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[15:8]	RW	0h	round((ohm/4.2424)*2^22)

8.5.127 LD_CFG3 (page=0x02 address=0x5F) [reset=0h]

Load Diagnostics Resistance Upper Threshold

Table 237. Load Diagnostics Resistance Upper Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[7:0]	RW	0h	round((ohm/4.2424)*2^22)

8.5.128 LD_CFG4 (page=0x02 address=0x60) [reset=0h]

Load Diagnostics Resistance Lower Threshold

Table 238. Load Diagnostics Resistance Lower Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[31:24]	RW	0h	round((ohm/4.2424)*2^22)

8.5.129 LD_CFG5 (page=0x02 address=0x61) [reset=19h]

Load Diagnostics Resistance Lower Threshold

Table 239. Load Diagnostics Resistance Lower Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[23:16]	RW	19h	round((ohm/4.2424)*2^22)

8.5.130 LD_CFG6 (page=0x02 address=0x62) [reset=99h]

Load Diagnostics Resistance Lower Threshold

Table 240. Load Diagnostics Resistance Lower Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[15:8]	RW	99h	round((ohm/4.2424)*2^22)

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8.5.131 LD_CFG7 (page=0x02 address=0x63) [reset=9Ah]

Load Diagnostics Resistance Lower Threshold

Table 241. Load Diagnostics Resistance Lower Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[7:0]	RW	9Ah	round((ohm/4.2424)*2^22)

8.5.132 IDC_CFG0 (page=0x02 address=0x64) [reset=0h]

Idle channel detection threshold

Table 242. Idle channel detection threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_DTH[31:24]	RW	0h	round(10^(idle channel threshold dB/20)*2^31)

8.5.133 IDC_CFG1 (page=0x02 address=0x65) [reset=20h]

Idle channel detection threshold

Table 243. Idle channel detection threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_DTH[23:16]	RW	20h	round(10^(idle channel threshold dB/20)*2^31)

8.5.134 IDC_CFG2 (page=0x02 address=0x66) [reset=C4h]

Idle channel detection threshold

Table 244. Idle channel detection threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_DTH[15:8]	RW	C4h	round(10^(idle channel threshold dB/20)*2^31)

8.5.135 IDC_CFG3 (page=0x02 address=0x67) [reset=9Ch]

Idle channel detection threshold

Table 245. Idle channel detection threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_DTH[7:0]	RW	9Ch	round(10^(idle channel threshold dB/20)*2^31)

8.5.136 IDC_CFG4 (page=0x02 address=0x68) [reset=2h]

MID Power Threshold

Table 246. MID Power Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_MTH[31:24]	RW	2h	round(10^(mid power mode threshold dB/20)*2^31)

8.5.137 IDC_CFG5 (page=0x02 address=0x69) [reset=46h]

MID Power Threshold

Table 247. MID Power Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_MTH[23:16]	RW	46h	round(10^(mid power mode threshold dB/20)*2^31)

8.5.138 IDC_CFG6 (page=0x02 address=0x6A) [reset=B4h]

MID Power Threshold

Table 248. MID Power Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_MTH[15:8]	RW	B4h	round(10^(mid power mode threshold dB/20)*2^31)

8.5.139 IDC_CFG7 (page=0x02 address=0x6B) [reset=E4h]

MID Power Threshold

Table 249. MID Power Threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_MTH[7:0]	RW	E4h	round(10^(mid power mode threshold dB/20)*2^31)

8.5.140 IDC_CFG8 (page=0x02 address=0x6C) [reset=0h]

Hystersis for idle channel detection

Table 250. Hystersis for idle channel detection Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_HYST[31:24]	RW	0h	round(time in seconds*fs)

8.5.141 IDC_CFG9 (page=0x02 address=0x6D) [reset=0h]

Hystersis for idle channel detection

Table 251. Hystersis for idle channel detection Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_HYST[23:16]	RW	0h	round(time in seconds*fs)

8.5.142 IDC_CFG10 (page=0x02 address=0x6E) [reset=12h]

Hystersis for idle channel detection

Table 252. Hystersis for idle channel detection Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_HYST[15:8]	RW	12h	round(time in seconds*fs)

8.5.143 IDC_CFG11 (page=0x02 address=0x6F) [reset=C0h]

Hystersis for idle channel detection

Table 253. Hystersis for idle channel detection Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IDC_HYST[7:0]	RW	C0h	round(time in seconds*fs)

8.5.144 IVHPFC_CFG1 (page=0x02 address=0x70) [reset=7Fh]

IVSENSE HPF N0 coefficient

Table 254. IVSENSE HPF N0 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N0[31:24]	RW	7Fh	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

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8.5.145 IVHPFC_CFG2 (page=0x02 address=0x71) [reset=FBh]

IVSENSE HPF N0 coefficient

Table 255. IVSENSE HPF N0 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N0[23:16]	RW	FBh	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.146 IVHPFC_CFG3 (page=0x02 address=0x72) [reset=B6h]

IVSENSE HPF N0 coefficient

Table 256. IVSENSE HPF N0 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N0[15:8]	RW	B6h	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.147 IVHPFC_CFG4 (page=0x02 address=0x73) [reset=14h]

IVSENSE HPF N0 coefficient

Table 257. IVSENSE HPF N0 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N0[7:0]	RW	14h	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(1)*2^31);

8.5.148 IVHPFC_CFG5 (page=0x02 address=0x74) [reset=80h]

IVSENSE HPF N1 coefficient

Table 258. IVSENSE HPF N1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N1[31:24]	RW	80h	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.149 IVHPFC_CFG6 (page=0x02 address=0x75) [reset=4h]

IVSENSE HPF N1 coefficient

Table 259. IVSENSE HPF N1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N1[23:16]	RW	4h	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.150 IVHPFC_CFG7 (page=0x02 address=0x76) [reset=49h]

IVSENSE HPF N1 coefficient

Table 260. IVSENSE HPF N1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N1[15:8]	RW	49h	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.151 IVHPFC_CFG8 (page=0x02 address=0x77) [reset=ECh]

IVSENSE HPF N1 coefficient

Table 261. IVSENSE HPF N1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_N1[7:0]	RW	ECh	[N, D] - butter(1, fc/(fs/2), 'high'); round(N(2)*2^31);

8.5.152 IVHPFC_CFG9 (page=0x02 address=0x78) [reset=7Fh]

IVSENSE HPF D1 coefficient

Table 262. IVSENSE HPF D1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_D1[31:24]	RW	7Fh	[N, D] - butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.153 IVHPFC_CFG10 (page=0x02 address=0x79) [reset=F7h]

IVSENSE HPF D1 coefficient

Table 263. IVSENSE HPF D1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_D1[23:16]	RW	F7h	[N, D] - butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.154 IVHPFC_CFG11 (page=0x02 address=0x7A) [reset=6Ch]

IVSENSE HPF D1 coefficient

Table 264. IVSENSE HPF D1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_D1[15:8]	RW	6Ch	[N, D] - butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.155 IVHPFC_CFG12 (page=0x02 address=0x7B) [reset=28h]

IVSENSE HPF D1 coefficient

Table 265. IVSENSE HPF D1 coefficient Field Descriptions

Bit	Field	Type	Reset	Description
7-0	IVHPF_D1[7:0]	RW	28h	[N, D] - butter(1, fc/(fs/2), 'high'); round(-D(2)*2^31);

8.5.156 TF_CFG_1 (page=0x02 address=0x7C) [reset=72h]

Thermal foldback limiter slope (in db/C)

Table 266. Thermal foldback limiter slope (in db/C) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[31:24]	RW	72h	round(10^(-slope/20)*2^31)

8.5.157 TF_CFG_2 (page=0x02 address=0x7D) [reset=14h]

Thermal foldback limiter slope (in db/C)

Table 267. Thermal foldback limiter slope (in db/C) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[23:16]	RW	14h	round(10^(-slope/20)*2^31)

8.5.158 TF_CFG_3 (page=0x02 address=0x7E) [reset=82h]

Thermal foldback limiter slope (in db/C)

Table 268. Thermal foldback limiter slope (in db/C) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[15:8]	RW	82h	round(10^(-slope/20)*2^31)

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8.5.159 TF_CFG_4 (page=0x02 address=0x7F) [reset=C0h]

Thermal foldback limiter slope (in db/C)

Table 269. Thermal foldback limiter slope (in db/C) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[7:0]	RW	C0h	round(10^(-slope/20)*2^31)

8.5.160 PAGE3 (page=0x03 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

Table 270. Device Page Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.5.161 DC_DET_THR1 (page=0x03 address=0x1C) [reset=18h]

Forward path DC detection threshold.

Table 271. DC detection threshold 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_THR[31:24]	RW	18h	round(dc_det_th*2^31)

8.5.162 DC_DET_THR2 (page=0x03 address=0x1D) [reset=2Ah]

Forward path DC detection threshold.

Table 272. DC detection threshold 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_THR[23:16]	RW	2Ah	round(dc_det_th*2^31)

8.5.163 DC_DET_THR3 (page=0x03 address=0x1E) [reset=FFh]

Forward path DC detection threshold.

Table 273. DC detection threshold 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_THR[15:8]	RW	FFh	round(dc_det_th*2^31)

8.5.164 DC_DET_THR4 (page=0x03 address=0x1F) [reset=53h]

Forward path DC detection threshold.

Table 274. DC detection threshold 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_THR[7:0]	RW	53h	round(dc_det_th*2^31)

8.5.165 DC_DET_HYST1 (page=0x03 address=0x20) [reset=0h]

DC detection hysteresis time 1

Table 275. DC detection hysteresis time 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_TIM[31:24]	RW	0h	round(time in seconds*fs)

8.5.166 DC_DET_HYST2 (page=0x03 address=0x21) [reset=0h]

DC detection hysteresis time 2

Table 276. DC detection hysteresis time 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_TIM[23:16]	RW	0h	round(time in seconds*fs)

8.5.167 DC_DET_HYST3 (page=0x03 address=0x22) [reset=27h]

DC detection hysteresis time 3

Table 277. DC detection hysteresis time 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_TIM[15:8]	RW	27h	round(time in seconds*fs)

8.5.168 DC_DET_HYST4 (page=0x03 address=0x23) [reset=10h]

DC detection hysteresis time 4

Table 278. DC detection hysteresis time 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DC_DET_TIM[7:0]	RW	10h	round(time in seconds*fs)

8.5.169 CLS_H_CFG1 (page=0x03 address=0x24) [reset=Ah]

slope (ClassD out to Vboost mapping)

Table 279. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_SLOPE[31:24]	RW	Ah	round(slope*2^27)

8.5.170 CLS_H_CFG2 (page=0x03 address=0x25) [reset=3Bh]

slope (ClassD out to Vboost mapping)

Table 280. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_SLOPE[23:16]	RW	3Bh	round(slope*2^27)

8.5.171 CLS_H_CFG3 (page=0x03 address=0x26) [reset=C7h]

slope (ClassD out to Vboost mapping)

Table 281. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_SLOPE[15:8]	RW	C7h	round(slope*2^27)

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8.5.172 CLS_H_CFG4 (page=0x03 address=0x27) [reset=DCh]

slope (ClassD out to Vboost mapping)

Table 282. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_SLOPE[7:0]	RW	DCh	round(slope*2^27)

8.5.173 CLS_H_CFG5 (page=0x03 address=0x28) [reset=0h]

Y - intercept (ClassD out to Vboost mapping)

Table 283. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_INTERCEPT[31:24]	RW	0h	round(intercept*2^27)

8.5.174 CLS_H_CFG6 (page=0x03 address=0x29) [reset=0h]

Y - intercept (ClassD out to Vboost mapping)

Table 284. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_INTERCEPT[23:16]	RW	0h	round(intercept*2^27)

8.5.175 CLS_H_CFG7 (page=0x03 address=0x2A) [reset=0h]

Y - intercept (ClassD out to Vboost mapping)

Table 285. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_INTERCEPT[15:8]	RW	0h	round(intercept*2^27)

8.5.176 CLS_H_CFG8 (page=0x03 address=0x2B) [reset=0h]

Y - intercept (ClassD out to Vboost mapping)

Table 286. ClassH Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_INTERCEPT[7:0]	RW	0h	round(intercept*2^27)

8.5.177 CLS_H_CFG9 (page=0x03 address=0x74) [reset=0h]

ClassH Minimum boost level in Voltage

Table 287. ClassH Minimum boost level in Voltage Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_MIN_LEVEL[31:24]	RW	0h	round((22*Voutmax-52)*2^8)

8.5.178 CLS_H_CFG10 (page=0x03 address=0x75) [reset=0h]

ClassH Minimum boost level in Voltage

Table 288. ClassH Minimum boost level in Voltage Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_MIN_LEVEL[23:16]	RW	0h	round((22*Voutmax-52)*2^8)

8.5.179 CLS_H_CFG11 (page=0x03 address=0x76) [reset=2h]

ClassH Minimum boost level in Voltage

Table 289. ClassH Minimum boost level in Voltage Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_MIN_LEVEL[15:8]	RW	2h	round((22*Voutmax-52)*2^8)

8.5.180 CLS_H_CFG12 (page=0x03 address=0x77) [reset=0h]

ClassH Minimum boost level in Voltage

Table 290. ClassH Minimum boost level in Voltage Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSH_MIN_LEVEL[7:0]	RW	0h	round((22*Voutmax-52)*2^8)

8.5.181 PAGE4 (page=0x04 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

Table 291. Device Page Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.5.182 LD_CFG8 (page=0x04 address=0x18) [reset=0h]

Load Resistance Value after load diagnostics is completed

Table 292. Load Resistance Value after load diagnostics is completed Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LD_RES_VAL1[31:24]	RW	0h	4.2424*((LD_RES_VAL1)/2^22) ohms

8.5.183 LD_CFG9 (page=0x04 address=0x19) [reset=0h]

Load Resistance Value after load diagnostics is completed

Table 293. Load Resistance Value after load diagnostics is completed Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LD_RES_VAL1[23:16]	RW	0h	4.2424*((LD_RES_VAL1)/2^22) ohms

8.5.184 LD_CFG10 (page=0x04 address=0x1A) [reset=0h]

Load Resistance Value after load diagnostics is completed

Table 294. Load Resistance Value after load diagnostics is completed Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LD_RES_VAL1[15:8]	RW	0h	4.2424*((LD_RES_VAL1)/2^22) ohms

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8.5.185 LD_CFG11 (page=0x04 address=0x1B) [reset=0h]

Load Resistance Value after load diagnostics is completed

Table 295. Load Resistance Value after load diagnostics is completed Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LD_RES_VAL1[7:0]	RW	0h	4.2424*((LD_RES_VAL1)/2^22) ohms

8.5.186 TF_CFG4 (page=0x04 address=0x58) [reset=0h]

Thermal foldback hold count (samples)

Table 296. Thermal foldback hold count (samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT[31:24]	RW	0h	round(seconds * 1000)

8.5.187 TF_CFG5 (page=0x04 address=0x59) [reset=0h]

Thermal foldback hold count (samples)

Table 297. Thermal foldback hold count (samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT[23:16]	RW	0h	round(seconds * 1000)

8.5.188 TF_CFG6 (page=0x04 address=0x5A) [reset=0h]

Thermal foldback hold count (samples)

Table 298. Thermal foldback hold count (samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT[15:8]	RW	0h	round(seconds * 1000)

8.5.189 TF_CFG7 (page=0x04 address=0x5B) [reset=64h]

Thermal foldback hold count (samples)

Table 299. Thermal foldback hold count (samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT[7:0]	RW	64h	round(seconds * 1000)

8.5.190 TF_CFG8 (page=0x04 address=0x5C) [reset=40h]

Thermal foldback limiter release rate (db/samples)

Table 300. Thermal foldback limiter release rate (db/samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[31:24]	RW	40h	round(10^(dB per sample/20)*2^30)

8.5.191 TF_CFG9 (page=0x04 address=0x5D) [reset=BDh]

Thermal foldback limiter release rate (db/samples)

Table 301. Thermal foldback limiter release rate (db/samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[23:16]	RW	BDh	round(10^(dB per sample/20)*2^30)

8.5.192 TF_CFG10 (page=0x04 address=0x5E) [reset=B7h]

Thermal foldback limiter release rate (db/samples)

Table 302. Thermal foldback limiter release rate (db/samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[15:8]	RW	B7h	round(10^(dB per sample/20)*2^30)

8.5.193 TF_CFG11 (page=0x04 address=0x5F) [reset=B0h]

Thermal foldback limiter release rate (db/samples)

Table 303. Thermal foldback limiter release rate (db/samples) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[7:0]	RW	B0h	round(10^(dB per sample/20)*2^30)

8.5.194 TF_CFG12 (page=0x04 address=0x60) [reset=39h]

Thermal foldback limiter temperature threshold

Table 304. Thermal foldback limiter temperature threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[31:24]	RW	39h	round(temperature in degree C*2^23)

8.5.195 TF_CFG13 (page=0x04 address=0x61) [reset=82h]

Thermal foldback limiter temperature threshold

Table 305. Thermal foldback limiter temperature threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[23:16]	RW	82h	round(temperature in degree C*2^23)

8.5.196 TF_CFG14 (page=0x04 address=0x62) [reset=60h]

Thermal foldback limiter temperature threshold

Table 306. Thermal foldback limiter temperature threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[15:8]	RW	60h	round(temperature in degree C*2^23)

8.5.197 TF_CFG16 (page=0x04 address=0x63) [reset=7Fh]

Thermal foldback limiter temperature threshold

Table 307. Thermal foldback limiter temperature threshold Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[7:0]	RW	7Fh	round(temperature in degree C*2^23)

8.5.198 TF_CFG17 (page=0x04 address=0x64) [reset=2Dh]

Thermal foldback max gain reduction (dB)

Table 308. Thermal foldback max gain reduction (dB) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[31:24]	RW	2Dh	round(10^(max attn dB/20)*2^31)

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8.5.199 TF_CFG18 (page=0x04 address=0x65) [reset=6Ah]

Thermal foldback max gain reduction (dB)

Table 309. Thermal foldback max gain reduction (dB) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[23:16]	RW	6Ah	round(10^(max attn dB/20)*2^31)

8.5.200 TF_CFG19 (page=0x04 address=0x66) [reset=86h]

Thermal foldback max gain reduction (dB)

Table 310. Thermal foldback max gain reduction (dB) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[15:8]	RW	86h	round(10^(max attn dB/20)*2^31)

8.5.201 TF_CFG20 (page=0x04 address=0x67) [reset=6Fh]

Thermal foldback max gain reduction (dB)

Table 311. Thermal foldback max gain reduction (dB) Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[7:0]	RW	6Fh	round(10^(max attn dB/20)*2^31)

8.5.202 DVC_SR1 (page=0x04 address=0x6C) [reset=2h]

Volume Control slew rate for 16kHz fs

Table 312. Volume Control slew rate for 16kHz fs Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_SLEW_LR[31:24]	RW	2h	round((1-exp(-1/(0.2*8*fs*time in seconds)))*2^31)

8.5.203 DVC_SR2 (page=0x04 address=0x6D) [reset=79h]

Volume Control slew rate for 16kHz fs

Table 313. Volume Control slew rate for 16kHz fs Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_SLEW_LR[23:16]	RW	79h	round((1-exp(-1/(0.2*8*fs*time in seconds)))*2^31)

8.5.204 DVC_SR3 (page=0x04 address=0x6E) [reset=CAh]

Volume Control slew rate for 16kHz fs

Table 314. Volume Control slew rate for 16kHz fs Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_SLEW_LR[15:8]	RW	CAh	round((1-exp(-1/(0.2*8*fs*time in seconds)))*2^31)

8.5.205 DVC_SR4 (page=0x04 address=0x6F) [reset=5Eh]

Volume Control slew rate for 16kHz fs

Table 315. Volume Control slew rate for 16kHz fs Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DVC_SLEW_LR[7:0]	RW	5Eh	round((1-exp(-1/(0.2*8*fs*time in seconds)))*2^31)

8.5.206 CD_CFG1 (page=0x04 address=0x70) [reset=56h]

Class D gain

Table 316. Class D gain Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSD_GAIN[31:24]	RW	56h	round(10^(dB/20)*2^27)

8.5.207 CD_CFG2 (page=0x04 address=0x71) [reset=B7h]

Class D gain

Table 317. Class D gain Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSD_GAIN[23:16]	RW	B7h	round(10^(dB/20)*2^27)

8.5.208 CD_CFG3 (page=0x04 address=0x72) [reset=96h]

Class D gain

Table 318. Class D gain Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSD_GAIN[15:8]	RW	96h	round(10^(dB/20)*2^27)

8.5.209 CD_CFG4 (page=0x04 address=0x73) [reset=FFh]

Class D gain

Table 319. Class D gain Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLASSD_GAIN[7:0]	RW	FFh	round(10^(dB/20)*2^27)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TAS2564 is a digital input high efficiency Class-D audio power amplifier with advanced battery current management and an integrated Class-H boost converter. In auto passthrough mode, the Class-H boost converter generates the Class-D amplifier supply rail. During low Class-D output power, the boost improves efficiency by deactivating and connecting VBAT directly to the Class-D amplifier supply. When high power audio is required, the boost quickly activates to provide louder audio than a stand-alone amplifier connected directly to the battery. To enable load monitoring, the TAS2564 constantly measures the current and voltage across the load and provides a digital stream of this information back to a processor. It is recommended to configure the TAS2564 using PurePath™ Console 3 Software.

9.2 Typical Application

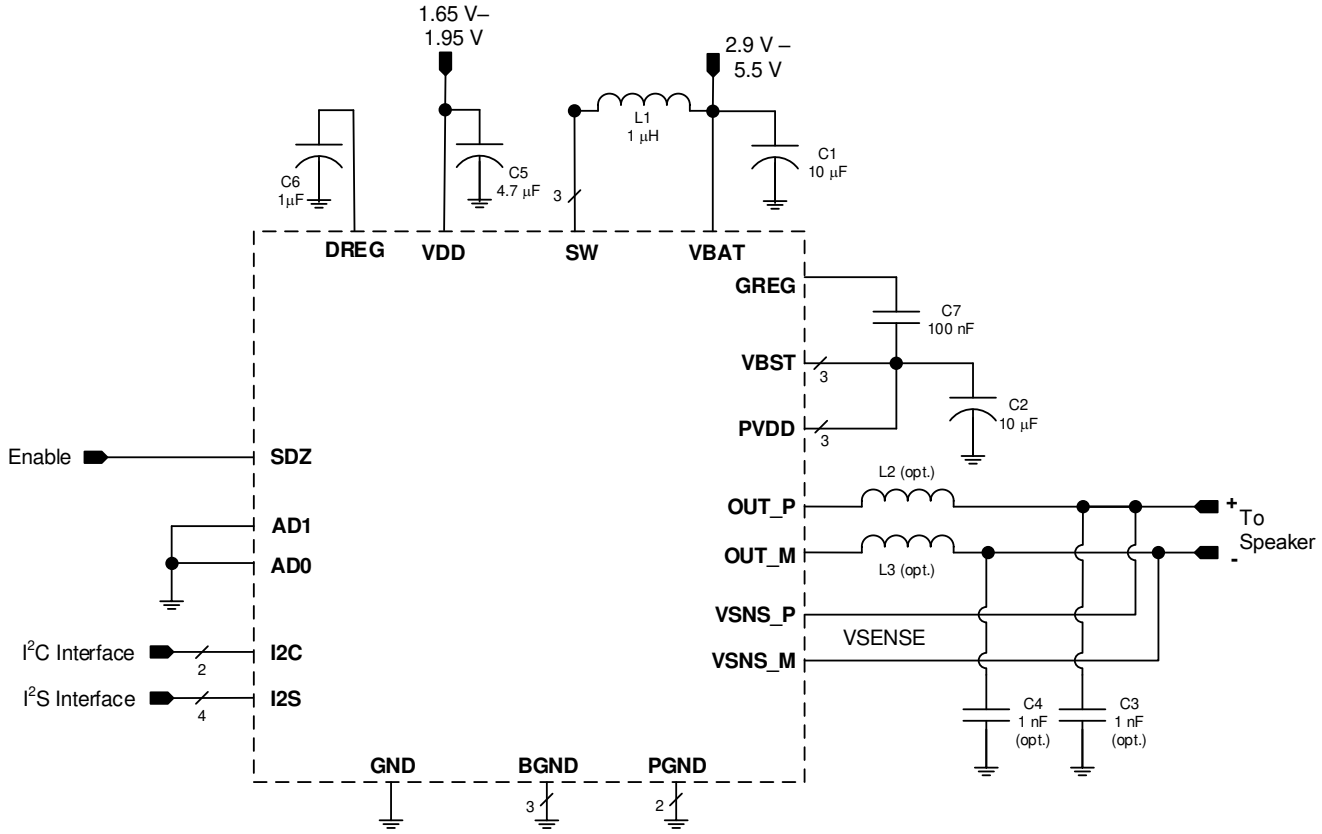

Figure 48. Typical Application - Digital Audio Input

Typical Application (continued)

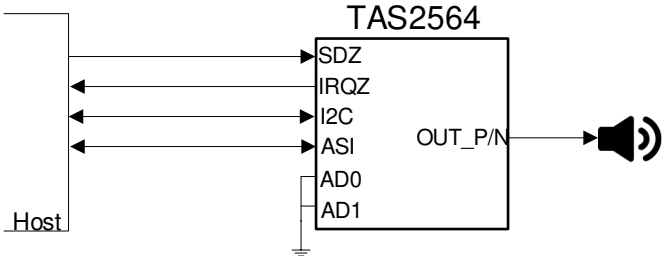

Figure 49. Typical Application - Mono

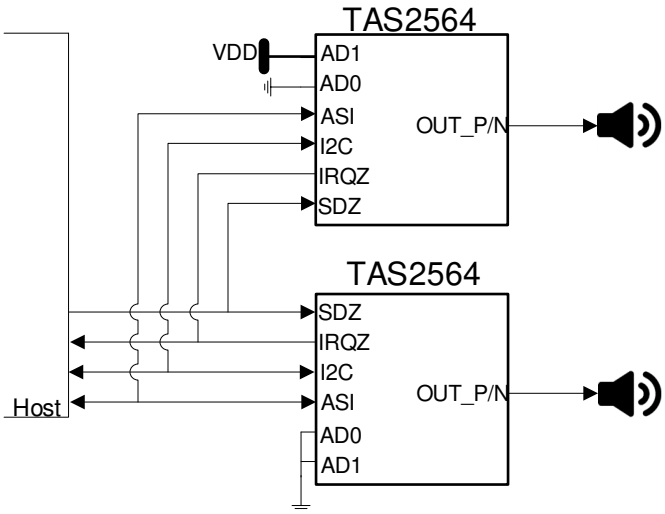

Figure 50. Typical Application - Stereo

Table 320. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
L1	Boost Converter Inductor(1)	Inductance, 20% Tolerance	0.47	1		µH
		Saturation Current		5.5		A
L2, L3	EMI Filter Inductors (optional). These are not recommended as it degrades THD+N performance. TAS2564 is a filter-less Class-D and does not require these bead inductors.	Impedance at 100 MHz		120		Ω
		DC Resistance			0.095	Ω
		DC Current			2	A
		Size		0402		EIA
C1	Boost Converter Input Capacitor(1)	Capacitance, 20% Tolerance	10			µF
C2	Boost Converter Output Capacitor	Type	X5R			
		Capacitance, 20% Tolerance	10		47	µF
		Rated Voltage	16			V
		Capacitance at 11.5 V derating	3.3			µF
C3, C4	EMI Filter Capacitors (optional, must use L2, L3 if C3, C4 used)	Capacitance		1		nF
C5	VDD Decoupling Capacitor	Capacitance	4.7			µF
C6	DREG Decoupling Capacitor	Capacitance	1			µF
C6	GREG Fly Capacitor	Capacitance	100			nF

(1) See section Boost Converter Passive Devices for additional requirements on derating, stability, and inductor value trade-offs.

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9.2.1 Design Requirements

For Figure 49 example, use the parameters shown in Table 321.

Table 321. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio Input	Digital Audio, I^2S
Current and Voltage Data Stream	Digital Audio, I^2S
Mono or Stereo Configuration	Mono
Max Output Power at 1% THD+N	7.0 W

9.2.2 Detailed Design Procedure

9.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See Device Mode and Address Selection for information on changing the I^2C address of the TAS2564 to support stereo operation. Mono or stereo configuration does not impact the device performance.

9.2.2.2 Boost Converter Passive Devices

The boost converter requires three passive devices that are labeled L1, C1 and C2 in and whose specifications are provided in Table 320. These specifications are based on the design of the TAS2564 and are necessary to meet the performance targets of the device. In particular, L1 should not be allowed to enter in the current saturation region. The saturation current for L1 should be > ILIM to deliver Class-D peak power.

Additionally, the ratio of L1/C2 (the derated value of C2 at 11.5 V should be used in this ratio) has to be lesser than 1/3 for boost stability. This 1/3 ratio should be maintained including the worst case variation of L1 and C2. To satisfy sufficient energy transfer, L1 needs to be ≥ 0.47 µH at the boost switching frequency (100 kHz to 4 MHz). Using a 0.47µH will have more boost ripple than a 1.0 µH or 2.2 µH but the high PSRR should minimize the effect from the additional ripple. Finally, the minimum C2 (derated value at programmed boost voltage) should be > 3.3 µF for Class-D power delivery specification.

9.2.2.3 EMI Passive Devices

The system designer may want to include passive devices on the Class-D output . These passive devices that are labeled L2, L3, C3 and C4 in and their recommended specifications are provided in Table 320. If C3 and C4 are used, L2 and L3 must also be installed, and C3 and C4 must be placed after L2 and L3 respectively to maintain the stability of the output stage.

9.2.2.4 Miscellaneous Passive Devices

The GREG Capacitor requires 100 nF to meet boost and Class-D power delivery and efficiency specs. For best device performance, the GREG capacitor should be placed very close to the device, star connected to PVDD and be routed with wide traces to minimize the impact of PCB parasitic effects.

DREG Capacitor should be placed and Ground Loop closed next to device. DREG is internal supply(1.5V typical, functional min of 1.35V) generated from external VDD supply. For best performance, noise on VDD should be reduced by wide traces or higher caps on VDD next to device based on board routings.

10 Power Supply Recommendations

10.1 Power Supplies

The TAS2564 requires four power supplies:

- Boost Input (terminal: VBAT)
  - Voltage: 2.9 V to 5.5 V
  - Max Current: 5 A for ILIM = 4.0 A (default)
- Analog Supply (terminal: VDD)
  - Voltage: 1.65 V to 1.95 V
  - Max Current: 30 mA
- Internal Supplies
  - Digital Supply (terminal: DREG): 1.35 V to 1.65 V
  - Boost Output (terminal: VBST) : VBAT to 13V
  - Class-D Power Supply (terminal: PVDD): Short to VBST

The decoupling capacitors for the power supplies should be placed close to the device terminals.

10.2 Power Supply Sequencing

The power rail may be brought up and down in any order. There is no requirement on sequencing. However if VDD is present without VBAT an additional rise in VDD current will be observed until VBAT is present.

When the supplies have settled, the SDZ terminal can be set HIGH to operate the device. Additionally the SDZ pin can be tied to VDD and the internal POR will perform a reset of the device. After a hardware or software reset additional commands to the device should be delayed for 100 uS to allow the OTP to load. The above sequence should be completed before any I^2C operation.

10.2.1 Boost Supply Details

The boost supply (VBAT) and associated passives need to be able to support the current requirements of the device. By default, the peak current limit of the boost is set to 5 A. Refer to Table 90 for information on changing the current limit. A minimum of a 10 µF capacitor is recommended on the boost supply to quickly support changes in required current. Refer to Figure 48 for the schematic.

The current requirements can also be reduced by lowering the gain of the amplifier, or in response to decreasing battery through the use of the battery-tracking feature of the TAS2564 described in Supply Tracking Limiters with Brown Out Prevention.

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11 Layout

11.1 Layout Guidelines

- Place the boost inductor between VBAT and SW close to device terminals with no VIAS between the device terminals and the inductor.
- Place the capacitor between VBSTand Ground close to device terminals with no VIAS between the device terminals and capacitor.
- Place the capacitor between VBAT and GND close to device terminals with no VIAS between the device terminals and capacitor.
- Minimize trace inductance between the GREG capacitor and TAS2564. This can be done by using multiple vias in parallel and by using wide routes where possible. This capacitor should have a star connection to PVDD.
- Do not use VIAS for traces that carry high current. These include the traces for VBST, SW, VBAT, PGND and the speaker OUT_P, OUT_M.
- SW, OUT_P and OUT_M are high switching nets and keep out should be kept from these signals to prevent corruption of digital signals.
- Use epoxy filled vias for the interior pads.
- Connect VSNS_P, VSNS_N as close as possible to the speaker.
  - VSNS_P, VSNS_N should be connected between the EMI ferrite and the speaker if EMI ferrites are used on OUT_P, OUT_M.
  - EMI ferrites must be used if EMI capacitors are used on OUT_P, OUT_M.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in and described in Power Supplies.
- Place EMI ferrites, if used, close to the device.

Table 322. Pin Layout Guidelines

PIN	MAX PARASITIC INDUCTANCE	LAYOUT RECOMMENDATIONS
BGND, GND, PGND, GNDD	150 pH	Short BGND, GND, GNDD, PGDN below the package and connect them to PCB ground plane strongly through multiple vias. Minimize inductance as much as possible
DREG	500 pH	Bypass to GND with capacitor recommended in Table 320. Do not connect to external load. Both ends of decoupling cap should see as low inductance as possible between this pin and gnd pins.
GREG	200 pH	Connect it to PVDD with a star connection and not to boost plane with recommended in Table 320. Do not connect to external load.
PVDD	100 pH	Short it to VBST(boost) plane through strong conneciton. Connect it to GREG with a star connection and not to boost plane.
SW		Connect to VBAT with boost inductor recommended in Table 320. Reduce parasitic capacitor and resistance for efficiency. Boost inductor should be as close as possible to the SW pin. Inductor should be connected to SW through thick plane. Traces should support currents up to device over-current limit.
VBAT	500 pH	Bypass to GND with capacitor recommended in Table 320. Should be connected to inductor through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBAT pin and PGND pin.
VBST	100 pH	Do not connect to external load. Bypass to GND with capacitor recommended in Table 320. Connect to PVDD through thick plane. Both ends of decoupling capacitor should see as low inductance as possible between VBST pin and BGND pin. Traces should support currents up to device over-current limit.

Layout Guidelines (continued)

Table 322. Pin Layout Guidelines (continued)

PIN	MAX PARASITIC INDUCTANCE	LAYOUT RECOMMENDATIONS
VDD	200 pH	Bypass to GND with capacitor recommended in Table 320. Both the end of decoupling cap should see as low inductance as possible between this pin and GND pin

11.2 Layout Example

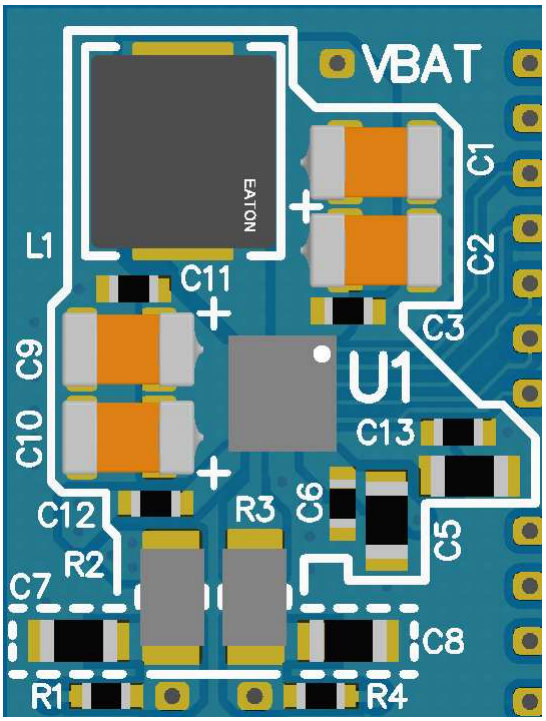

Figure 51. Board Layout

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Layout Example (continued)

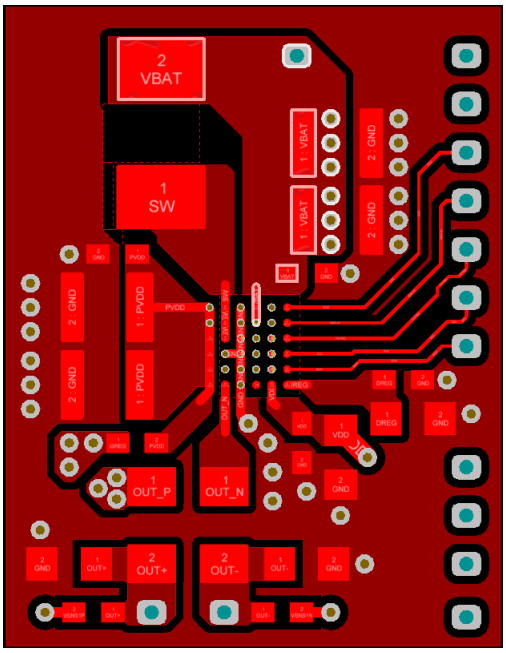

Figure 52. Top Copper

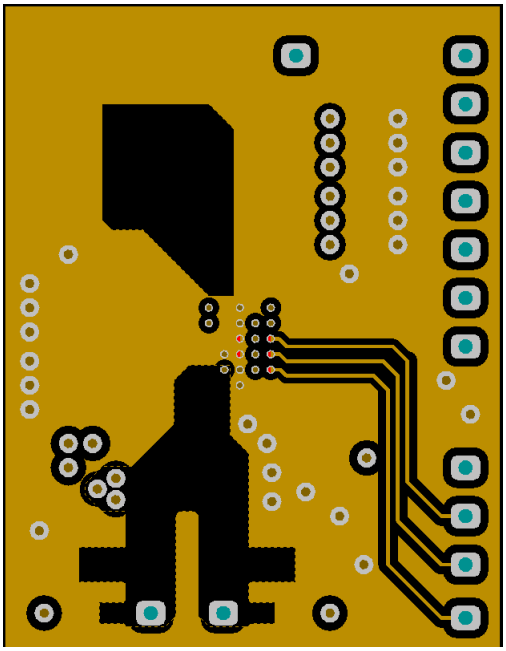

Figure 53. Second Copper Layer

Layout Example (continued)

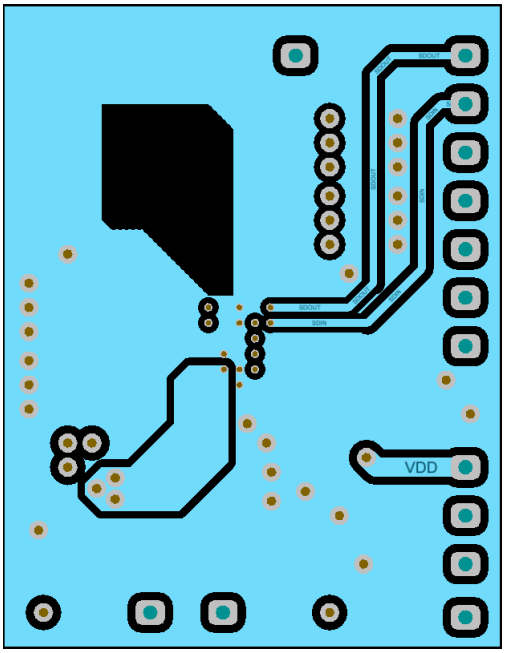

Figure 54. Third Copper Layer

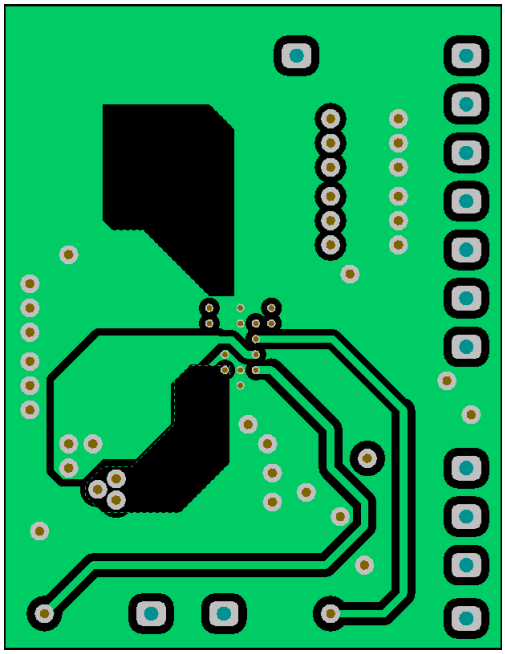

Figure 55. Fourth Copper Layer

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Layout Example (continued)

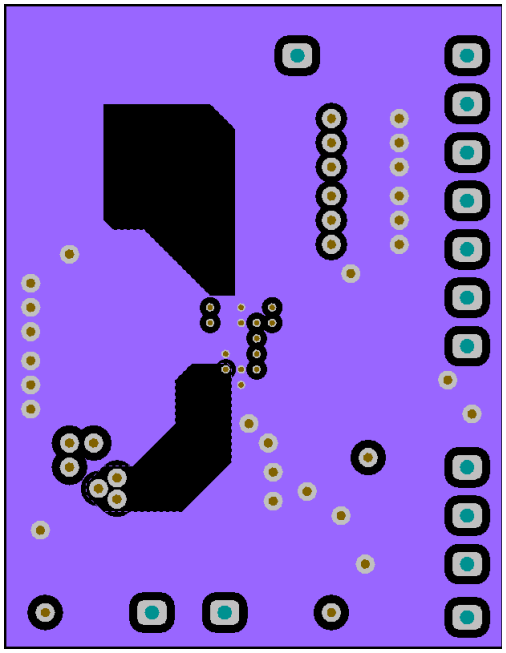

Figure 56. Fifth Copper Layer

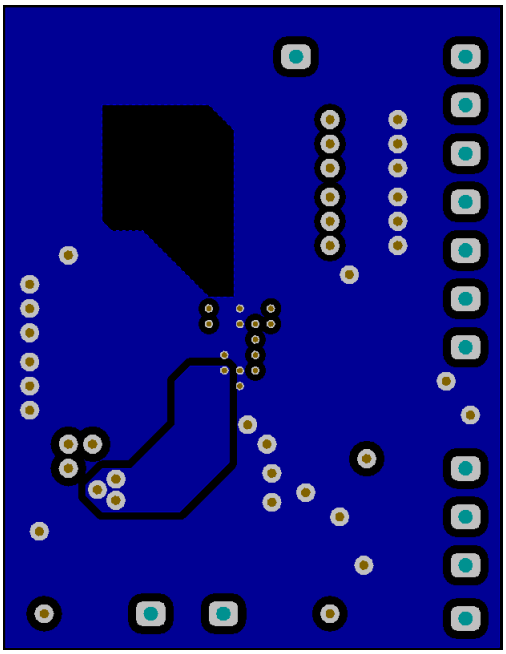

Figure 57. Bottom Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following: *TAS2563YBGEVM-DC Evaluation module user's guide*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

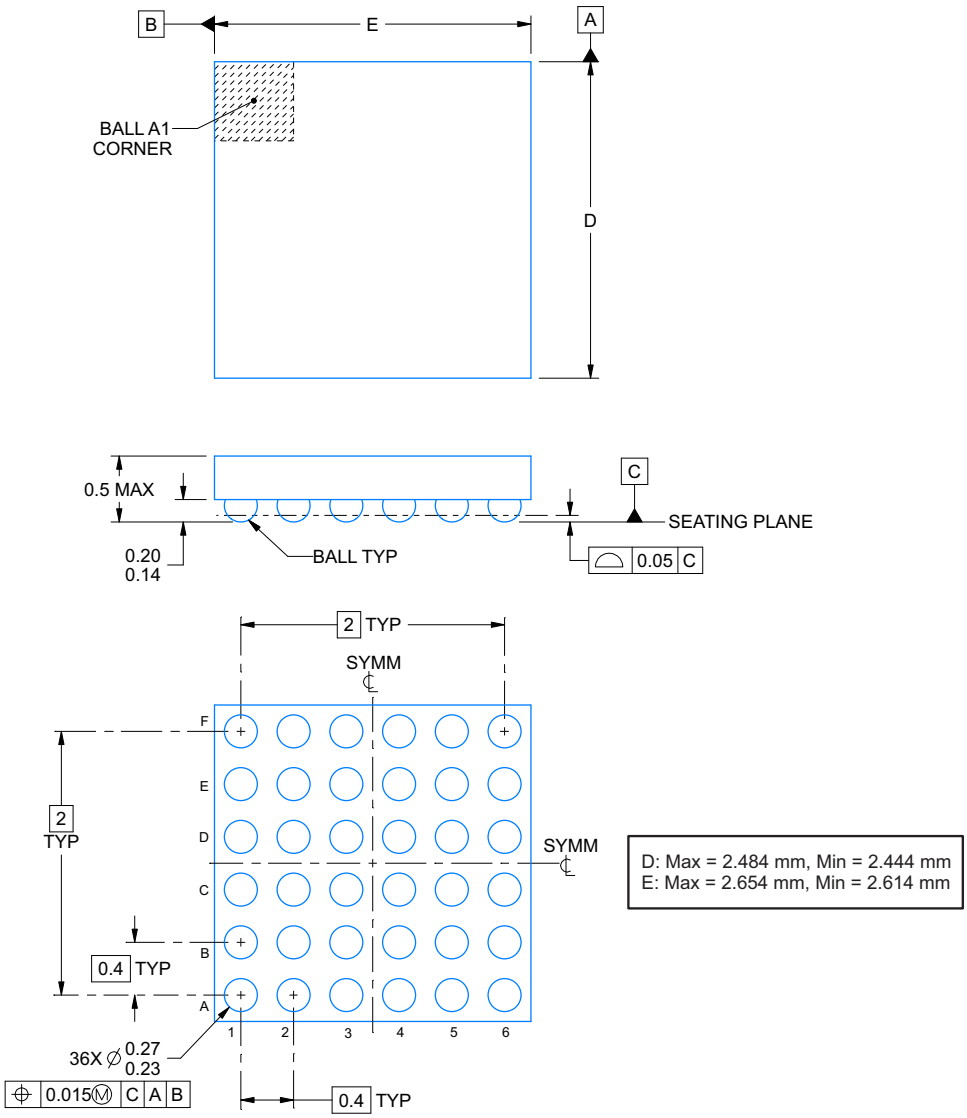
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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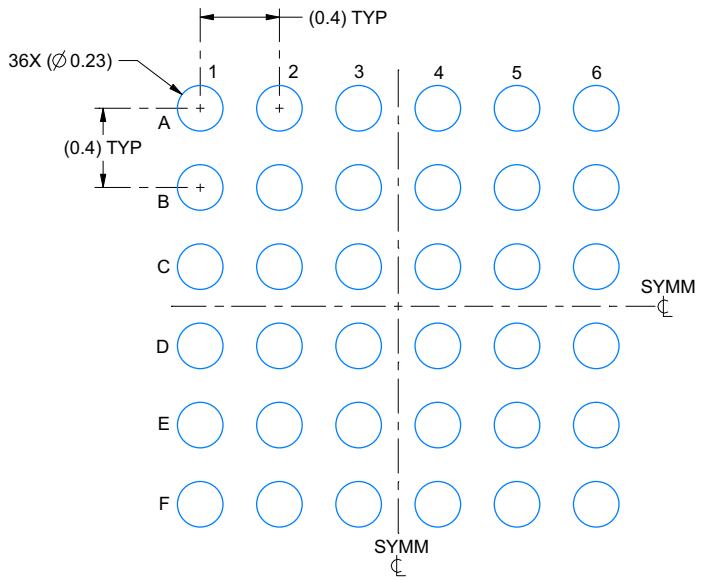
EXAMPLE BOARD LAYOUT

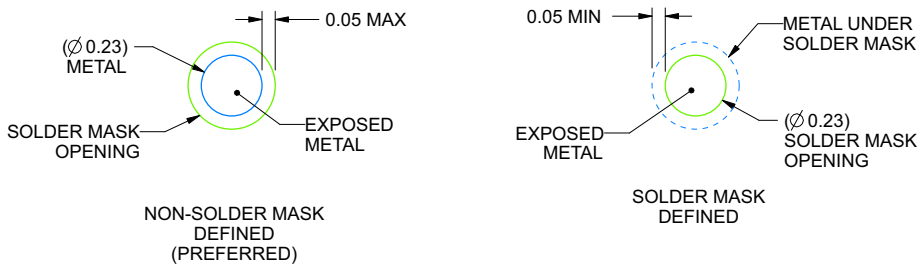
YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4224846/A 03/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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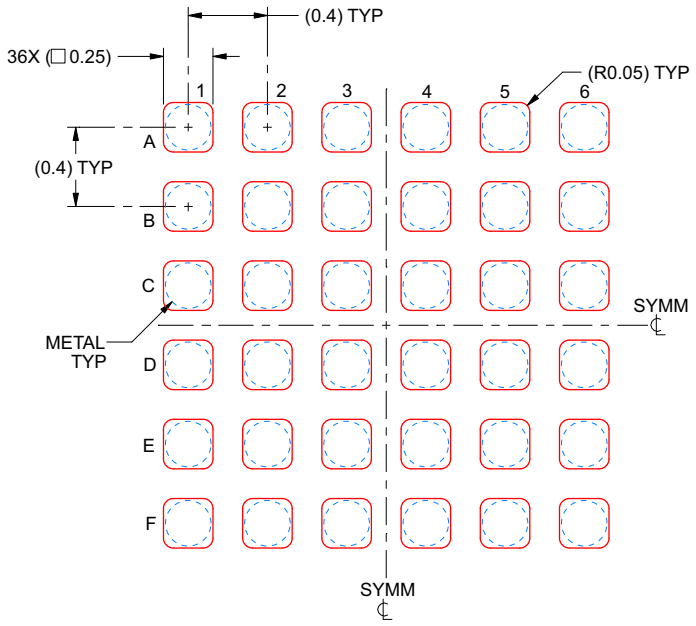
EXAMPLE STENCIL DESIGN

YBG0036

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224846/A 03/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

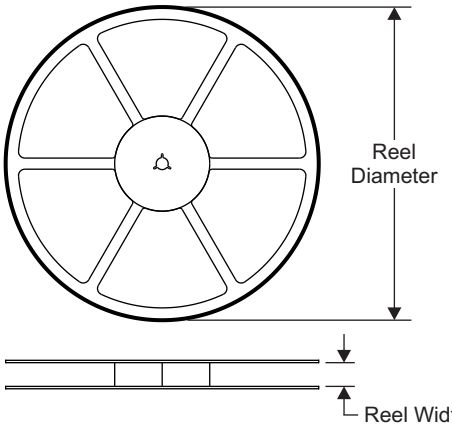
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

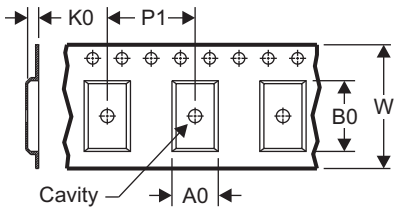
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

13.1.2 Tape and Reel Information

REEL DIMENSIONS

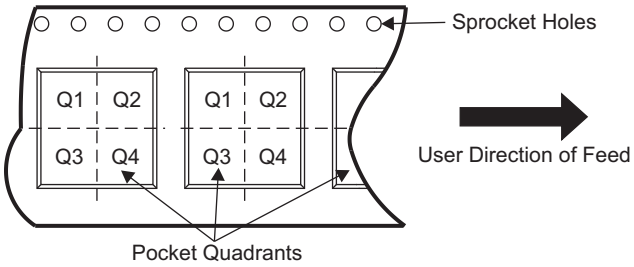


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant

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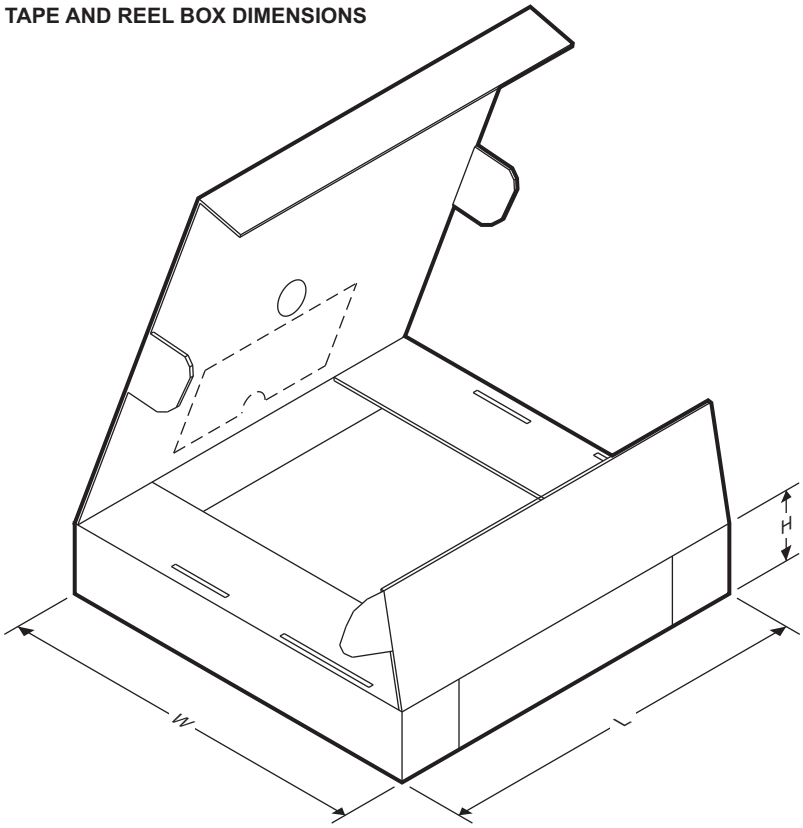
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS2564YBGR	Active	Production	DSBGA (YBG) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2564
TAS2564YBGR.A	Active	Production	DSBGA (YBG) | 36	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2564
TAS2564YBGT	Active	Production	DSBGA (YBG) | 36	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2564
TAS2564YBGT.A	Active	Production	DSBGA (YBG) | 36	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TAS2564

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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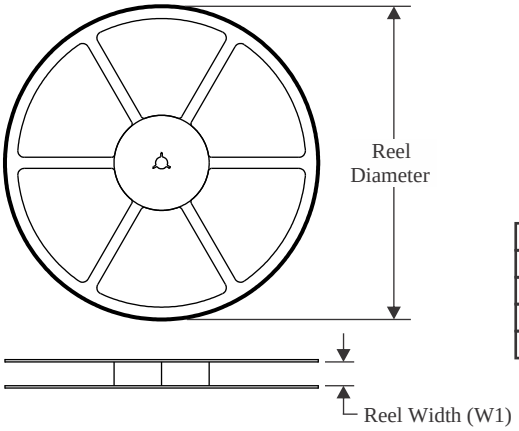
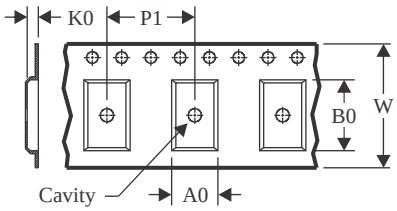
TAPE AND REEL INFORMATION

REEL DIMENSIONS

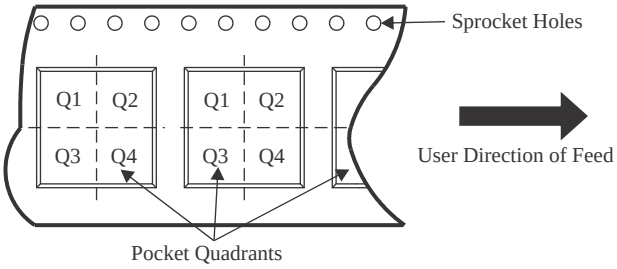


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

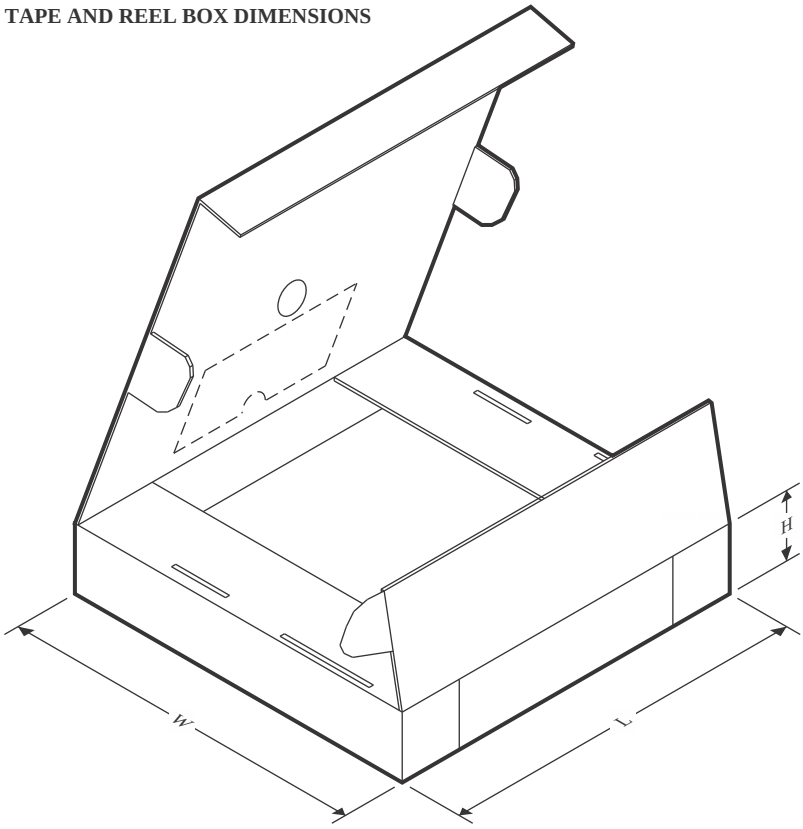
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

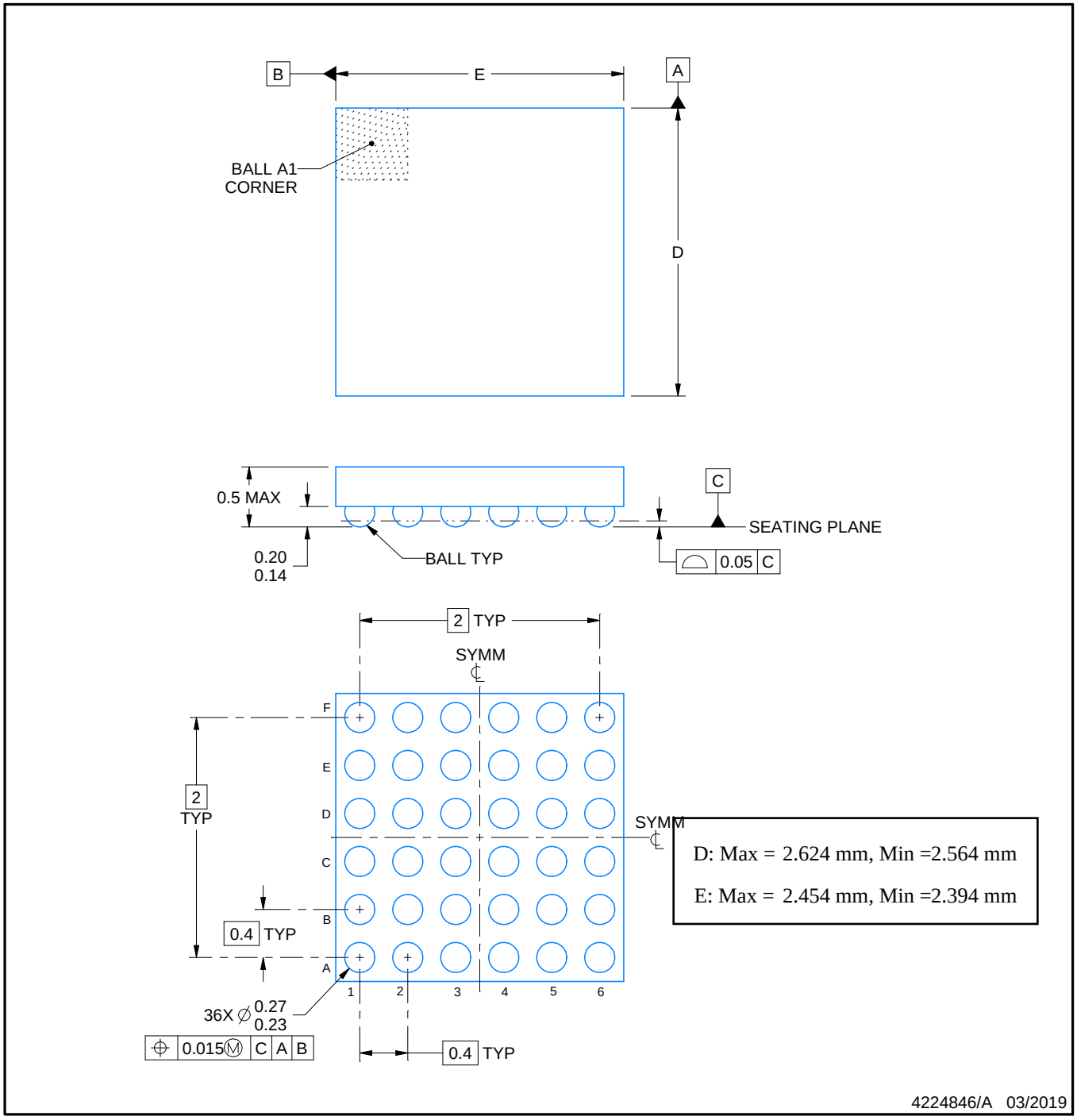
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2564YBGR	DSBGA	YBG	36	3000	180.0	8.4	2.64	2.81	0.7	4.0	8.0	Q2
TAS2564YBGT	DSBGA	YBG	36	250	180.0	8.4	2.64	2.81	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



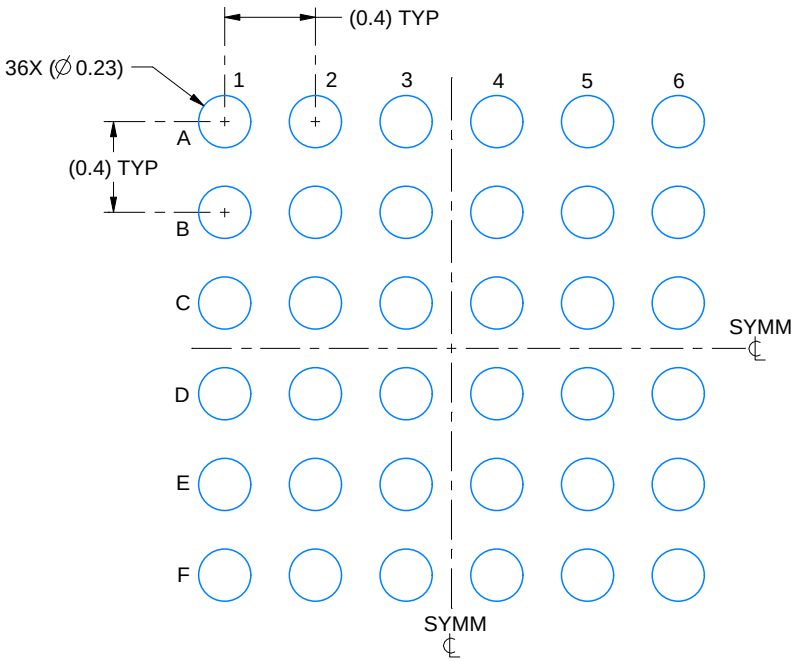
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2564YBGR	DSBGA	YBG	36	3000	182.0	182.0	20.0
TAS2564YBGT	DSBGA	YBG	36	250	182.0	182.0	20.0

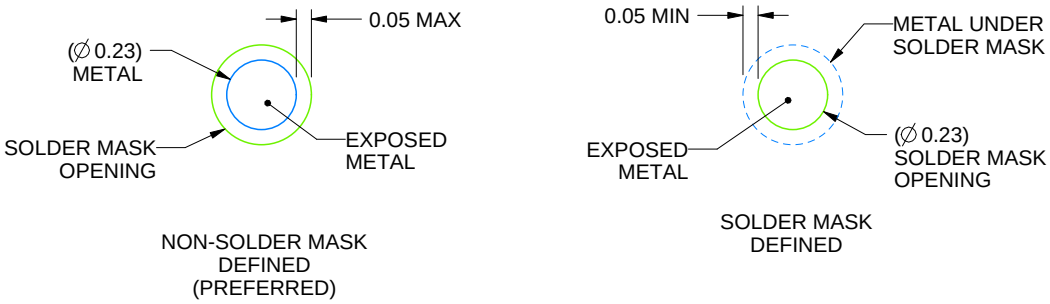


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

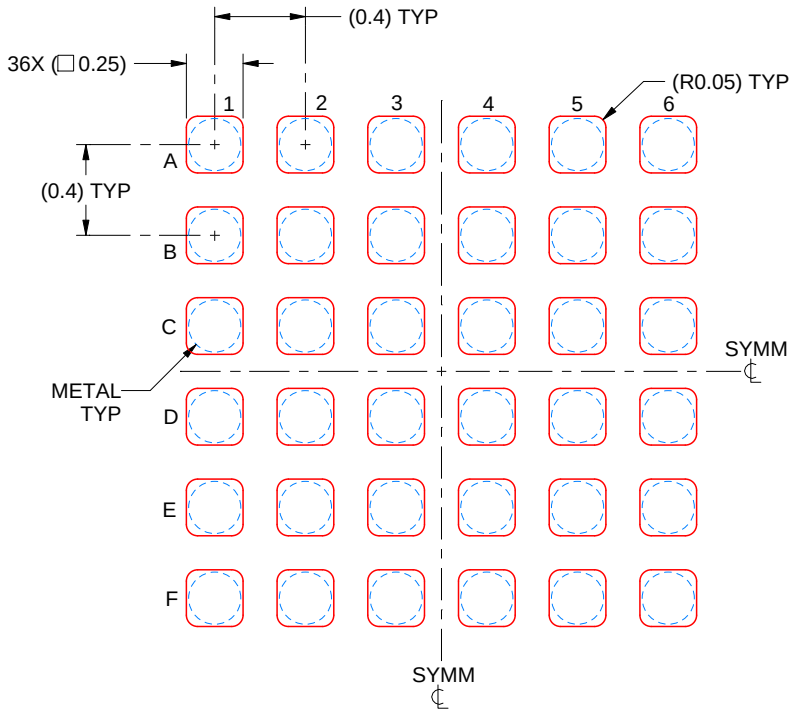


SOLDER MASK DETAILS
NOT TO SCALE

4224846/A 03/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4224846/A 03/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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