125W STEREO / 250W MONO PurePath™ HD DIGITAL-INPUT POWER STAGE

Check for Samples: TAS5612A

FEATURES

- **PurePath™ HD Enabled Integrated Feedback Provides:**
  - **Signal Bandwidth up to 80kHz for High Frequency Content From HD Sources**
  - **Ultralow 0.03% THD at 1W into 4Ω**
  - **Ultralow 0.01% THD at 1W into 8Ω**
  - **Flat THD at all Frequencies for Natural Sound**
  - **80dB PSRR (BTL, No Input Signal)**
  - **>100dB (A weighted) SNR**
  - **Click and Pop Free Startup**
- **Pin compatible with TAS5631, TAS5616 and TAS5614**
- **Multiple Configurations Possible on the Same PCB With Stuffing Options:**
  - **Mono Parallel Bridge Tied Load (PBTL)**
  - **Stereo Bridge Tied Load (BTL)**
  - **2.1 Single Ended Stereo Pair and Bridge Tied Load Subwoofer**
- **Total Output Power at 10%THD+N**
  - **250W in Mono PBTL Configuration**
  - **125W per Channel in Stereo BTL Configuration**
- **Total Output Power in BTL configuration at 1%THD+N**
  - **130W Stereo into 3Ω**
  - **105W Stereo into 4Ω**
  - **70W Stereo into 6Ω**
  - **55W Stereo into 8Ω**
- **>90% Efficient Power Stage With 60-mΩ Output MOSFETs**
- **Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting**
- **EMI Compliant When Used With Recommended System Design**
- **Thermally Enhanced Package:**
  - **PHD (64-Pin QFP)**

APPLICATIONS

- **Home Theater Systems**
- **AV Receivers**
- **DVD/Blu-ray™ Disc Receivers**
- **Mini Combo Systems**
- **Active Speakers and Subwoofers**

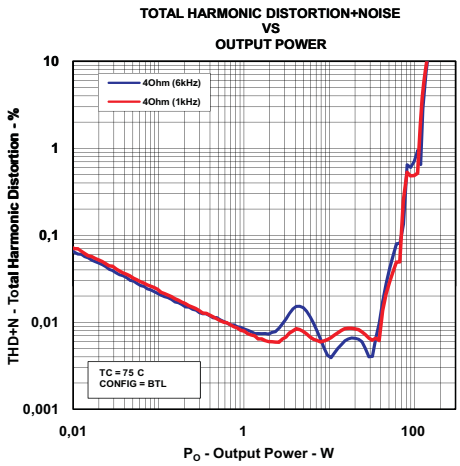
DESCRIPTION

The TAS5612A is a high performance digital input Class D amplifier with integrated closed loop feedback technology (known as PurePath™ HD) with the ability to drive up to 125W (1) Stereo into 4 to 8 Ω Speakers from a single 32.5V supply.

PurePath™ HD technology enables traditional AB-Amplifier performance (<0.03% THD) levels while providing the power efficiency of traditional class D amplifiers.

Unlike traditional Class D amplifiers, the distortion curve only increases once the output levels move into clipping.

PurePath™ HD technology enables lower idle losses making the device even more efficient.



(1) Achievable output power levels are dependent on the thermal configuration of the target application. A high performance thermal interface material between the package exposed heatslug and the heat sink should be used to achieve high output power levels.

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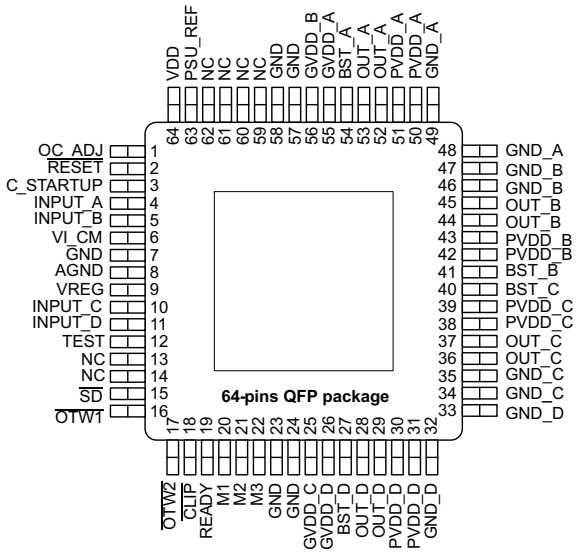
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

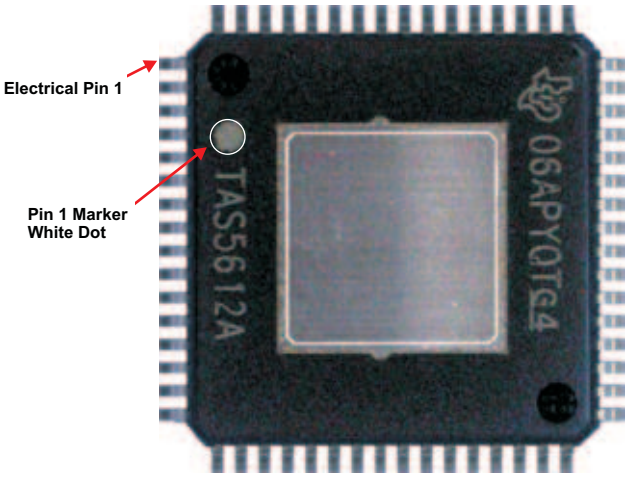
Terminal Assignment

The package type contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heat sink.

PHD PACKAGE (TOP VIEW)



PIN ONE LOCATION PHD PACKAGE



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MODE SELECTION PINS

MODE PINS			PWM INPUT[1]	OUTPUT CONFIGURATION	DESCRIPTION		
M3	M2	M1					
0	0	0	2N	2 × BTL	AD mode		
0	0	1	—	—	Reserved		
0	1	0	2N	2 × BTL	BD mode		
0	1	1	1N	1 × BTL +2 ×SE	AD mode		
1	0	0	1N	4 × SE	AD mode		
1	0	1	2N 1N	1 × PBTL	INPUT_C[2]	INPUT_D[2]	
					0	0	AD mode
					1	0	BD mode
1	1	0	Reserved				
1	1	1					

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) INPUT_C and D are used to select between a subset of AD and BD mode operations in PBTL mode

PACKAGE HEAT DISSIPATION RATINGS [1]

PARAMETER	TAS5612APHD
$R_{\theta JC}$ (°C/W) – 2 BTL or 4 SE channels	3.2
$R_{\theta JC}$ (°C/W) – 1 BTL or 2 SE channel(s)	5.4
$R_{\theta JC}$ (°C/W) – 1 SE channel	7.9
Pad Area [2]	64mm^2

(1) J_C is junction-to-case, C_H is case-to-heat sink
(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of thermal grease with a thermal conductivity of 2.5 W/mK between the pad area and the heat sink and both channels active. The $R_{\theta CH}$ with this condition is 1.1°C/W for the PHD package and 0.44°C/W for the DKD package.

Table 1. ORDERING INFORMATION [1]

T_A	PACKAGE	DESCRIPTION
0°C–70°C	TAS5612APHD	64 pin HTQFP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted [1]

TAS5612A			UNIT
VDD to GND		–0.3 to 13.2	V
GVDD to GND		–0.3 to 13.2	V
PVDD_X to GND_X[2]		–0.3 to 53	V
OUT_X to GND_X[2]		–0.3 to 53	V
BST_X to GND_X[2]		–0.3 to 66.2	V
BST_X to GVDD_X[2]		–0.3 to 53	V
VREG to GND		–0.3 to 4.2	V
GND_X to GND		–0.3 to 0.3	V
GND to AGND		–0.3 to 0.3	V
OC_ADJ, M1, M2, M3, OSC_IO+, OSC_IO-, FREQ_ADJ, VI_CM, C_STARTUP, PSU_REF to GND		–0.3 to 4.2	V
INPUT_X		–0.3 to 7	V
$\overline{\text{RESET}}$, $\overline{\text{SD}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$ to GND		–0.3 to 7	V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$)		9	mA
Maximum operating junction temperature range, T_J		0 to 150	°C
Storage temperature, T_{stg}		–40 to 150	°C
Electrostatic discharge	Human body model[3] (all pins)	±2	kV
	Charged device model[3] (all pins)	±500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.
(3) Failure to follow good anti-static ESD handling during manufacture and rework will contribute to device malfunction. Make sure the operators handling the device are adequately grounded through the use of ground straps or alternative ESD protection.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	16	32.5	34.1	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance	Output filter according to schematics in the application information section.	3.5	4		Ω
R_L(SE)			1.8	2		
R_L(PBTL)			1.6	2		
R_L(BTL)	Load Impedance	Output filter according to schematics in the application information section. (R_{OC} = 22kΩ, add Schottky diodes from OUT_X to GND_X)	2.8	3		Ω
L_{OUTPUT}(BTL)	Output filter inductance	Minimum output inductance at I_{OC}	7	10		μH
L_{OUTPUT}(SE)			7	15		
L_{OUTPUT}(PBTL)			7	10		
F_{PWM}	PWM frame rate		352	384	500	kHz
C_{PVDD}	PVDD close decoupling capacitors			2.0		μF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%	22	30		kΩ
$R_{OC_LACTHED}$	Over-current programming resistor	Resistor tolerance = 5%	47	64		kΩ
T_J	Junction temperature		0		125	°C

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PIN FUNCTIONS

PIN		Function[1]	DESCRIPTION
NAME	PHD NO.		
AGND	8	P	Analog ground
BST_A	54	P	HS bootstrap supply (BST), external 0.033µF capacitor to OUT_A required.
BST_B	41	P	HS bootstrap supply (BST), external 0.033µF capacitor to OUT_B required.
BST_C	40	P	HS bootstrap supply (BST), external 0.033µF capacitor to OUT_C required.
BST_D	27	P	HS bootstrap supply (BST), external 0.033µF capacitor to OUT_D required.
$\overline{\text{CLIP}}$	18	O	Clipping warning; open drain; active low
C_STARTUP	3	O	Startup ramp requires a charging capacitor of 4.7nF to GND
TEST	12	I	Connect to VREG node
GND	7, 23, 24, 57, 58	P	Ground
GND_A	48, 49	P	Power ground for half-bridge A
GND_B	46, 47	P	Power ground for half-bridge B
GND_C	34, 35	P	Power ground for half-bridge C
GND_D	32, 33	P	Power ground for half-bridge D
GVDD_A	55	P	Gate drive voltage supply requires 0.1µF capacitor to GND
GVDD_B	56	P	Gate drive voltage supply requires 0.1µF capacitor to GND
GVDD_C	25	P	Gate drive voltage supply requires 0.1µF capacitor to GND
GVDD_D	26	P	Gate drive voltage supply requires 0.1µF capacitor to GND
GVDD_AB	—	P	Gate drive voltage supply requires 0.22µF capacitor to GND
GVDD_CD	—	P	Gate drive voltage supply requires 0.22µF capacitor to GND
INPUT_A	4	I	Input signal for half bridge A
INPUT_B	5	I	Input signal for half bridge B
INPUT_C	10	I	Input signal for half bridge C
INPUT_D	11	I	Input signal for half bridge D
M1	20	I	Mode selection
M2	21	I	Mode selection
M3	22	I	Mode selection
NC	59–62	—	No connect, pins may be grounded.
NC	13, 14	—	No connect, pins may be grounded.
OC_ADJ	1	O	Analog overcurrent programming pin requires resistor to ground.
$\overline{\text{OTW}}$	—	O	Overtemperature warning signal, open drain, active low.
$\overline{\text{OTW1}}$	16	O	Overtemperature warning signal, open drain, active low.
$\overline{\text{OTW2}}$	17	O	Overtemperature warning signal, open drain, active low.
OUT_A	52, 53	O	Output, half bridge A
OUT_B	44, 45	O	Output, half bridge B
OUT_C	36, 37	O	Output, half bridge C
OUT_D	28, 29	O	Output, half bridge D
PSU_REF	63	P	PSU Reference requires close decoupling of 4.7µF to GND
PVDD_A	50, 51	P	Power supply input for half bridge A requires close decoupling of 2uF capacitor GND_A
PVDD_B	42, 43	P	Power supply input for half bridge B requires close decoupling of 2uF capacitor GND_B
PVDD_C	38, 39	P	Power supply input for half bridge C requires close decoupling of 2uF capacitor GND_C
PVDD_D	30, 31	P	Power supply input for half bridge D requires close decoupling of 2uF capacitor GND_D
READY	19	O	Normal operation; open drain; active high
$\overline{\text{RESET}}$	2	I	Device reset Input; active low
$\overline{\text{SD}}$	15	O	Shutdown signal, open drain, active low
VDD	64	P	Power supply for digital voltage regulator requires a 47µF capacitor in parallel with a 0.1µF capacitor to GND for decoupling.
VI_CM	6	O	Analog comparator reference node requires close decoupling of 4.7µF to GND
VREG	9	P	Digital regulator supply filter pin requires 0.1µF capacitor to GND

(1) I = Input, O = Output, P = Power

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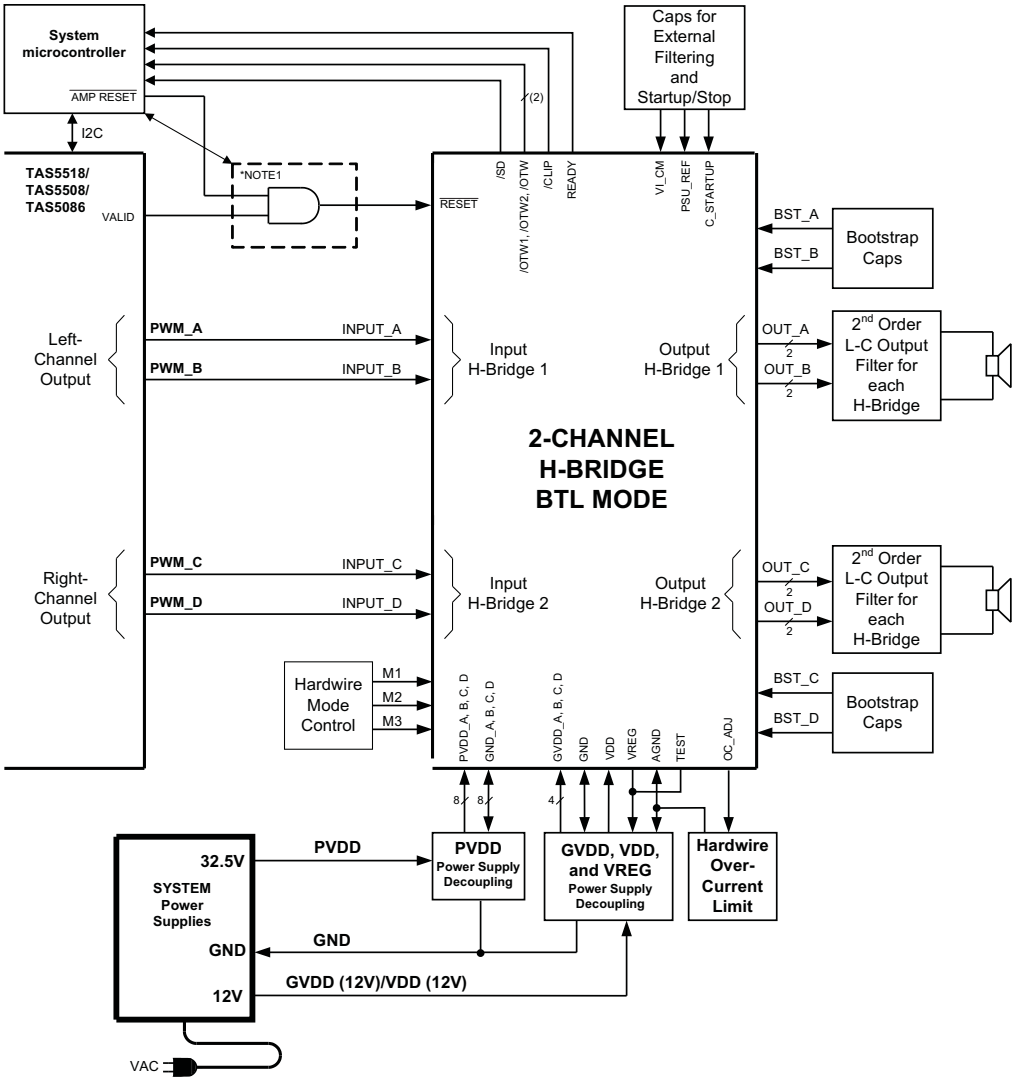
TYPICAL SYSTEM BLOCK DIAGRAM



(1) Logic AND is inside or outside the micro controller.

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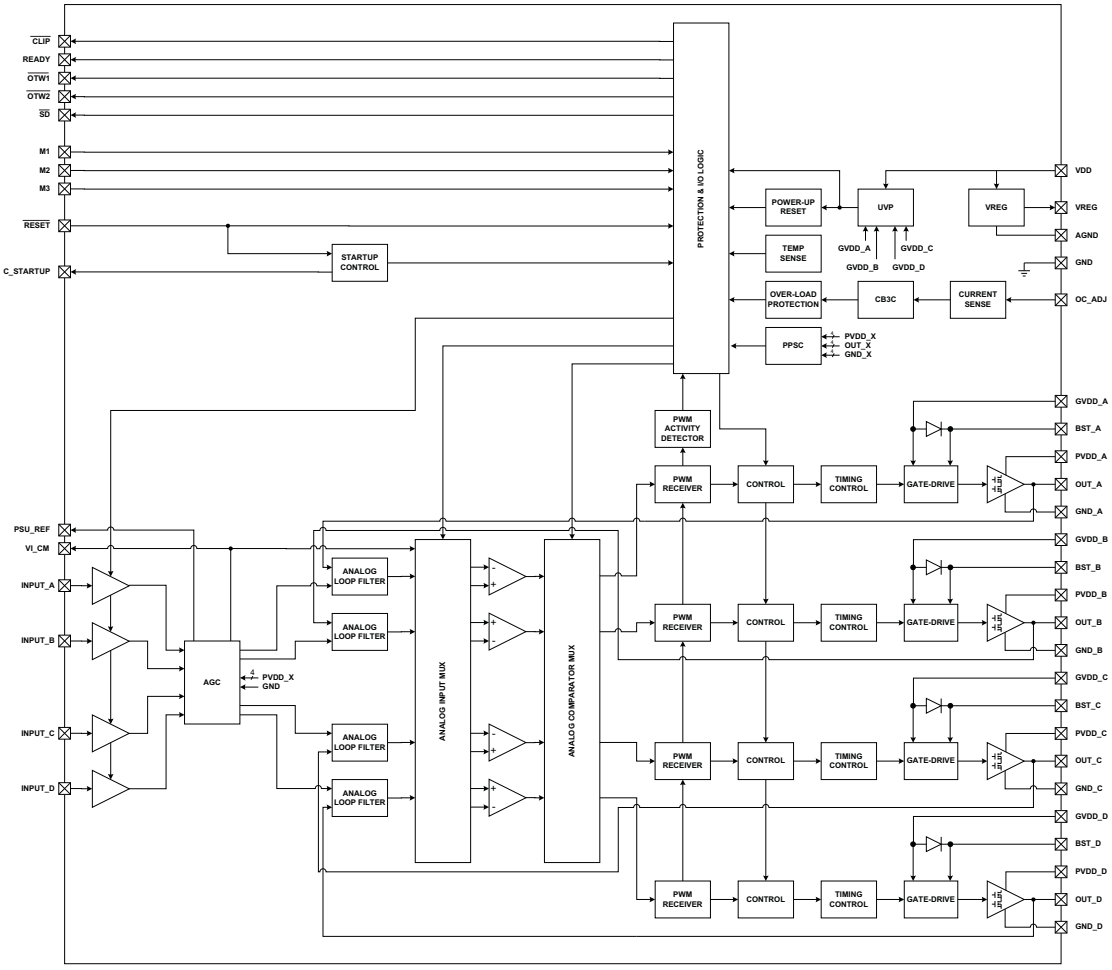
FUNCTIONAL BLOCK DIAGRAM



AUDIO CHARACTERISTICS (BTL)

Audio performance is recorded as a chipset consisting of a TAS5518 PWM Processor (modulation index limited to 97.7%) and a TAS5612A power stage. PCB and system configurations are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 32.5V, GVDD_X = 12V, R_L = 4Ω, f_S = 384 kHz, R_{OC} = 30kΩ, T_C = 75°C, Output Filter: L_{DEM} = 7µH, C_{DEM} = 680nF, MODE = 000, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3Ω, 10% THD+N (ROC=22kΩ, add Schottky diodes from OUT_X to GND_X)		165		W
		R_L = 4Ω, 10% THD+N		125		
		R_L = 3Ω, 1% THD+N (ROC=22kΩ, add Schottky diodes from OUT_X to GND_X)		130		
		R_L = 4Ω, 1% THD+N		105		
THD+N	Total harmonic distortion + noise	1 W, R_L = 4Ω		0.03%		
		1 W, R_L = 8Ω		0.01%		
V_n	Output integrated noise	A-weighted, TAS5518 Modulator		114		µV
$\|V_{OS}\|$	Output offset voltage	No signal		5	18	mV
SNR	Signal-to-noise ratio(1)	A-weighted, TAS5518 Modulator		103		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5518 modulator		103		dB
P_{idle}	Power dissipation due to Idle losses (I_{PVDD_X})	P_O = 0, 4 channels switching(2)		2		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

AUDIO CHARACTERISTICS (PBTL)

Audio performance is recorded as a chipset consisting of a TAS5518 PWM Processor (modulation index limited to 97.7%) and a TAS5612A power stage. PCB and system configurations are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 32.5V, GVDD_X = 12V, R_L = 2Ω, f_S = 384kHz, R_{OC} = 30kΩ, T_C = 75°C, Output Filter: L_{DEM} = 7µH, C_{DEM} = 1µF, MODE = 101-00, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2Ω, 10%, THD+N		250		W
		R_L = 3Ω, 10% THD+N		165		
		R_L = 4Ω, 10% THD+N		125		
		R_L = 2Ω, 1% THD+N		210		
		R_L = 3Ω, 1% THD+N		135		
		R_L = 4Ω, 1% THD+N		105		
THD+N	Total harmonic distortion + noise	1 W		0.03%		
V_n	Output integrated noise	A-weighted, TAS5518 Modulator		120		µV
SNR	Signal to noise ratio(1)	A-weighted, TAS5518 Modulator		103		dB
DNR	Dynamic range	A-weighted, input level –60 dBFS using TAS5518 modulator		103		dB
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0, 4 channels switching(2)		1.7		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

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ELECTRICAL CHARACTERISTICS

PVDD_X = 32.5V, GVDD_X = 12V, VDD = 12V, T_C (Case temperature) = 75°C, f_S = 384kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as reference node, VREG	VDD = 12V	3	3.3	3.6	V
VI_CM	Analog comparator reference node, VI_CM		1.5	1.75	1.9	V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		20		mA
		Idle, reset mode		20		
I_{GVDD_x}	Gate-supply current per half-bridge	50% duty cycle		10		mA
		Reset mode		1.5		
I_{PVDD_x}	Half-bridge idle current	50% duty cycle without output filter or load		15		mA
		Reset mode, No switching		540		µA
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, excludes metallization resistance, GVDD = 12V		60	100	mΩ
	Drain-to-source resistance, high side (HS)			60	100	mΩ
I/O PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_x, VDD			9.5		V
$V_{uvp,hyst}$ (1)				0.6		V
OTW1 (1)	Overtemperature warning 1		95	100	105	°C
OTW2 (1)	Overtemperature warning 2		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{OTW}$ to be inactive after $\overline{OTW}$ event.			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
	OTE-OTW differential			30		°C
OTE_{HYST} (1)	A reset needs to occur for $\overline{SD}$ to be released following an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 384kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 30kΩ		12.6		A
		Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 22kΩ (With Schottky diodes from OUT_X to GND_X)		16.3		
	Overcurrent limit protection, latched	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 64kΩ		12.6		A
		Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 47kΩ (With Schottky diodes from OUT_X to GND_X)		16.3		
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected half bridge		150		ns
I_{PD}	Internal pulldown resistor at output of each half bridge	Connected when $\overline{RESET}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA

(1) Specified by design.

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ELECTRICAL CHARACTERISTICS (continued)

PVDD_X = 32.5V, GVDD_X = 12V, VDD = 12V, T_C (Case temperature) = 75°C, f_S = 384kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	INPUT_X, M1, M2, M3, RESET	1.9			V
V_{IL}	Low level input voltage				0.8	V
I_{lkg}	Input leakage current				100	µA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW1}$ to VREG, $\overline{OTW2}$ to VREG, $\overline{SD}$ to VREG		20	26	33	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7kΩ to 5V	4.5		5	
V_{OL}	Low level output voltage	I_O = 4mA		200	500	mV
FANOUT	Device fanout $\overline{OTW1}$, $\overline{OTW2}$, $\overline{SD}$, $\overline{CLIP}$, $\overline{READY}$	No external pullup		30		devices

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TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC+NOISE vs OUTPUT POWER

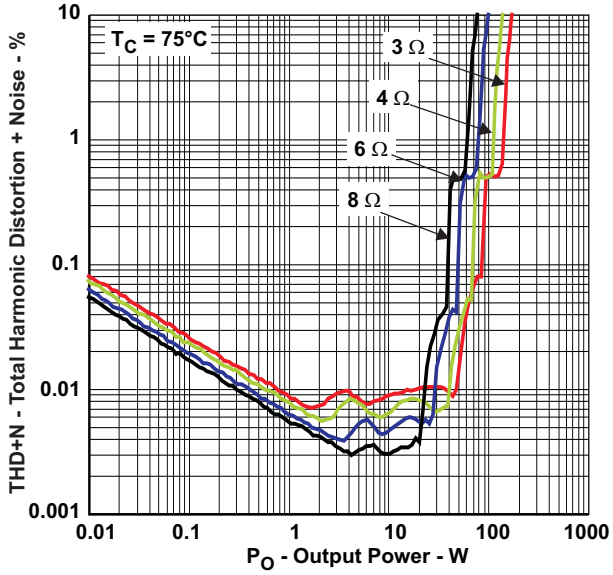

Figure 1.

OUTPUT POWER vs SUPPLY VOLTAGE

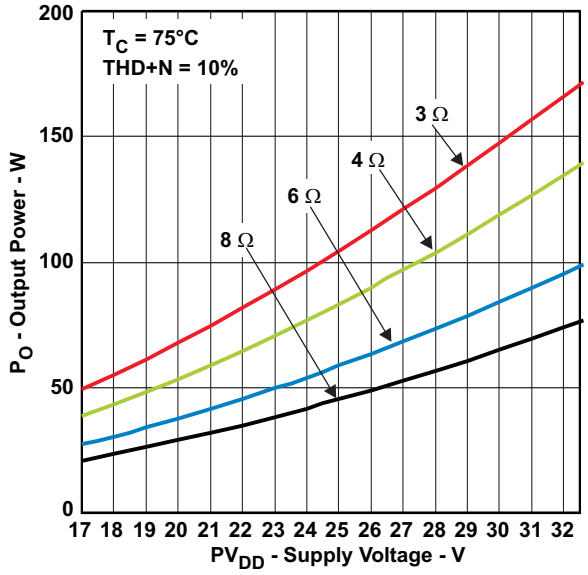

Figure 2.

UNCLIPPED OUTPUT POWER vs SUPPLY VOLTAGE

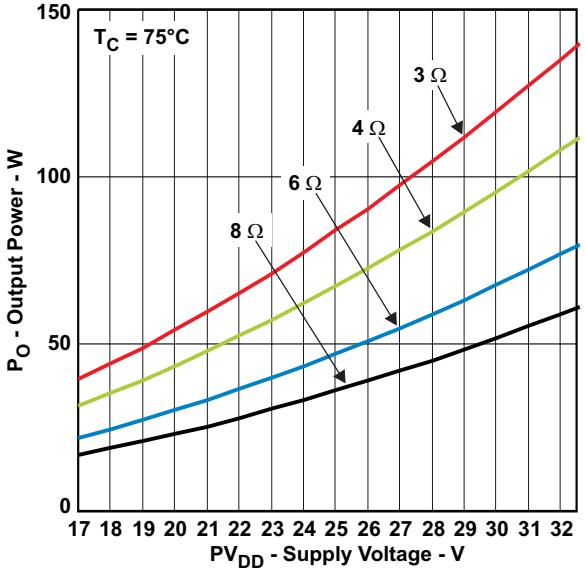

Figure 3.

SYSTEM EFFICIENCY vs OUTPUT POWER

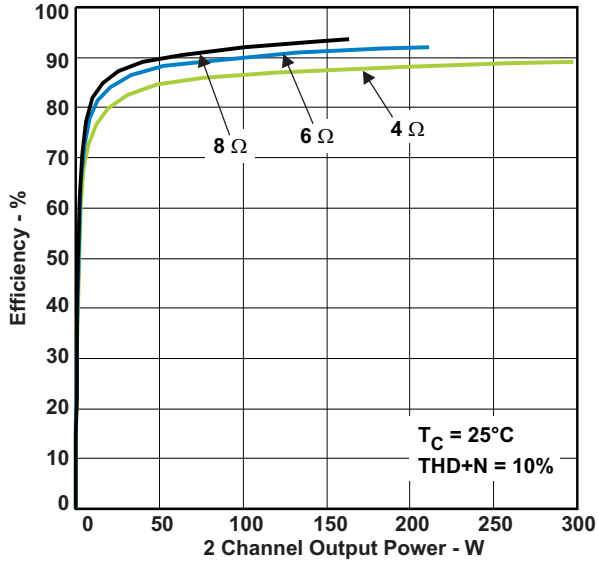

Figure 4.

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TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

SYSTEMS POWER LOSS vs OUTPUT POWER

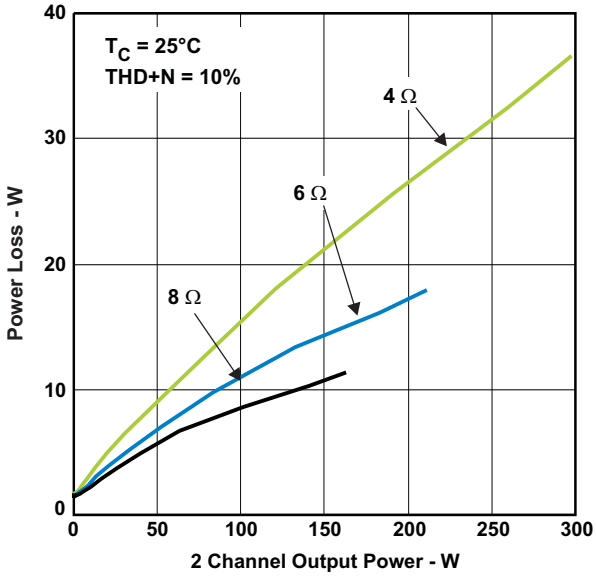

Figure 5.

OUTPUT POWER vs CASE TEMPERATURE

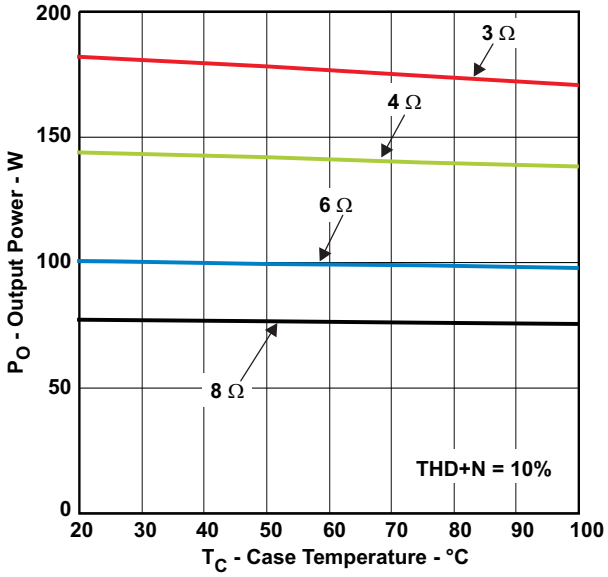

Figure 6.

NOISE AMPLITUDE vs FREQUENCY

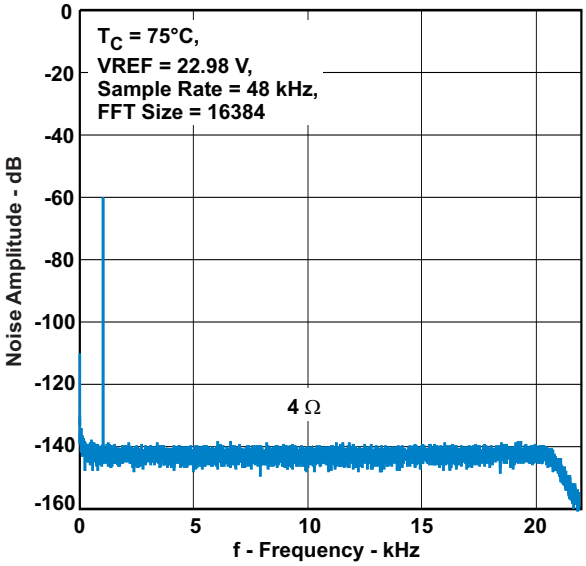

Figure 7.

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

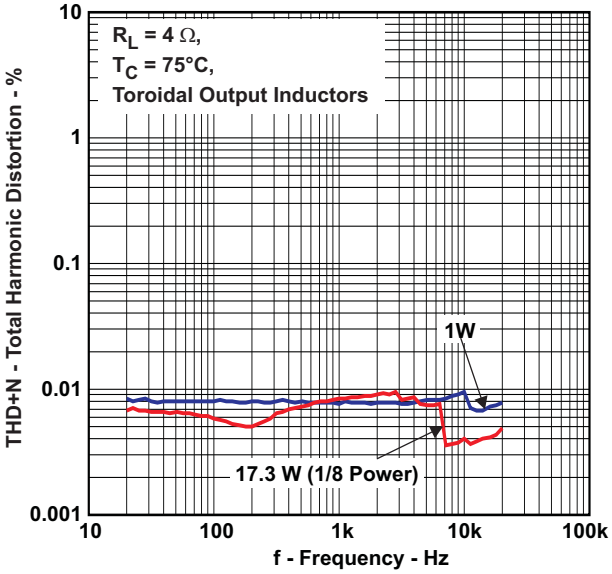

Figure 8.

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TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

TOTAL HARMONIC+NOISE vs OUTPUT POWER

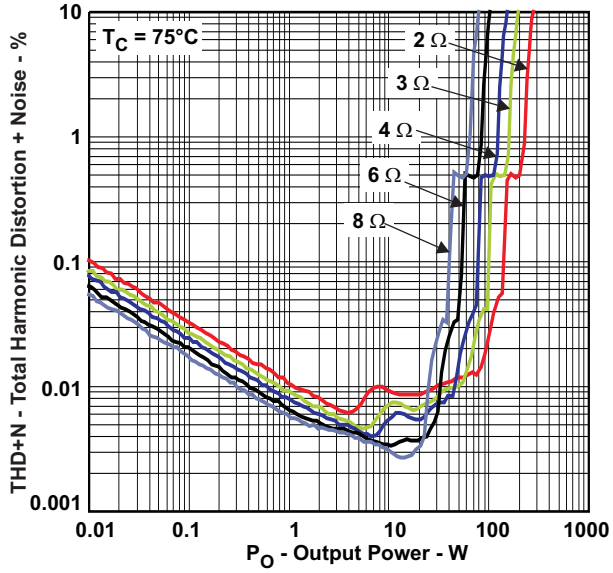

Figure 9.

OUTPUT POWER vs SUPPLY VOLTAGE

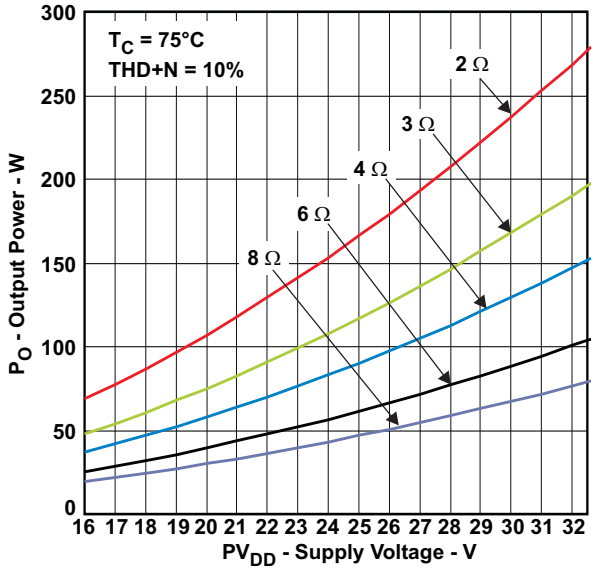

Figure 10.

OUTPUT POWER vs CASE TEMPERATURE

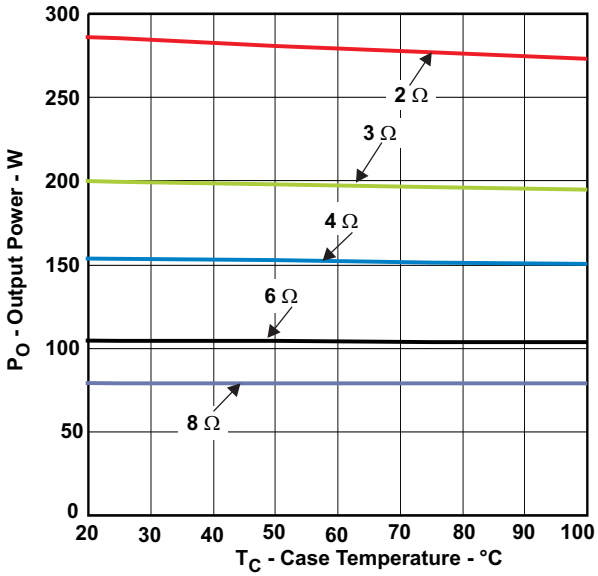

Figure 11.

APPLICATION INFORMATION

PCB MATERIAL RECOMMENDATION

FR-4 Glass Epoxy material with 2oz. (70µm) is recommended for use with the TAS5612A. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

PVDD CAPACITOR RECOMMENDATION

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000µF, 50V support more applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

DECOUPLING CAPACITOR RECOMMENDATION

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 0.1µF that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50V is required for use with a 32.5v power supply.

SYSTEM DESIGN RECOMMENDATIONS

The following schematics and PCB layouts illustrate *best practices* in the use of the TAS5612A.

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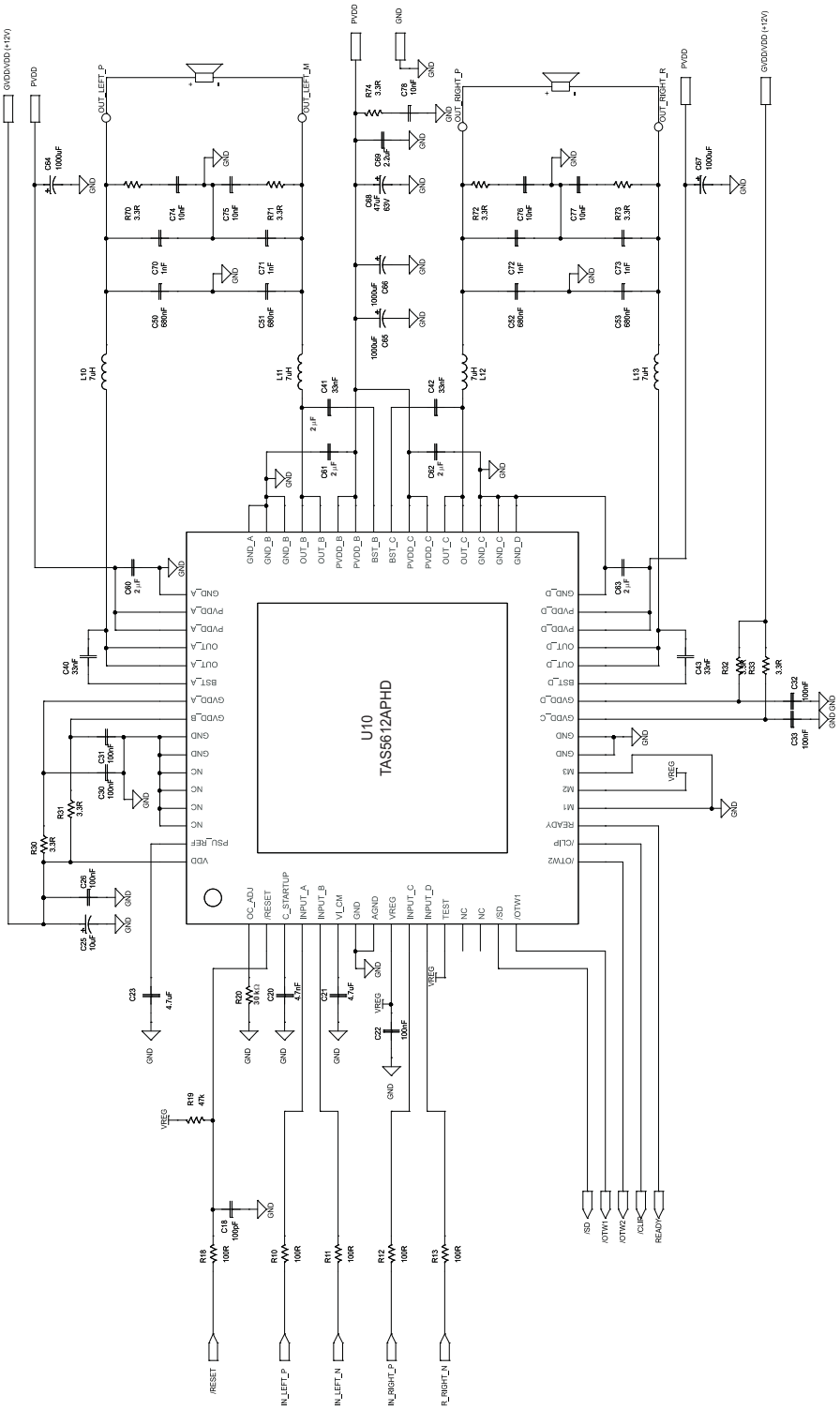

Figure 12. Typical Differential (2N) BTL Application With BD Modulation Filters

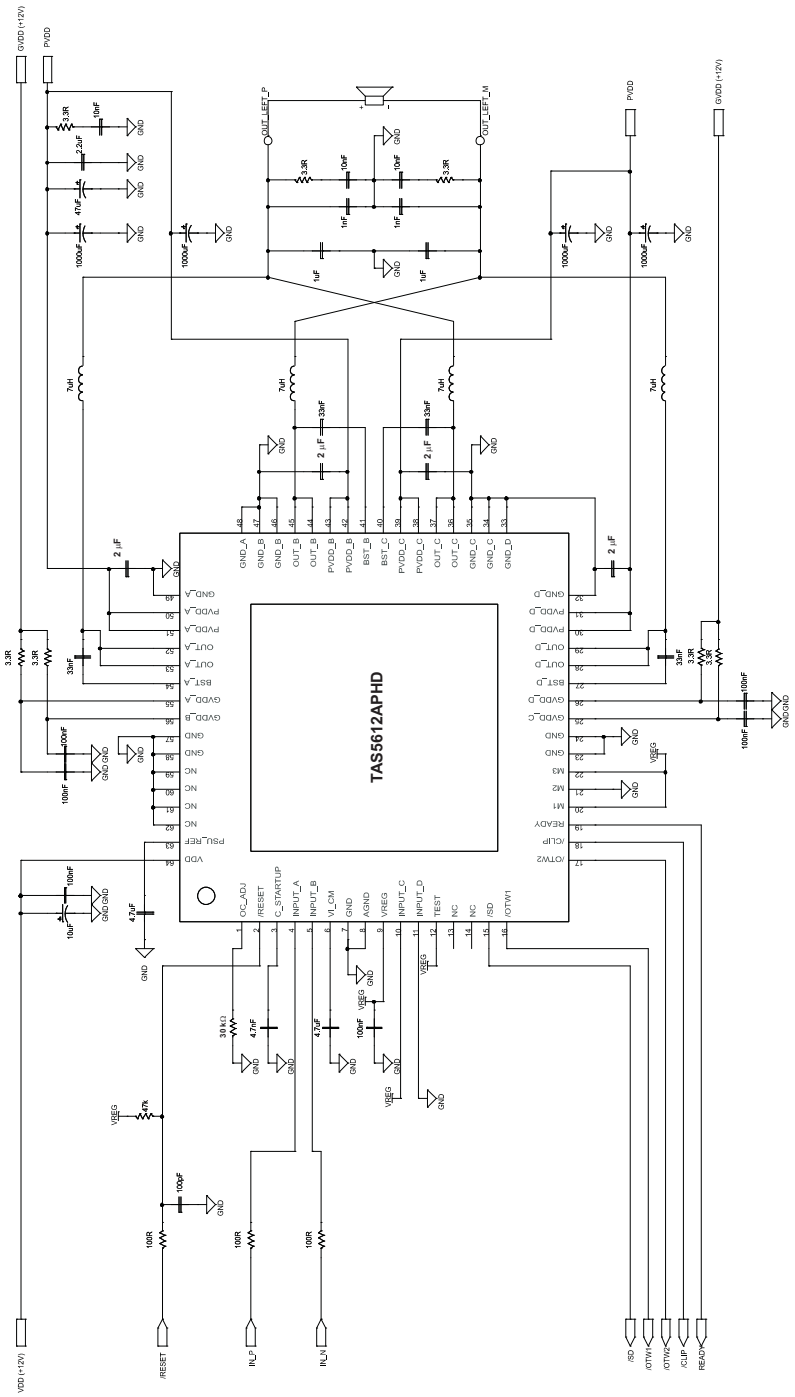

Figure 13. Typical (2N) PBTL Application With BD Modulation Filters

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THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5612A needs only a 12V supply in addition to the (typical) 32.5V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12 V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300kHz to 4000kHz, it is recommended to use 33nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2µF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5612A reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 32.5V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5612A is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the Recommended Operating Conditions table of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5612A does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

Powering Down

The TAS5612A does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks.

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ERROR REPORTING

The $\overline{SD}$, $\overline{OTW}$, $\overline{OTW1}$ and $\overline{OTW2}$ pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ and $\overline{OTW2}$ goes low when the device junction temperature exceeds 125°C and $\overline{OTW1}$ goes low when the junction temperature exceeds 100°C (see the following table).

$\overline{SD}$	$\overline{OTW1}$	$\overline{OTW2}$, $\overline{OTW}$	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP)
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting $\overline{RESET}$ low forces the $\overline{SD}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{OTW}$ signal using the system micro controller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3V is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5V logic can be obtained by adding external pullup resistors to 5V (see the Electrical Characteristics table of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

The TAS5612A contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5612A responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the SD pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, i.e., the supply voltage has increased.

The device will function on errors, as shown in the following table.

BTL Mode		PBTL Mode		SE Mode	
Local Error In	Turns Off	Local Error In	Turns Off	Local Error In	Turns Off
A	A+B	A	A+B+C+D	A	A+B
B		B		B	
C	C+D	C		C	C+D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge.

PIN-TO-PIN SHORT CIRCUIT PROTECTION (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an over current after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup i.e. when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup will not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed, the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is

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<15 ms/µF. While the PPSC detection is in progress, $\overline{SD}$ is kept low, and the device will not react to changes applied to the $\overline{RESET}$ pins. If no shorts are present the PPSC detection passes, and $\overline{SD}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert resistive load to GND_X or PVDD_X.

OVERTEMPERATURE PROTECTION

PHD Package

The TAS5612A PHD package option has a three-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW1}$) when the device junction temperature exceeds 100°C (typical), ($\overline{OTW2}$) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{RESET}$ must be asserted. Thereafter, the device resumes normal operation.

UNDERVOLTAGE PROTECTION (UVP) AND POWER-ON RESET (POR)

The UVP and POR circuits of the TAS5612A fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the Electrical Characteristics table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the $\overline{SD}$ output, i.e., SD is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{SD}$.

SYSTEM DESIGN CONSIDERATION

A rising-edge transition on reset input allows the device to execute the startup sequence and starts switching.

Apply only audio when the state of READY is high that will start and stop the amplifier without having audible artifacts that is heard in the output transducers. If an overcurrent protection event is introduced the READY signal goes low, hence, filtering is needed if the signal is intended for audio muting in non micro controller systems.

The CLIP signal is indicating that the output is approaching clipping. The signal can be used to either an audio volume decrease or intelligent power supply controlling a low and a high rail.

The device is inverting the audio signal from input to output.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

PRINTED CIRCUIT BOARD RECOMMENDATION

Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high fast switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing the audio input should be kept short and together with the accompanied audio source ground. A local ground area underneath the device is important to keep solid to minimize ground bounce.

Netlist for this printed circuit board is generated from the schematic in Figure 12.

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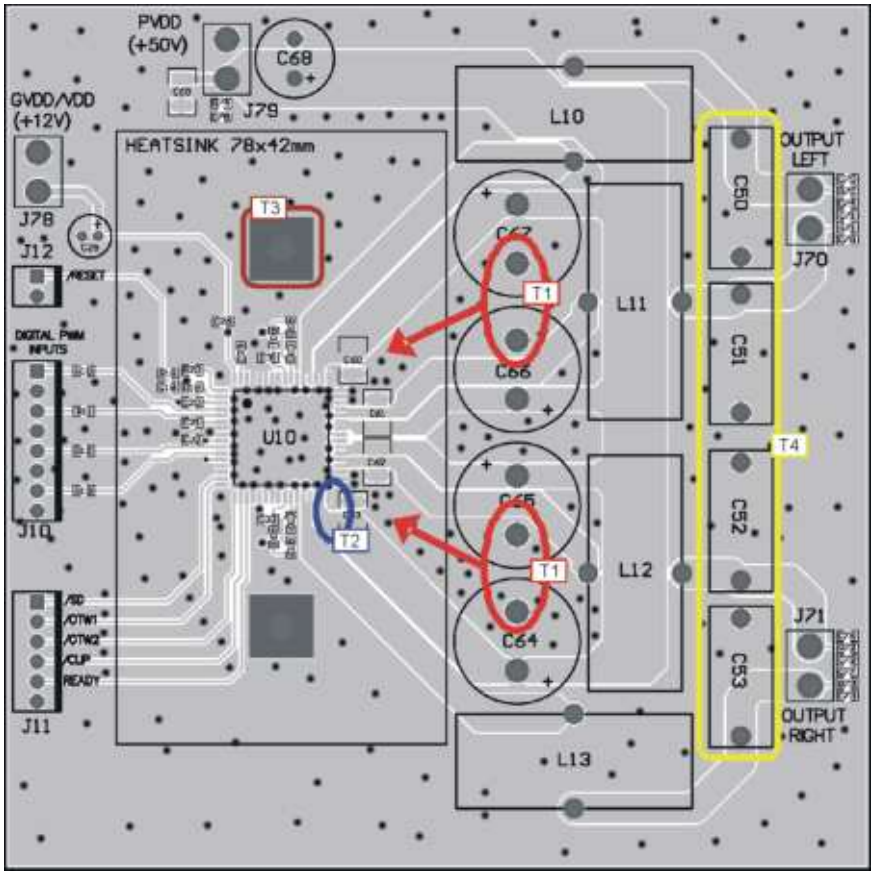

Note T1: PVDD decoupling bulk capacitors C60-C64 should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

Note T2: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

Note T3: Heat sink needs to have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range preferable metal film types.

Figure 14. Printed Circuit Board - Top Layer

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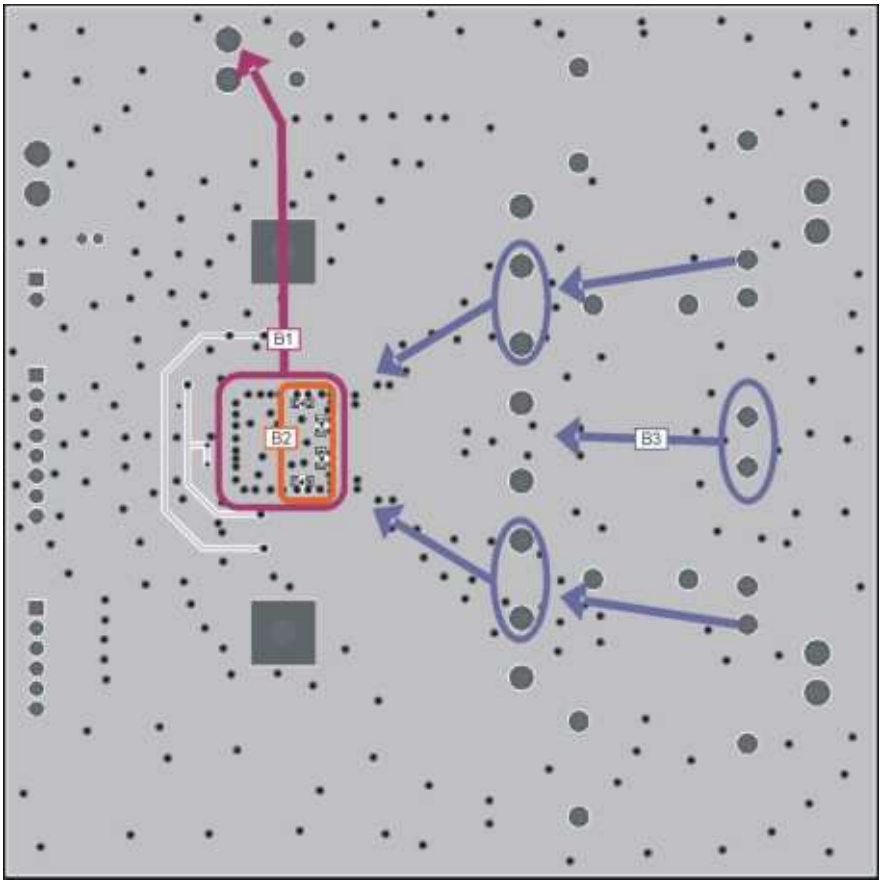

Note B1: It is important to have a direct low impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low impedance X7R ceramic capacitors placed on bottom side providing a short low inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors.

Figure 15. Printed Circuit Board - Bottom Layer

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REVISION HISTORY

Note: Page numbers of current version may differ from previous versions.

Changes from Original (June 2010) to Revision A	Page
• Deleted DKD (44-Pin PSOP3 from the Features	1
• Changed "Both pakage types" to "The package type" in paragraph under Terminal Assignment and deleted the DKD PACKAGE drawing	2
• Deleted the TAS5612ADKD column in the PACKAGE HEAT DISSIPATON RATINGS table	3
• Deleted the TAS5612ADKD row in the ORDERING INFORMATION table	3
• Changed the Junction temperature in the ROC table in the MAX column from 150 to 125	4
• Deleted the DKD NO. column from the PIN FUNCTIONS table	5
• Deleted figure showing BTL application with BD modulation filters for the DKD device from SYSTEM DESIGN RECOMMENDATIONS section	14

Changes from Revision A (March 2011) to Revision B	Page
• Changed the AUDIO CHARAC (BTL) table $\|V_{OS}\|$ row, TYP column from 20 to 5 mV and MAX column from 30 to 18 mV	8
• Changed V_{UVP}, G spec (first row under I/O PROTECTION in ELEC CHARA table) from "Undervoltage.....GVDD_x" to "Undervoltage.....GVDD_x, VDD" and the TYP column from "10" to "9.5" V	9

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5612APHD	Active	Production	HTQFP (PHD) | 64	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5612A
TAS5612APHD.A	Active	Production	HTQFP (PHD) | 64	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5612A
TAS5612APHD.B	Active	Production	HTQFP (PHD) | 64	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5612A
TAS5612APHDR	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5612A
TAS5612APHDR.A	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5612A
TAS5612APHDR.B	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5612A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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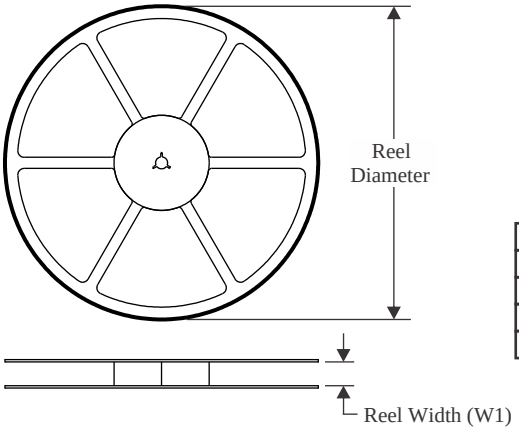
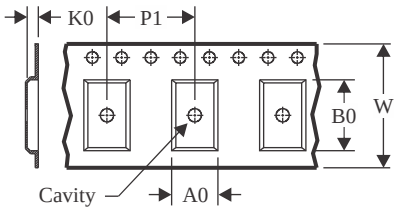
TAPE AND REEL INFORMATION

REEL DIMENSIONS

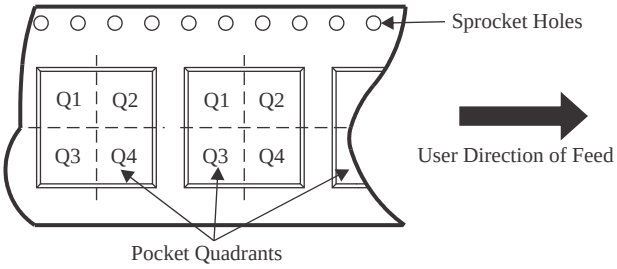


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

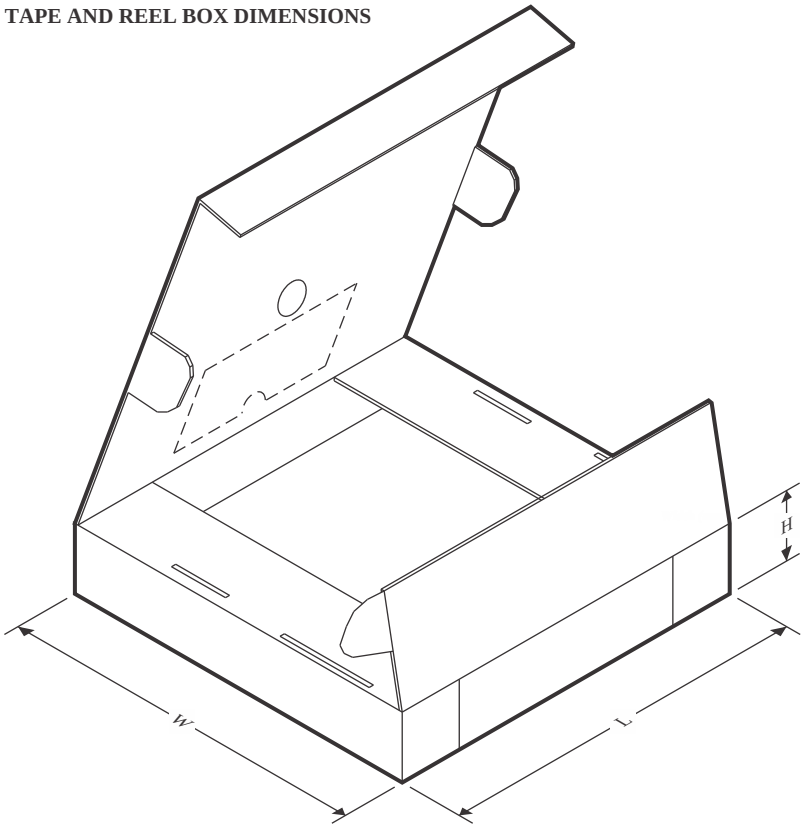
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5612APHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

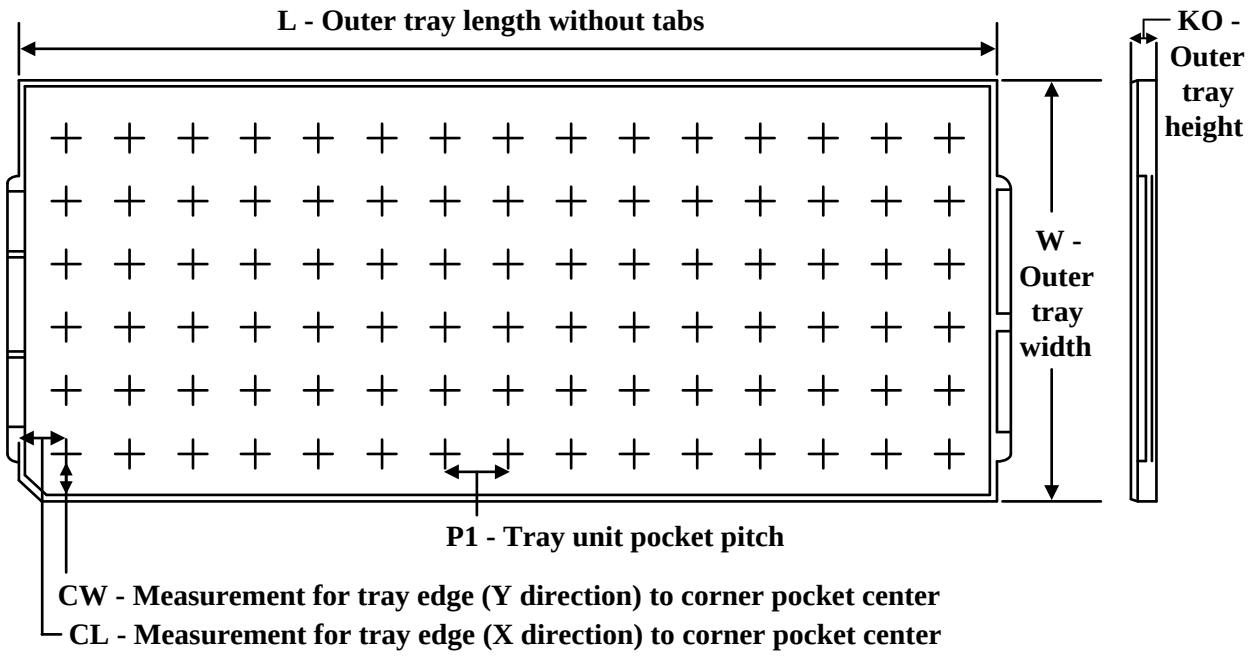
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5612APHDR	HTQFP	PHD	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TAS5612APHD	PHD	HTQFP	64	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
TAS5612APHD.A	PHD	HTQFP	64	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
TAS5612APHD.B	PHD	HTQFP	64	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45

GENERIC PACKAGE VIEW

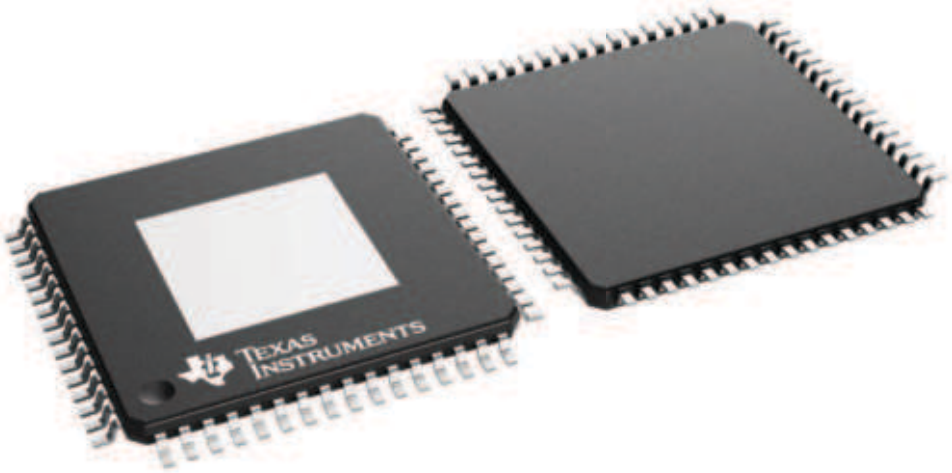
PHD 64

HTQFP - 1.2 mm max height

14 x 14, 0.8 mm pitch

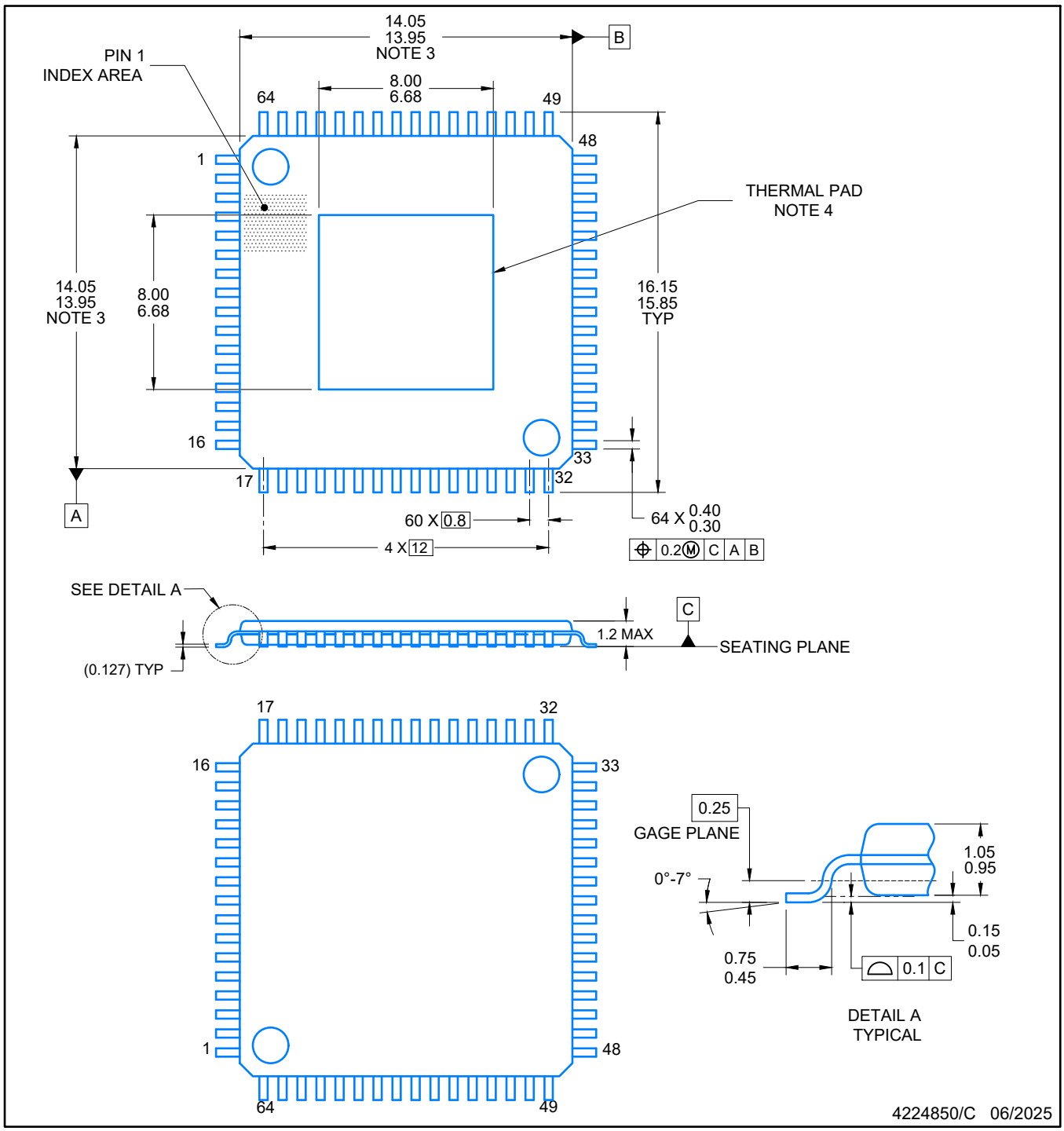
PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



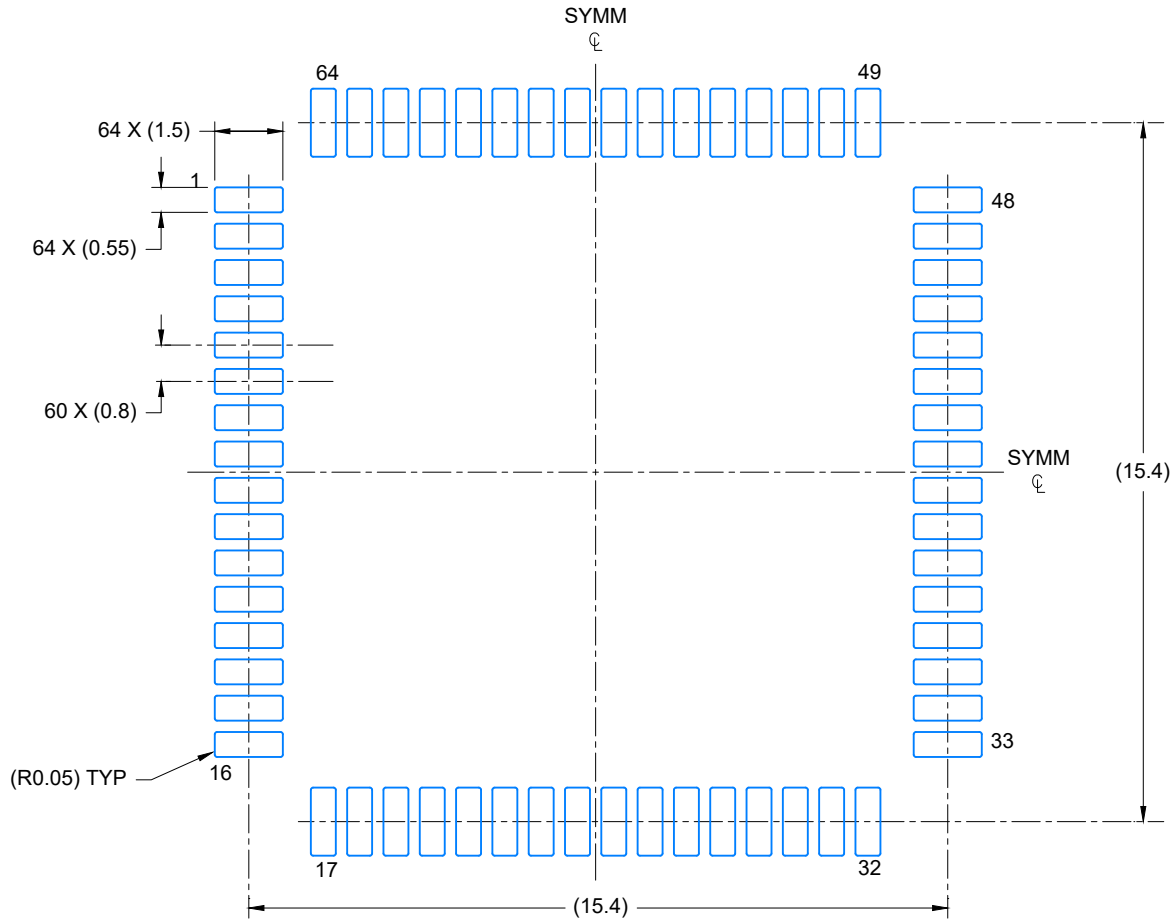
4224851/B

PLASTIC QUAD FLATPACK

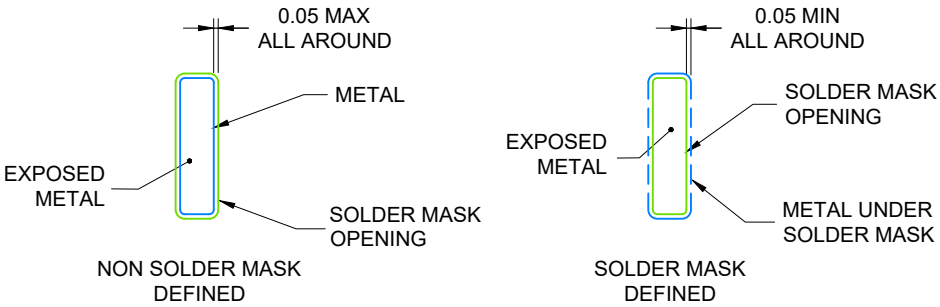


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



SOLDER MASK DETAILS

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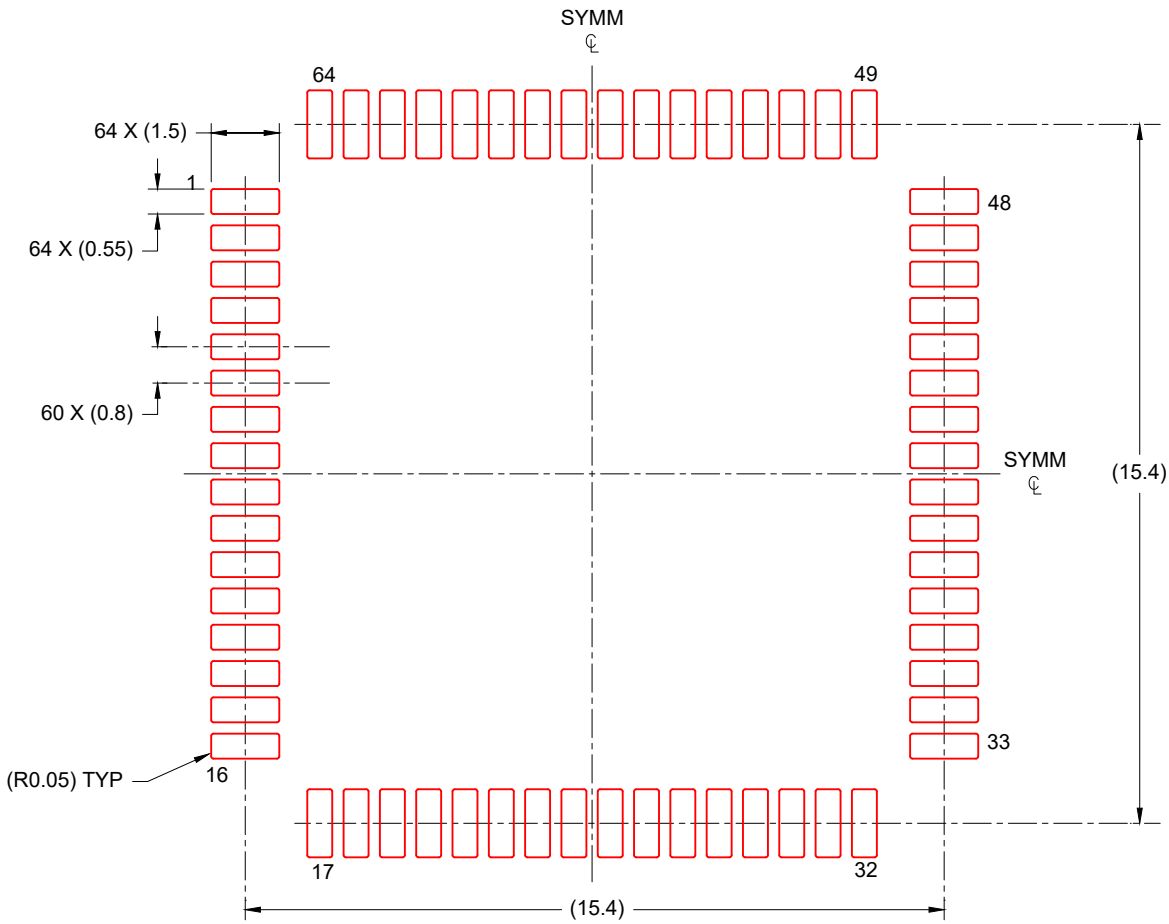
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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