TAS5630B 300-W Stereo and 400-W Mono PurePath™ HD Analog-Input Power Stage

1 Features

- PurePath™ HD Enabled Integrated Feedback Provides:
  - Signal Bandwidth up to 80 kHz for High-Frequency Content From HD Sources
  - Ultralow 0.03% THD at 1 W into 4 Ω
  - Flat THD at All Frequencies for Natural Sound
  - 80-dB PSRR (BTL, No Input Signal)
  - > 100-dB (A-weighted) SNR
  - Click- and Pop-Free Start-up
- Multiple Configurations Possible on the Same PCB With Stuffing Options:
  - Mono Parallel Bridge-Tied Load (PBTL)
  - Stereo Bridge-Tied Load (BTL)
  - 2.1 Single-Ended Stereo Pair and BTL Subwoofer
  - Quad Single-Ended Outputs
- Total Output Power at 10% THD+N
  - 400 W in Mono PBTL Configuration
  - 300 W per Channel in Stereo BTL Configuration
  - 145 W per Channel in Quad Single-Ended Configuration
- High-Efficiency Power Stage (> 88%) With 60-mΩ Output MOSFETs
- Two Thermally Enhanced Package Options:
  - PHD (64-Pin QFP)
  - DKD (44-Pin PSOP3)
- Self-Protection Design (Including Undervoltage, Overtemperature, Clipping, and Short-Circuit Protection) With Error Reporting
- EMI Compliant When Used With Recommended System Design

2 Applications

- Mini Combo System
- AV Receivers
- DVD Receivers
- Active Speakers

3 Description

The TAS5630B device is a high-performance analog-input class-D amplifier with integrated closed-loop feedback technology (known as PurePath HD technology) with the ability to drive up to 300 W [(1)] stereo into 4-Ω to 8-Ω speakers from a single 50-V supply.

PurePath HD technology enables traditional AB-amplifier performance (< 0.03% THD) levels while providing the power efficiency of traditional class-D amplifiers.

Unlike traditional class-D amplifiers, the distortion curve does not increase until the output levels move into clipping.

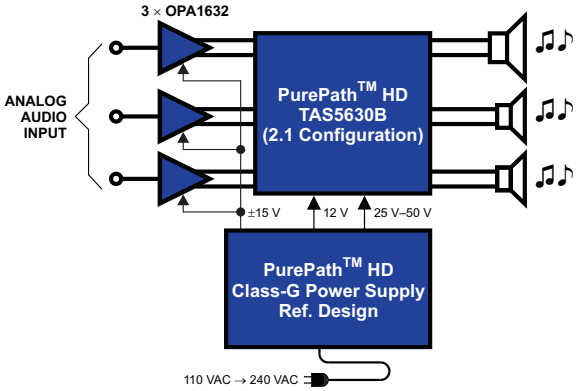
PurePath HD technology enables lower idle losses, making the device even more efficient. When coupled with TI's class-G power-supply reference design for TAS563x, industry-leading levels of efficiency can be achieved.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5630B	HSSOP (44)	15.90 mm × 11.00 mm
	HTQFP (64)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical TAS5630B Application Block Diagram



(1) Achievable output power levels are dependent on the thermal configuration of the target application. A high-performance thermal interface material between the exposed package heat slug and the heat sink should be used to achieve high output power levels.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (September 2012) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Thermal Information table data. ... 8

Changes from Revision B (November 2011) to Revision C — **Page**

- Changed Analog comparator reference node, VI_CM Vlaues From: MIN = 1.5 TYP = 1.75 MAX = 1.9 To: MIN = 1.75 TYP = 2 MAX = 2.15 ... 8
- Changed ANALOG INPUTS - V_{IN} TYP value From 3.5 to 5 V_{PP} ... 8
- Changed the V_{IH} and V_{IL} Test Conditions From: INPUT_X, M1, M2, M3, RESET To: M1, M2, M3, RESET ... 9
- Deleted - R_L = 2 Ω, 1% THD+N, unclipped output signal From P_O in the Audio Specification (PBTL) table ... 11

Changes from Revision A (November 2011) to Revision B — **Page**

- Changed the R_{INT_PU} parameters from /OTW1 to VREG, /OTW2 to VREG, /SD to VREG to /OTW, /OTW1, /OTW2, /CLIP, READY, /SD to VRE ... 9
- Added text to the PHD Package section. ... 17
- Added text to the DKD Package section ... 17

Changes from Original (November 2010) to Revision A — **Page**

- Changed Title From: 600-W MONO To: 400-W MONO ... 1
- Changed Feature From: 600 W per Channel in Mono PBTL Configuration To: 400 W per Channel in Mono PBTL Configuration ... 1
- Changed the Pin One Location Package image ... 5
- Changed R_L(PBTL) Load Impedance Min value From: 1.6 Ω To: 2.4 Ω, and Typ value From 2 To: 3 Ω ... 7
- Added footnotes to the ROC table ... 7
- Added R_{OCP} information to the ROC Table ... 8

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- Changed the I_{OC} Typical Value From: 19 A To: 15 A 9
- Deleted - R_L = 2 Ω, 10%, THD+N, clipped input signal From P_O in the Audio Specification (PBTL) table 11
- Replaced the TYPICAL CHARACTERISTICS, PBTL CONFIGURATION graphs 12
- Added section - Click and Pop in SE-Mode 18
- Added section - PBTL Overload and Short Circuit 18
- Replaced the PACKAGE HEAT DISSIPATION RATINGS table with the THERMAL INFORMATION table 18

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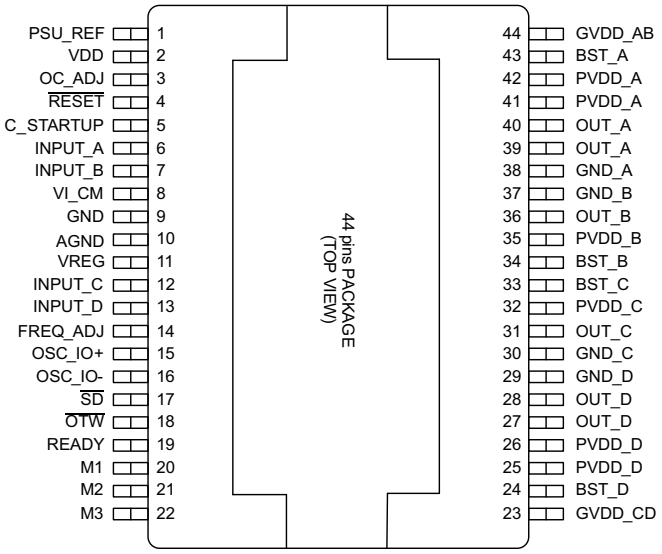
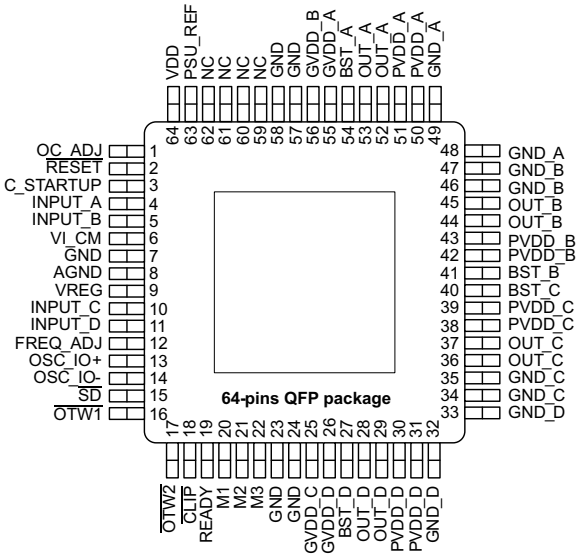
5 Pin Configuration and Functions

DKD Package
44 Pins HSSOP
Top View



PHD Package
64 Pins HTQFP
Top View



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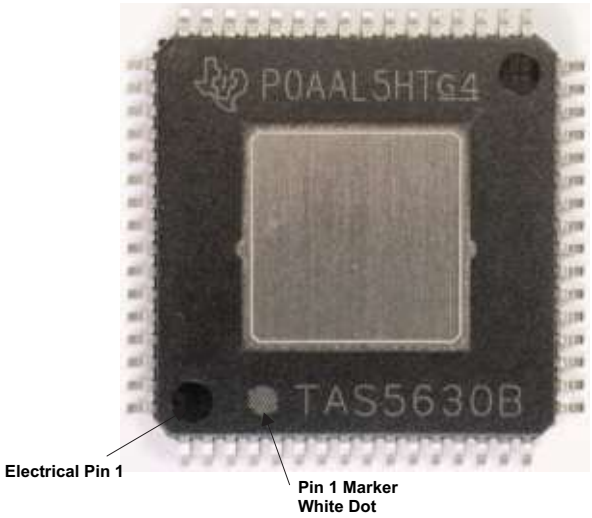

Figure 1. Pin One Location PHD Package

Pin Functions

PIN			FUNCTION(1)	DESCRIPTION
NAME	HTQFP	HSSOP		
AGND	8	10	P	Analog ground
BST_A	54	43	P	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_A required.
BST_B	41	34	P	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_B required.
BST_C	40	33	P	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_C required.
BST_D	27	24	P	HS bootstrap supply (BST), external 0.033-µF capacitor to OUT_D required.
$\overline{\text{CLIP}}$	18	—	O	Clipping warning; open drain; active-low
C_STARTUP	3	5	O	Start-up ramp requires a charging capacitor of 4.7 nF to AGND in BTL mode
FREQ_ADJ	12	14	I	PWM frame-rate-programming pin requires resistor to AGND
GND	7, 23, 24, 57, 58	9	P	Ground
GND_A	48, 49	38	P	Power ground for half-bridge A
GND_B	46, 47	37	P	Power ground for half-bridge B
GND_C	34, 35	30	P	Power ground for half-bridge C
GND_D	32, 33	29	P	Power ground for half-bridge D
GVDD_A	55	—	P	Gate-drive voltage supply requires 0.1-µF capacitor to GND_A
GVDD_B	56	—	P	Gate drive voltage supply requires 0.1-µF capacitor to GND_B
GVDD_C	25	—	P	Gate drive voltage supply requires 0.1-µF capacitor to GND_C
GVDD_D	26	—	P	Gate drive voltage supply requires 0.1-µF capacitor to GND_D
GVDD_AB	—	44	P	Gate drive voltage supply requires 0.22-µF capacitor to GND_A/GND_B
GVDD_CD	—	23	P	Gate drive voltage supply requires 0.22-µF capacitor to GND_C/GND_D
INPUT_A	4	6	I	Input signal for half-bridge A
INPUT_B	5	7	I	Input signal for half-bridge B
INPUT_C	10	12	I	Input signal for half-bridge C
INPUT_D	11	13	I	Input signal for half-bridge D
M1	20	20	I	Mode selection
M2	21	21	I	Mode selection
M3	22	22	I	Mode selection
NC	59–62	–	—	No connect; pins may be grounded.

(1) I = Input, O = Output, P = Power

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Pin Functions (continued)

PIN			FUNCTION(1)	DESCRIPTION
NAME	HTQFP	HSSOP		
OC_ADJ	1	3	O	Analog overcurrent-programming pin requires resistor to AGND. 64-pin package (PHD) = 22 kΩ. 44-pin PSOP3 (DKD) = 24 kΩ
OSC_IO+	13	15	I/O	Oscillator master/slave output/input
OSC_IO–	14	16	I/O	Oscillator master/slave output/input
$\overline{\text{OTW}}$	—	18	O	Overtemperature warning signal, open-drain, active-low
$\overline{\text{OTW1}}$	16	—	O	Overtemperature warning signal, open-drain, active-low
$\overline{\text{OTW2}}$	17	—	O	Overtemperature warning signal, open-drain, active-low
OUT_A	52, 53	39, 40	O	Output, half-bridge A
OUT_B	44, 45	36	O	Output, half-bridge B
OUT_C	36, 37	31	O	Output, half-bridge C
OUT_D	28, 29	27, 28	O	Output, half-bridge D
PSU_REF	63	1	P	PSU reference requires close decoupling of 330 pF to AGND.
PVDD_A	50, 51	41, 42	P	Power-supply input for half-bridge A requires close decoupling of 0.01-µF capacitor in parallel with 2.2-µF capacitor to GND_A.
PVDD_B	42, 43	35	P	Power-supply input for half-bridge B requires close decoupling of 0.01-µF capacitor in parallel with 2.2-µF capacitor to GND_B.
PVDD_C	38, 39	32	P	Power-supply input for half-bridge C requires close decoupling of 0.0- µF capacitor in parallel with 2.2-µF capacitor to GND_C.
PVDD_D	30, 31	25, 26	P	Power-supply input for half-bridge D requires close decoupling of 0.01-µF capacitor in parallel with 2.2-µF capacitor to GND_D.
READY	19	19	O	Normal operation; open-drain; active-high
$\overline{\text{RESET}}$	2	4	I	Device reset input; active-low
$\overline{\text{SD}}$	15	17	O	Shutdown signal, open-drain, active-low
VDD	64	2	P	Power supply for digital voltage regulator requires a 10-µF capacitor in parallel with a 0.1-µF capacitor to GND for decoupling.
VI_CM	6	8	O	Analog comparator reference node requires close decoupling of 1 nF to AGND.
VREG	9	11	P	Regulator supply filter pin requires 0.1-µF capacitor to AGND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted (1)

	MIN	MAX	UNIT
VDD to AGND	–0.3	13.2	V
GVDD to AGND	–0.3	13.2	V
PVDD_X to GND_X(2)	–0.3	69	V
OUT_X to GND_X(2)	–0.3	69	V
BST_X to GND_X(2)	–0.3	82.2	V
BST_X to GVDD_X(2)	–0.3	69	V
VREG to AGND	–0.3	4.2	V
GND_X to GND	–0.3	0.3	V
GND_X to AGND	–0.3	0.3	V
OC_ADJ, M1, M2, M3, OSC_IO+, OSC_IO–, FREQ_ADJ, VI_CM, C_STARTUP, PSU_REF to AGND	–0.3	4.2	V
INPUT_X	–0.3	7	V
$\overline{\text{RESET}}$, $\overline{\text{SD}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$ to AGND	–0.3	7	V
Continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW1}}$, $\overline{\text{OTW2}}$, $\overline{\text{CLIP}}$, $\overline{\text{READY}}$)		9	mA
Operating junction temperature, T_J	0	150	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	25	50	52.5	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance (1)	Output filter according to schematics in the application information section	3.5	4		Ω
R_L(SE) (2)			1.8	2		
R_L(PBTL) (2)			2.4	3		
L_{OUTPUT}(BTL)	Output filter inductance (1)	Minimum output inductance at I_{OC}	7	10		µH
L_{OUTPUT}(SE) (2)			7	15		
L_{OUTPUT}(PBTL) (2)			7	10		
f_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% resistor tolerance.	Nominal	385	400	415	kHz
		AM1	315	333	350	
		AM2	260	300	335	
R_{FREQ_ADJ}	PWM frame-rate-programming resistor	Nominal; master mode	9.9	10	10.1	kΩ
		AM1; master mode	19.8	20	20.2	
		AM2; master mode	29.7	30	30.3	

(1) Values are for actual measured impedance over all combinations of tolerance, current and temperature and not simply the component rating.
(2) See additional details for SE and PBTL in *System Design Considerations*.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{FREQ_ADJ}	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
R_{OCP}	Overcurrent-protection-programming resistor, cycle-by-cycle mode	64-pin QFP package (PHD)	22		33	kΩ
		44-Pin PSOP3 package (DKD)	24		33	
	Overcurrent-protection-programming resistor, latching mode	PHD or DKD	47		68	
T_J	Junction temperature		0		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TAS5630B		UNIT
		PHD (HTQFP)	DKD (HSSOP)	
		64 PINS	44 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	8.6	8.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	0.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	2.1	3.0	
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	
ψ_{JB}	Junction-to-board characterization parameter	2.1	3.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 400 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
VREG	Voltage regulator, only used as reference node, VREG	VDD = 12 V	3	3.3	3.6	V
VI_CM	Analog comparator reference node, VI_CM		1.75	2	2.15	V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		22.5		mA
		Idle, reset mode		22.5		
I_{GVDD_X}	GVDD_x gate-supply current per half-bridge	50% duty cycle		12.5		mA
		Reset mode		1.5		
I_{PVDD_X}	Half-bridge supply current	50% duty cycle with recommended output filter		13.3		mA
		Reset mode, No switching		870		µA
ANALOG INPUTS						
R_{IN}	Input resistance	READY = HIGH		33		kΩ
V_{IN}	Maximum input voltage with symmetrical output swing			5		V_{PP}
I_{IN}	Maximum input current			342		µA
G	Voltage gain (V_{OUT}/V_{IN})			23		dB
OSCILLATOR						
f_{OSC_IO+}	Nominal, master mode	F_{PWM} × 10	3.85	4	4.15	MHz
	AM1, master mode		3.15	3.33	3.5	
	AM2, master mode		2.6	3	3.35	
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V

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Electrical Characteristics (continued)

PVDD_X = 50 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 400 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, excludes metallization resistance, GVDD = 12 V		60	100	mΩ
	Drain-to-source resistance, high side (HS)			60	100	
I/O PROTECTION						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_x and VDD			9.5		V
$V_{uvp,hyst}$ (1)				0.6		V
OTW1 (1)	Overtemperature warning 1		95	100	105	°C
OTW2 (1)	Overtemperature warning 2		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{OTW}$ to be inactive after $\overline{OTW}$ event			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
	OTE-OTW differential			30		°C
OTE_{hyst} (1)	A reset must occur for $\overline{SD}$ to be released following an OTE event.			25		
OLPC	Overload protection counter	f_{PWM} = 400 kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1-Ω load, 64-pin QFP package (PHD) R_{OCP} = 22 kΩ		15		A
		Resistor – programmable, nominal peak current in 1-Ω load, 44-pin PSOP3 package (DKD), R_{OCP} = 24 kΩ		15		
	Overcurrent limit protection, latched	Resistor – programmable, nominal peak current in 1-Ω load, R_{OCP} = 47 kΩ		15		
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent		150		ns
I_{PD}	Internal pulldown resistor at output of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap charge. Not used in SE mode		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High-level input voltage	M1, M2, M3, RESET	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{lkg}	Input leakage current				100	µA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$, $\overline{OTW1}$, $\overline{OTW2}$, $\overline{CLIP}$, READY, $\overline{SD}$ to VREG		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		200	500	mV
FANOUT	Device fanout $\overline{OTW}$, $\overline{OTW1}$, $\overline{OTW2}$, $\overline{SD}$, $\overline{CLIP}$, READY	No external pullup		30		devices

(1) Specified by design.

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6.6 Audio Characteristics (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 400 kHz, R_{OC} = 22 kΩ, T_C = 75°C; output filter: L_{DEM} = 7 µH, C_{DEM} = 680 nF, MODE = 010, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 4 Ω, 10% THD+N, clipped output signal		300		W
		R_L = 6 Ω, 10% THD+N, clipped output signal		210		
		R_L = 8 Ω, 10% THD+N, clipped output signal		160		
		R_L = 4 Ω, 1% THD+N, unclipped output signal		240		
		R_L = 6 Ω, 1% THD+N, unclipped output signal		160		
		R_L = 8 Ω, 1% THD+N, unclipped output signal		125		
THD+N	Total harmonic distortion + noise	1 W		0.03%		
V_n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded		270		µV
$\|V_{OS}\|$	Output offset voltage	Inputs ac-coupled to AGND		20	50	mV
SNR	Signal-to-noise ratio (1)	A-weighted, AES17 filter		100		dB
DNR	Dynamic range	A-weighted, AES17 filter		100		dB
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0, four channels switching (2)		2.7		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

6.7 Audio Specification (Single-Ended Output)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 400 kHz, R_{OC} = 22 kΩ, T_C = 75°C; output filter: L_{DEM} = 15 µH, C_{DEM} = 470 µF, MODE = 100, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N, clipped output signal		145		W
		R_L = 3 Ω, 10% THD+N, clipped output signal		100		
		R_L = 4 Ω, 10% THD+N, clipped output signal		75		
		R_L = 2 Ω, 1% THD+N, unclipped output signal		110		
		R_L = 3 Ω, 1% THD+N, unclipped output signal		75		
		R_L = 4 Ω, 1% THD+N, unclipped output signal		55		
THD+N	Total harmonic distortion + noise	1 W		0.07%		
V_n	Output integrated noise	A-weighted, AES17 filter, input capacitor grounded		340		µV
SNR	Signal-to-noise ratio (1)	A-weighted, AES17 filter		93		dB
DNR	Dynamic range	A-weighted, AES17 filter		93		dB
P_{idle}	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0, four channels switching (2)		2		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

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6.8 Audio Specification (PBTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 50 V, GVDD_X = 12 V, R_L = 3 Ω, f_S = 400 kHz, R_{OC} = 22 kΩ, T_C = 75°C; output filter: L_{DEM} = 7 µH, C_{DEM} = 1.5 µF, MODE = 101-10, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N, clipped output signal		400		W
		R_L = 4 Ω, 10% THD+N, clipped output signal		300		
		R_L = 3 Ω, 1% THD+N, unclipped output signal		310		
		R_L = 4 Ω, 1% THD+N, unclipped output signal		230		
THD+N	Total harmonic distortion + noise	1 W		0.05%		
V_n	Output integrated noise	A-weighted		260		µV
SNR	Signal to noise ratio (1)	A-weighted		100		dB
DNR	Dynamic range	A-weighted		100		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, four channels switching (2)		2.7		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

6.9 Typical Characteristics

6.9.1 BTL Configuration

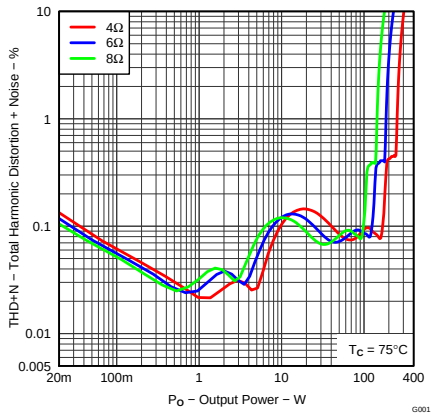

Figure 2. Total Harmonic + Noise vs Output Power

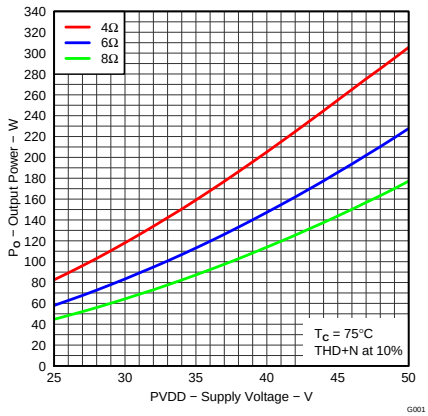

Figure 3. Output Power vs Supply Voltage

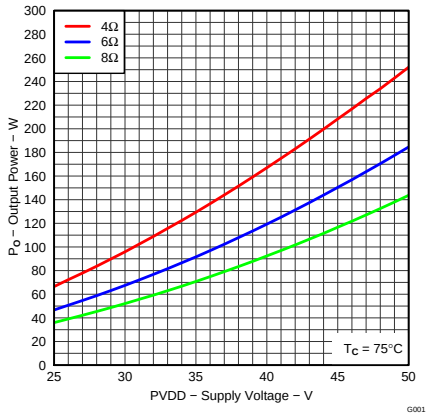

Figure 4. Unclipped Output Power vs Supply Voltage

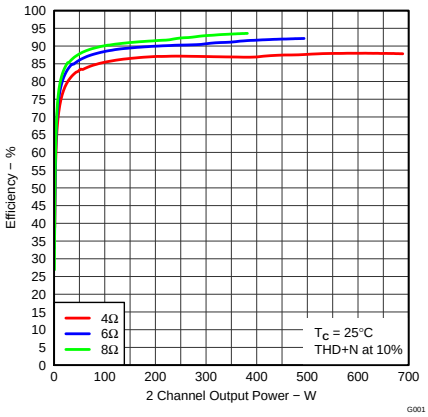

Figure 5. System Efficiency vs Output Power

BTL Configuration (continued)

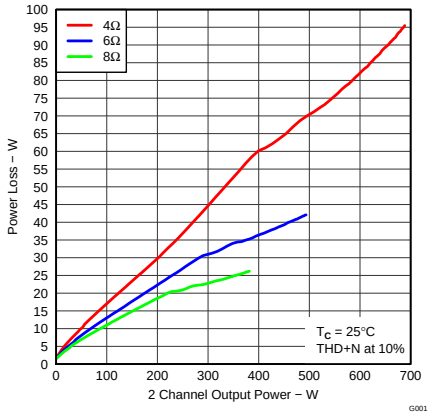

Figure 6. System Power Loss vs Output Power

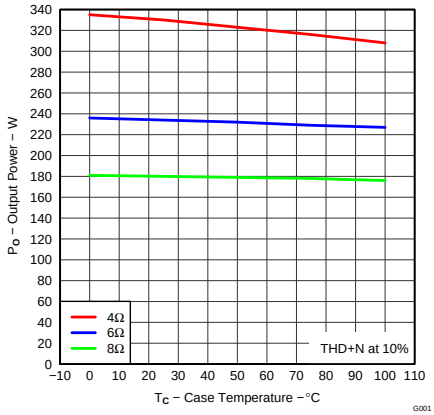

Figure 7. Output Power vs Case Temperature

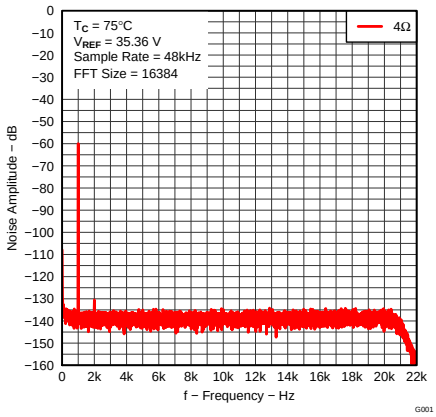

Figure 8. Noise Amplitude vs Frequency

6.9.2 SE Configuration

1 Channel Driven

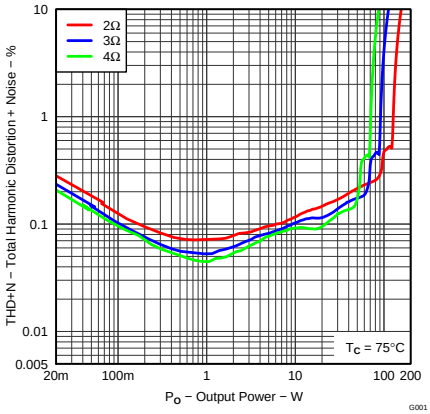

Figure 9. Total Harmonic Distortion + Noise vs Output Power

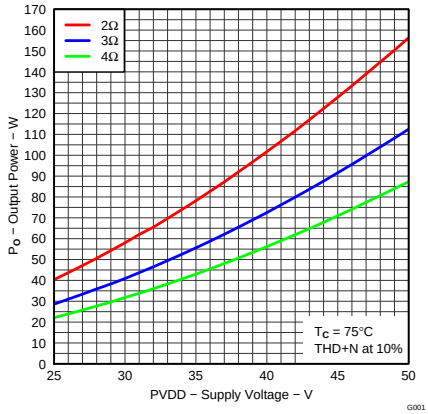

Figure 10. Output Power vs Supply Voltage

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SE Configuration (continued)

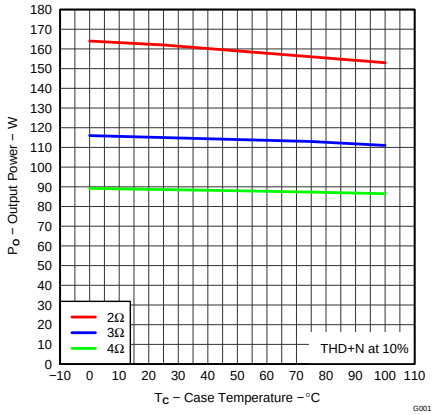


Figure 11. Output Power vs Case Temperature

6.9.3 PBTL Configuration

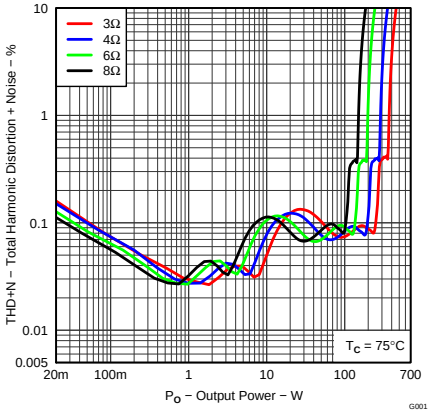


Figure 12. Total Harmonic Distortion + Noise vs Output Power

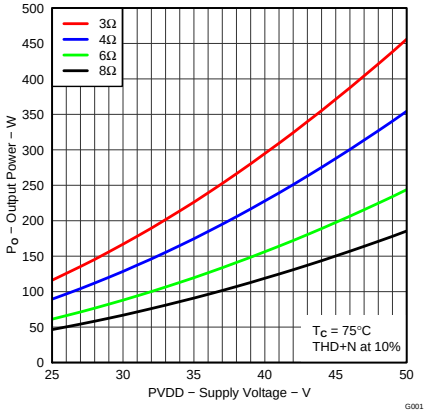


Figure 13. Output Power vs Supply Voltage

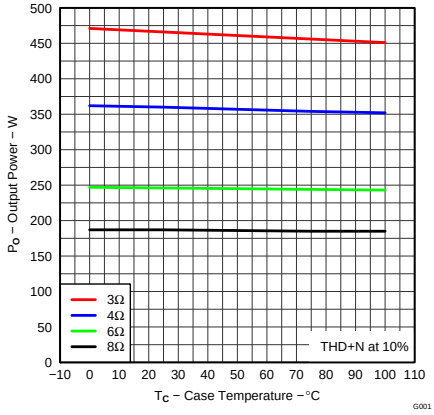


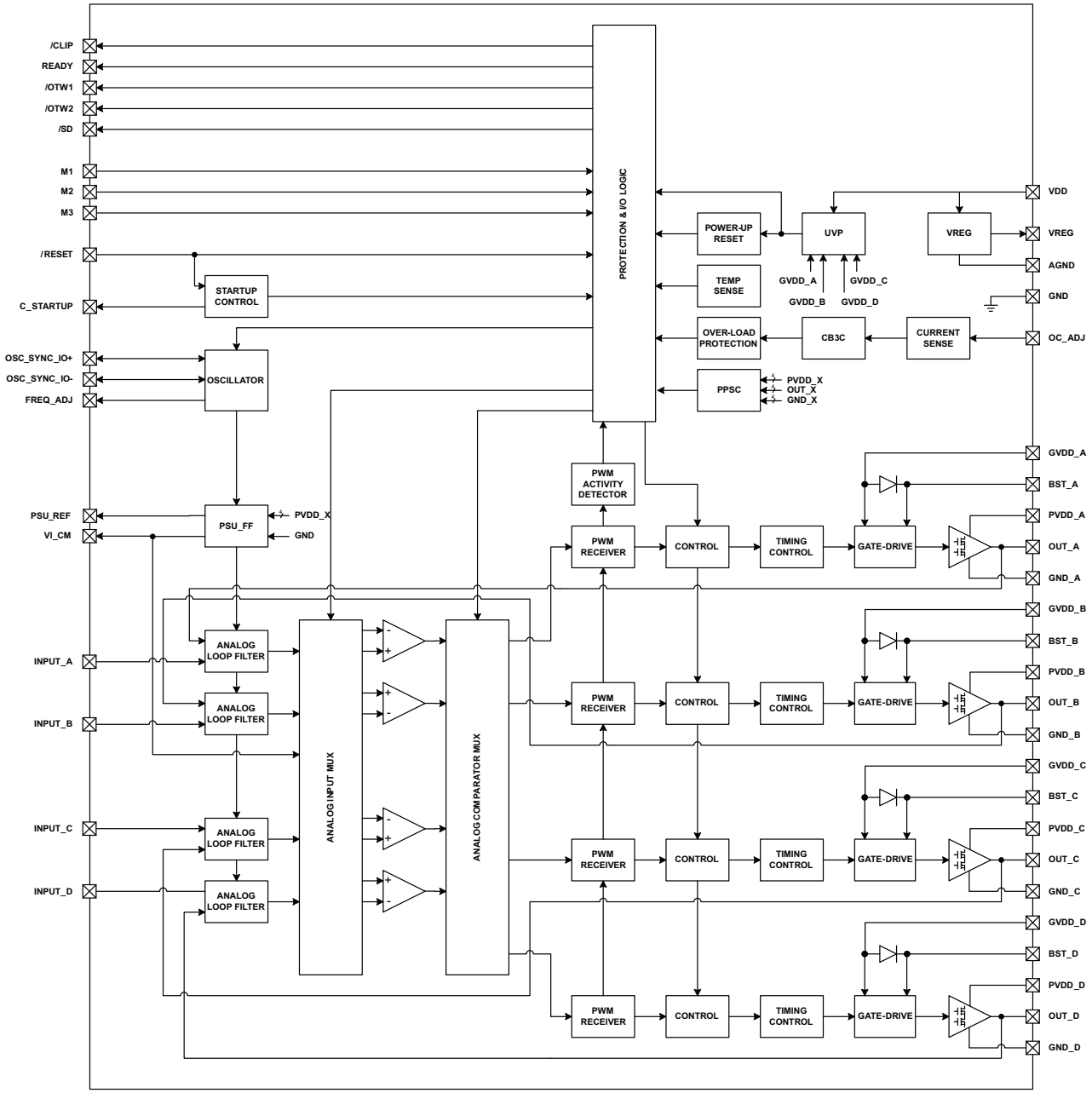
Figure 14. Output Power vs Case Temperature

7 Detailed Description

7.1 Overview

TAS5630B is an analog input, audio PWM (class-D) amplifier. The output of the TAS5630B can be configured for single-ended, bridge-tied load (BTL) or parallel BTL (PBTL) output. It requires two rails for power supply, PVDD and 12 V (GVDD and VDD). The following functional block diagram shows interconnections of internal supplies, control logic, gate drives and power amplifiers. Detailed schematic can be viewed in TAS5630B EVM User's Guide (SLAU287).

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Power Supplies

To facilitate system design, the TAS5630B needs only a 12-V supply in addition to the (typical) 50-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path, including gate drive and output stage, is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply pins (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see *Typical Application* for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See SLAU287 for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 400 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 2.2-µF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5630B reference design. For additional information on recommended power supply and required components, see *Typical Application*.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 50-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5630B is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see *Recommended Operating Conditions*).

7.3.2 System Power-Up and Power-Down Sequence

7.3.2.1 Powering Up

The TAS5630B does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see *Electrical Characteristics*). Although not specifically required, it is recommended to hold $\overline{\text{RESET}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

7.3.2.2 Powering Down

The TAS5630B does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see *Electrical Characteristics*). Although not specifically required, it is a good practice to hold $\overline{\text{RESET}}$ low during power down, thus preventing audible artifacts including pops or clicks.

7.3.3 Error Reporting

The $\overline{\text{SD}}$, $\overline{\text{OTW}}$, $\overline{\text{OTW1}}$, and $\overline{\text{OTW2}}$ pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Feature Description (continued)

Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ and $\overline{OTW2}$ go low when the device junction temperature exceeds 125°C and $\overline{OTW1}$ goes low when the junction temperature exceeds 100°C (see Table 1).

Table 1. Error Reporting

$\overline{SD}$	$\overline{OTW1}$	$\overline{OTW2}$, $\overline{OTW}$	DESCRIPTION
0	0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	0	1	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 100°C (overtemperature warning)
0	1	1	Overload (OLP) or undervoltage (UVP)
1	0	0	Junction temperature higher than 125°C (overtemperature warning)
1	0	1	Junction temperature higher than 100°C (overtemperature warning)
1	1	1	Junction temperature lower than 100°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{RESET}$ low forces the $\overline{SD}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{OTW}$ signal using the system microcontroller and responding to an overtemperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see *Electrical Characteristics* for further specifications).

7.3.4 Device Protection System

The TAS5630B contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5630B responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the SD pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device functions on errors, as shown in the following table.

Table 2. Device Protection System

BTL Mode		PBTL Mode		SE Mode	
Local error in	Turns Off or in	Local error in	Turns Off or in	Local error in	Turns Off or in
A	A + B	A	A + B + C + D	A	A + B
B		B		B	
C	C + D	C		C	C + D
D		D		D	

Bootstrap UVP does not shut down according to the table; it shuts down the respective half-bridge.

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7.3.5 Pin-to-Pin Short-Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter, whereas PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup, that is, when VDD is supplied; consequently, a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two-step sequence. The first step ensures that there are no shorts from OUT_X to GND_X; the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is <15 ms/µF. While the PPSC detection is in progress, $\overline{SD}$ is kept low, and the device does not react to changes applied to the $\overline{RESET}$ pins. If no shorts are present the PPSC detection passes, and $\overline{SD}$ is released, a device reset does not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations; the detection is not performed in SE mode. To make sure the PPSC detection system is not tripped, it is recommended not to insert resistive load between OUT_X and GND_X or PVDD_X.

7.3.6 Overtemperature Protection

The two different package options have individual overtemperature protection schemes.

PHD Package:
The TAS5630B PHD package option has a three-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW1}$) when the device junction temperature exceeds 100°C (typical), ($\overline{OTW2}$) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{RESET}$ must be asserted. Thereafter, the device resumes normal operation. For highest reliability, the $\overline{RESET}$ should not be asserted until $\overline{OTW1}$ has cleared.

DKD Package:
The TAS5630B DKD package option has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{OTW}$) when the device junction temperature exceeds 125°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{RESET}$ must be asserted. It is recommended to wait until $\overline{OTW}$ has cleared before asserting $\overline{RESET}$. Thereafter, the device resumes normal operation.

7.3.7 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5630B fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach the levels stated in *Electrical Characteristics*. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{SD}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

7.3.8 Device Reset

When $\overline{RESET}$ is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high-impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the $\overline{SD}$ output; that is, $\overline{SD}$ is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{SD}$.

7.3.9 Click and Pop in SE-Mode

The BTL startup has low click and pop due to the trimmed output dc offset, see *Audio Characteristics (BTL)*.

The startup of the BTL+2 x SE system (Figure 21) or 4xSE (Figure 20) is more difficult to get click and pop free, than the pure BTL solution; therefore, evaluating the resulting click and pop before designing in the device is recommended.

7.3.10 PBTL Overload and Short Circuit

The TAS5630B has extensive overload and short circuit protection. In BTL and SE mode, it is fully protected against speaker terminal overloads, terminal-to-terminal short circuit, and short circuit to GND or PVDD. The protection works by limiting the current, by flipping the state of the output MOSFETs; thereby, ramping currents down in the inductor. This only works when the inductor is NOT saturated, the recommended minimum inductor values are listed in *Recommended Operating Conditions*. In BTL mode, the short circuit currents can reach more than 15 A, so when connecting the device in PBTL mode (Mono), the currents double – that is more than 30 A, and with these high currents, the protection system will limit PBTL speaker overloads, terminal-to-terminal shorts, and terminal-to-GND shorts. PBTL mode short circuit to PVDD is not recommended.

7.3.11 Oscillator

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

To reduce interference problems while using a radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower values. These values should be chosen such that the nominal and the lower-value switching frequencies together result in the fewest cases of interference throughout the AM band, and can be selected by the value of the FREQ_ADJ resistor connected to AGND in master mode.

For slave-mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to VREG. This configures the OSC_I/O pins as inputs, which must be slaved from an external clock.

7.4 Device Functional Modes

Table 3. Mode Selection Pins

MODE PINS			ANALOG INPUT	OUTPUT CONFIGURATION	DESCRIPTION		
M3	M2	M1					
0	0	0	Differential	2 × BTL	AD mode		
0	0	1	—	—	Reserved		
0	1	0	Differential	2 × BTL	BD mode		
0	1	1	Differential single-ended	1 × BTL +2 ×SE	BD mode, BTL differential		
1	0	0	Single-ended	4 × SE	AD mode		
1	0	1	Differential	1 × PBTL	**INPUT_C** (1)	**INPUT_D** (1)	
					0	0	AD mode
					1	0	BD mode
1	1	0	Reserved				
1	1	1					

(1) INPUT_C and D are used to select between a subset of AD and BD mode operations in PBTL mode (1=VREG and 0=AGND).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 PCB Material Recommendation

TI recommends FR-4 2-oz. (70-µm) glass epoxy material for use with the TAS5630B. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace resistance).

8.1.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full bridge are referred to as the PVDD capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed system power supply, 1000 µF, 63-V supports more applications. The PVDD capacitors should be the low-ESR type, because they are used in a circuit associated with high-speed switching.

8.1.3 Decoupling Capacitor Recommendations

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 2.2-µF capacitor that is placed on the power supply to each half-bridge. The decoupling capacitor must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 63 V is required for use with a 50-V power supply.

8.1.4 System Design Considerations

A rising-edge transition on the reset input allows the device to execute the startup sequence and starts switching.

Apply audio only when the state of READY is high; that starts and stops the amplifier without having audible artifacts that are heard in the output transducers. If an overcurrent protection event is introduced, the READY signal goes low; hence, filtering is needed if the signal is intended for audio muting in non-microcontroller systems.

The CLIP signal indicates that the output is approaching clipping. The signal can be used either to activate a volume decrease or to signal an intelligent power supply to increase the rail voltage from low to high for optimum efficiency.

The device inverts the audio signal from input to output.

The VREG pin is not recommended to be used as a voltage source for external circuitry.

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8.2 Typical Application

The following schematics and PCB layouts illustrate *best practices* used for the TAS5630B.

8.2.1 Typical Application Schematic

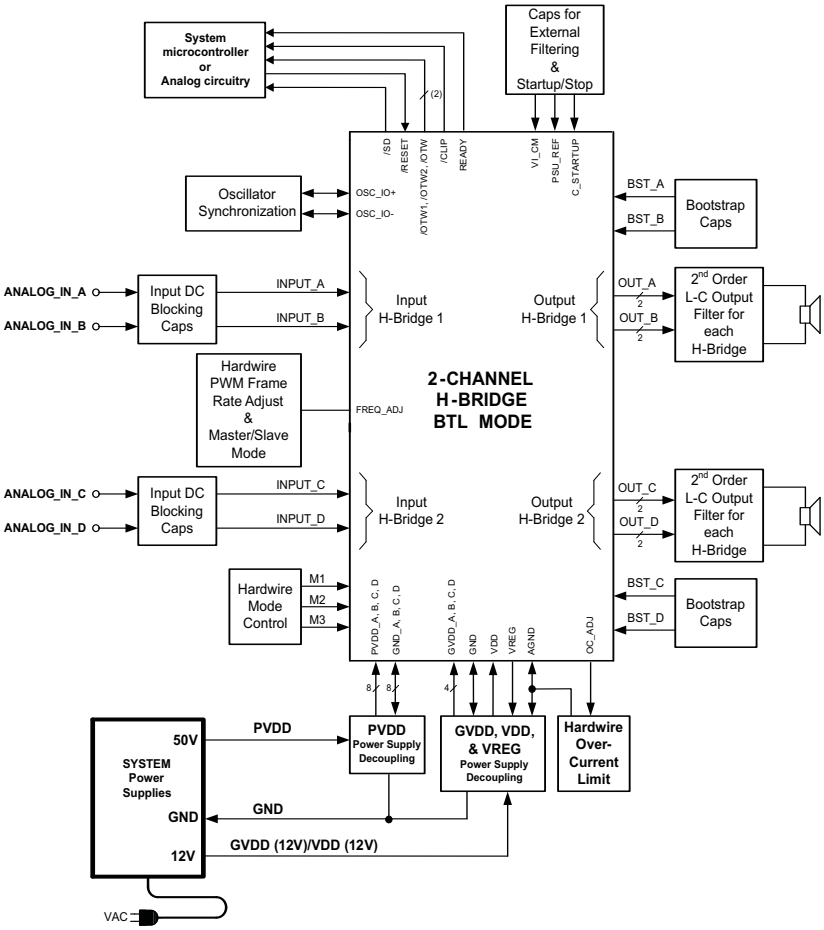

Figure 15. Typical Application Schematic

8.2.1.1 Design Requirements

This device can be configured for BTL, PBTL, or SE mode. Each mode will require a different output configuration.

8.2.1.2 Detailed Design Procedure

- Pin 1 – Overcurrent adjust resistor can be between 24 kΩ to 68 kΩ depending on the application. The lower resistance corresponds to the higher over-current protection level.
- Pin 2 – RESET pin when asserted, it keeps outputs Hi-Z and no PWM switching. This pin can be controlled by a microprocessor.
- Pin 3 – Start-up ramp capacitor should be 4.7 nF for BTL and PBTL configurations, and 10 nF for SE configuration.
- Pins 4, 5, 10, 11 – Differential pair inputs AB and CD. A DC blocking capacitor of 10 µF and an RC of 100 Ω and 100 pF should be placed on each analog input.
- Pin 6 – Analog comparator reference node requires close decoupling capacitor of 1 nF to ground.
- Pin 7, 8, 23, 24, 57, 58 – Ground pins are connected to board ground.
- Pin 9 – Regulator supply filter pin requires 0.1 uF to AGND.
- Pin 12 – Frequency adjust resistor is discussed in *Oscillator*.

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Typical Application (continued)

- Pin 13, 14 – Oscillator input/output. When frequency adjust pin is pulled up to VREG, the oscillator pins are configured as inputs.
- Pin 15 – Shutdown pin can be monitored by a microcontroller through GPIO pin. System can decide to assert reset or power down. See *Error Reporting*.
- Pin 16, 17 – There are two overtemperature warning pins for PHD package. They have two different levels of warning. OTW1 is lower temperature level warning than OTW2. They can be monitored by a microcontroller through GPIO pins. System can decide to turn on fan, lower output power or shutdown. See *Error Reporting*.
- Pin 18 – Output clip indicator can be monitored by a microcontroller through a GPIO pin. System can decide to lower the volume.
- Pin 19 – Ready pin can be used to signal the system that the device is up and running.
- Pin 20-22 – Mode pins set the input and output configurations. See Table 2 for configuration setting of these pins.
- Pin 25, 26, 55, 56 – Gate drive power pins provide gate voltage for half-bridges. Each needs a 3.3-Ω isolation resistor and a 0.1-uF decoupling capacitor.
- Pins 27, 40, 41, 54 – Bootstrap pins for half-bridges A, B, C, D. Connect 33 nF from this pin to corresponding output pins.
- Pins 28, 29, 36, 37, 44, 45, 53, 54 – Output pins from half-bridges A, B, C, D. Connect appropriate bootstrap capacitors to the output pins. For PWM filtering, each output mode is used with different LC configuration.
- Pins 30, 31, 38, 39, 42, 43, 50, 51 – Power supply pins to half-bridges A, B, C, D. Each PVDD_X has decoupling capacitor connecting to the appropriate GND_X pin.
- Pins 32, 33, 34, 35, 46, 47, 48, 49 – Connect decoupling capacitors of each power input pin to power supply ground pins. Connect these pins to board ground.
- Pins 59-62 – Connect “No connect” pins to board ground. There is no internal connection to these pins.

8.2.1.3 Application Curves

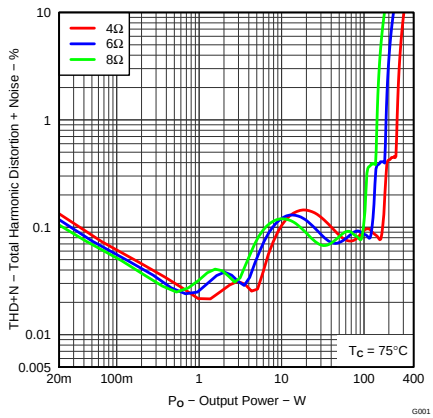

Figure 16. Total Harmonic + Noise vs Output Power

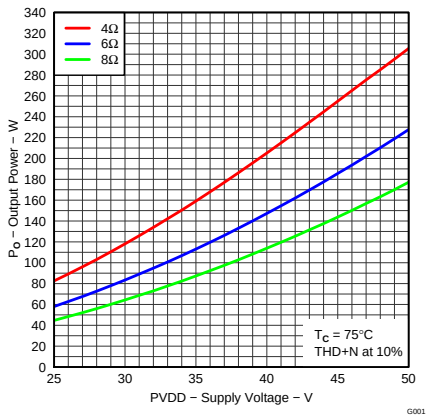

Figure 17. Output Power vs Supply Voltage

8.2.2 Typical Differential-Input BTL Application With BD Modulation Filters

BTL output and differential input configuration is a typical audio class-D (PWM) amplifier. With differential input, the output can be configured for BTL application with BD modulation. The configuration below can also be used with AD modulation. BD modulation gives better channel separation and PSSR performance.

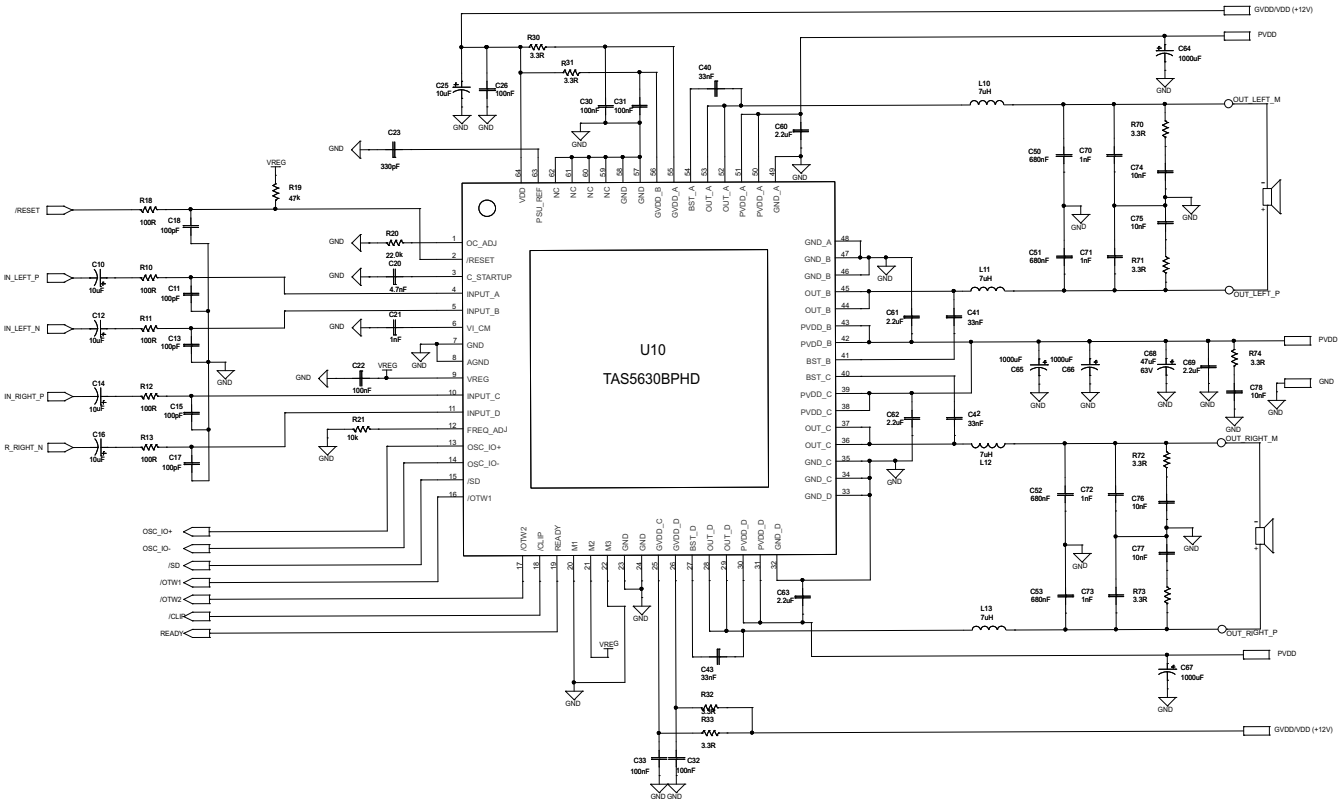

Figure 18. Typical Differential-Input BTL Application With BD Modulation Filters

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8.2.3 Typical Differential (2N) PBTL Application With BD Modulation Filters

When there is a need for more power in an audio system, PBTL is a good choice for this application. Paralleling the output after the inductors is recommended. In this configuration, the device can be driven with higher current (lower load impedance). Figure 19 shows the component and pin connections.

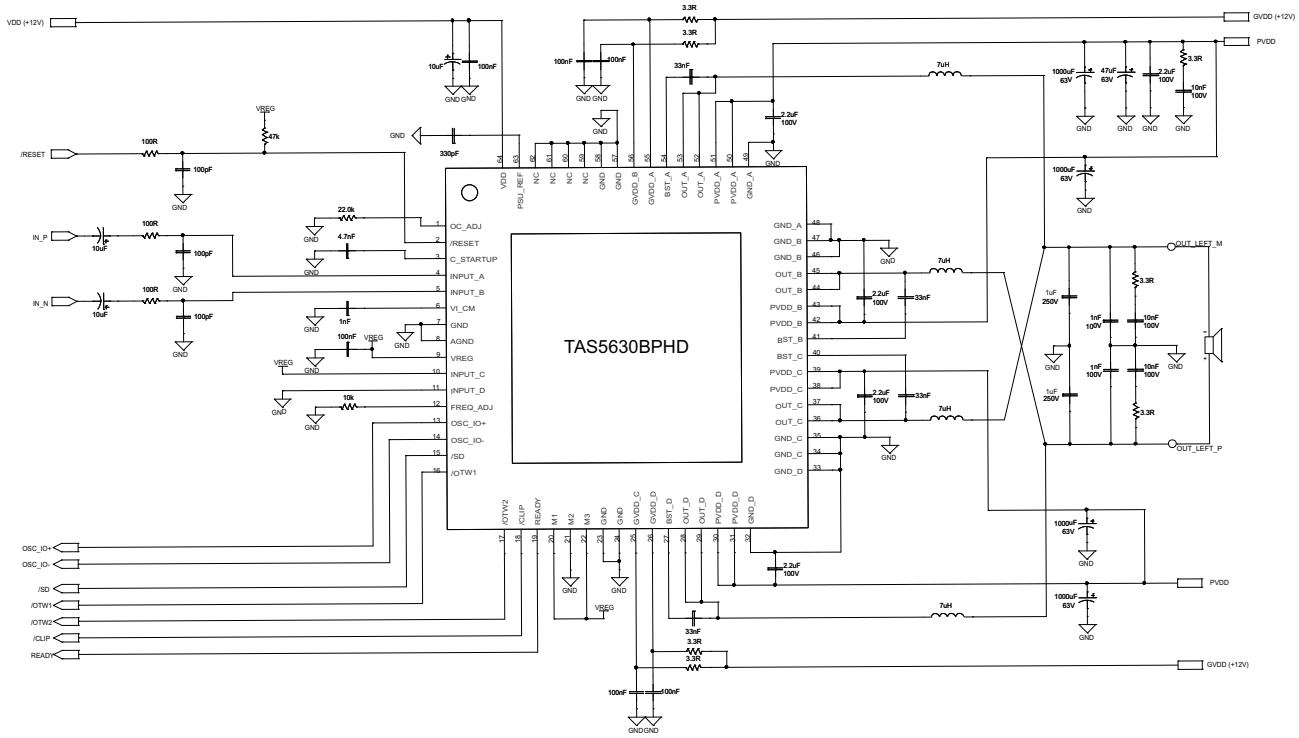
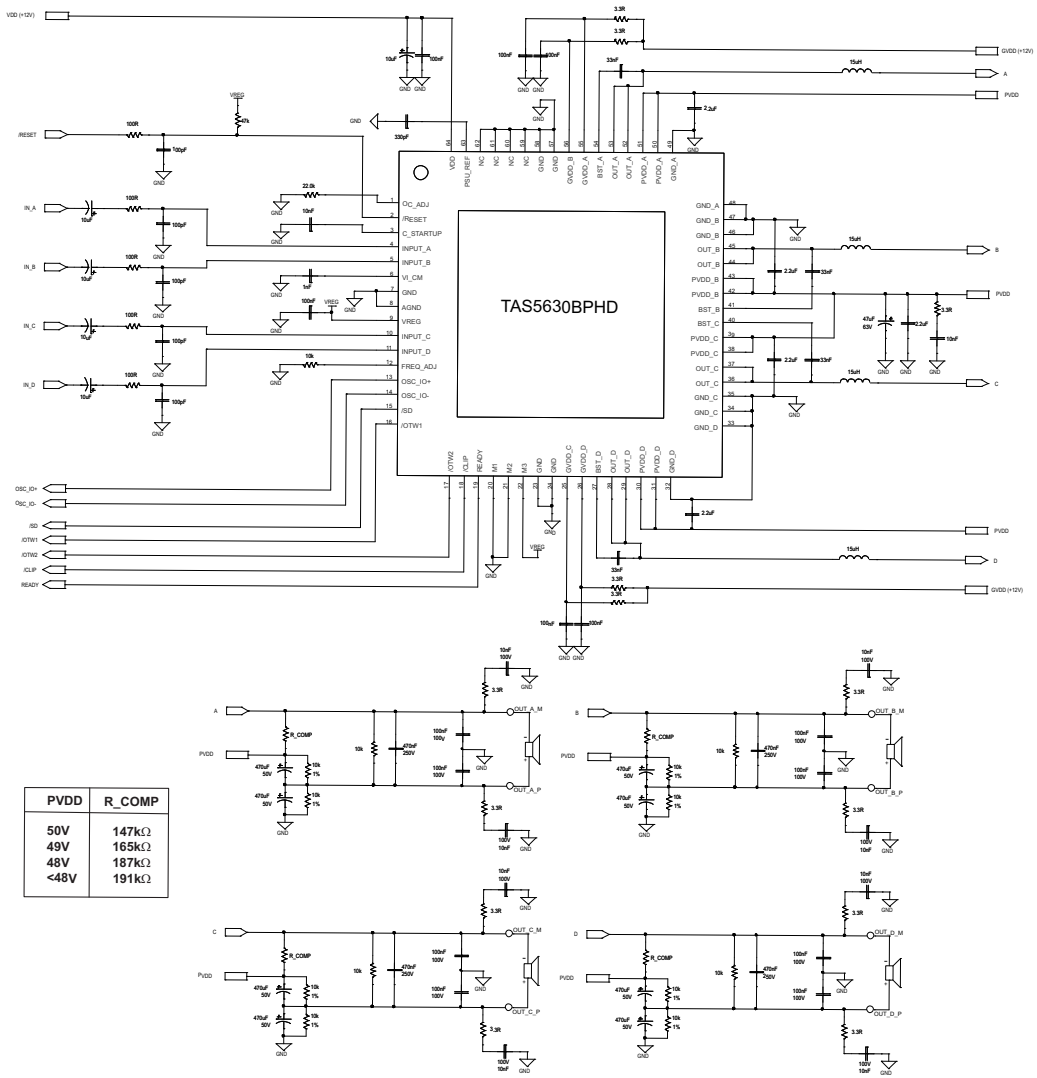


Figure 19. Typical Differential (2N) PBTL Application With BD Modulation Filters

8.2.4 Typical SE Application

Single-ended output configuration is often used for cost effective systems. This device can be configured to drive four independent channels with four different inputs. The delivered power is not as much as BTL configuration. The advantage is that the component count for four channels is the same as two BTL channels. The schematic in this section shows the component and pin connections.



PVDD	R_COMP
50V	147kΩ
49V	165kΩ
48V	187kΩ
<48V	191kΩ

Figure 20. Typical SE Application

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8.2.5 Typical 2.1 System Differential-Input BTL and Unbalanced-Input SE Application

One of the attractive features of this device is that it can be configured for mixed BTL and SE outputs. One BTL plus two SE channels make up a 2.1 audio system. While the SE channels are used to drive the front end and right speakers, the BTL channel can deliver higher power and is used to drive a subwoofer. Figure 21 shows the component and pin connections.

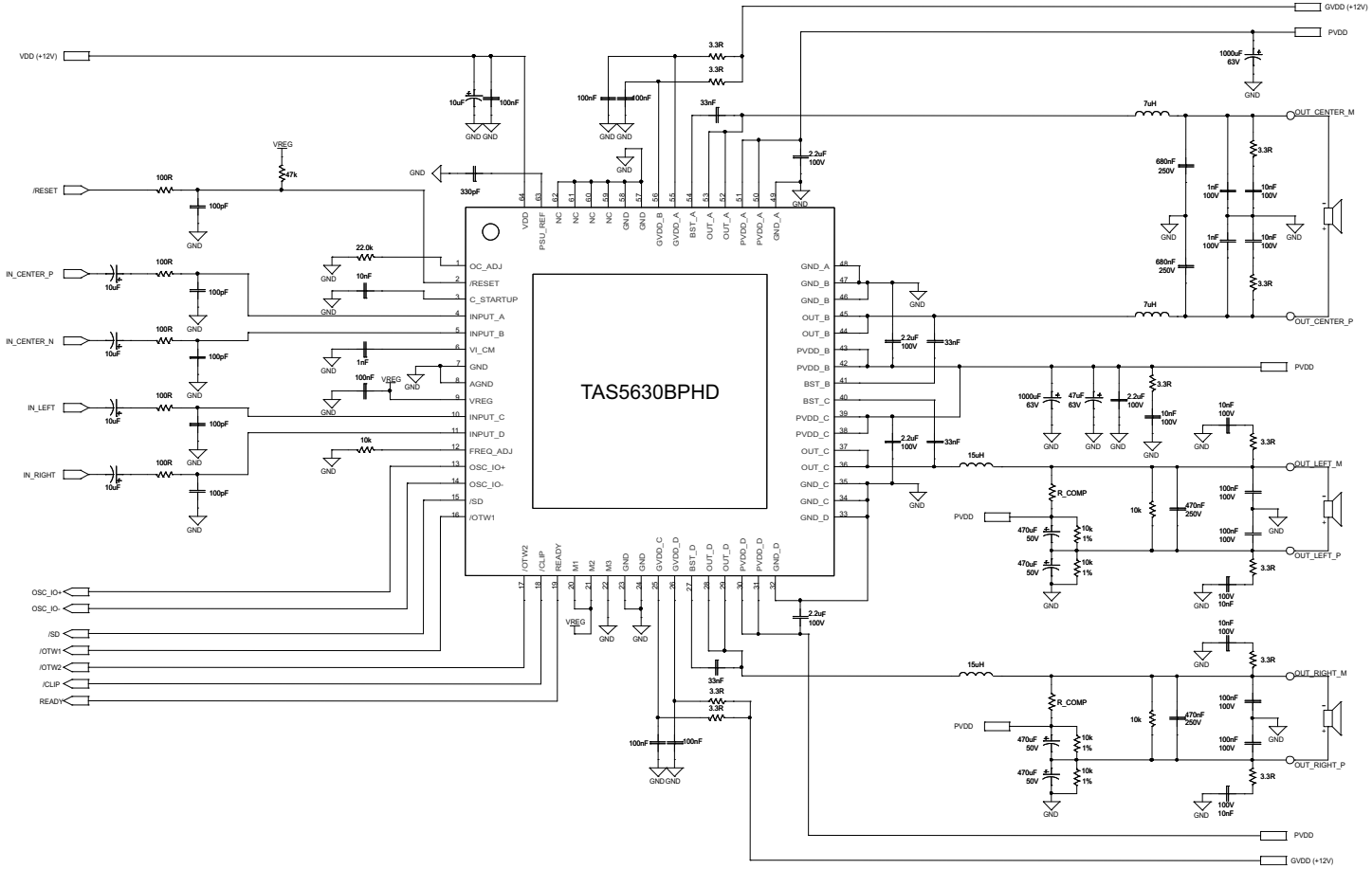

Figure 21. Typical 2.1 System Differential-Input BTL and Unbalanced-Input SE Application

8.2.6 Typical Differential-Input BTL Application With BD Modulation Filters, DKD Package

This is the same application as described in *Typical Differential-Input BTL Application With BD Modulation Filters* with PHD package. For DKD package an external heatsink is required to dissipate excess heat. In this package, the PCB space is not a limiting factor for dissipating excess heat.

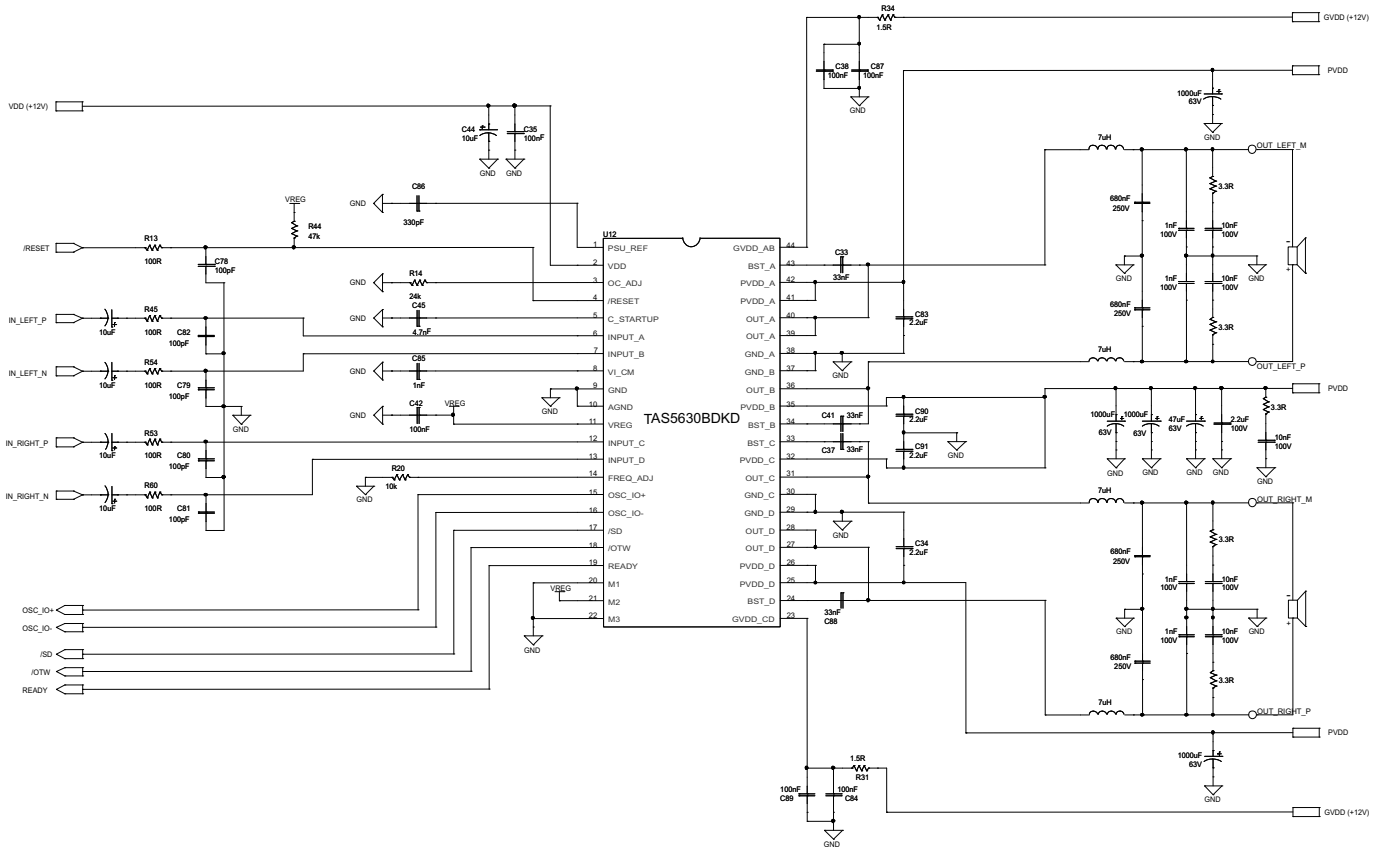

Figure 22. Typical Differential-Input BTL Application With BD Modulation Filters, DKD Package

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9 Power Supply Recommendations

Absolute Maximum Ratings discusses most of the requirements on TAS5630B power supply. There are a few more important guidelines that should be considered. The most important parameters are the absolute maximum rating on PVDD pins, bootstrap pins and output pins. Over stress the device with higher that maximum voltage rating may shorten device lifetime operation and even cause device damage. Be sure that the specifications in section 6 are observed. For best audio performance, low ESR bulk capacitors are recommended. Depending on the application 470-µF capacitor or higher should be used. As always, decoupling capacitors must be placed no more than 1 mm from the power supply pins. If PCB space is not allowed for close decoupling capacitor placement, the decoupling capacitors can be placed on the back side of the device with vias. However, it still needs to be right below the pins.

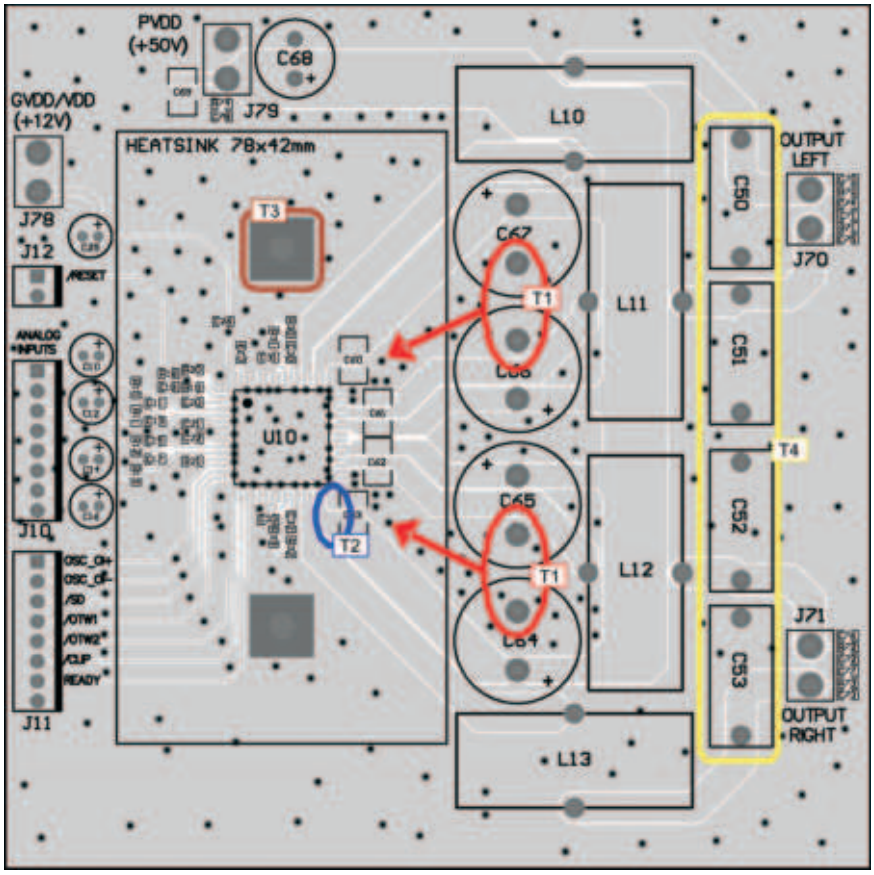
10 Layout

10.1 Layout Guidelines

Use an unbroken ground plane to have a good low-impedance and -inductance return path to the power supply for power and audio signals. PCB layout, audio performance and EMI are linked closely together. The circuit contains high, fast-switching currents; therefore, care must be taken to prevent damaging voltage spikes. Routing of the audio input should be kept short and together with the accompanying audio-source ground. A local ground area underneath the device is important to keep solid to minimize ground bounce. It is always good practice to follow the EVM layout as a guideline.

Netlist for this printed circuit board is generated from the schematic in Figure 18.

10.2 Layout Example



Note T1: PVDD bulk decoupling capacitors C60–C64 should be as close as possible to the PVDD_X and GND_X pins; the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

Note T2: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins. This is valid for C60, C61, C62, and C63.

Note T3: Heat sink must have a good connection to PCB ground.

Note T4: Output filter capacitors must be linear in the applied voltage range, preferably metal film types.

Figure 23. Printed Circuit Board – Top Layer

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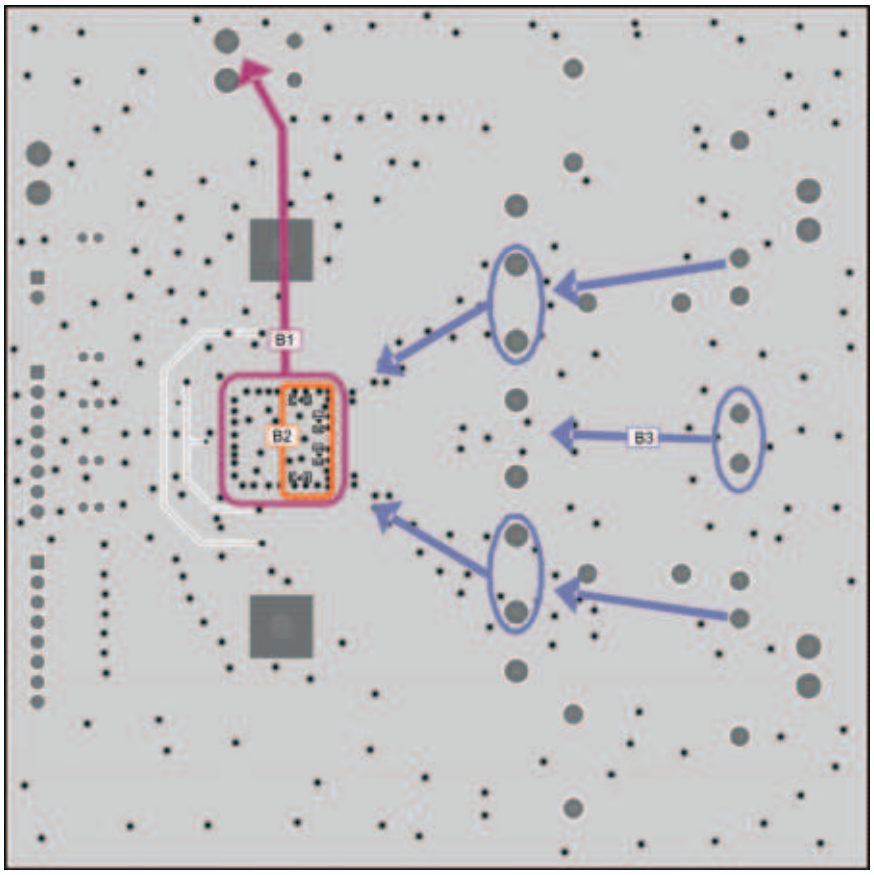
Layout Example (continued)



Note B1: It is important to have a direct-low impedance return path for high current back to the power supply. Keep impedance low from top to bottom side of PCB through a lot of ground vias.

Note B2: Bootstrap low-impedance X7R ceramic capacitors placed on bottom side provide a short, low-inductance current loop.

Note B3: Return currents from bulk capacitors and output filter capacitors

Figure 24. Printed Circuit Board – Bottom Layer

11 Device and Documentation Support

11.1 Trademarks

PurePath is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5630BPHD	Active	Production	HTQFP (PHD) | 64	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5630B
TAS5630BPHD.A	Active	Production	HTQFP (PHD) | 64	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5630B
TAS5630BPHDR	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5630B
TAS5630BPHDR.A	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5630B
TAS5630BPHDRG4	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5630B
TAS5630BPHDRG4.A	Active	Production	HTQFP (PHD) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	0 to 70	TAS5630B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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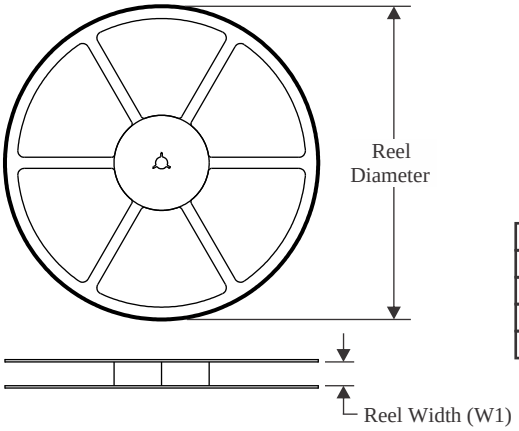
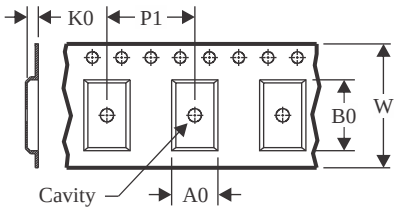
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

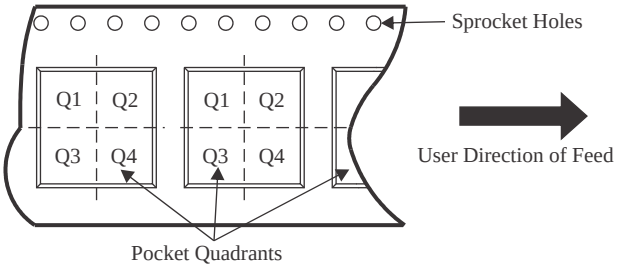


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

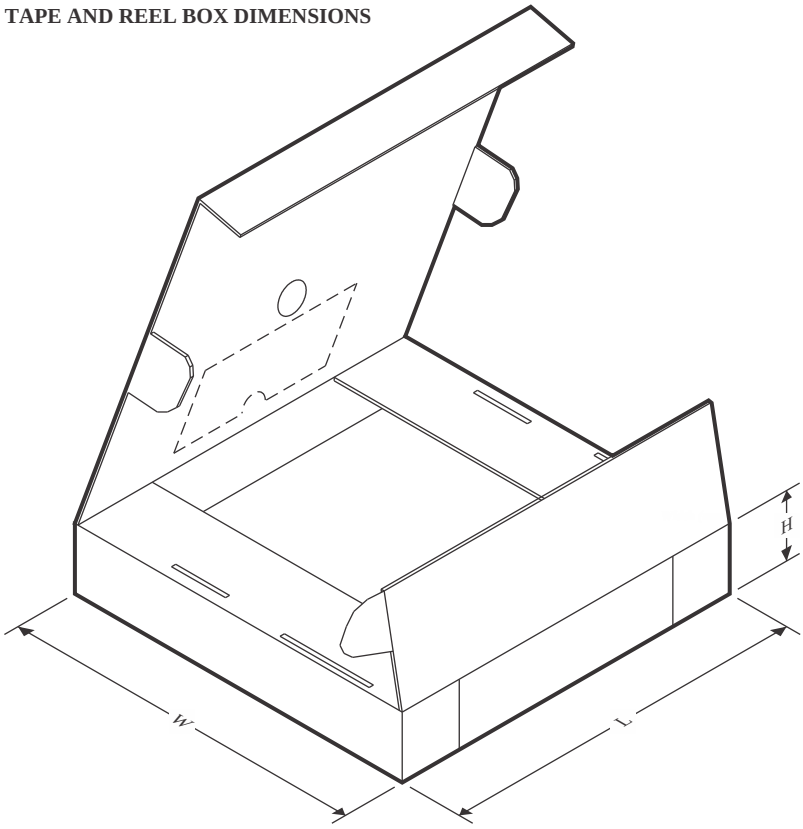
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5630BPHDR	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2
TAS5630BPHDRG4	HTQFP	PHD	64	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

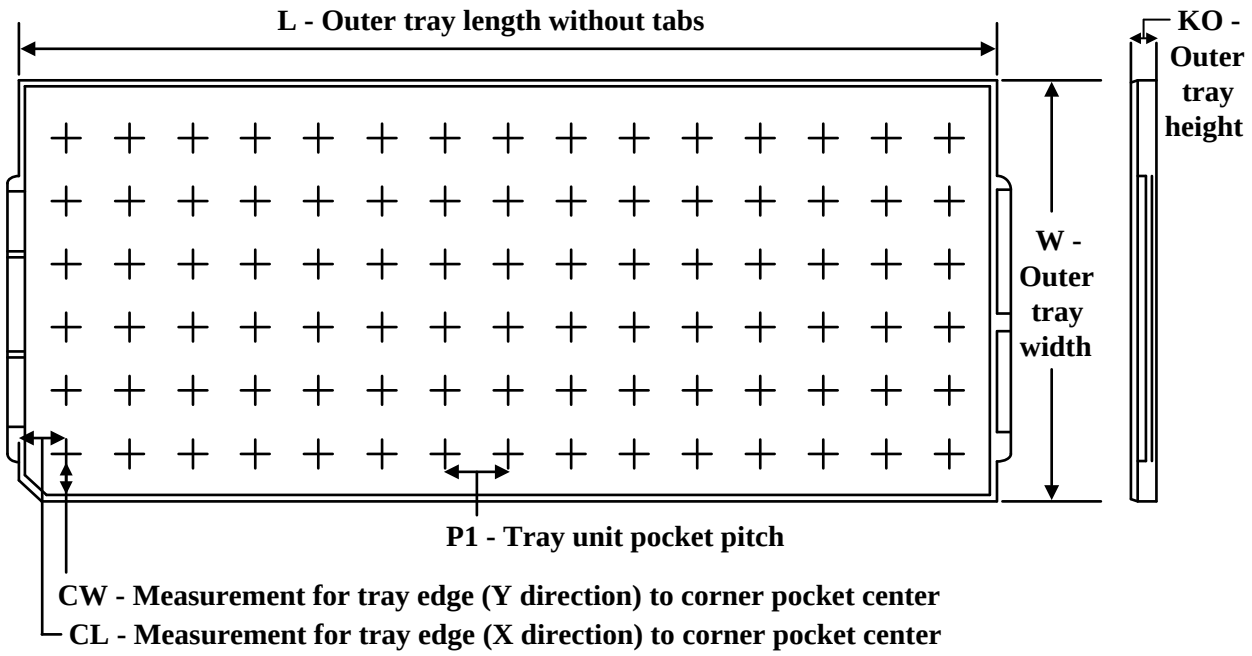
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5630BPHDR	HTQFP	PHD	64	1000	350.0	350.0	43.0
TAS5630BPHDRG4	HTQFP	PHD	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TAS5630BPHD	PHD	HTQFP	64	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45
TAS5630BPHD.A	PHD	HTQFP	64	90	6 X 15	150	315	135.9	7620	20.3	15.4	15.45

GENERIC PACKAGE VIEW

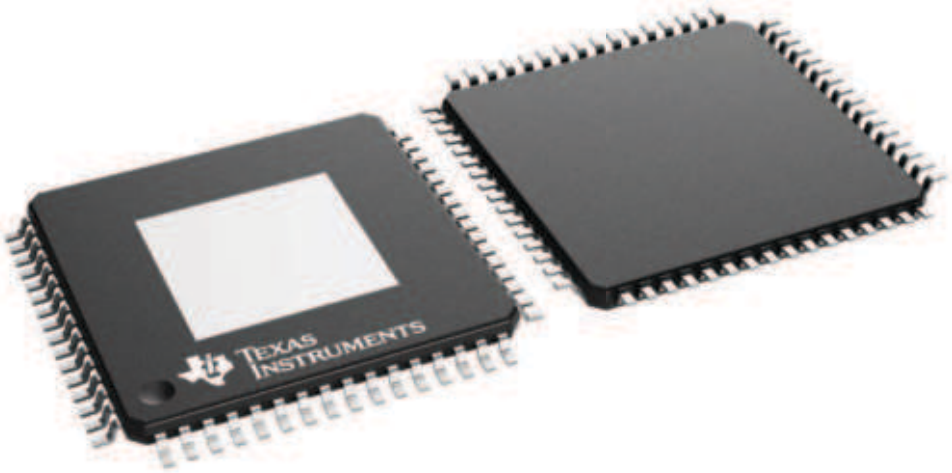
PHD 64

HTQFP - 1.2 mm max height

14 x 14, 0.8 mm pitch

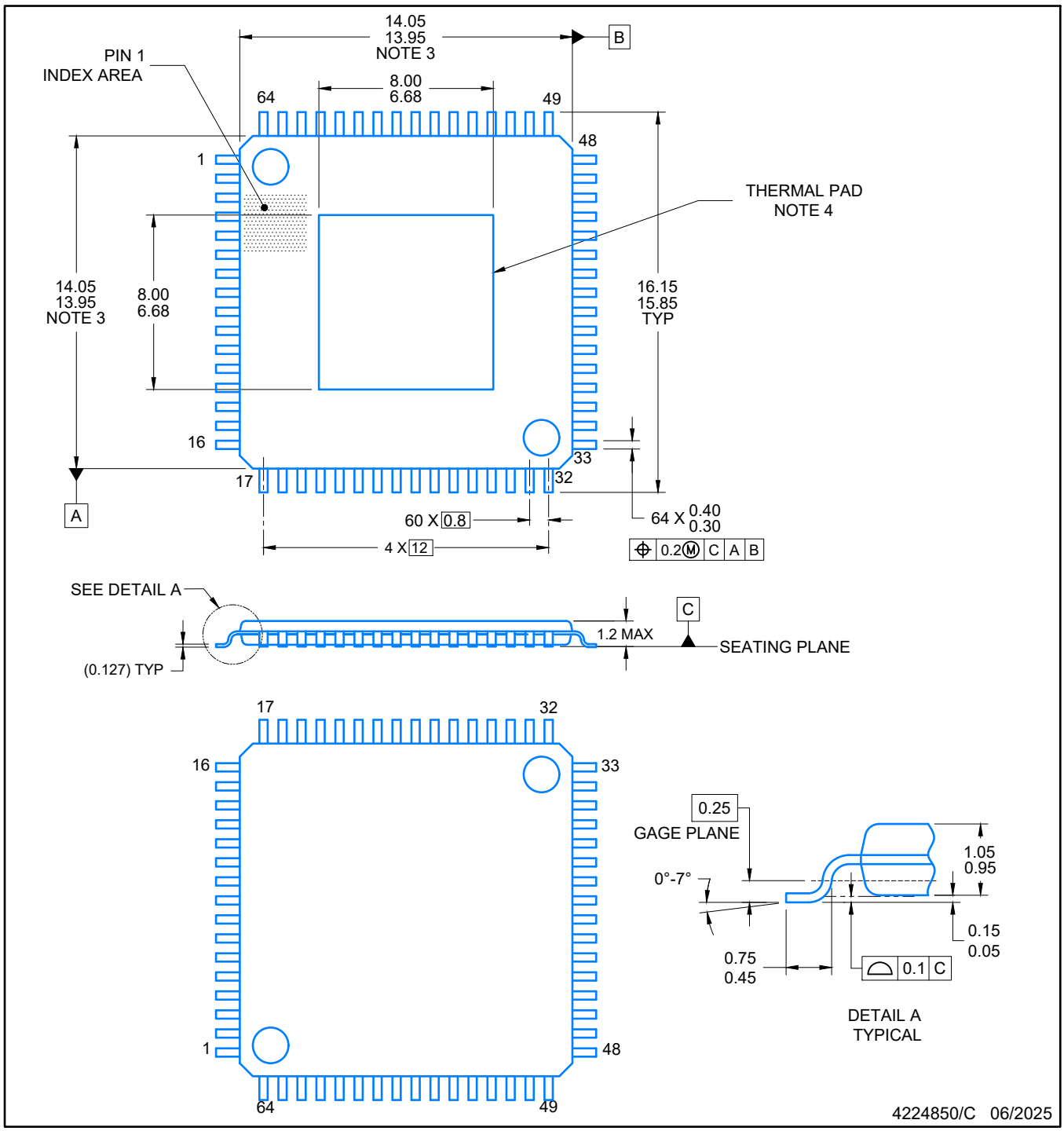
PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



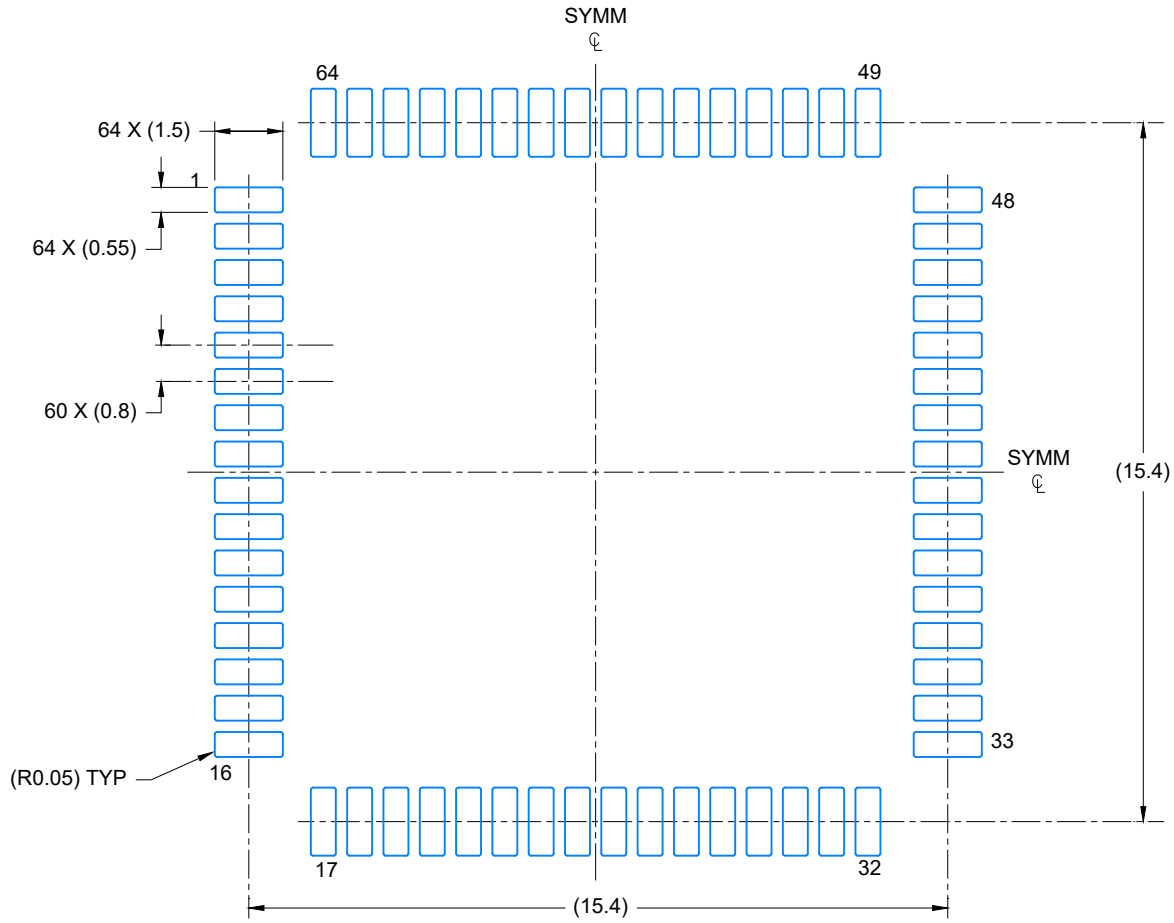
4224851/B

PLASTIC QUAD FLATPACK

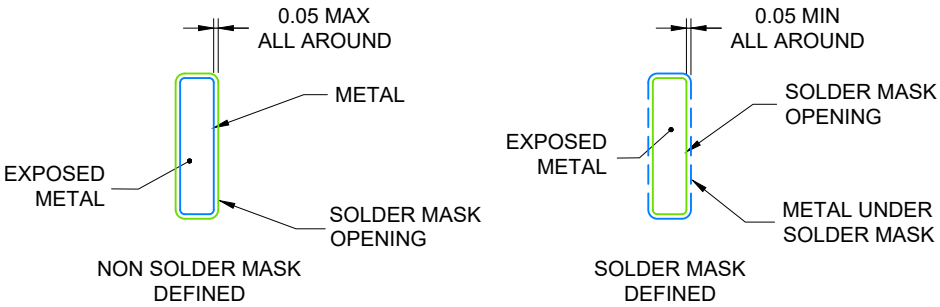


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. See technical brief. PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004) for information regarding recommended board layout.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X

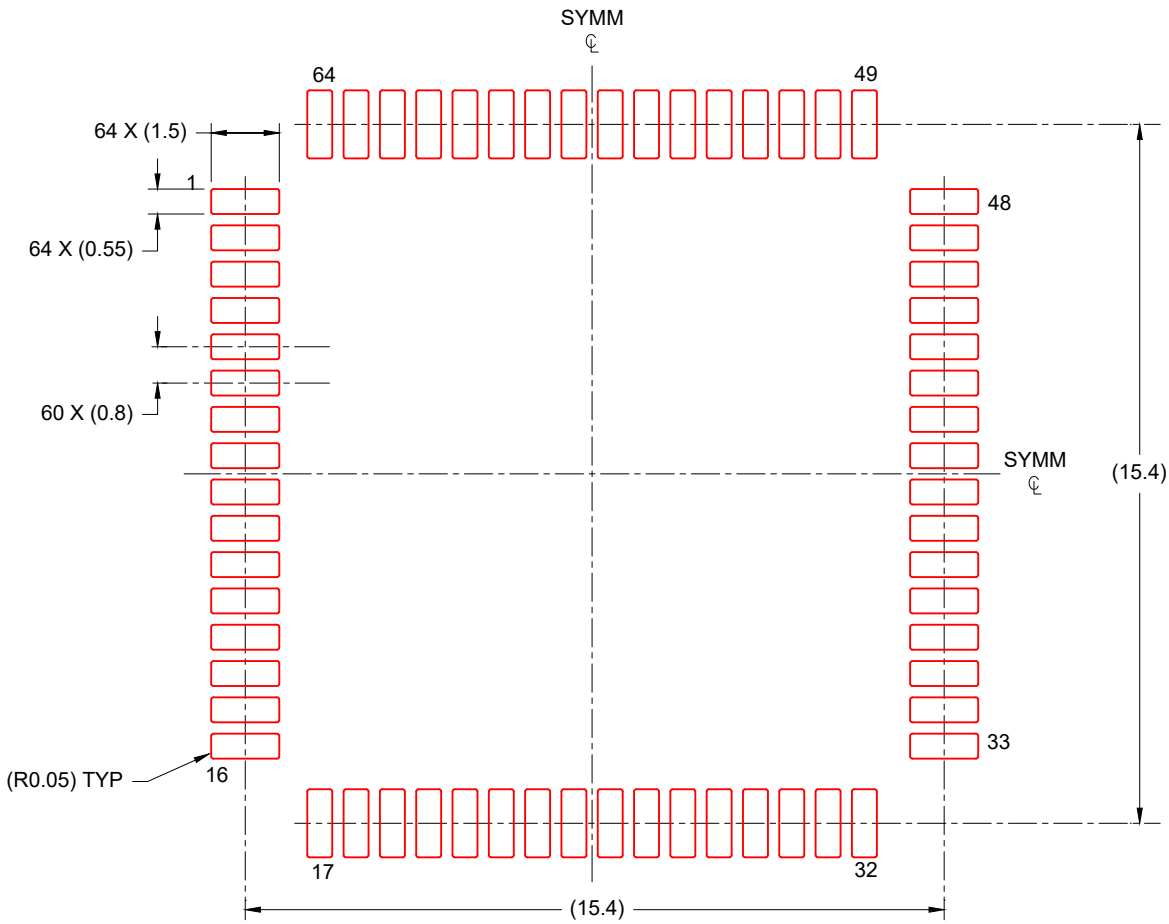


SOLDER MASK DETAILS

4224850/C 06/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4224850/C 06/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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