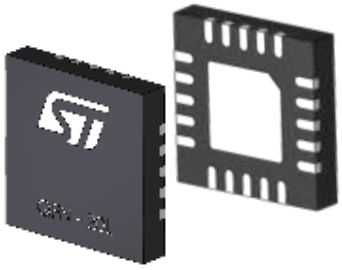
TCPP03-M20

Datasheet

USB-C PD protection for dual role power (DRP)



QFN-20L 4.0 x 4.0 x 0.75 mm

Product labels

SUSTAINABLE TECHNOLOGY

LONGEVITY 10 YEARS COMMITMENT

Product status link

TCPP03-M20

Expansion board

X-NUCLEO-DRP1M1

Software example code

X-CUBE-TCPP

I2C address

0110 10x (LSB = 'x')

Features

- High voltage protected USB-C power delivery controller with STM32 UCPD peripheral
- USB-IF certified on X-NUCLEO-DRP1M1-G4 (TID6408)
- Embeded gate drivers for N-MOSFET on consumer and provider paths
- 24 V tolerant on VBUS and CC pins
- Integrated discharge on VBUS and VCONN
- Over voltage protection against short to VBUS and ESD protection on CC lines
- VBUS current sense analog output through amplifier
- VBUS adjustable over voltage protection and adjustable over current protection
- 100 mW OCP and 6 V OVP on VCONN
- Integrated "Dead Battery" management
- Over temperature protection (150 °C typ.)
- I^2C communication with two I^2C addresses available
- ECOPACK2, and RoHS compliant

Complies with the following standards

- UL94, V0
- USB-C power delivery standard 3.1, standard power range (SPR) up to 100 W
- IEC 61000-4-2 level 4 on CC1, CC2 pins:
  - ±8 kV contact discharge
  - ±15 kV air discharge

Description

The TCPP03-M20 is a power delivery controller designed to meet USB Power Delivery revision 3.1 up to 100 W (20 V – 5 A, SPR) and PPS for fast charging.

The TCPP03 is a microcontroller companion chip enabling USB Type-C® PD for:

- Dual role power (DRP) or dual role data (DRD)
- Sink configuration or device data role when current sense on VBUS is required

It provides a solution to interface and protect USB Type-C ports on a power delivery side and has been developed to be used with the STM32 family embedding UCPD (USB Type-C and power delivery).

By reusing the STM32 of the application, it is the more cost effective solution as it requires only a few devices to be added:

- The TCPP03 to drive external N-MOSFETs on the VBUS line for consumer and provider paths
- A few discrete devices.

It provides over voltage and over current protections on VBUS and CC pins.

Software is available.

1 Pinout and functions

Figure 1. QFN-20L 4.0 x 4.0 x 0.75 mm

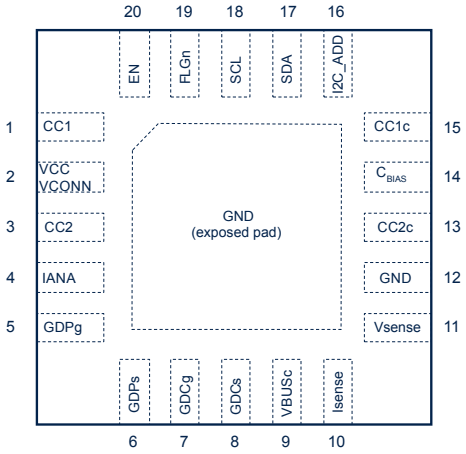


Table 1. Pinout and functions

Name	Pin #	Type	Description
CC1	1	Input / output	Configuration channel 1 pin on power delivery controller side.
VCC_VCONN	2	Power	Power supply for V_{CONN} power pin. Connect to 3.3 V or 5.5 V.
CC2	3	Input / output	Configuration channel 2 pin on power delivery controller side.
I_{ANA}	4	Output	V_{BUS} current analog measurement.
GDPg	5	Output	Gate driver provider: gate pin of external N-channel MOSFET on source path.
GDPs	6	Input	Gate driver provider: source pin of external N-channel MOSFET on source path.
GDCg	7	Output	Gate driver consumer: gate pin of external N-channel MOSFET on sink path.
GDCs	8	Input	Gate driver consumer: source pin of external N-channel MOSFET on sink path.
VBUSc	9	Input	VBUS connector side.
I_{sense}	10	Input	VBUS current measurement.
V_{sense}	11	Input	VBUS voltage measurement.
GND	12	GND	Ground.
CC2c	13	Input / output	Configuration channel 2 pin on USB Type-C connector side.
C_{BIAS}	14	Output	ESD capacitor
CC1c	15	Input / output	Configuration channel 1 pin on USB Type-C connector side.
I2C_ADD	16	Input	Least significant bit on I2C address. Connected to GND or 1.8 V / 3.3 V.
SDA	17	Input / output	Serial data line on I2C bus
SCL	18	Input / output	Serial clock line on I2C bus
FLGn	19	Output	Open-drain output flag (active low). Floating when not connected.
EN	20	Input	Enable pin.
GND	Pad	GND	Ground exposed pad.

2 Block diagram

Figure 2. **Functional block diagram**

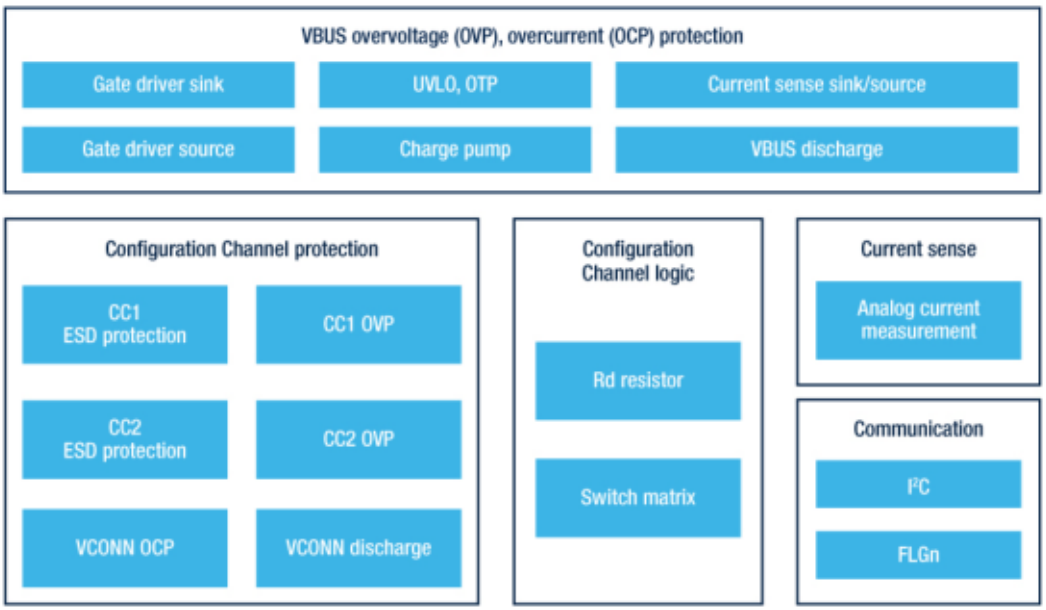
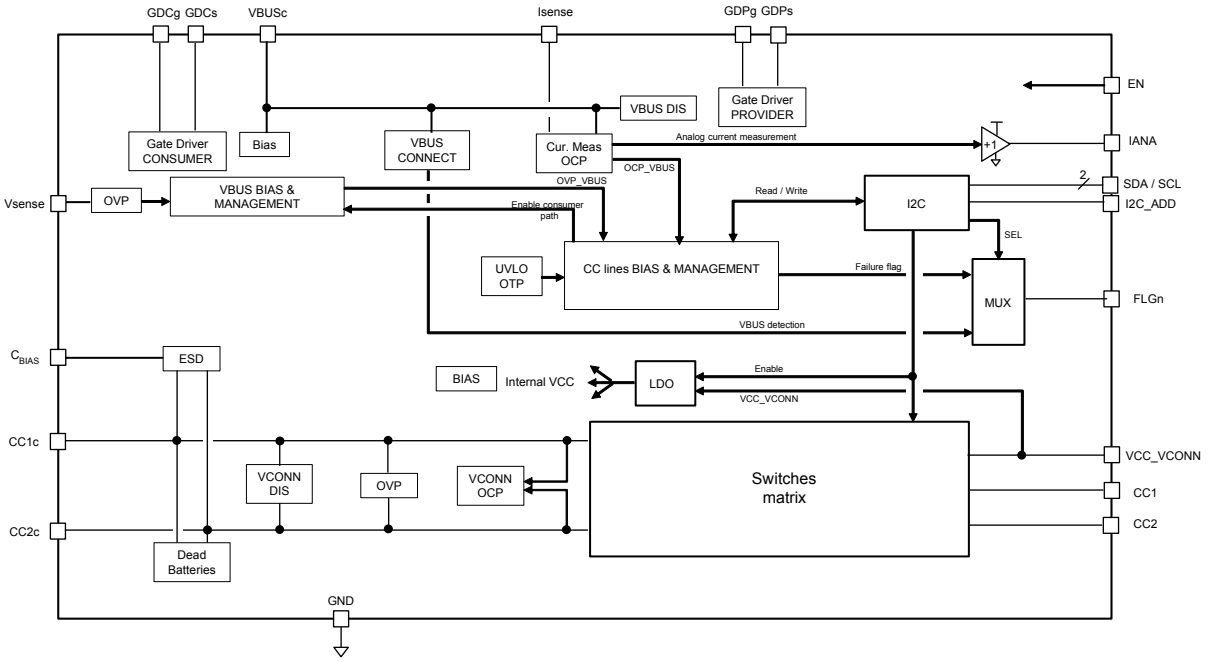
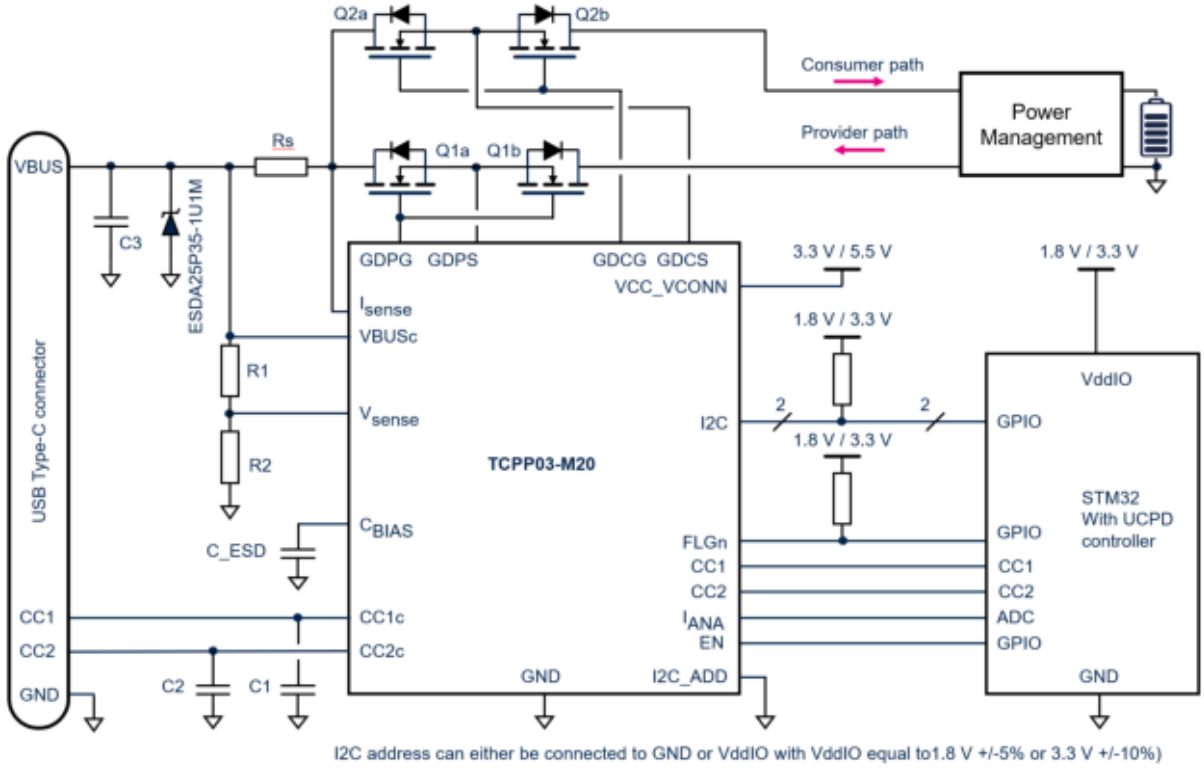


Figure 3. **Internal block diagram**



3 Typical USB-C DRP, DRD application block diagram

Figure 4. Application block diagram example



Provider and consumer gate drivers are exclusive. To merge consumer and provider paths in a single bidirectional power path, two small signal Schottky diodes (D1 , D2) and a 5 MΩ resistor are needed. OVP / OCP reaction time will be increased to 5 ms. TCPP03-M20 source inputs can be shorted together. Small signal Schottky diodes can either be :

- BAS70KFILM : 1 diodes in a SOD-523 package
- BAS70-05FILM : 1 diode in a SOD23 package
- BAS70-05WFILM : 2 diode in a single SOT-323 package
- SDM02M30LP3 : 1 diode in a 0201 package

Diode reverse leakage current at 5 V shall be lower than 1 µA.

Figure 5. **Bi-directional power path gate drive diagram**

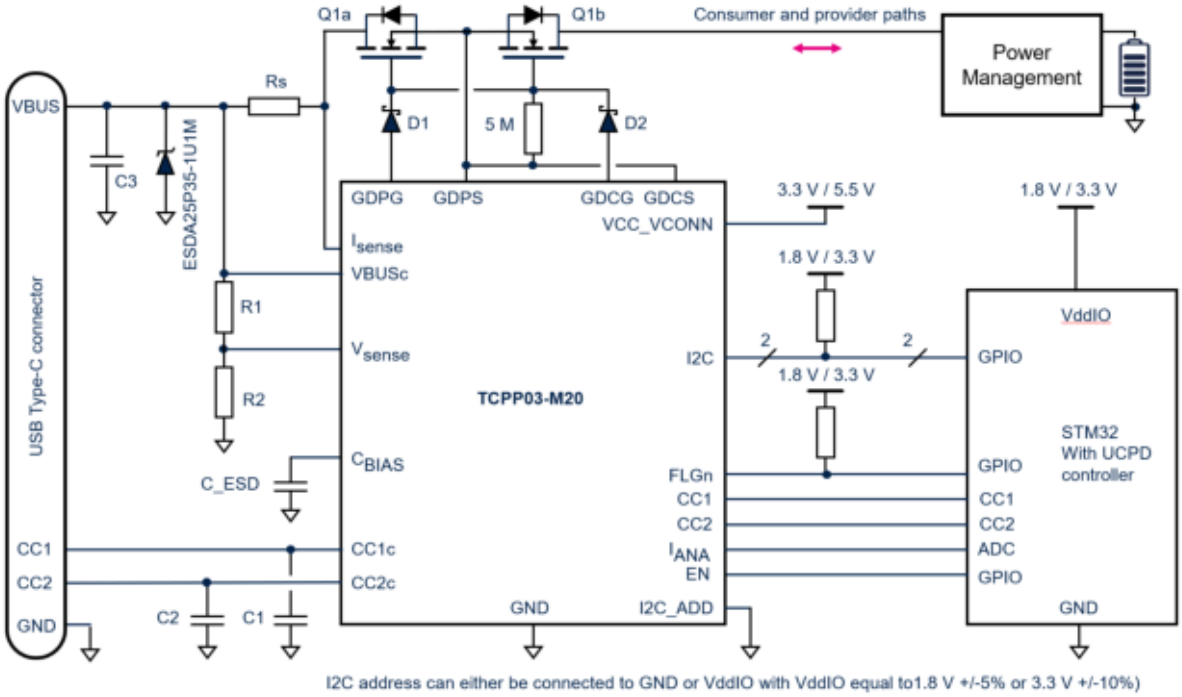
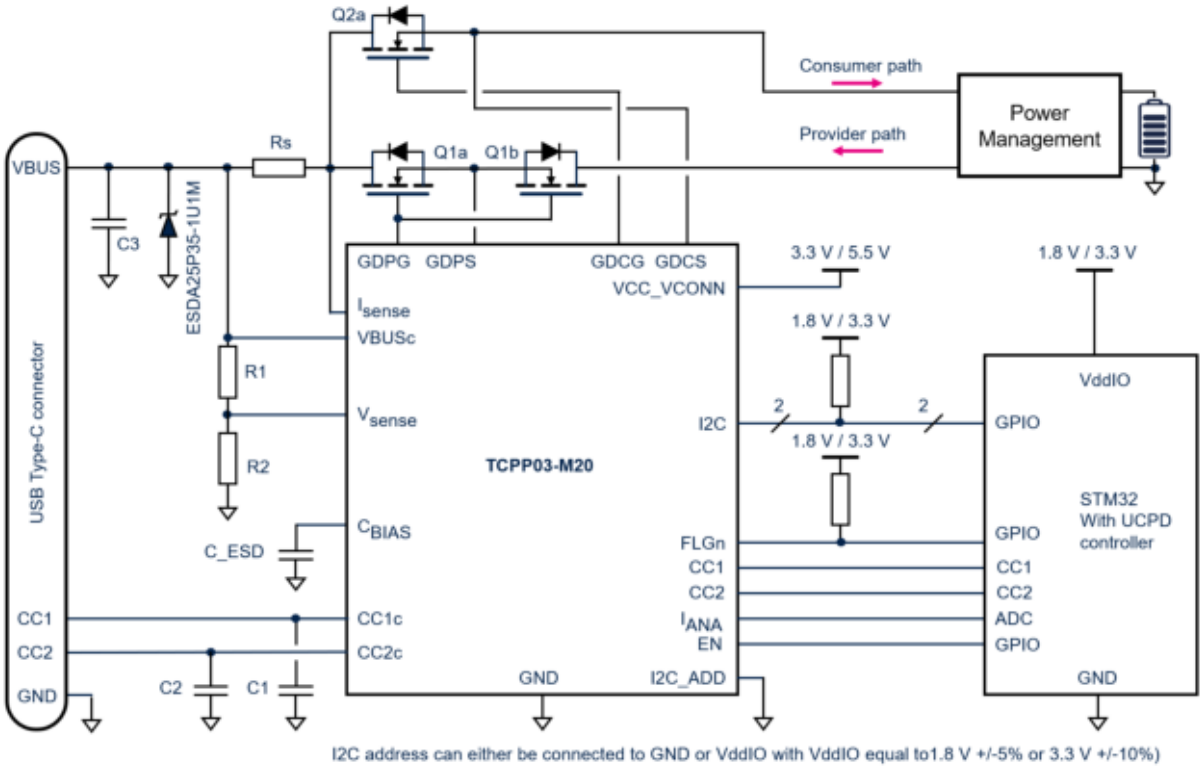


Figure 6. **Application schematic when no residual voltage on consumer path**



4 Electrical specification

4.1 Parameter conditions

Unless otherwise specified:

- All voltages are referenced to GND
- The minimum and maximum values are guaranteed in the worst conditions of operating temperature, supply voltage and frequencies, by tests in production on 100 % of the devices

4.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings, -40 °C < T_j < 125 °C

Symbol	Parameter	Pins	Value	Unit
V_{POWER}	Voltage for power pins	VCC_VCONN	7	V_{DC}
V_{IN}	Voltage for input pins	EN, V_{sense}, I2C_ADD	7	
		VBUSc, I_{sense}, GDPs, GDCs	24	
V_{OUT}	Voltage for output pins	I_{ANA}, FLGn	7	
		C_{BIAS}, GDPg, GDCg	24	
$V_{I/O}$	Voltage for input, output pins	SDA,SCL, CC1,CC2	7	
		CC1c,CC2c	24	
T_J	Operating junction temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C

Table 3. ESD ratings, -40 °C < T_j < 125 °C

Symbol	Description	Pins	Value	Unit
V_{ESD_c}	System level ESD robustness on USB Type-C connector side(1) IEC61000-4-2 Level 4, contact discharge IEC61000-4-2 Level 4, air discharge	CC1c, CC2c	 8 15	kV
V_{HBM}	V_{ESD} ratings human body model (JESD22-A114D, level 2)	All pins	2	kV

1. *Internal ESD protection functionality is associated with external capacitor connected on pin C_{BIAS}.*

4.3 Thermal resistances

Table 4. Thermal resistance parameters

Symbol	Parameter	Max. value	Unit
R_{thj-a}	Junction to ambient thermal resistance	150	°C/W

4.4 Recommended operating conditions

Table 5. Recommended operating conditions, -40 °C < T_j < 125 °C

Pins	Min.	Max.	Unit
VCC_VCONN, CC1, CC2, V_{SENSE}	2.7	5.5	V
EN, I_{ANA}, I2C_ADD, SDA, SCL, FLGn	1.7	3.6	V
CC1c, CC2c, VBUSc, I_{SENSE}, GDPs, GDCs	0	22	V

4.5 Power supply (VCC_VCONN, VBUSc)

Table 6. Electrical characteristics, -40 °C < T_j < 125 °C

Symbol	Parameter	Test conditions	Value		Unit
			Min..	Max.	
ICC_VCONN	V_{cc} supply current	Normal mode	-	2.7	mA
		Low power mode	-	1	µA
I_{enable}	Supply current of EN pin(1)	Low power mode 1.7 V - 2.7 V	-	3	µA
		Low power mode 2.7 V - 3.6 V	-	10	µA
I_{L_VBUSc}	VBUSc Supply current	V_{BUSc} = 22 V	-	2	mA
		V_{BUSc} = 5 V	-	0.7	
t_{DIS_VBUSc}	VBUSc discharge time(2)		-	220	ms

1. *EN pin is dynamically triggered then rise time lower than 50 µs is mandatory.*
2. *Equivalent discharge resistor is 2.5 kΩ.*

4.6 VBUS OVP, OCP, gate drivers, current monitoring

Table 7. Electrical characteristics for V_{BUS}, -40 °C < T_j < 125 °C

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
VBUS_UVLO	VBUS under voltage lock out		1.9	2.4	2.9	V
V_{GS}	Gate to source voltage		4.5	5	5.5	V
V_{OVP_TH}	OVP V_{BUS} threshold voltage	Vsense pin voltage	1.1	1.16	1.25	V
$t_{OVP_ON_VBUS}$	OVP V_{BUS} turn-on time			95	145	ns
$V_{TH_OCP_VBUS}$	V_{BUS} OCP threshold voltage	Across sense resistor Rs	35	42	45	mV
$t_{OFF_OCP_VBUS}$	V_{BUS} OCP response time			3	8	µs
Gain_I_{ANA}	Current sensing gain measured between 30 % and 60 % of maximal range.	($V_{Iana_60\%}$ - $V_{Iana_30\%}$) / ($V_{Rsense_60\%}$ - $V_{Rsense_30\%}$)	39	42	45	V/V
Offset_I_{ANA}	Input offset measurement between 30 % and 60 % of maximal range.	V_{Rsense} - $V_{I_{ANA}}$ / Gain	-2	0	2	mV
$V_{I_{ANA}}$	I_{ANA} pin output voltage during OCP event on VBUS line			1.7	1.95	V
t_{ON}(1)	V_{BUS} turn-on time			1	3	ms

1. *t_{ON} time can be reduced by addition of CGD capacitor.*

4.7 CC lines OVP and ESD response

Table 8. Electrical characteristics, -40 °C < T_j < 125 °C

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
R_{ON_CC}	ON resistance	Normal mode		0.7	1.5	Ω
		Low power mode	8	17	28	
C_{ON_CC}	Equivalent ON capacitance in normal mode	0 < V_{CCxc} < 1.2 V, f = 400 kHz	40	60	100	pF
V_{TH_CC}	OVP threshold voltage		5.5	5.75	6	V
V_{MIN}	Minimum voltage	Current on CC1c or CC2c < 60 µA	0.7			V
R_{DB}	DB resistor	Measured with 400 µA on CC1c / CC2c	4.1	5.1	5.6	kΩ
t_{OVP_CC}	OVP response time			60	100	ns
BW_{CCx}	Bandwidth	at -3dB and 0 < V_{CCxc} < 1.2 V		10		MHz

Table 9. IEC61000-4-2 ±8 kV contact discharge response

TCPP03-M20 and STM32G071 state	ESD	First peak	V_{CL} 30 ns
OFF	+8 kV	9.2 V	3.3 V
OFF	-8 kV	-7.7 V	-1.0 V
ON	+8 kV	14.8 V	6.3 V
ON	-8 kV	-11.8 V	-1.5 V

Note: Measurements are performed on X-NUCLEO-DRP1M1 board plugged on top of NUCLEO-G071RB. Ten ESD discharges are applied on connector (CC1c and CC2c) and voltage measurement is done on MCU side (CC1 and CC2), STM32 is still functional after the ESD discharges.

4.8 VCONN OCP

Table 10. Electrical characteristics, -40 °C < T_j < 125 °C

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
R_{ON_VCONN}	ON resistance		2.1	3	5.5	Ω
I_{VCONN}	FET max operating current	VCONN = 3.0 V - 5.5 V			40	mA
$R_{dis\text{-}vconn}$	Discharge resistor		2.5	4	5	kΩ
OCP_{TH_VCONN}	OCP threshold		40	47	55	mA
t_{OCP_VCONN}	OCP response time			0.9	2	µs

5 Electrical characteristic curves

Figure 7. VBUS turn-on time (t_{ON})

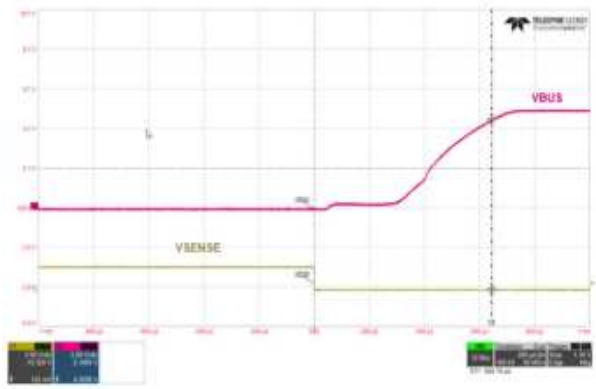
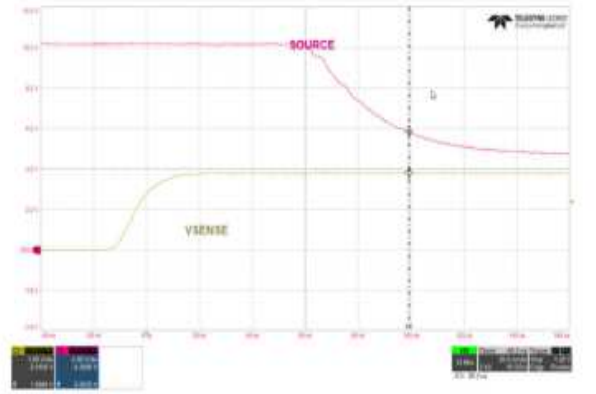
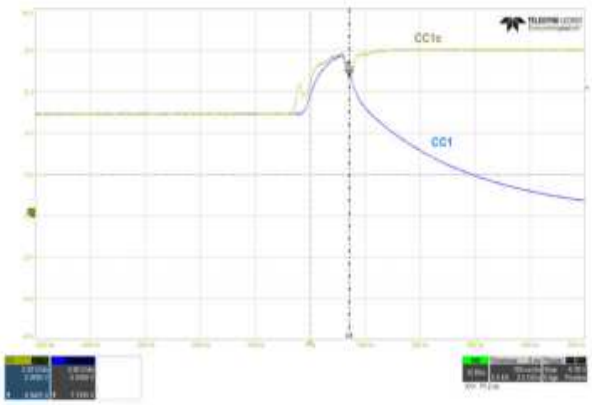


Figure 8. VBUS OVP response time



Note: Test conditions for Figure 7 and Figure 8: TCPP03-M20 is in hibernate mode VCC_VCONN = ENABLE = 0 V, VBUS = 5 V.

Figure 9. CC line (CC1 or CC2) OVP response time



Note: Test conditions for Figure 9: TCPP03-M20 in normal mode VCC_VCONN = +5 V, ENABLE = 3.3 V, VBUS = 0 V.

6 Functional description

6.1 Overview

The TCPP03-M20 is a cost effective solution to protect microcontrollers featuring built-in USB-C power delivery (UCPD) controller or other low voltage power delivery controller. It is especially adapted to dual role power, dual role data applications but also for sink applications requiring a current sense functionality.

6.2 Power modes

The TCPP03-M20 embeds three distinct power modes controlled by the UCPD controller via the I2C bus.

Figure 10. Power mode process

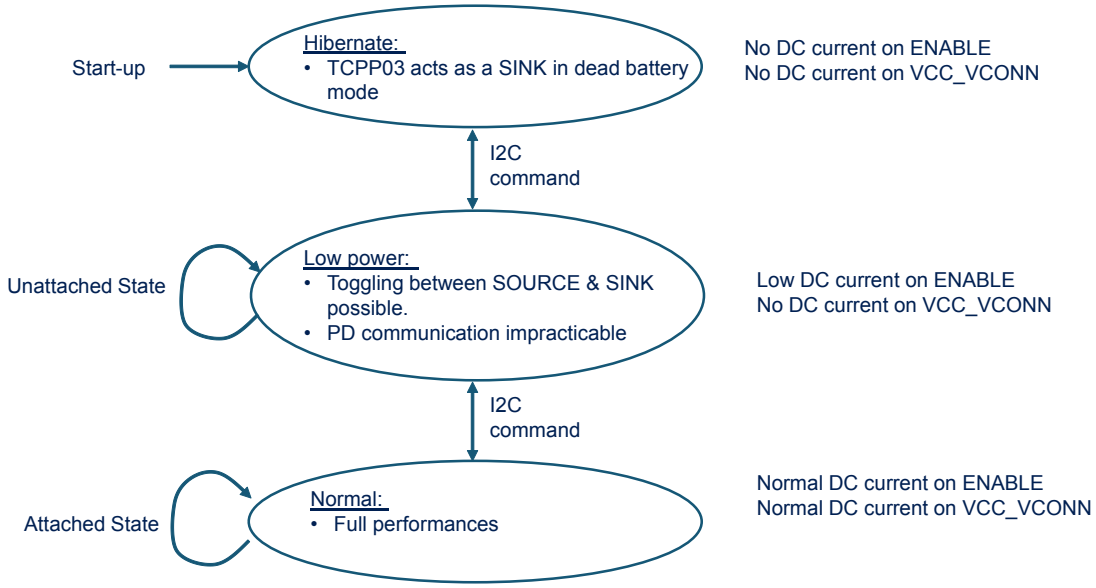


Table 11. Power modes versus power supply

VCC_VCONN	ENABLE	I_{DC} VCC_VCONN	I_{DC} ENABLE	Mode	Comments
X	0 V	0 µA	0 µA(1)	OFF (reset)	Dead batteries enabled FLGn indicates VBUS voltage I2C inactive / I2C registers reset
X	1.8 V ±5%, or 3.3 V ±10%	0 µA	0 µA(1)	Wake-up / Hibernate	Dead batteries enabled FLGn indicates VBUS voltage I2C active Default state at start-up
X	1.8 V ±5%, or 3.3 V ±10%	0 µA	< 10 µA(1)	Low power	Dead batteries disabled High ohmic CC => No PD communication possible OVP protection by clamping FLGn indicates VBUS voltage I2C active
2.7 V to 5.5 V	1.8 V ±5%, or 3.3 V ±10%	2.7 mA	< 30 µA(1)	Normal	Dead batteries disabled Full performance mode I2C active FLGn indicates failures

1. *Dynamic currents of I2C interface have to be added to the values indicated when the I2C bus is used.*

Table 12. TCPP03-M20 states versus power modes

Power mode	CC switches	OVP CC	Dead batteries	Gate driver consumer	Gate driver provider	OVP VBUS	FLGn	I2C	I_{ANA}	OCP VBUS	V_{CONN} VBUS Dis.	Comment
OFF	OFF	NA	ON	ON(1)	OFF	ON	VBUS connect	OFF	OFF	OFF	OFF	TCPP not powered
Wake-up / Hibernate	OFF	NA	ON	Controlled by I2C	OFF	ON	VBUS connect	ON	OFF	OFF	OFF	Default state at start-up
Low power	High ohmic	5 V clamp	OFF	Controlled by I2C	OFF	ON	VBUS connect	ON	OFF	OFF	OFF	Signaling only
Normal	Full perf.	Active OVP	OFF	Controlled by I2C		ON	Failure flags	ON	ON	ON	Controlled by I2C	PD communication active

1. *Consumer (sink) gate driver is self biased with VBUSc voltage*

6.3 I2C

6.3.1 I2C registers

The I2C address used by TCPP03-M20 is 0110 10x, with LSB = ‘x’.

The LSB bit of the I2C address is set when connecting TCPP03-M20 pin I2C_ADD to GND (for LSB = ‘0’) or VddIIO (for LSB = ’1’).

Figure 11. I2C registers

I2C address : 0110 10x, x=LSB

VCONND=1:
- VCONN discharge ON

VCONND=0:
- VCONN discharge OFF

VBUSD=1:
- VBUS discharge ON

VBUSD=0:
- VBUS discharge OFF

PM2	PM1	Power Mode
0	0	Hibernate
1	0	Low power
0	1	Normal
1	1	Not Used

GDC=1:
- Switch load opened

GDC=0:
- Switch load closed

GDP=1:
- Switch load closed

GDP=0:
- Switch load opened

V2	V1	VCONN switch	
		VC2	VC1
0	0	Open	Open
1	0	Close	Open
0	1	Open	Close
1	1	Open	Open

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Writing register (address = 0)	VCONN DISCHARGE (VCONND)	VBUS DISCHARGE (VBUSD)	PM2 Power Mode 2	PM1 Power Mode 1	Gate Driver Consumer (GDC)	Gate Driver Provider (GDP)	V2	V1
Reading register n°1 (address = 1) Flags are set to '1' when active	VCONN DISCHARGE Acknowledge	VBUS DISCHARGE Acknowledge	PM2 Acknowledge	PM1 Acknowledge	Gate Driver Consumer Acknowledge	Gate Driver Provider Acknowledge	VCONN2 Acknowledge	VCONN1 Acknowledge
Reading register n°2 (address = 2) Flags are set to '1' when active	0 => TCPP03 1 => TCPP02	0	FLGn VBUS_OK	FLGn OVP_CC	FLGn OTP	FLGn OVP_VBUS	FLGn OCP_VBUS	FLGn OCP_VCONN

6.3.2 I2C data rate

The I2C slave data rate is limited to 1 Mbps.

6.3.3 I2C voltage selection

I2C voltage is set by the voltage applied on ENABLE pin (1.8 V or 3.3 V).

7 Protection features

TCPP03-M20 embeds protection features for dual role power (DRP), dual role data (DRD) applications, as required by:

- USB-C specification
- USB power delivery specification 3.1
- International electrotechnical commission (IEC)

7.1 FLGn pin description

FLGn pin is an open-drain output flag in steady state, it must be left floating when not connected.

In hibernate and low power modes FLGn indicates voltage presence on VBUS.

In normal mode, FLGn indicates an error (OVP, OCP or OTP): I2C registers must be read to identify the error. Recovery for each error type is described in each section of below paragraphs.

7.2 How to protect against ESD (electrostatic discharge) applied on the USB Type-C connector?

Electrostatic discharges can be conducted by the USB Type-C connector and may damage the electronic circuitry of the application.

The TCPP03-M20 integrates ESD protection for CC1 and CC2 lines up to +8 kV contact discharge (IEC 61000-4-2), associated with an external 100 nF - 50 V capacitor on C_{BIAS} pin.

7.3 VBUS management

An overvoltage protection is required on VBUS when the absolute maximum ratings of your power management integrated circuit is below the maximum voltage that can be applied on VBUS.

Until now, it was common to find the protection circuit inside a controller dedicated to USB-C power delivery. However, by supporting USB-C PD with an embedded module inside an MCU and a companion Type-C port protection device, you can lower your bill of material and facilitate the transition, without requiring an expensive USB-C PD ASIC controller. One of the reasons the MCU and TCPP03-M20 bundle is such a compelling financial proposition is that the latter device integrates the VBUS gate drivers, which enable the use of cost-effective and smaller N-MOSFETs, instead of the P-MOSFETs usually used by ASIC controllers.

This is an added value of TCPP03-M20, specially when the VBUS line is misfed if a defective charger is stuck at a higher voltage than negotiated or a defective cable is inserted.

Overvoltage protection is always required on the VBUS line to prevent against a voltage higher than negotiated on the VBUS.

This use case can occur even when power delivery is not used i.e when theVBUS voltage is 5 V.

7.3.1 VBUS turn-on

VBUS turn-on time after I2C command is achieved in t_{ON} = 1 ms (see Figure 7).

7.3.2 VBUS UVLO (under voltage lock out)

This block continuously monitors VBUS voltage. It acts as:

- An UVLO (under voltage lock out) for the VBUS circuitry: OVP_VBUS and consumer gate driver are enabled once the VBUS voltage reaches VBUS_UVLO voltage level (2.4 V typ.)
- It signals to the I2C block the presence of a voltage on VBUS when the VBUS voltage reach VBUS_UVLO voltage level (2.4 V typ.)

7.3.3 VBUS OVP turn-on and turn-off

When V_{SENSE} pin voltage goes above V_{OVP_TH}, OVP is turned ON in less than 95 ns ($t_{OVP_ON_VBUS}$ typical value), and FLGn pin goes to 'low-Z' state.

Fast shut-down is enabled by TCPP03-M20 gate driver by shorting the MOSFET gate and source pin. As a result, source pin goes safely to 0 V and I2C register is updated with relevant value.

OVP recovery is ensured after a typical delay of 64 µs: the external power mosfet is turned-on and Flag pin FLGn goes back to Hi-Z state after the end of the OVP condition.

7.3.4 How to set TCPP03-M20 OVP threshold according to VBUS maximum voltage allowed by the application

As shown in Figure 4, R1 / R2 bridge gives an image of VBUS voltage to set TCPP03-M20 OVP threshold.

With fixed R1 value (10 kΩ), the table provides R2 values for various TCPP03-M20 OVP threshold according to VBUS maximum voltage allowed by the application.

Table 13. R2 values versus VBUS OVP threshold when R1 = 10 kΩ

R2	VBUS max.	P max.
2.4 kΩ	6 V	15 W
1.3 kΩ	10 V	27 W
976 Ω	13 V	36 W
732 Ω	17 V	45 W
560 Ω	22 V	100 W

7.4 VBUS current sense (I_{ANA} pin)

The I_{ANA} output pin is active only in normal mode.

The I_{ANA} output can be connected directly to the STM32 ADC input because it is internally biased by EN pin.

The I_{ANA} output voltage is lower than 1.8 V to be compatible with 1.8 V and 3.3 V MCU I/O.

7.5 V_{BUS} analog current measurement and bidirectional OCP

The over current protection on VBUS is bidirectional i.e active for both consumer (i.e sink or UFP application) and provider (i.e source or DFP application) power paths.

VBUS OCP threshold is set by external serial resistor on VBUS. The gain for the analog reading is set to 42 V/V.

The OCP VBUS is biased by VCC_VCONN and works only in normal mode.

Equivalent block diagram in TCPP03-M20 for V_{BUS} analog current measurement and OCP is given here after:

Figure 12. Equivalent block diagram in TCPP03-M20

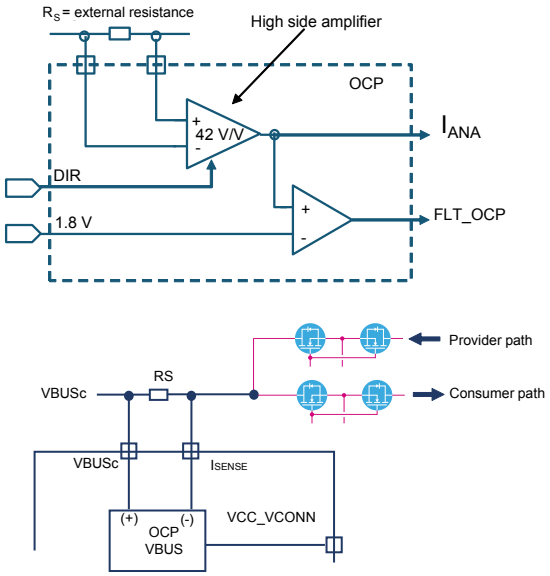


Table 14. Recommended values

Typical current	VBUS OCP threshold	Rs - Sense resistor (normalized values)
0.5 A	0.9 A	47 mΩ
1.5 A	1.9 A	22 mΩ
3.0 A	4.2 A	10 mΩ
5.0 A	6.0 A	7 mΩ

The OCP is biased continuously: inrush current magnitude is controlled by the user through an external capacitor.

Please refer to the X-NUCLEO-DRP1M1 user manual for more informations on external capacitor to control the insrush current magnitude.

If an OCP event occurs:

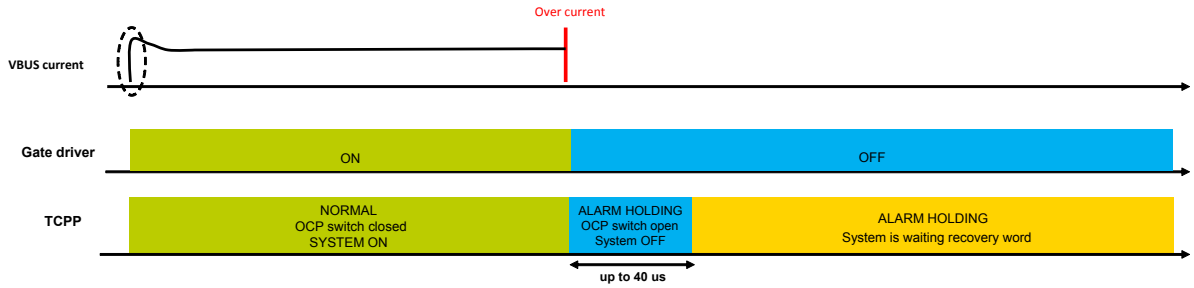
- V_{CONN} switches, CC switches and gate drivers are shutting down
- During up to 40 µs typ., this OCP alarm is held (no recovery is possible)
- After this delay, CC switches are turned ON but V_{CONN} switches and gate drivers are held OFF

The system can be restarted only with a recovery word sent by the MCU via the I2C bus.

- The FLGn signal stays low as long as the recovery word has not been sent

The recovery word is described in the next paragraph

Figure 13. Typical chronograms of TCPP03-M20 VBUS OCP



Note:

- *In case of VBUS OCP event, the TCPP03-M20 switches OFF:*
  - *V_{CONN} switches*
  - *VBUS gate driver (provider and consumer)*
  - *V_{CONN} and V_{BUS} discharge paths are activated*
  - *CC lines remain active*
- *It is signaled to the user by several ways:*
  - *I2C corresponding state bits are cleared (i.e. VCONN1_ACK = 0, VCONN2_ACK = 0…)*
  - *I2C relevant OCP flag is set (FLGn_OCP_VBUS is the OCP event coming from VBUS switch for example)*
  - *Failure flag pin (FLGn) is active (i.e. in LowZ state)*
- *After a delay of up to 40 µs, recovery word can be written and the MCU can resume a start-up procedure.*

Table 15. VBUS OCP recovery bit sequence table

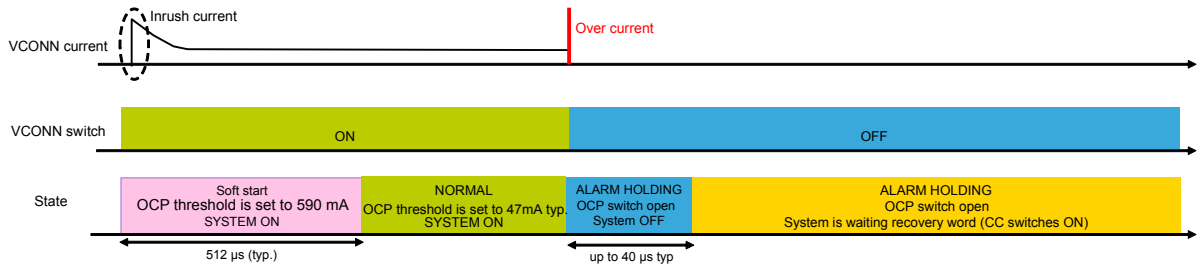
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	PM2	PM1	1	0	0	0

Refer to Figure 11 more further information.

7.6 V_{CONN} OCP

- At start-up, a soft start sets the tripping current to about 590 mA during 512 µs min. (1ms max.)
- After this delay, the soft start is ended and the normal OCP threshold occurs (50 mA)
- If an OCP event occurs:
  - V_{CONN} switches, CC switches and gate drivers are shutting down
  - During up to 40 µs, this OCP alarm is held (no recovery is possible)
  - After this delay, CC switches are turned ON but V_{CONN} switches and gate drivers are held OFF. The system can be restarted only with a recovery word send by the MCU via the I2C bus.
  - The FLGn signal stays low as long as the recovery word has not been sent

Figure 14. V_{CONN} OCP chronograms



After a delay up to 40 µs, recovery word can be written and the MCU can resume a start-up procedure.

Table 16. V_{CONN} OCP recovery bit sequence table

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	PM2	PM1	1	0	0	0

Refer to Figure 11 more further information.

7.7 CC line OVP

7.7.1 CC lines short to VBUS

USB Type-C standard specifies a pitch of 0.5 mm between connector pins. Considering tolerances on the connector dimensions, the distance between two pins can be as low as 0.21 mm.

VBUS pin being adjacent to the CC pins, when removing the USB Type-C plug from the connector, VBUS can be shorted to CC lines and apply a voltage higher than specified for CC lines.

Over voltage protection is needed on the CC lines because VBUS typical voltage can be as high as 20 V while CC pins are usually 5 V tolerant I/Os on low voltage USB-PHY controllers.

The TCPP03-M20 integrates this protection against CC lines short to VBUS thanks to an overvoltage protection (integrated FET).

When the voltage on the CC line goes above V_{TH_CC}, the OVP on CC line turns-on in less than 60ns (t_{OVP_CC}) and FLGn pin goes to '0' state.

When the OVP event disappears, the OVP on the CC line is turned-off and the FLGn pin goes back to 'Hi-Z' state.

7.8 VBUS discharge

VBUS discharge is activated via I2C bus and controlled via firmware by the USB-C power delivery controller.

The VBUS discharge feature allows to discharge 10 µF in less than 220 ms (t_{DIS_VBUS}).

This discharge time is in line with USB-C specification:

Table 17. Common source electrical parameters from USB-C specification

Parameter	Description	Min.	Typ.	Max.	Units
tSafe0V	Time to reach vSafe0V max.	-	-	650	ms
tSafe5V	Time to reach vSafe5V max.	-	-	275	ms

7.9 V_{CONN} discharge

V_{CONN} discharge is activated via I2C bus and controlled via firmware by the USB-C power delivery controller.

The V_{CONN} discharge feature integrated in TCPP03-M20 allows to discharge V_{CONN} in R_{DIS_VCONN} < 5.5 kΩ, as per USB-C specification table extracted below:

Table 18. V_{CONN} source characteristics from USB-C power delivery specification

Parameter	Min.	Max.	Notes
R_{dch}	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

Note:

- *V_{CONN} discharge is activated and stopped via I2C software from USB-PD controller*
- *To avoid short-circuit, V_{CONN} discharge cannot be activated if V_{CONN} switch are closed*
- *The last active CC pin used for V_{CONN} is discharged.*

7.10 OTP (over temperature protection)

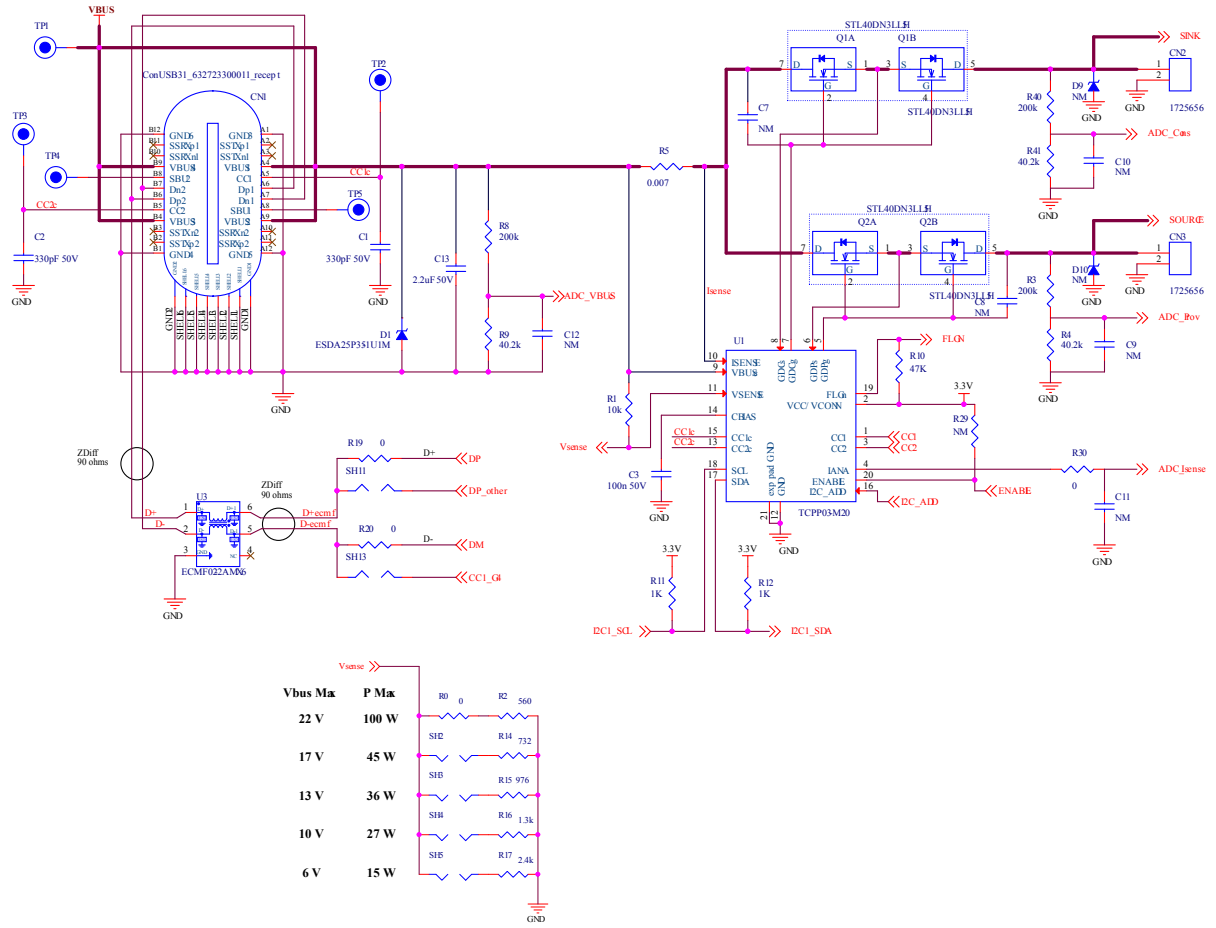
Above 150°C, the OTP triggers the FLGn pin.

OVP and OCP on VCONN, CC lines, VBUS are shut down.

Auto recovery is ensured when the temperature goes back below OTP threshold.

8 USB-C dual role power schematic example

Figure 15. **Schematic extract of nucleo expansion board X-NUCLEO-DRP1M1 using TCPP03-M20**



8.1 External components description

Table 19. **Schematic description**

Component reference	Component name or value	Description
D1	ESDA25P35-1U1M	TVS protecting against 25 A 8/20 µs surge waveforms and ESD transients (see Transient voltage suppressor on VBUS).
C1, C2	330 pF, 25 V	EMI capacitor, required to comply with USB-C specification.
C3	100 nF, 50 V	X7R ESD protection capacitance with low ESL required to comply with USB-C specification.
C13	2.2 µF, 50 V	VBUSc bulk capacitance, required in the USB-C power delivery specification.
R5	0.007 Ω	Serial resistor which value sets the VBUS OCP threshold.
R1 R2 or R14 or R15 or R16 or R17	See Table 13	Resistor bridge to set VBUS OVP threshold.

8.2 Bulk capacitance

USB-C power delivery specification defines cSnkBulk and cSrcBulk capacitances as the sum of bulk capacitances on both sides of the ohmic path of VBUSc.

To insure compliance with the standard and TCPP03-M20 protection performances, it is mandatory to place this capacitance on VBUSc, as close as possible to the USB-C connector with a value of 2.2 µF - 50 V.

9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN-20L package information

Figure 16. QFN-20L 4.0 x 4.0 x 0.75 mm package outline

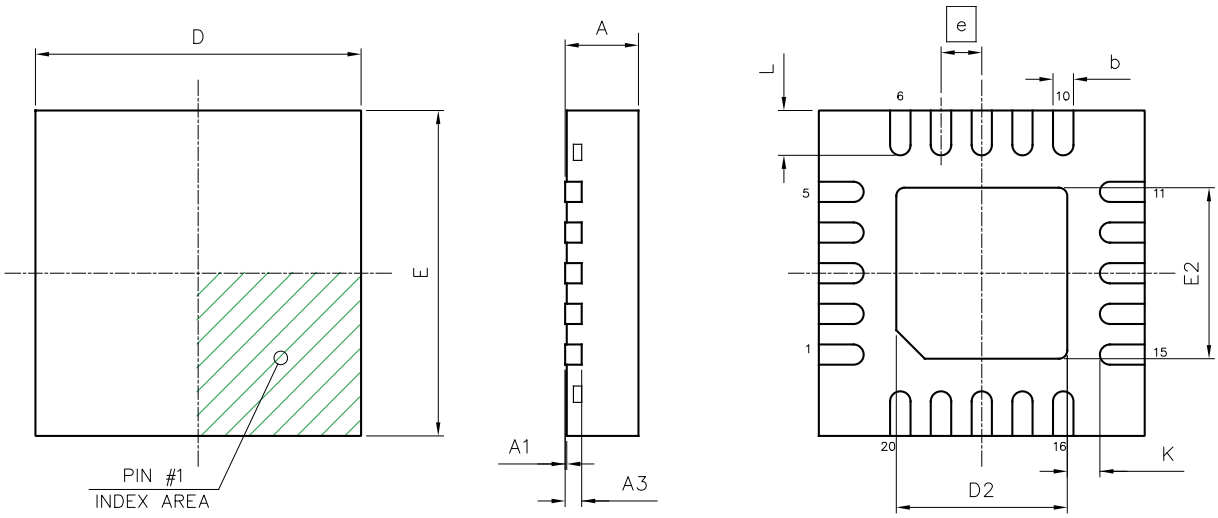


Table 20. QFN-20L package mechanical data

Ref.	Dimensions in millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1		0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.95	4.00	4.05
D2	1.95	2.10	2.20
E	3.95	4.00	4.05
E2	1.95	2.10	2.20
e		0.50 BSC	
L	0.45	0.55	0.65
K	0.20		

Figure 17. recommended footprint (dimensions are in mm)

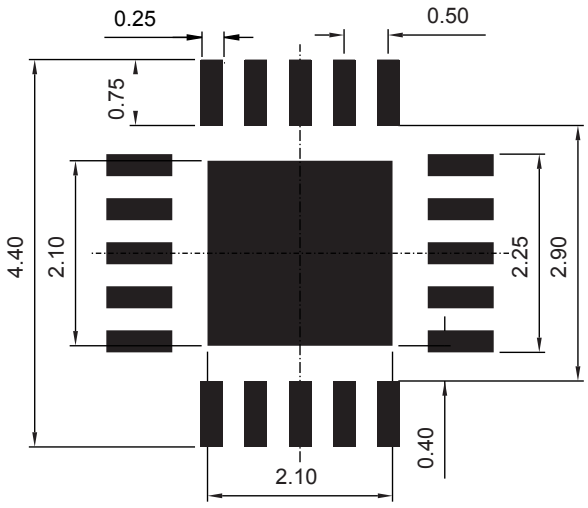


Figure 18. Marking layout

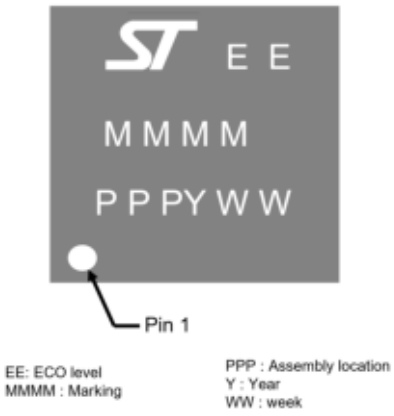
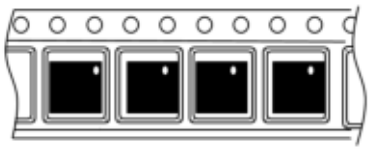


Figure 19. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 20. Tape and reel orientation

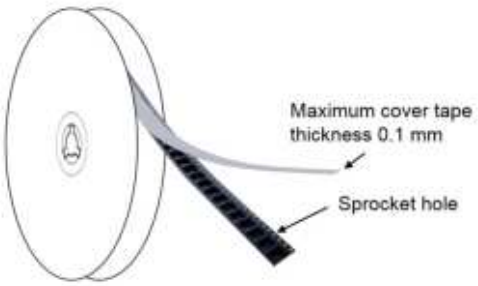


Figure 21. Reel dimensions (mm)

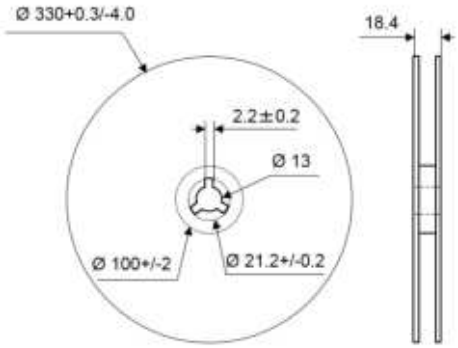


Figure 22. Inner box dimensions (mm)

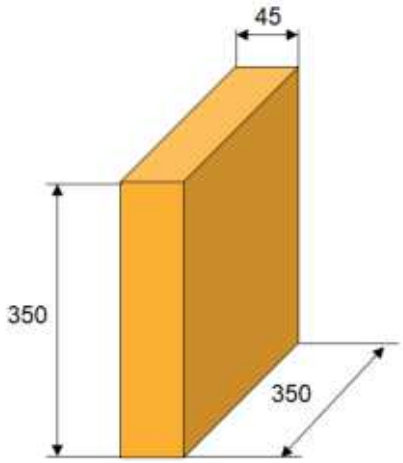
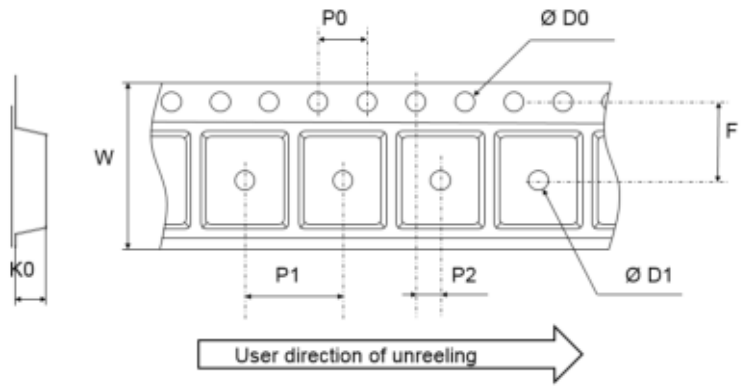


Figure 23. **Tape outline**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 21. **Tape dimension values**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.5	1.55	1.6
D1	1.5		
F	5.4	5.5	5.6
K0	1.0	1.1	1.2
P0	3.9	4.0	4.1
P1	7.9	8.0	8.1
P2	1.9	2.0	2.1
W	11.7	12	12.3

10 Ordering information

Table 22. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TCPP03-M20	TCPP03	QFN-20L 4.0 x 4.0 x 0.75 mm	36.1 mg	3000	Tape and reel

Appendix A Appendix A Reference documents

Table 23. Reference documents

Doc name	ID	Title
TA0357	DM00496853	Overview of USB Type-C and Power Delivery technologies.
AN5225	DM00536349	USB Type-C® Power Delivery using STM32 MCUs and MPUs.
AN4871	DM00294046	USB Type-C® protection and filtering.
AN3353	DM00023467	IEC 61000-4-2 standard testing.

Table 24. Associated expansion boards

Expansion board	Part number	SW expansion board	USB type-C application
X-NUCLEO-SNK1M1	TCPP01-M12	X-CUBE-TCPP	Sink, UFP, consumer
X-NUCLEO-SRC1M1	TCPP02-M18		Source, DFP, provider
X-NUCLEO-DRP1M1	TCPP03-M20		DRP, dual role power DRD, dual role data Sink requiring current sense and OCP

Table 25. Certifications and tools

Reference	Description
TID6408	https://groups.usb.org/cas/login?service=https%3A//cms.usb.org/casservice%3Fdestination%3D/usb_device/certificate/43767
wiki.st.com	https://wiki.st.com/stm32mcu/wiki/Category:USB_Power_Delivery
github.com	https://github.com/STMicroelectronics/x-cube-tcpp

Revision history

Table 26. **Document revision history**

Date	Revision	Changes
21-Jun-2021	1	Initial release.
04-Oct-2021	2	Updated Features, *Table 6* and *Table 26*.
01-Jun-2023	3	Added note in *Table 6*. Minor text changes. Minor text changes.
27-Jan-2025	4	Updated Iana Gain in Table 7 .
25-Sep-2025	5	Updated Figure 1.

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