- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Digital Visual Interface (DVI) Compliant(1)**
- **Supports Pixel Rates Up to 165MHz (Including 1080p and WUXGA at 60Hz)**
- **Universal Graphics Controller Interface**
  - **12-Bit Dual-Edge and 24-Bit Single-Edge Input Modes**
  - **Adjustable 1.1-V to 1.8-V and Standard 3.3-V CMOS Input Signal Levels**
  - **Fully Differential and Single-Ended Input Clocking Modes**
  - **Standard Intel™ 12-Bit Digital Video Port Compatible as on Intel 81x Chipsets**
- **Enhanced PLL Noise Immunity**
  - **On-Chip Regulators and Bypass Capacitors for Reducing System Costs**
- **Enhanced Jitter Performance**
  - **No HSYNC Jitter Anomaly**
  - **Negligible Data-Dependent Jitter**
- **Programmable Using I²C Serial Interface**
- **Monitor Detection Through Hot-Plug and Receiver Detection**
- **Single 3.3-V Supply Operation**
- **64-Pin Thin Quad Flat Pack (TQFP) Using TI's PowerPAD™ Package**
- **TI Advanced 0.18-µm EPIC-5™ CMOS Process Technology**
- **Pin Compatible With Sil164 DVI Transmitter**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description

The TFP410 is a Texas Instruments PanelBus™ flat panel display product, part of a comprehensive family of end-to-end digital visual interface (DVI) 1.0-compliant solutions, targeted at the PC and consumer electronics industry.

The TFP410 provides a universal interface to allow a glueless connection to most commonly available graphics controllers. Some of the advantages of this universal interface include selectable bus widths, adjustable signal levels, and differential and single-ended clocking. The adjustable 1.1-V to 1.8-V digital interface provides a low-EMI, high-speed bus that connects seamlessly with 12-bit or 24-bit interfaces. The DVI interface supports flat panel display resolutions up to UXGA at 165 MHz in 24-bit true color pixel format.

The TFP410 combines PanelBus circuit innovation with TI advanced 0.18-µm EPIC-5 CMOS process technology and ultralow ground inductance PowerPAD™ package. The result is a compact 64-pin thin quad flat pack (TQFP) package providing a reliable, low-current, low-noise, high-speed digital interface solution.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PAP – TQFP	Tape and reel	TFP410MPAPREP	TFP410MEP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

1. The digital visual interface (DVI) specification is an industry standard developed by the digital display working group (DDWG) for high-speed digital connection to digital displays and has been adopted by industry-leading PC and consumer electronics manufacturers. The TFP410 is compliant to the DVI Revision 1.0 specification.

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VESA is a trademark of Video Electronics Standards Association.
Intel is a trademark of Intel Corporation.

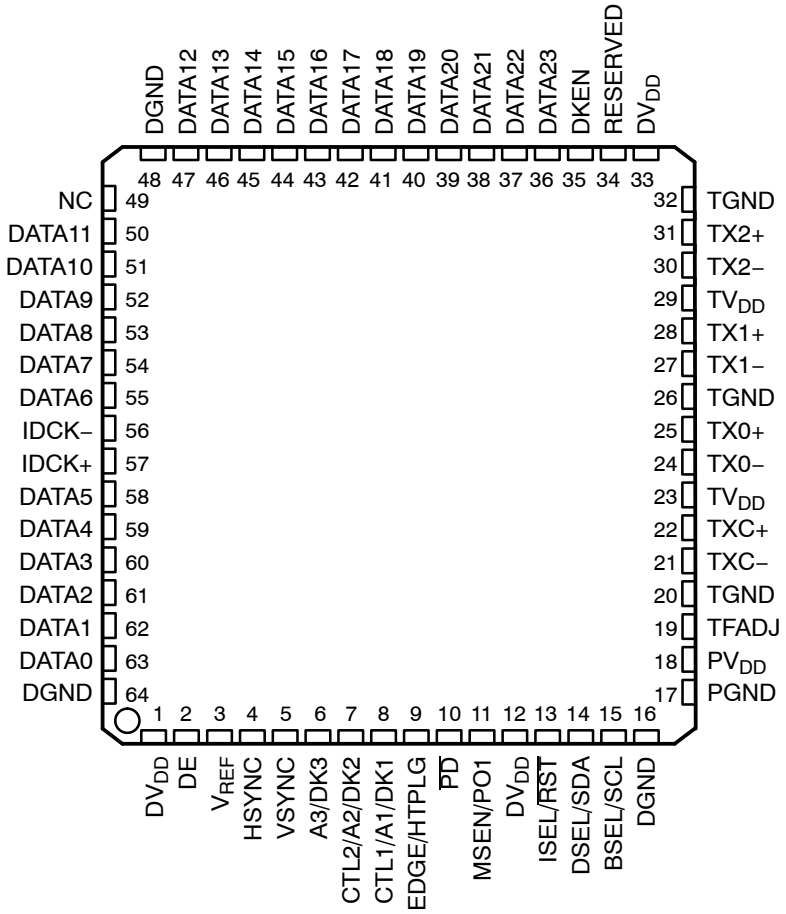
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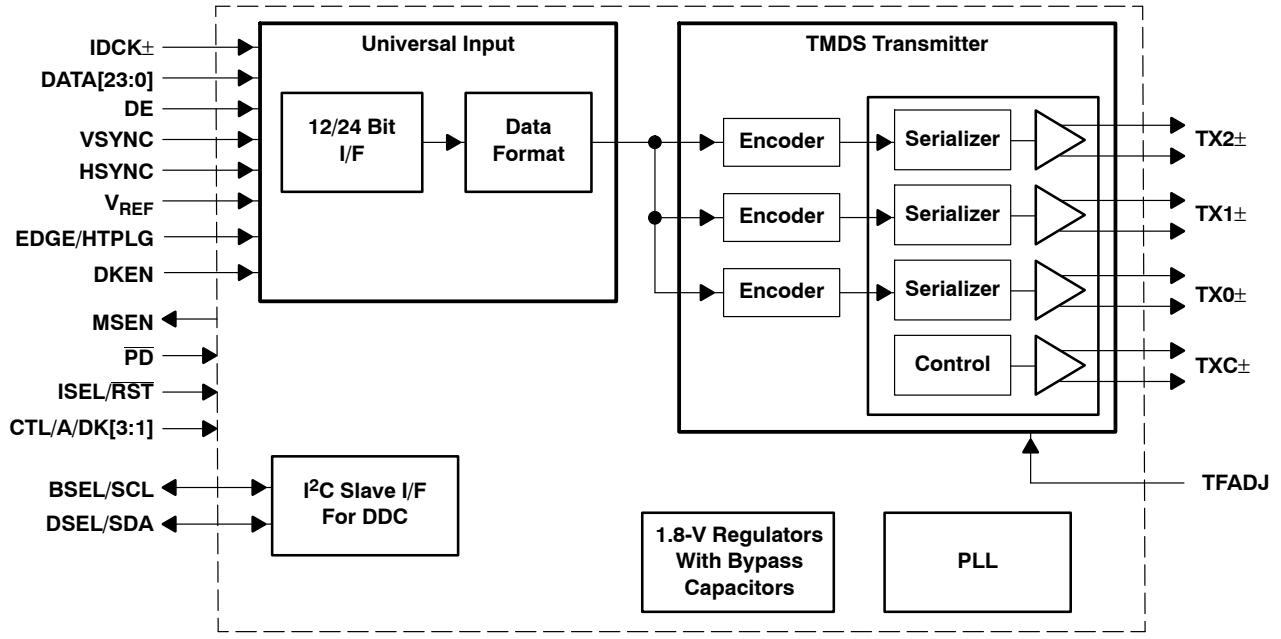
This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

pin assignments

PAP PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
Input			
A3/DK3 CTL2/A2/DK2 CTL1/A1/DK1	6 7 8	I	The operation of these three multifunction inputs depends on the settings of the ISEL (pin 13) and DKEN (pin 35) inputs. All three inputs support 3.3-V CMOS signal levels and contain weak pulldown resistors so that, if left unconnected, they default to all low. When the I^2C bus is disabled (ISEL = low) and the deskew mode is disabled (DKEN = low), pins 7 and 8 become the control inputs, CTL[2:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). Pin 6 is not used. When the I^2C bus is disabled (ISEL = low) and the deskew mode is enabled (DKEN = high), these three inputs become the deskew inputs DK[3:1], used to adjust the setup and hold times of the pixel data inputs DATA[23:0], relative to the clock input IDCK±. When the I^2C bus is enabled (ISEL = high), these three inputs become the three LSBs of the I^2C slave address, A[3:1].
DATA[23:12]	36–47	I	Upper 12 bits of the 24-bit pixel bus In 24-bit, single-edge input mode (BSEL = high), this bus inputs the top half of the 24-bit pixel bus. In 12-bit, dual-edge input mode (BSEL = low), these bits are not used to input pixel data. In this mode, the state of DATA[23:16] is input to the I^2C register CFG. This allows eight bits of user configuration data to be read by the graphics controller through the I^2C interface (see the I^2C *register descriptions* section). Note: All unused data inputs should be tied to GND or V_{DD}.
DATA[11:0]	50–55, 58–63	I	Lower 12 bits of the 24-bit pixel bus/12-bit pixel bus input In 24-bit, single-edge input mode (BSEL = high), this bus inputs the bottom half of the 24-bit pixel bus. In 12-bit, dual-edge input mode (BSEL = low), this bus inputs one-half a pixel (12 bits) at every latch edge (both rising and falling) of the clock.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DE	2	I	Data enable. As defined in DVI 1.0 specification, the DE signal allows the transmitter to encode pixel data or control data on any given input clock cycle. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC, VSYNC, and CTL[3:1].
HSYNC	4	I	Horizontal sync input
IDCK– IDCK+	56 57	I	Differential clock input. The TFP410 supports both single-ended and fully differential clock input modes. In the single-ended clock input mode, the IDCK+ input (pin 57) should be connected to the single-ended clock source and the IDCK– input (pin 56) should be tied to GND. In the differential clock input mode, the TFP410 uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data DATA[23:0], DE, HSYNC, and VSYNC. The differential clock input mode is only available in the low signal swing mode.
VSYNC	5	I	Vertical sync input
Configuration/Programming			
BSEL/SCL	15	I	Input bus select/I^2C clock input. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin is only 3.3-V tolerant. When I^2C is disabled (ISEL = low), a high level selects 24-bit input, single-edge input mode. A low level selects 12-bit input, dual-edge input mode. When I^2C is enabled (ISEL = high), this pin functions as the I^2C clock input (see the I^2C r*egister descriptions* section). In this configuration, this pin has an open-drain output that requires an external 5-kΩ pullup resistor connected to V_{DD}.
DKEN	35	I	Data deskew enable. The deskew function can be enabled either through I^2C or by this pin when I^2C is disabled. When deskew is enabled, the input clock to data setup/hold time can be adjusted in discrete trim increments. The amount of trim per increment is defined by $t_{(STEP)}$. When I^2C is disabled (ISEL = low), a high level enables deskew with the trim increment determined by pins DK[3:1] (see the d*ata deskew* section). A low level disables deskew and the default trim setting is used. When I^2C is enabled (ISEL = high), the value of DKEN and the trim increment are selected through I^2C. In this configuration, the DKEN pin should be tied to either GND or V_{DD} to avoid a floating input.
DSEL/SDA	14	I/O	DSEL/I^2C data. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin is only 3.3-V tolerant. When I^2C is disabled (ISEL = low), this pin is used with BSEL and V_{REF} to select the single-ended or differential input clock mode (see the *universal graphics controller interface modes* section). When I^2C is enabled (ISEL = high), this pin functions as the I^2C bidirectional data line. In this configuration, this pin has an open-drain output that requires an external 5-kΩ pullup resistor connected to V_{DD}.
EDGE/HTPLG	9	I	Edge select/hot plug input. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This input is 3.3-V tolerant only. When I^2C is disabled (ISEL = low), a high level selects the primary latch to occur on the rising edge of the input clock IDCK+. A low level selects the primary latch to occur on the falling edge of the input clock IDCK+. This is the case for both single-ended and differential input clock modes. When I^2C is enabled (ISEL = high), this pin is used to monitor the *hot plug* detect signal (see the DVI or VESA™ P&D and DFP standards). When used for hot-plug detection, this pin requires a series 1-KΩ resistor.
ISEL/$\overline{RST}$	13	I	I^2C interface select/I^2C reset (active low, asynchronous) If ISEL is high, the I^2C interface is active. Default values for the I^2C registers can be found in the I^2C r*egister descriptions* section. If ISEL is low, I^2C is disabled and the chip configuration is specified by the configuration pins (BSEL, DSEL, EDGE, V_{REF}) and state pins ($\overline{PD}$, DKEN). If ISEL is brought low and then back high, the I^2C state machine is reset. The register values are changed to their default values and are not preserved from before the reset.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MSEN/PO1	11	O	Monitor sense/programmable output 1. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin has an open-drain output and is only 3.3-V tolerant. An external 5-kΩ pullup resistor connected to V_{DD} is required on this pin. When I^2C is disabled (ISEL = low), a high level indicates a powered-on receiver is detected at the differential outputs. A low level indicates a powered-on receiver is not detected. This function is valid only in dc-coupled systems. When I^2C is enabled (ISEL = high), this output is programmable through the I^2C interface (see the I^2C *register descriptions* section).
$\overline{PD}$	10	I	Power down (active low). In the power-down state, only the digital I/O buffers and I^2C interface remain active. When I^2C is disabled (ISEL = low), a high level selects the normal operating mode. A low level selects the power-down mode. When I^2C is enabled (ISEL = high), the power-down state is selected through I^2C. In this configuration, $\overline{PD}$ should be tied to GND. Note**:** The default register value for $\overline{PD}$ is low, so the device is in power-down mode when I^2C is first enabled or after an I^2C reset.
V_{REF}	3	I	Input reference voltage. Selects the swing range of the digital data inputs (DATA[23:0], DE, HSYNC, VSYNC, and IDCK±). For high-swing 3.3-V input signal levels, V_{REF} should be tied to V_{DD}. For low-swing input signal levels, V_{REF} should be set to half of the maximum input voltage level. See the *recommended operating conditions* section for the allowable range for V_{REF}. The desired V_{REF} voltage level is typically derived using a simple voltage-divider circuit.
Reserved			
RESERVED	34	In	This pin is reserved and must be tied to GND for normal operation.
DVI Differential Signal Output			
TFADJ	19	I	Full-scale adjust. This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor R_{TFADJ} connected to TV_{DD}.
TX0+ TX0–	25 24	O	Channel 0 DVI differential output pair. TX0± transmits the 8-bit blue pixel data during active video and HSYNC and VSYNC during the blanking interval.
TX1+ TX1–	28 27	O	Channel 1 DVI differential output pair. TX1± transmits the 8-bit green pixel data during active video and CTL[1] during the blanking interval.
TX2+ TX2–	31 30	O	Channel 2 DVI differential output pair. TX2± transmits the 8-bit red pixel data during active video and CTL[3:2] during the blanking interval.
TXC+ TXC–	22 21	O	DVI differential output clock
Power and Ground			
DGND	16, 48, 64	Ground	Digital ground
DV_{DD}	1, 12, 33	Power	Digital power supply. Must be set to 3.3-V nominal.
NC	49	NC	No connection required. If connected, tie high.
PGND	17	Ground	PLL ground
PV_{DD}	18	Power	PLL power supply. Must be set to 3.3-V nominal.
TGND	20, 26, 32	Ground	Transmitter differential output driver ground
TV_{DD}	23, 29	Power	Transmitter differential output driver power supply. Must be set to 3.3-V nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, DV_{DD}, PV_{DD}, TV_{DD} . . . . . –0.5 V to 4 V
Input voltage, logic/analog signals . . . . . –0.5 V to 4 V
External DVI single-ended termination resistance, R_T . . . . . 0 Ω to open circuit
External TFADJ resistance, R_{TFADJ} . . . . . 300 Ω to open circuit
Storage temperature range‡, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 s . . . . . 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s . . . . . 260°C
ESD protection: DVI pins . . . . . 4 kV, Human-Body Model
All other pins . . . . . 2 kV, Human-Body Model
JEDEC latch up (EIA/JESD78) . . . . . 100 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

dissipation ratings

PACKAGE	AIR FLOW (cfm)	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
PAP	0	2.962 W	23.7 mW/°C	1.895 W	1.54 W	592 mW

NOTE: See Table 2 for the thermal properties of the 64-pin TQFP PowerPAD package.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (DV_{DD}, PV_{DD}, TV_{DD})		3	3.3	3.6	V
Input reference voltage, V_{REF}	Low-swing mode	0.55	$V_{DDQ}/2$§	0.9	V
	High-swing mode			DV_{DD}	
DVI termination supply voltage, AV_{DD} (see Note 1)	DVI receiver	3.14	3.3	3.46	V
DVI Single-ended termination resistance, R_T (see Note 2)	DVI receiver	45	50	55	Ω
TFADJ resistor for DVI-compliant $V_{(SWING)}$, $R_{(TFADJ)}$	400 mV = $V_{(SWING)}$ = 600 mV	505	510	515	Ω
Operating free-air temperature, T_A		–55	25	125	°C

§ V_{DDQ} defines the maximum low-level input voltage, it is not an actual input voltage.

NOTES: 1. AV_{DD} is the termination supply voltage of the DVI link.
2. R_T is the single-ended termination resistance at the receiver end of the DVI link.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

dc specifications

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Data, DE, VSYNC, HSYNC, and IDCK+/–	$V_{REF} = DV_{DD}$	0.7 V_{DD}			V
			0.5 V ≤ V_{REF} ≤ 0.95 V	V_{REF} + 0.2			
		Other inputs		0.7 V_{DD}			
V_{IL}	Low-level input voltage (CMOS input)	Data, DE, VSYNC, HSYNC, and IDCK+/–	$V_{REF} = DV_{DD}$			0.3 V_{DD}	V
			0.5 V ≤ V_{REF} ≤ 0.95 V			V_{REF} – 0.2	
		Other inputs				0.3V_{DD}	
V_{OH}	High-level digital output voltage (open-drain output)		V_{DD} = 3 V, I_{OH} = 20 μA	2.4			V
V_{OL}	Low-level digital output voltage (open-drain output)		V_{DD} = 3.6 V, I_{OL} = 4 mA			0.4	V
I_{IH}	High-level input current		V_I = 3.6 V			±50	μA
I_{IL}	Low-level input current		V_I = 0			±50	μA
V_H	DVI single-ended high-level output voltage		AV_{DD} = 3.3 V ± 5%, R_T† = 50 Ω ± 10%, R_{TFADJ} = 510 Ω ± 1%	AV_{DD} – 0.01		AV_{DD} + 0.01	V
V_L	DVI single-ended low-level output voltage		AV_{DD} = 3.3 V ± 5%, R_T† = 50 Ω ± 10%, R_{TFADJ} = 510 Ω ± 1%	AV_{DD} – 0.6		AV_{DD} – 0.4	V
V_{SWING}	DVI single-ended output swing voltage		AV_{DD} = 3.3 V ± 5%, R_T† = 50 Ω ± 10%, R_{TFADJ} = 510 Ω ± 1%	400		600	mV_{P-P}
V_{OFF}	DVI single-ended standby/off output voltage		AV_{DD} = 3.3 V ± 5%, R_T† = 50 Ω ± 10%, R_{TFADJ} = 510 Ω ± 1%	AV_{DD} – 0.01		AV_{DD} + 0.01	V
I_{PD}	Power-down current (see Note 1)				200	500	μA
I_{IDD}	Normal power-supply current		Worst-case pattern‡		200	250	mA

† R_T is the single-ended termination resistance at the receiver end of the DVI link.
‡ Black and white checkerboard pattern, each checker is one pixel wide.
NOTE 1: Assumes all inputs to the transmitter are not toggling.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) – (continued)

ac specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IDCK)}$	IDCK frequency			25		165	MHz
$t_{(pixel)}$	Pixel time period (see Note 1)			6.06		40	ns
$t_{(IDCK)}$	IDCK duty cycle			30%		70%	
$t_{(ijit)}$	IDCK clock jitter tolerance				2		ns
t_r	DVI output rise time (20-80%) (see Note 2)	$f_{(IDCK)}$ = 165 MHz	0°C to 70°C	75		240	ps
			–55°C to 125°C	45		320	
t_f	DVI output fall time (20-80%) (see Note 2)	$f_{(IDCK)}$ = 165 MHz	0°C to 70°C	75		240	ps
			–55°C to 125°C	45		320	
$t_{sk(D)}$	DVI output intra-pair + to – differential skew (see Note 3)	$f_{(IDCK)}$ = 165 MHz			50		ps
$t_{sk(CC)}$	DVI output inter-pair or channel-to-channel skew (see Note 3)	$f_{(IDCK)}$ = 165 MHz				1.2	ns
t_{ojit}	DVI output clock jitter, max. (see Note 4)	$f_{(IDCK)}$ = 165 MHz	0°C to 70°C			150	ps
			–55°C to 125°C			190	
$t_{su(IDF)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ falling edge	Single edge (BSE = 1, DSEL = 0, DKEN = 0, EDGE = 0)	IDCK = 165 MHz	1.5			ns
$t_{h(IDF)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ falling edge	Single edge (BSE = 1, DSEL = 0, DKEN = 0, EDGE = 0)	IDCK = 165 MHz	1.5			ns
$t_{su(IDR)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ rising edge	Single edge (BSEL = 1, DSEL = 0, DKEN = 0, EDGE = 1)	IDCK = 165 MHz	1.5			ns
$t_{h(IDR)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ rising edge	Single edge (BSEL = 1, DSEL = 0, DKEN = 0, EDGE = 1)	IDCK = 165 MHz	1.5			ns
$t_{su(ID)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ falling/rising edge	Dual edge (BSEL = 0, DSEL = 1, DKEN = 0)	IDCK = 165 MHz	0.9			ns
$t_{h(ID)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ falling/rising edge	Dual edge (BSEL = 0, DSEL = 1, DKEN = 0)	IDCK = 165 MHz	1			ns
$t_{(STEP)}$	De-skew trim increment	DKEN = 1	IDCK = 165 MHz		350		ps

NOTES: 1. $t_{(pixel)}$ is the pixel time defined as the period of the TXC output clock. The period of IDCK is equal to $t_{(pixel)}$.
2. Rise and fall times are measured as the time between 20% and 80% of signal amplitude.
3. Measured differentially at the 50% crossing point using the IDCK+ input clock as a trigger
4. Relative to input clock (IDCK)

timing diagrams

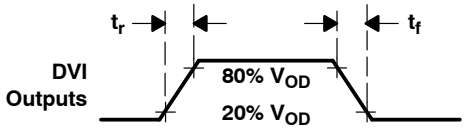


Figure 1. Rise and Fall Time for DVI Outputs

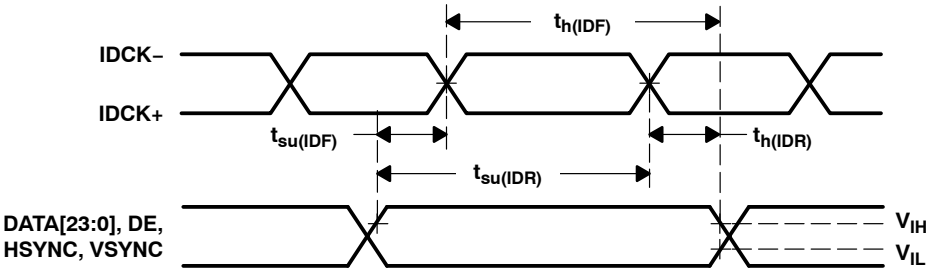


Figure 2. Control and Single-Edge-Data Setup/Hold Time to IDCK±

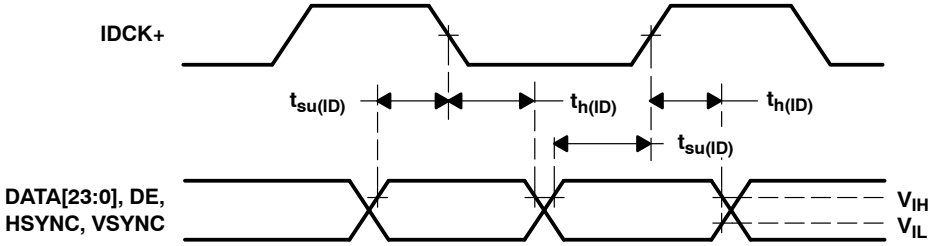


Figure 3. Dual-Edge Data Setup/Hold Times to IDCK+

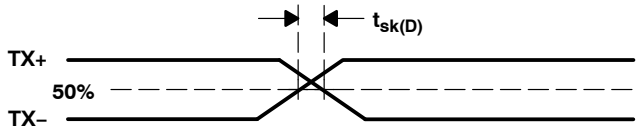


Figure 4. Analog Output Intra-Pair ± Differential Skew

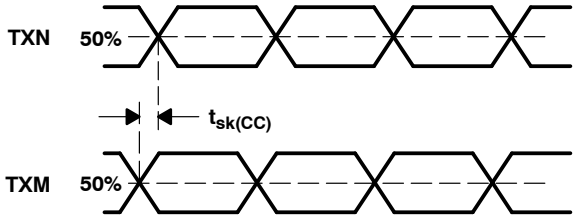


Figure 5. Analog Output Channel-to-Channel Skew

functional description

The TFP410 is a DVI-compliant digital transmitter that is used in digital host monitor systems to transition minimized differential signaling (TMDS) encode and serialize RGB pixel data streams. The TFP410 supports resolutions from VGA to WUXGA (and 1080p) and can be controlled in two ways: 1) configuration and state pins or 2) the programmable I^2C serial interface (see the t*erminal functions* section).

The host in a digital display system, usually a PC or consumer electronics device, contains a DVI-compatible transmitter, such as the TFP410, that receives 24-bit pixel data along with appropriate control signals. The TFP410 encodes the signals into a high-speed, low-voltage, differential serial bit stream optimized for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a DVI-compatible receiver like the TFP401 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat-panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred (see the *TMDS pixel data and control signal encoding, pixel data and control signal encoding, universal graphics contoller interface voltage signal levels,* and *universal graphics controller interface clock inputs* sections).

The TFP410 integrates a high-speed digital interface, a TMDS encoder, and three differential TMDS drivers. Data is driven to the TFP410 encoder across 12 or 24 data lines, along with differential clock pair and sync signals. The flexibility of the TFP410 allows for multiple clock and data formats that enhance system performance.

The TFP410 also has enhanced PLL noise immunity, an enhancement accomplished with on-chip regulators and bypass capacitors.

The TFP410 is versatile and highly programmable to provide maximum flexibility for the user. An I^2C host interface is provided to allow enhanced configurations in addition to power on default settings programmed by pin-strapping resistors.

The TFP410 offers monitor detection through receiver detection, or hot-plug detection when I^2C is enabled. The monitor detection feature allows the user enhanced flexibility when attaching to digital displays or receivers (see *terminal functions, hot plug/unplug,* and *register descriptions* sections).

The TFP410 has a data deskew feature allowing the users to deskew the input data with respect to the IDCK± (see the *data deskew feature* section).

transition minimized differential signaling (TMDS) pixel data and control signal encoding

For TMDS, only one of two possible TMDS characters for a given pixel is transmitted at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent and transmits the character that minimizes the number of transitions and approximates a dc balance of the transmission line. Three TMDS channels are used to transmit RGB pixel data during the active video interval (DE = High). These same three channels are also used to transmit HSYNC, VSYNC, and the control signals, CTL[2:1], during the inactive display or blanking interval (DE = Low). The following table maps the transmitted output data to the appropriate TMDS output channel in a DVI-compliant system.

INPUT PINS (VALID FOR DE = High)	TMDS OUTPUT CHANNEL	TRANSMITTED PIXEL DATA ACTIVE DISPLAY (DE = High)
DATA[23:16]	Channel 2 (TX2 ±)	Red[7:0]
DATA[15:8]	Channel 1 (TX1 ±)	Green[7:0]
DATA[7:0]	Channel 0 (TX0 ±)	Blue[7:0]
INPUT PINS (VALID FOR DE = Low)	**TMDS OUTPUT CHANNEL**	**TRANSMITTED CONTROL DATA BLANKING INTERVAL (DE = Low)**
CTL3, CTL2 (see Note 1)	Channel 2 (TX2 ±)	CTL[3:2]
CTL1 (See Note 1)	Channel 1 (TX1 ±)	CTL[1]
HSYNC, VSYNC	Channel 0 (TX0 ±)	HSYNC, VSYNC

NOTE 1: The TFP410 encodes and transfers the CTL[3:1] inputs during the vertical blanking interval. CTL3 is reserved for HDCP and is always encoded as 0. The CTL[2:1] inputs are reserved for future use. When DE = high, CTL and SYNC pins must be held constant.

universal graphics controller interface voltage signal levels

The universal graphics controller interface can operate in the following two distinct voltage modes:

- High-swing mode where standard 3.3-V CMOS signaling levels are used
- Low-swing mode where adjustable 1.1-V to 1.8-V signaling levels are used

To select the high-swing mode, the V_{REF} input pin must be tied to the 3.3-V power supply.
To select the low-swing mode, the V_{REF} must be 0.55 to 0.95 V.

In the low-swing mode, V_{REF} is used to set the midpoint of the adjustable signaling levels. The allowable range of values for V_{REF} is from 0.55 V to 0.9 V. The typical approach is to provide this from off chip by using a simple voltage-divider circuit. The minimum allowable input signal swing in the low-swing mode is $V_{REF} \pm 0.2$ V. In low-swing mode, the V_{REF} input is common to all differential input receivers.

universal graphics controller interface clock inputs

The universal graphics controller interface of the TFP410 supports both fully differential and single-ended clock input modes. In the differential clock input mode, the universal graphics controller interface uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data (DATA[23:0], DE, HSYNC, and VSYNC). Differential clock inputs provide greater common-mode noise rejection. The differential clock input mode is only available in the low-swing mode. In the single-ended clock input mode, the IDCK+ input (pin 57) should be connected to the single-ended clock source and the IDCK– input (pin 56) should be tied to GND.

The universal graphics controller interface of the TFP410 provides selectable 12-bit dual-edge and 24-bit single-edge input clocking modes. In the 12-bit dual-edge mode, the 12-bit data is latched on each edge of the input clock. In the 24-bit single-edge mode, the 24-bit data is latched on the rising edge of the input clock when EDGE = 1 and the falling edge of the input clock when EDGE = 0.

DKEN and DK[3:1] allow the user to compensate the skew between IDCK± and the pixel data and control signals. See the description of the CTL_3_MODE register for details.

universal graphics controller interface modes

Table 1 is a tabular representation of the different modes for the universal graphics controller interface. The 12-bit mode is selected when BSEL = 0 and the 24-bit mode when BSEL = 1. The 12-bit mode uses dual-edge clocking and the 24-bit mode uses single-edge clocking. The EDGE input is used to control the latching edge in 24-bit mode, or the primary latching edge in 12-bit mode. When EDGE = 1, the data input is latched on the rising edge of the input clock and when EDGE = 0, the data input is latched on the falling edge of the input clock. A fully differential input clock is available only in the low-swing mode. Single-ended clocking is not recommended in the low-swing mode as this decreases common-mode noise rejection.

Note that BSEL, DSEL, and EDGE are determined by register CTL_1_MODE when I^2C is enabled (ISEL = 1) and by input pins when I^2C is disabled (ISEL = 0).

Table 1. Universal Graphics Controller Interface Options (Tabular Representation)

V_{REF}	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK EDGE	CLOCK MODE
0.55 V to 0.9 V	0	0	0	12 bit	Dual edge	Falling	Differential (see Note 1 and Note 2)
0.55 V to 0.9 V	0	0	1	12 bit	Dual edge	Falling	Single ended
0.55 V to 0.9 V	0	1	0	12 bit	Dual edge	Rising	Differential (see Note 1 and Note 2)
0.55 V to 0.9 V	0	1	1	12 bit	Dual edge	Rising	Single ended
0.55 V to 0.9 V	1	0	0	24 bit	Single edge	Falling	Single ended
0.55 V to 0.9 V	1	0	1	24 bit	Single edge	Falling	Differential (see Note 1 and Note 3)
0.55 V to 0.9 V	1	1	0	24 bit	Single edge	Rising	Single ended
0.55 V to 0.9 V	1	1	1	24 bit	Single edge	Rising	Differential (see Note 1 and Note 3)
DV_{DD}	0	0	X	12 bit	Dual edge	Falling	Single ended (see Note 4)
DV_{DD}	0	1	X	12 bit	Dual edge	Rising	Single ended (see Note 4)
DV_{DD}	1	0	X	24 bit	Single edge	Falling	Single ended (see Note 4)
DV_{DD}	1	1	X	24 bit	Single edge	Rising	Single ended (see Note 4)

NOTES: 1. The differential clock input mode is only available in the low signal swing mode (i.e., $V_{REF} \leq 0.9$ V).
2. The TFP410 does not support a 12-bit dual-clock, single-edge input clocking mode.
3. The TFP410 does not support a 24-bit single-clock, dual-edge input clocking mode.
4. In the high-swing mode ($V_{REF} = DV_{DD}$), DSEL is a don't care; therefore, the device is always in the single-ended latch mode.

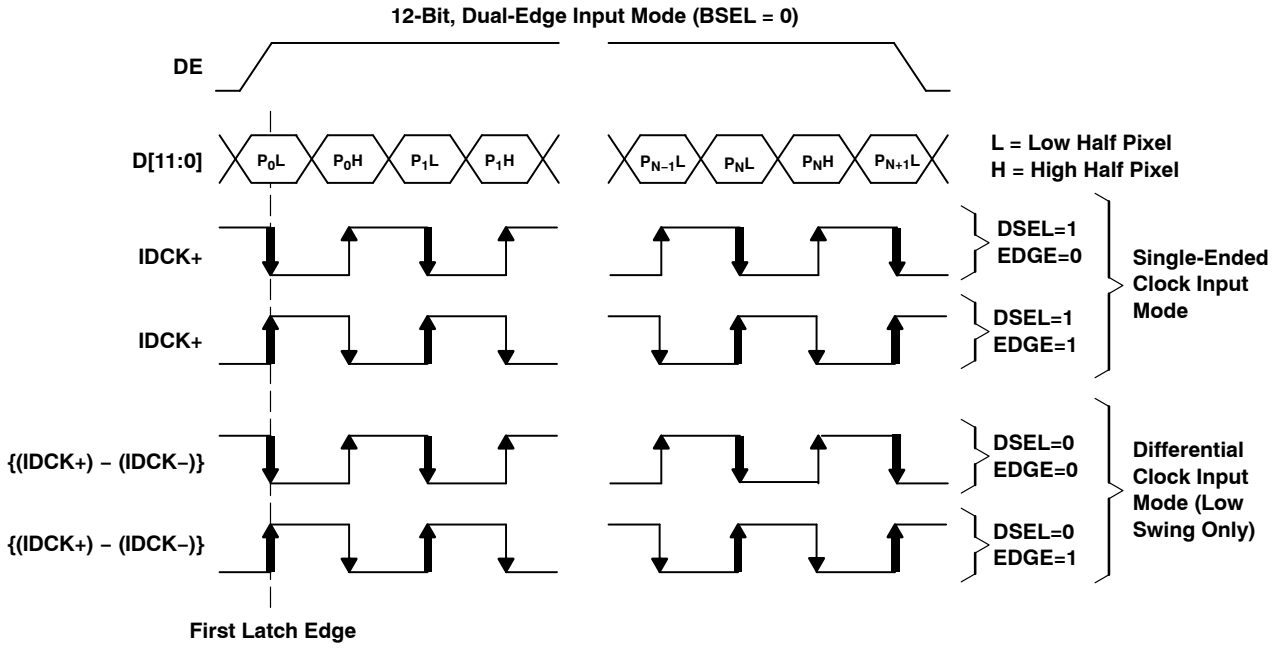


Figure 6. Universal Graphics Controller Interface Options for 12-Bit Mode (Graphical Representation)

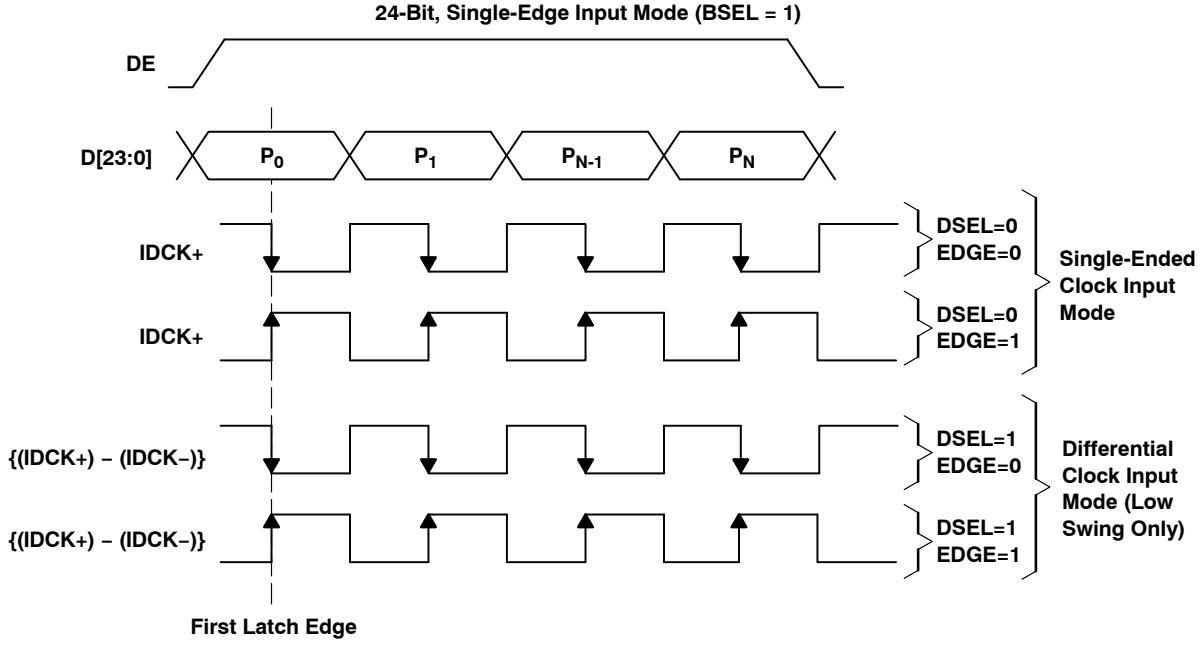


Figure 7. Universal Graphics Controller Interface Options for 24-Bit Mode (Graphical Representation)

12-bit mode data mapping

PIN NAME	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
	LOW	HIGH	LOW	HIGH	LOW	HIGH
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

24-bit mode data mapping

PIN NAME	P0	P1	P2	PIN NAME	P0	P1	P2
D23	R0[7]	R1[7]	R2[7]	D11	G0[3]	G1[3]	G2[3]
D22	R0[6]	R1[6]	R2[6]	D10	G0[2]	G1[2]	G2[2]
D21	R0[5]	R1[5]	R2[5]	D9	G0[1]	G1[1]	G2[1]
D20	R0[4]	R1[4]	R2[4]	D8	G0[0]	G1[0]	G2[0]
D19	R0[3]	R1[3]	R2[3]	D7	B0[7]	B1[7]	B2[7]
D18	R0[2]	R1[2]	R2[2]	D6	B0[6]	B1[6]	B2[6]
D17	R0[1]	R1[1]	R2[1]	D5	B0[5]	B1[5]	B2[5]
D16	R0[0]	R1[0]	R2[0]	D4	B0[4]	B1[4]	B2[4]
D15	G0[7]	G1[7]	G2[7]	D3	B0[3]	B1[3]	B2[3]
D14	G0[6]	G1[6]	G2[6]	D2	B0[2]	B1[2]	B2[2]
D13	G0[5]	G1[5]	G2[5]	D1	B0[1]	B1[1]	B2[1]
D12	G0[4]	G1[4]	G2[4]	D0	B0[0]	B1[0]	B2[0]

data deskew feature

The deskew feature allows adjustment of the input setup/hold time. Specifically, the input data DATA[23:0] can be latched slightly before or after the latching edge of the clock IDCK± depending on the amount of deskew desired. When deskew enable (DKEN) is enabled, the amount of deskew is programmable by setting the three bits DK[3:1]. When disabled, a default deskew setting is used. To allow maximum flexibility and ease of use, DKEN and DK[3:1] are accessed directly through configuration pins when I^2C is disabled, or through registers of the same name when I^2C is enabled. When using I^2C mode, DKEN should be tied to ground to avoid a floating input.

The input setup/hold time can be varied with respect to the input clock by an amount $t_{(CD)}$ given by the formula:

$$t_{(CD)} = (DK[3:1] - 4) \times t_{(STEP)}$$

Where:

$t_{(STEP)}$ = Adjustment increment amount
DK[3:1] = Number from 0 to 7 represented as a 3-bit binary number
$t_{(CD)}$ = Cumulative deskew amount

(DK[3:1] − 4) is simply a multiplier in the range {–4, –3, –2, –1, 0, 1, 2, 3} for $t_{(STEP)}$. Therefore, data can be latched in increments from four times the value of $t_{(STEP)}$ before the latching edge of the clock to three times the value of $t_{(STEP)}$ after the latching edge. Note that the input clock is not changed, only the time when data is latched with respect to the clock.

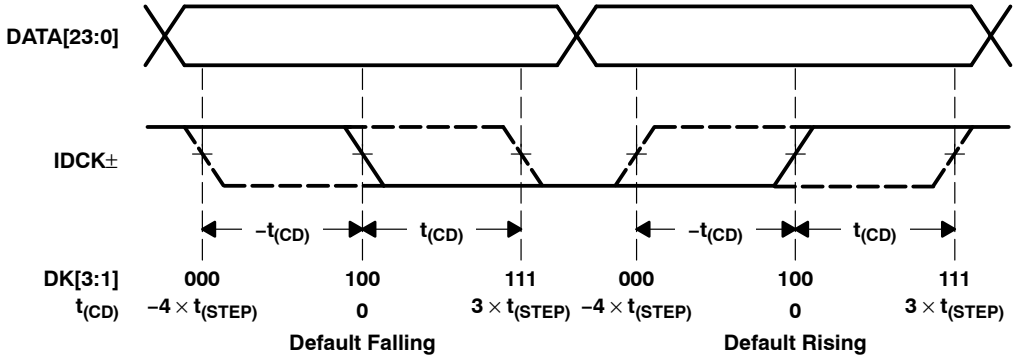


Figure 8. A Graphical Representation of the De-Skew Function

hot plug/unplug (auto connect/disconnect detection)

The TFP410 supports hot plug/unplug (auto connect/disconnect detection) for the DVI link. The receiver sense (RSEN) input bit indicates if a DVI receiver is connected to TXC+ and TXC–. The HTPLG bit reflects the current state of the HTPLG pin connected to the monitor via the DVI connector. When I^2C is disabled (ISEL = 0), the RSEN value is available on the MSEN pin. When I^2C is enabled, the connection status of the DVI link and HTPLG sense pins are provided by the CTL_2_MODE register. The MSEL bits of the CTL_2_MODE register can be used to program the MSEN to output the HTPLG value, the RSEN value, an interrupt, or be disabled.

The source of the interrupt event is selected by TSEL in the CTL_2_MODE register. An interrupt is generated by a change in status of the selected signal. The interrupt status is indicated in the MDI bit of CTL_2_MODE and can be output via the MSEN pin. The interrupt continues to be asserted until a 1 is written to the MDI bit, resetting the bit back to 0. Writing 0 to the MDI bit has no effect.

device configuration and I²C reset description

The TFP410 device configuration can be programmed by several different methods to allow maximum flexibility for the user's application. Device configuration is controlled depending on the state of the ISEL/$\overline{\text{RST}}$ pin, configuration pins (BSEL, DSEL, EDGE, V_{REF}), and state pins ($\overline{\text{PD}}$, DKEN). I²C bus select and I²C reset (active low) are shared functions on the ISEL/$\overline{\text{RST}}$ pin, which operates asynchronously.

Holding ISEL/$\overline{\text{RST}}$ low causes the device configuration to be set by the configuration pins (BSEL, DSEL, EDGE, and V_{REF}) and state pins ($\overline{\text{PD}}$, DKEN). The I²C bus is disabled.

Holding ISEL/$\overline{\text{RST}}$ high causes the chip configuration to be set based on the configuration bits (BSEL, DSEL, EDGE) and state bits ($\overline{\text{PD}}$, DKEN) in the I²C registers. The I²C bus is enabled.

Momentarily bringing ISEL/$\overline{\text{RST}}$ low and then back high while the device is operating in normal or power-down mode resets the I²C registers to their default values. The device configuration is changed to the default power-up state with I²C enabled. After power up, the device must be reset. It is suggested that this pin be tied to the system reset signal, which is low during power up and is then asserted high after all the power supplies are fully functional.

DE generator

The TFP410 contains a DE generator that can be used to generate an internal DE signal when the original data source does not provide one. There are several I²C programmable values that control the DE generator (see Figure 9). DE_GEN in the DE_CTL register enables this function. When enabled, the DE pin is ignored.

DE_TOP and DE_LIN are line counts used to control the number of lines after VSYNC goes active that DE is enabled and the total number of lines that DE remains active, respectively. The polarity of VSYNC must be set by VS_POL in the DE_CTL register.

DE_DLY and DE_CNT are pixel counts used to control the number of pixels after HSYNC goes active that DE is enabled and the total number of pixels that DE remains active, respectively. The polarity of HSYNC must be set by HS_POL in the DE_CTL register.

The TFP410 also counts the total number of HSYNC pulses between VSYNC pulses and the total number of pixels between HSYNC pulses. These values, the total vertical and horizontal resolutions, are available in V_RES and H_RES, respectively. These values are available at all times, whether or not the DE generator is enabled.

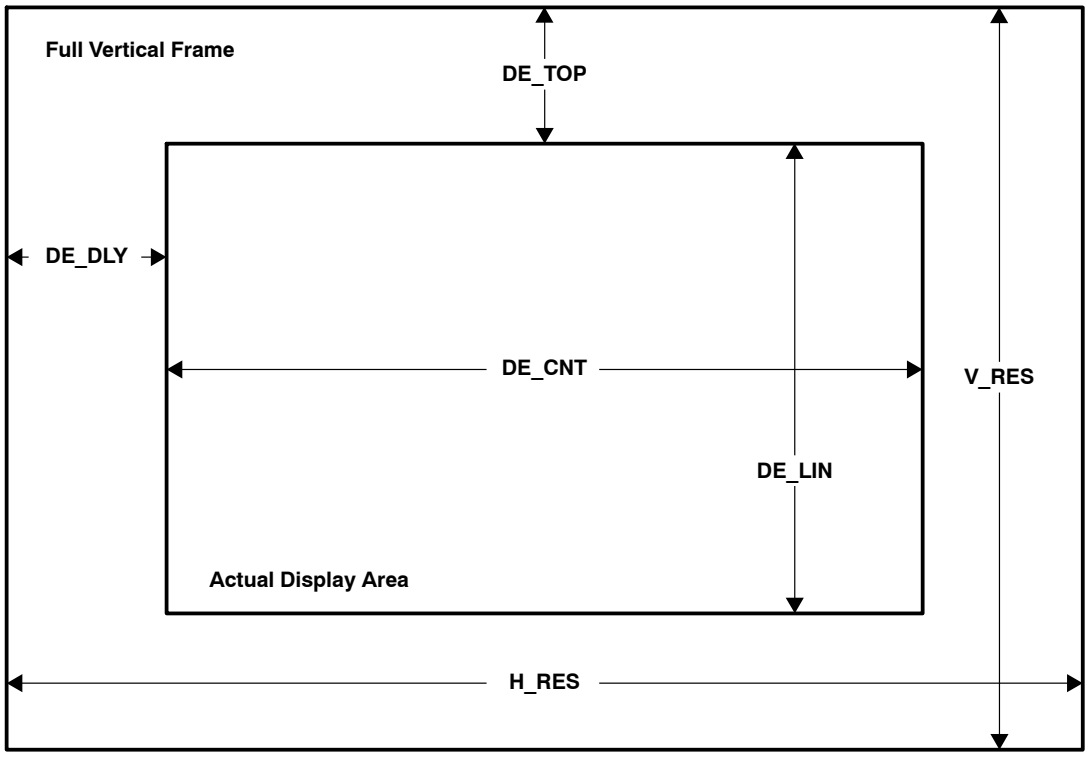


Figure 9. DE Generator Register Functions

register map

The TFP410 is a standard I^2C slave device. All the registers can be written and read through the I^2C interface (unless otherwise specified). The TFP410 slave machine supports only byte read and write cycles. Page mode is not supported. The 8-bit binary address of the I^2C machine is 0111 $A_3A_2A_1X$, where A[3:1] are pin programmable or set to 000 by default. The I^2C base address of the TFP410 is dependent on A[3:1] (pins 6, 7, and 8 respectively) as shown:

A[3:1]	WRITE ADDRESS (Hex)	READ ADDRESS (Hex)
000	70	71
001	72	73
010	74	75
011	76	77
100	78	79
101	7A	7B
110	7C	7D
111	7E	7F

register map (continued)

REGISTER	RW	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VEN_ID	R	00	VEN_ID[7:0]							
	R	01	VEN_ID[15:8]							
DEV_ID	R	02	DEV_ID[7:0]							
	R	03	DEV_ID[15:8]							
REV_ID	R	04	REV_ID[7:0]							
RESERVED	R	05-07	Reserved							
CTL_1_MODE	RW	08	RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{PD}$
CTL_2_MODE	RW	09	VLOW	MSEL			TSEL	RSEN	HTPLG	MDI
CTL_3_MODE	RW	0A	DK			DKEN	CTL			RSVD
CFG	R	0B	CFG							
RESERVED	RW	0C-31	Reserved							
DE_DLY	RW	32	DE_DLY[7:0]							
DE_CTL	RW	33	RSVD	DE_GEN	VS_POL	HS_POL	RSVD			DE_DLY[8]
DE_TOP	RW	34	RSVD	DE_DLY[6:0]						
RESERVED	RW	35	Reserved							
DE_CNT	RW	36	DE_CNT[7:0]							
	RW	37	Reserved					DE_CNT[10:8]		
DE_LIN	RW	38	DE_LIN[7:0]							
	RW	39	Reserved					DE_LIN[10:8]		
H_RES	R	3A	H_RES[7:0]							
	R	3B	Reserved					H_RES[10:8]		
V_RES	R	3C	V_RES[7:0]							
	R	3D	Reserved					V_RES[10:8]		
RESERVED	R	3E–FF								

register descriptions

VEN_ID **Sub-Address = 01–00** **Read Only** **Default = 0x014C**

7	6	5	4	3	2	1	0
VEN_ID[7:0]							
VEN_ID[15:8]							

These read-only registers contain the 16-bit TI vendor ID. VEN_ID is hardwired to 0x014C.

DEV_ID **Sub-Address = 03–02** **Read Only** **Default = 0x0410**

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
DEV_ID[15:8]							

These read-only registers contain the 16-bit device ID for the TFP410. DEV_ID is hardwired to 0x0410.

REV_ID **Sub-Address = 04** **Read Only** **Default = 0x00**

7	6	5	4	3	2	1	0
REV_ID[7:0]							

This read-only register contains the revision ID.

register descriptions (continued)

RESERVED	Sub-Address = 07–05	Read Only	Default = 0x641400

7	6	5	4	3	2	1	0
RESERVED[7:0]							
RESERVED[7:0]							
RESERVED[15:8]							

CTL_1_MODE	Sub-Address = 08	Read/Write	Default = 0xBE

7	6	5	4	3	2	1	0
RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{PD}$

$\overline{PD}$: This read/write register contains the power-down mode.

0: Power down (default after RESET)
1: Normal operation

EDGE: This read/write register contains the edge select mode.

0: Input data latches to the falling edge of IDCK+
1: Input data latches to the rising edge of IDCK+

BSEL: This read/write register contains the input bus select mode.

0: 12-bit operation with dual-edge clock
1: 24-bit operation with single-edge clock

DSEL: This read/write register is used in combination with BSEL and V_{REF} to select the single-ended or differential input clock mode. In the high-swing mode, DSEL is a don't care since IDCK is always single-ended.

HEN: This read/write register contains the horizontal sync enable mode.

0: HSYNC input is transmitted as a fixed low.
1: HSYNC input is transmitted in its original state.

VEN: This read/write register contains the vertical sync enable mode.

0: VSYNC input is transmitted as a fixed low.
1: VSYNC input is transmitted in its original state.

TDIS: This read/write register contains the TMDS disable mode.

0: TMDS circuitry enable state is determined by $\overline{PD}$.
1: TMDS circuitry is disabled.

CTL_2_MODE	Sub-Address = 09	Read/Write	Default = 0x00

7	6	5	4	3	2	1	0
VLOW	MSEL[3:1]			TSEL	RSEN	HTPLG	MDI

MDI: This read/write register contains the monitor detect interrupt mode.

0: Detected logic level change in detection signal (to clear, write one to this bit)
1: Logic level remains the same.

register descriptions (continued)

HTPLG: This read only register contains the hot-plug detection input logic state.

0: Logic level detected on EDGE/HTPLG (pin 9)
1: High level detected on EDGE/HTPLG (pin 9)

RSEN: This read-only register contains the receiver sense input logic state, which is valid only for dc-coupled systems.

0: A powered-on receiver is not detected.
1: A powered-on receiver is detected (i.e., connected to the DVI transmitter outputs).

TSEL: This read/write register contains the interrupt generation source select.

0: Interrupt bit (MDI) is generated by monitoring RSEN.
1: Interrupt bit (MDI) is generated by monitoring HTPLG.

MSEL: This read/write register contains the source select of the monitor sense output pin.

000: Disabled. MSEN output high.
001: Outputs the MDI bit (interrupt)
010: Outputs the RSEN bit (receiver detect)
011: Outputs the HTPLG bit (hot-plug detect)

VLOW: This read-only register indicates the V_{REF} input level.

0: This bit is a logic level 0 if the V_{REF} analog input selects high-swing inputs.
1: This bit is a logic level 1 if the V_{REF} analog input selects low-swing inputs.

CTL_3_MODE **Sub-Address = 0A** **Read/Write** **Default = 0x80**

7	6	5	4	3	2	1	0
DK[3:1]			DKEN	RSVD	CTL[2:1]		RSVD

CTL[2:1]: This read/write register contains the values of the two CTL[2:1] bits that are output on the DVI port during the blanking interval.

DKEN: This read/write register controls the data deskew enable.

0: Data deskew is disabled, the values in DK[3:1] are not used.
1: Data deskew is enabled, the deskew setting is controlled through DK[3:1].

DK[3:1]: This read/write register contains the deskew setting, each increment adjusts the skew by $t_{(STEP)}$.

000: Step 1 (minimum setup/maximum hold)
001: Step 2
010: Step 3
011: Step 4
100: Step 5 (default)
101: Step 6
110: Step 7
111: Step 8 (maximum setup/minimum hold)

register descriptions (continued)

CFG	Sub-Address = 0B				Read Only		
7	6	5	4	3	2	1	0
CFG[7:0] (D[23:16])							

This read-only register contains the state of the inputs D[23:16]. These pins can be used to provide the user with selectable configuration data through the I^2C bus.

RESERVED	Sub-Address = 0E–0C				Read/Write		Default = 0x97D0A9
7	6	5	4	3	2	1	0
RESERVED							
RESERVED							
RESERVED							

These read/write registers have no effect on TFP410 operation.

DE_DLY	Sub-Address = 32				Read/Write		Default = 0x00
7	6	5	4	3	2	1	0
DE_DLY[7:0]							

This read/write register defines the number of pixels after HSYNC goes active when the DE is generated and when the DE generator is enabled. The value must be less than or equal to (2047 – DE_CNT).

DE_CTL	Sub-Address = 33				Read/Write		Default = 0x00
7	6	5	4	3	2	1	0
Reserved	DE_GEN	VS_POL	HS_POL	Reserved			DE_DLY[8]

DE_DLY[8]: This read/write register contains the top bit of DE_DLY.

HS_POL: This read/write register sets the HSYNC polarity.

0: HSYNC is considered active low.
1: HSYNC is considered active high.
Pixel counts are reset on the HSYNC active edge.

VS_POL: This read/write register sets the VSYNC polarity.

0: VSYNC is considered active low.
1: VSYNC is considered active high.
Line counts are reset on the VSYNC active edge.

DE_GEN: This read/write register enables the internal DE generator.

0: DE generator is disabled. Signal required on DE pin.
1: DE generator is enabled. DE pin is ignored.

DE_TOP	Sub-Address = 34				Read/Write		Default = 0x00
7	6	5	4	3	2	1	0
DE_TOP[7:0]							

This read/write register defines the number of pixels after VSYNC goes active when the DE is generated and when the DE generator is enabled.

register descriptions (continued)

DE_CNT	Sub-Address = 37–36				Read/Write		Default = 0x0000
7	6	5	4	3	2	1	0
DE_CNT[7:0]							
Reserved					DE_CNT[10:8]		

These read/write registers define the width of the active display, in pixels, when the DE generator is enabled. The value must be less than or equal to (2047 – DE_DLY).

DE_LIN	Sub-Address = 39–38				Read/Write		Default = 0x0000
7	6	5	4	3	2	1	0
DE_LIN[7:0]							
Reserved					DE_LIN[10:8]		

These read/write registers define the height of the active display, in lines, when the DE generator is enabled.

H_RES	Sub-Address = 3B–3A				Read Only		
7	6	5	4	3	2	1	0
H_RES[7:0]							
Reserved					H_RES[10:8]		

These read-only registers return the number of pixels between consecutive HSYNC pulses.

V_RES	Sub-Address = 3D–3C				Read Only		
7	6	5	4	3	2	1	0
V_RES[7:0]							
Reserved					V_RES[10:8]		

These read-only registers return the number of lines between consecutive VSYNC pulses.

I^2C interface

The I^2C interface is used to access the internal TFP410 registers. This 2-pin interface consists of the SCL clock line and the SDA serial data line. The basic I^2C access cycles are shown in Figure 10 and Figure 11.

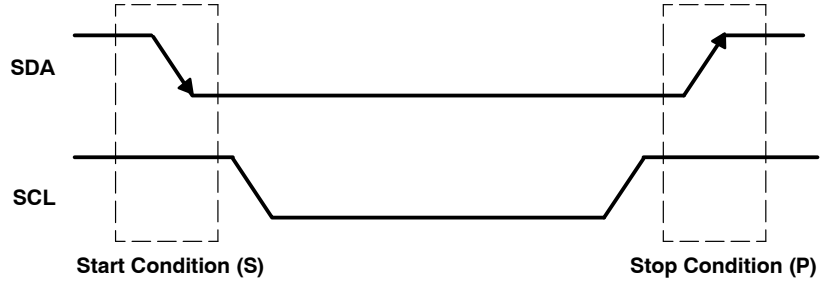


Figure 10. I^2C Start and Stop Conditions

I²C interface (continued)

The basic access write cycle consists of:

- Start condition
- Slave address cycle
- Sub-address cycle
- Any number of data cycles
- Stop condition

The basic access read cycle consists of:

- Start condition
- Slave write address cycle
- Sub-address cycle
- Restart condition
- Slave read address cycle
- Any number of data cycles
- Stop condition

The start and stop conditions are shown in Figure 10. The high-to-low transition of SDA while SCL is high defines the start condition. The low-to-high transition of SDA while SCL is high defines the stop condition. Each cycle, data or address, consists of eight bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains nine bits (see Figure 11).

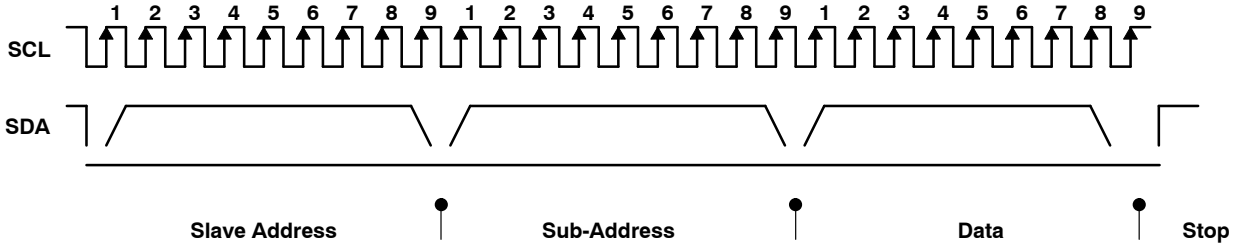


Figure 11. I²C Access Cycles

Following a start condition, each I²C device decodes the slave address. The TFP410 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent sub-address and data cycles, the TFP410 responds with acknowledge (see Figure 12). The sub-address is auto-incremented after each data cycle.

The transmitting device must not drive the SDA signal during the acknowledge cycle so that the receiving device may drive the SDA signal low. The master indicates a not acknowledge condition (/A) by keeping the SDA signal high just before it asserts the stop condition (P). This sequence terminates a read cycle (see Figure 13).

The slave address consists of seven bits of address along with one bit of read/write information (read = 1, write = 0) (see Figure 11 and Figure 12). For the TFP410, the selectable slave addresses (including the R/W bit) using A[3:1] are 0x70, 0x72, 0x74, 0x76, 0x78, 0x7A, 0x7C, and 0x7E for write cycles, and 0x71, 0x73, 0x75, 0x77, 0x79, 0x7B, 0x7D, and 0x7F for read cycles.

S	Slave Address	W	A	Sub-Address	A	Data	A	Data	A	P

Where:

From Master
From Slave

A Acknowledge
S Start condition
P Stop Condition

Figure 12. I²C Write Cycle

S	Slave Address	W	A	Sub-Address	A	Sr	Slave Address	R	A	Data	A	Data	/A	P

Where:

From Master
From Slave

A Acknowledge
S Start condition

/A Not acknowledge (SDA high)
R Read Condition = 1
W Write Condition = 0

P Stop Condition
Sr Restart Condition

Figure 13. I²C Read Cycle

PowerPAD™ 64-pin TQFP package

The TFP410 is available in TI's thermally-enhanced 64-pin TQFP PowerPAD package. The PowerPAD package is a 10-mm × 10-mm × 1-mm TQFP outline with 0,5-mm lead pitch. The PowerPAD package has a specially designed die-mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The PowerPAD package also offers a backside solder plane that connects directly to the die-mount pad for enhanced thermal conduction. For thermal considerations, soldering the back side of the TFP410 to the application board is not required, as the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the back-side pad, they should be protected by suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed back-side pad.

Soldering the back side of the device to a thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD package using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5,9 mm minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low-impedance connection to the ground plane. Vias in the exposed pad should be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.

PowerPAD™ 64-pin TQFP package (continued)

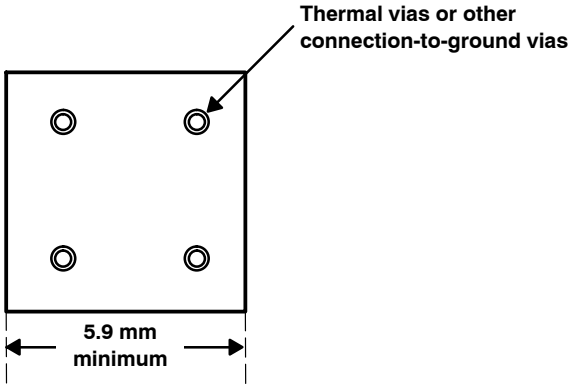


Figure 14. Recommended Pad Size

More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application report *PowerPAD ™ Thermally-Enhanced Package*, TI literature number SLMA002, available at www.ti.com.

Table 2 shows the thermal properties of the 64-pin TQFP PowerPAD package. The 64-pin TQFP non-PowerPAD package is included only for reference.

Table 2. 64-Pin TQFP (10 mm × 10 mm × 1 mm)/0,5-mm Lead Pitch

PARAMETER		WITHOUT PowerPAD	PowerPAD NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD CONNECTED TO PCB THERMAL PLANE (see Note 1)
$R_{\theta JA}$	Thermal resistance, junction to ambient (see Note 1 and Note 2)	75.83°C/W	42.2°C/W	21.47°C/W
$R_{\theta JC}$	Thermal resistance, junction to case (see Note 1 and Note 2)	7.8°/W	0.38°C/W	0.38°C/W
P_D	Power-handling capabilities of package (see Note 1, Note 2, and Note 3)	0.92 W	1.66 W	3.26 W

NOTES: 1. Specified with the PowerPAD bond pad on the back side of the package soldered to a 2-oz Cu plate PCB thermal plane
2. Airflow is at 0 LFM (no airflow).
3. Specified at 150°C junction temperature and 80°C ambient temperature

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TFP410MPAPREP	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TFP410MEP
TFP410MPAPREP.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TFP410MEP
TFP410MPAPREPG4	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TFP410MEP
V62/06653-01XE	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TFP410MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TFP410-EP :

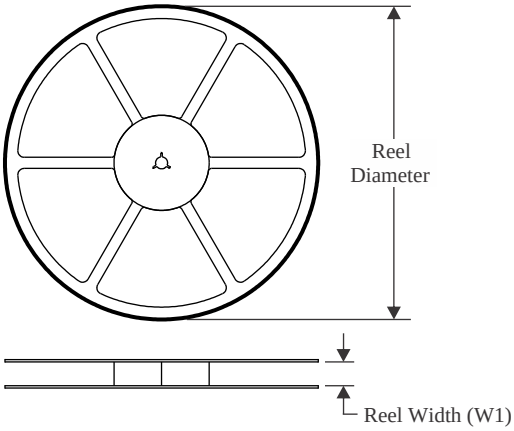
- Catalog : TFP410

NOTE: Qualified Version Definitions:

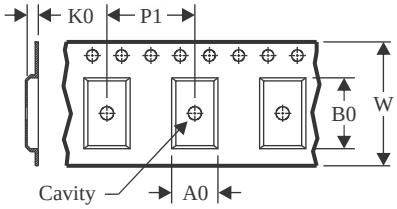
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

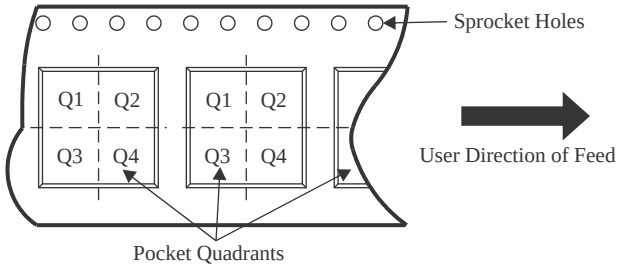


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

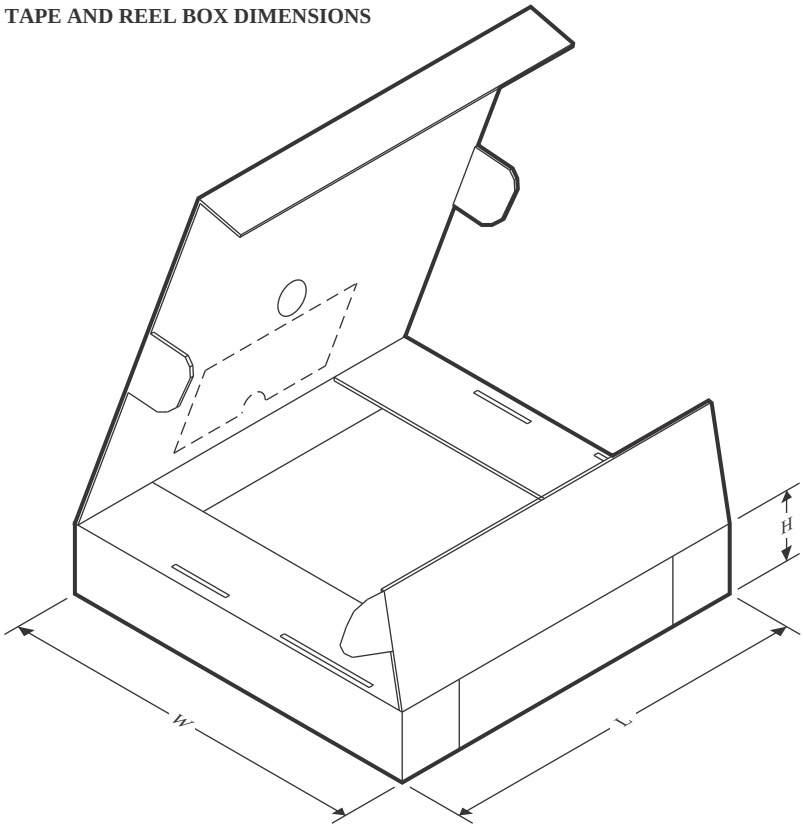
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TFP410MPAPREP	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TFP410MPAPREP	HTQFP	PAP	64	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

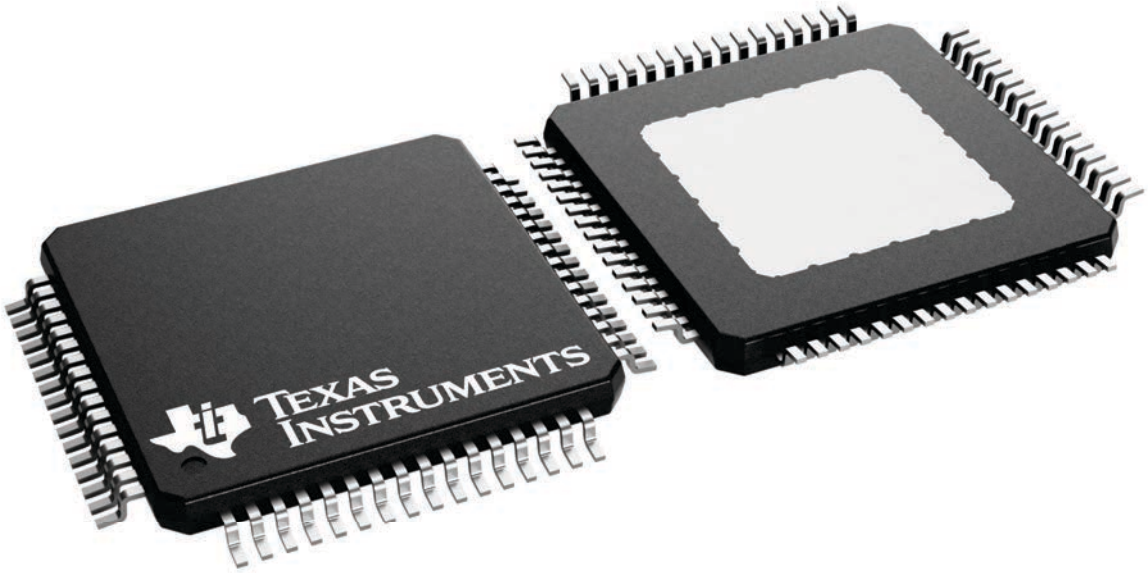
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

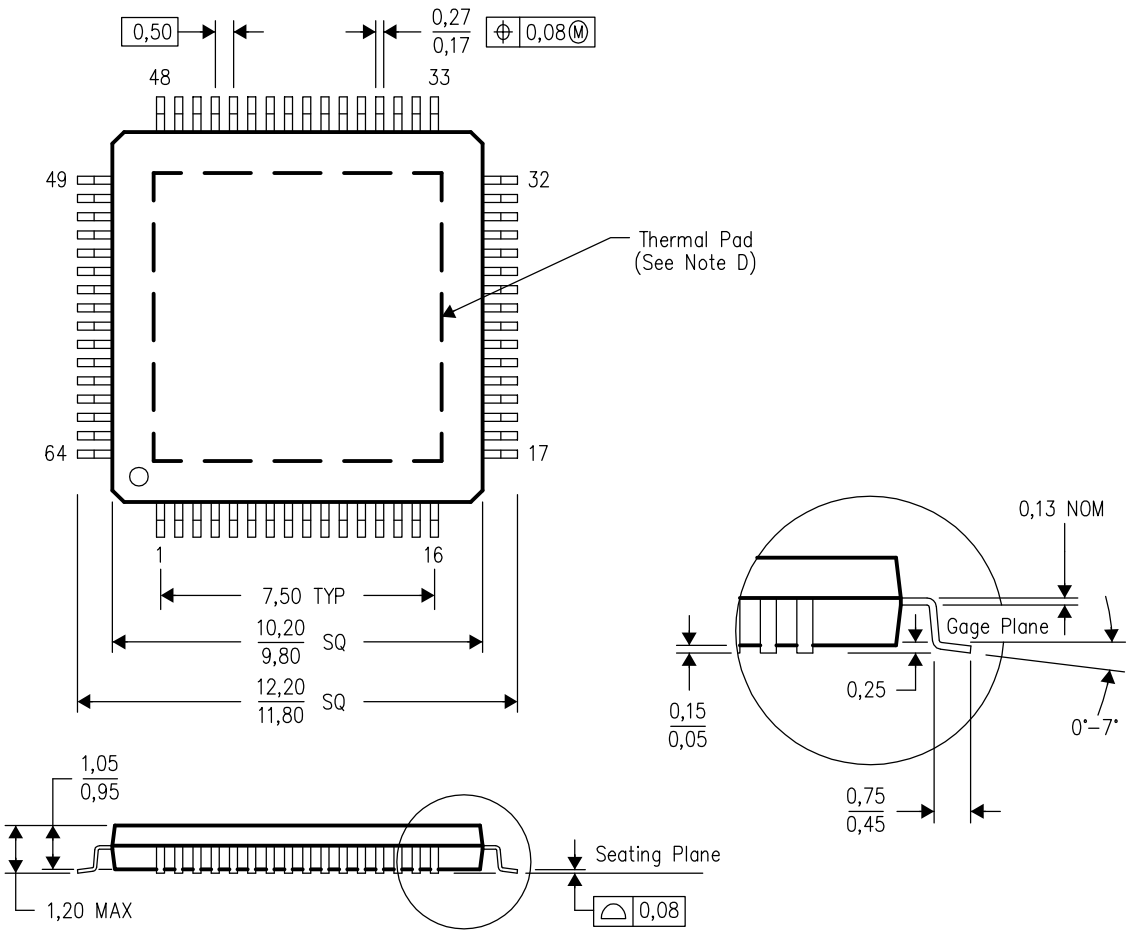
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

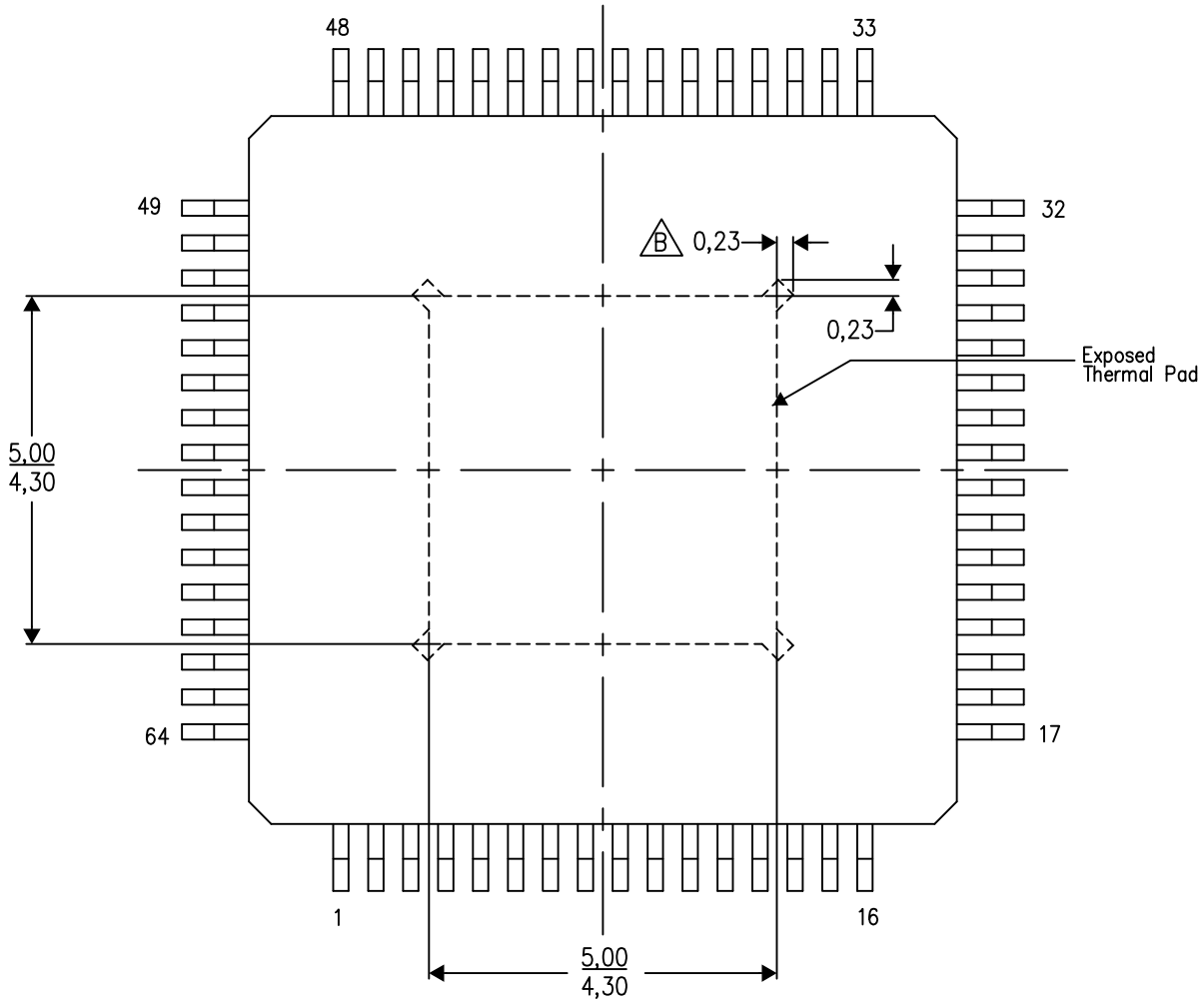
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

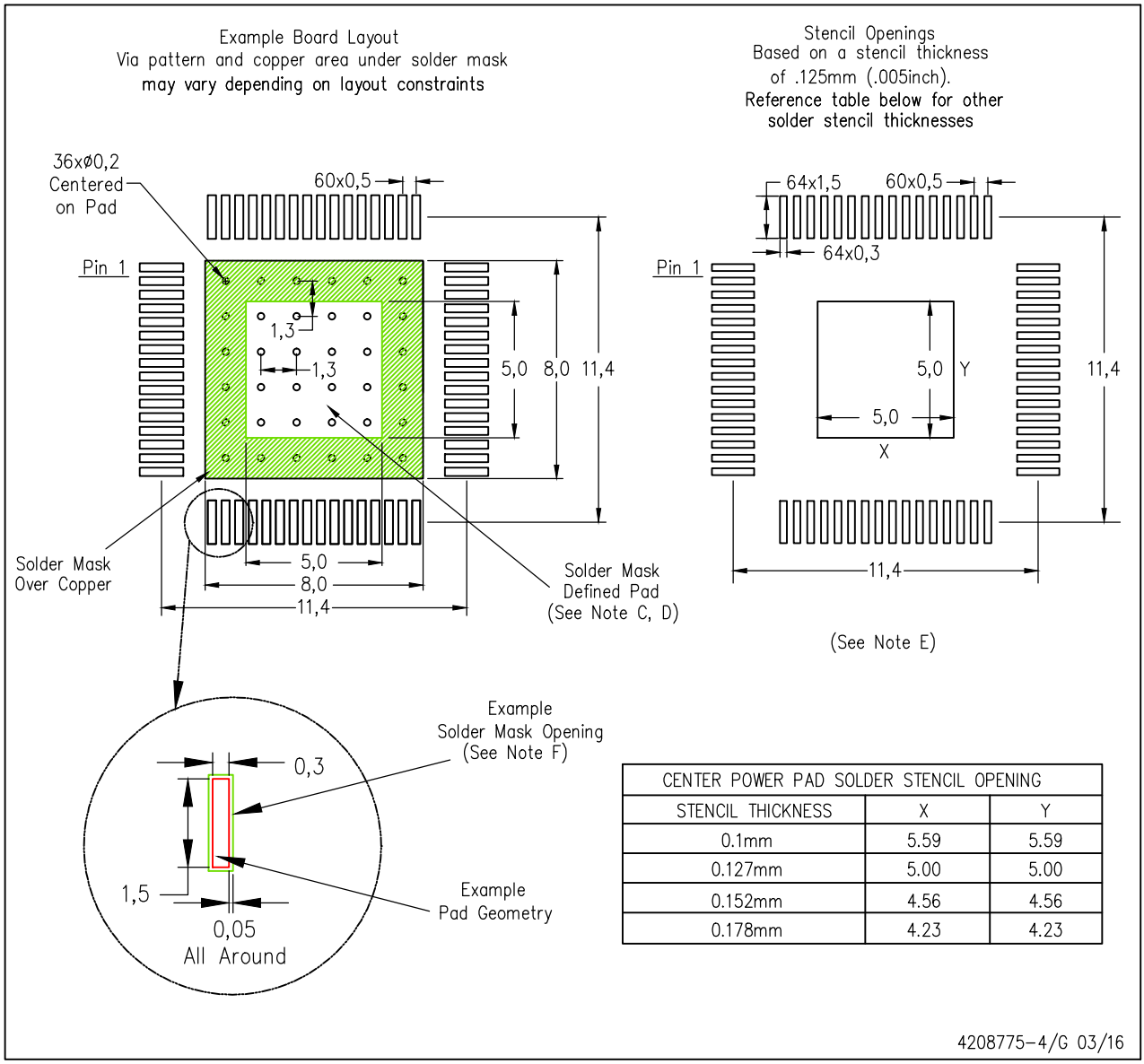
4206326–3/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	5.59	5.59
0.127mm	5.00	5.00
0.152mm	4.56	4.56
0.178mm	4.23	4.23

4208775–4/G 03/16

PowerPAD is a trademark of Texas Instruments

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Last updated 10/2025