6-Channel Video Amplifier with 3 SD and 3 Full-HD Filters with 6-dB Gain

Check for Samples: THS7364

FEATURES

- **Three SDTV Video Amplifiers for CVBS, S-Video, Y'/P'$_B$/P'$_R$, 480i/576i, Y'U'V', or G'B'R'**
- **Three Full-HD Selectable Filters for Y'/P'$_B$/P'$_R$, G'B'R', or Computer RGB**
- **Bypassable Sixth-Order Low-Pass Filters:**
  - **Fixed SD Channels: 9.5-MHz**
  - **Fixed Full-HD Channels: 72-MHz**
- **Versatile Input Biasing:**
  - **DC-Coupled with 300-mV Output Shift**
  - **AC-Coupled with Sync-Tip Clamp or Bias**
- **Built-in 6-dB Gain (2 V/V)**
- **+2.7-V to +5-V Single-Supply Operation**
- **Rail-to-Rail Output:**
  - **Output Swings within 100 mV from the Rails: Allows AC or DC Output Coupling**
  - **Supports Driving Two Video Lines/Channel**
- **Low Total Quiescent Current: 23.4 mA at 3.3 V**
- **Disabled Supply Current Function: 0.1 μA**
- **Low Differential Gain/Phase: 0.25%/0.4°**

APPLICATIONS

- **Set Top Box Output Video Buffering**
- **PVR/DVDR Output Buffering**
- **BluRay™ Output Video Buffer**

DESCRIPTION

Fabricated using the revolutionary, complementary Silicon-Germanium (SiGe) BiCom3X process, the THS7364 is a low-power, single-supply, 2.7-V to 5-V, six-channel integrated video buffer. It incorporates three SDTV filters and three Full-HD (also known as True-HD) HDTV filters. All filters feature bypassable sixth-order Butterworth characteristics that are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) anti-aliasing filters.

The THS7364 has flexible input coupling capabilities, and can be configured for either ac- or dc-coupled inputs. The 300-mV output level shift allows for a full sync dynamic range at the output with 0-V input. AC-coupled modes include a transparent sync-tip clamp for CVBS, Y', and G'B'R' signals. AC-coupled biasing for C'/P'$_B$/P'$_R$ channels can easily be achieved by adding an external resistor to V_{S+}.

The THS7364 is an ideal choice for a wide range of video buffer applications. Its rail-to-rail output stage with 6-dB gain allows for both ac and dc line driving. The ability to drive two lines, or 75-Ω loads, allows for maximum flexibility as a video line driver. The 23.4-mA total quiescent current at 3.3 V and 0.1 μA (disabled mode) makes it well-suited for systems that must meet power-sensitive Energy Star® standards.

The THS7364 is available in a TSSOP-20 package that is lead-free and green (RoHS-compliant).

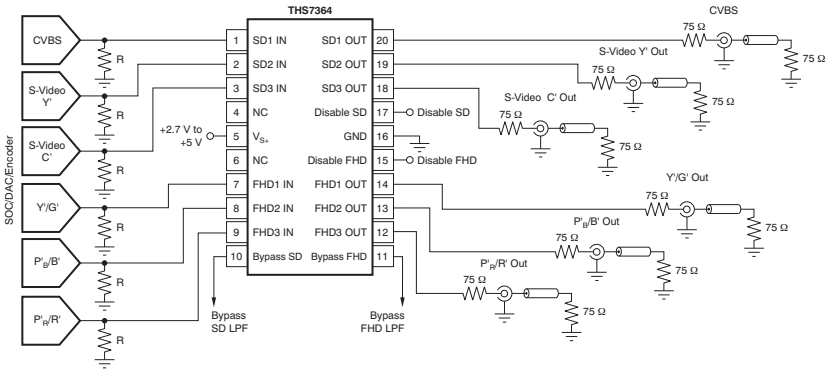


Figure 1. Single-Supply, DC-Input/DC-Output Coupled Video Line Driver

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)(2)

PRODUCT	PACKAGE-LEAD	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
THS7364IPW	TSSOP-20	Rails, 70	Pb-Free, Green
THS7364IPWR		Tape and Reel, 2000	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at ti.com.
(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS7364		UNIT
		MIN	MAX	
Supply voltage, V_{S+} to GND			5.5	V
Input voltage, V_I		–0.4	V_{S+}	V
Output current, I_O			±90	mA
Maximum junction temperature, any condition(2), T_J			+150	°C
Maximum junction temperature, continuous operation, long-term reliability(3), T_J			+125	°C
Storage temperature range, T_{STG}		–60	+150	°C
ESD rating:	Human body model (HBM)		4000	V
	Charge device model (CDM)		1000	V
	Machine model (MM)		200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

THERMAL INFORMATION

THERMAL METRIC(1)		THS7364 PW 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	108.0	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	41.6	
θ_{JB}	Junction-to-board thermal resistance	61.3	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	58.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	2.7		5	V
Ambient temperature, T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7364			UNITS	TEST LEVEL(1)
		MIN	TYP	MAX		
AC PERFORMANCE (SD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	6.6	8.2	10	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	8	9.5	11	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	85	150		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	70	100		V/μs	B
Attenuation	With respect to 500 kHz(2), f = 6.75 MHz	–0.9	0.2	1.2	dB	B
	With respect to 500 kHz(2), f = 27 MHz	42	54		dB	B
Group delay	f = 100 kHz		78		ns	C
Group delay variation	f = 5.1 MHz with respect to 100 kHz		11		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.25/0.35		%	C
Differential phase	NTSC/PAL		0.4/0.5		Degrees	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–69		dB	C
Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 6.75 MHz, Filter mode		0.9		Ω	C
	f = 6.75 MHz, Bypass mode		0.9		Ω	C
	Disabled		20 || 3		kΩ || pF	C
Return loss	f = 6.75 MHz, Filter mode		44		dB	C
Crosstalk	f = 1 MHz, SD to SD channels		–72		dB	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.
(2) 3.3-V supply filter specifications are ensured by 100% testing at 5-V supply together with design and characterization.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7364 MIN	THS7364 TYP	THS7364 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (FULL-HD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	53	60	66	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	60	72	83	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	250	350		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	400	500		V/µs	B
Attenuation	With respect to 500 kHz(3), f = 54 MHz	–0.5	0.6	2	dB	B
	With respect to 500 kHz(3), f = 148 MHz	33	40		dB	B
Group delay	f = 100 kHz		12		ns	C
Group delay variation	f = 54 MHz with respect to 100 kHz		4.5		ns	C
Channel-to-channel delay			0.3		ns	C
Total harmonic distortion	f = 20 MHz, V_O = 1.4 V_{PP}		–54		dB	C
Signal-to-noise ratio	100 kHz to 60 MHz, non-weighted		60		dB	C
	Unified weighting		70		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 60 MHz, Filter mode		9		Ω	C
	f = 60 MHz, Bypass mode		9		Ω	C
	Disabled		2 || 3		kΩ || pF	C
Return loss	f = 60 MHz, Filter mode		25		dB	C
Crosstalk	f = 25 MHz, FHD to SD channels		–55		dB	C
	f = 25 MHz, SD to FHD channels		–70		dB	C
	f = 25 MHz, FHD to FHD channels		–45		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V, SD channels	200	305	400	mV	A
	V_{IN} = 0 V, FHD channels	200	300	400	mV	A
Input voltage range	DC input, limited by output		–0.1/1.46		V	C
Sync-tip clamp charge current	V_{IN} = –0.1 V, SD channels	140	200		µA	A
	V_{IN} = –0.1 V, FHD channels	280	400		µA	A
Input impedance			800 || 2		kΩ || pF	C
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to +1.65 V		3.15		V	C
	R_L = 150 Ω to GND	2.85	3.1		V	A
	R_L = 75 Ω to +1.65 V		3.1		V	C
	R_L = 75 Ω to GND		3		V	C
Low output voltage swing	R_L = 150 Ω to +1.65 V (V_{IN} = –0.2 V)		0.06		V	C
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.05	0.12	V	A
	R_L = 75 Ω to +1.65 V (V_{IN} = –0.2 V)		0.1		V	C
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
Output current (sourcing)	R_L = 10 Ω to +1.65 V		80		mA	C
Output current (sinking)	R_L = 10 Ω to +1.65 V		70		mA	C

(3) 3.3-V supply filter specifications are ensured by 100% testing at 5-V supply together with design and characterization.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7364 MIN	THS7364 TYP	THS7364 MAX	UNITS	TEST LEVEL(1)
POWER SUPPLY						
Operating voltage		2.6	3.3	5.5	V	B
Total quiescent current, no load	V_{IN} = 0 V, all channels on	18.8	23.4	28.5	mA	A
	V_{IN} = 0 V, SD channels on, FHD channels off	5.6	6.9	9	mA	A
	V_{IN} = 0 V, SD channels off, FHD channels on	13.2	16.5	19.5	mA	A
	V_{IN} = 0 V, all channels off, $V_{DISABLE}$ = 3 V		0.1	10	µA	A
Power-supply rejection ratio (PSRR)	At dc		52		dB	C
LOGIC CHARACTERISTICS(4)						
V_{IH}	Disabled or Bypass engaged	1.6	1.4		V	A
V_{IL}	Enabled or Bypass disengaged		0.75	0.6	V	A
I_{IH}	Applied voltage = 3.3 V		1		µA	C
I_{IL}	Applied voltage = 0 V		1		µA	C
Disable time			200		ns	C
Enable time			250		ns	C
Bypass/filter switch time			15		ns	C

(4) The logic input pins default to a logic '0' condition when left floating.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7364 MIN	THS7364 TYP	THS7364 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (SD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	6.6	8.2	10.2	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	8	9.5	11.3	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	85	150		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	70	100		V/µs	B
Attenuation	With respect to 500 kHz, f = 6.75 MHz	–0.9	0.25	1.2	dB	A
	With respect to 500 kHz, f = 27 MHz	42	54		dB	A
Group delay	f = 100 kHz		78		ns	C
Group delay variation	f = 5.1 MHz with respect to 100 kHz		11		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.25/0.35		%	C
Differential phase	NTSC/PAL		0.4/0.5		Degrees	C
Total harmonic distortion	f = 1 MHz, V_O = 1.4 V_{PP}		–71		dB	C
Signal-to-noise ratio	100 kHz to 6 MHz, non-weighted		70		dB	C
	100 kHz to 6 MHz, unified weighting		78		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 6.75 MHz, Filter mode		0.9		Ω	C
	f = 6.75 MHz, Bypass mode		0.9		Ω	C
	Disabled		20 || 3		kΩ || pF	C
Return loss	f = 6.75 MHz, Filter mode		44		dB	C
Crosstalk	f = 1 MHz, SD to SD channels		–72		dB	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7364 MIN	THS7364 TYP	THS7364 MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE (FULL-HD CHANNELS)						
Passband bandwidth	–1 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	53	60	66	MHz	B
Small- and large-signal bandwidth	–3 dB; V_O = 0.2 V_{PP} and 2 V_{PP}	60	72	83	MHz	B
Bypass mode bandwidth	–3 dB; V_O = 0.2 V_{PP}	250	350		MHz	B
Slew rate	Bypass mode; V_O = 2 V_{PP}	400	500		V/µs	B
Attenuation	With respect to 500 kHz, f = 54 MHz	–0.5	0.4	2	dB	A
	With respect to 500 kHz, f = 148 MHz	33	40		dB	A
Group delay	f = 100 kHz		12		ns	C
Group delay variation	f = 54 MHz with respect to 100 kHz		4.5		ns	C
Channel-to-channel delay			0.3		ns	C
Total harmonic distortion	f = 20 MHz, V_O = 1.4 V_{PP}		–50		dB	C
Signal-to-noise ratio	100 kHz to 60 MHz, non-weighted		60		dB	C
	Unified weighting		70		dB	C
Gain	All channels, T_A = +25°C	5.7	6	6.3	dB	A
	All channels, T_A = –40°C to +85°C	5.65		6.35	dB	B
Output impedance	f = 60 MHz, Filter mode		9		Ω	C
	f = 60 MHz, Bypass mode		9		Ω	C
	Disabled		2 || 3		kΩ || pF	C
Return loss	f = 60 MHz, Filter mode		25		dB	C
Crosstalk	f = 25 MHz, FHD to SD channels		–55		dB	C
	f = 25 MHz, SD to FHD channels		–70		dB	C
	f = 25 MHz, FHD to FHD channels		–45		dB	C

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ELECTRICAL CHARACTERISTICS: V_{S+} = +5 V (continued)

At T_A = +25°C, R_L = 150 Ω to GND, Filter mode, and dc-coupled input/output, unless otherwise noted.

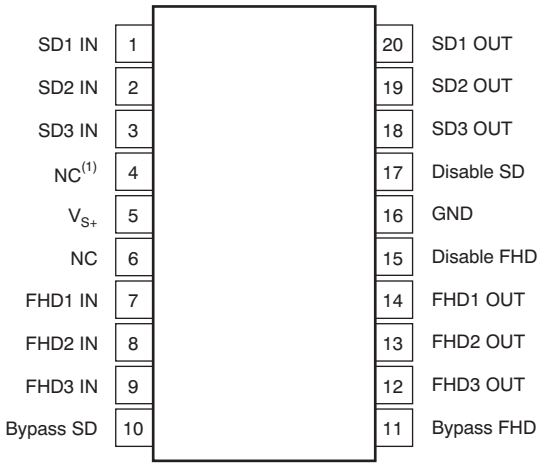
PARAMETER	TEST CONDITIONS	THS7364 MIN	THS7364 TYP	THS7364 MAX	UNITS	TEST LEVEL(1)
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V, SD channels	200	305	400	mV	A
	V_{IN} = 0 V, FHD channels	200	300	400	mV	A
Input voltage range	DC input, limited by output		–0.1/2.3		V	C
Sync-tip clamp charge current	V_{IN} = –0.1 V, SD channels	140	200		µA	A
	V_{IN} = –0.1 V, FHD channels	280	400		µA	A
Input impedance			800 || 2		kΩ || pF	C
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to +2.5 V		4.85		V	C
	R_L = 150 Ω to GND	4.4	4.75		V	A
	R_L = 75 Ω to +2.5V		4.7		V	C
	R_L = 75 Ω to GND		4.5		V	C
Low output voltage swing	R_L = 150 Ω to +2.5 V (V_{IN} = –0.2 V)		0.06		V	C
	R_L = 150 Ω to GND (V_{IN} = –0.2 V)		0.05	0.12	V	A
	R_L = 75 Ω to +2.5 V (V_{IN} = –0.2 V)		0.1		V	C
	R_L = 75 Ω to GND (V_{IN} = –0.2 V)		0.05		V	C
Output current (sourcing)	R_L = 10 Ω to +2.5 V		90		mA	C
Output current (sinking)	R_L = 10 Ω to +2.5 V		85		mA	C
POWER SUPPLY						
Operating voltage		2.6	5	5.5	V	B
Total quiescent current, no load	V_{IN} = 0 V, all channels on	19.7	24.5	30.2	mA	A
	V_{IN} = 0 V, SD channels on, FHD channels off	6	7.2	9.5	mA	A
	V_{IN} = 0 V, SD channels off, FHD channels on	13.7	17.3	20.7	mA	A
	V_{IN} = 0 V, all channels off, $V_{DISABLE}$ = 3 V		1	10	µA	A
Power-supply rejection ratio (PSRR)	At dc		52		dB	C
LOGIC CHARACTERISTICS(2)						
V_{IH}	Disabled or Bypass engaged	2.1	1.9		V	A
V_{IL}	Enabled or Bypass disengaged		1.2	1	V	A
I_{IH}	Applied voltage = 3.3 V		1		µA	C
I_{IL}	Applied voltage = 0 V		1		µA	C
Disable time			150		ns	C
Enable time			200		ns	C
Bypass/filter switch time			10		ns	C

(2) The logic input pins default to a logic '0' condition when left floating.

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PIN CONFIGURATION

PW PACKAGE
TSSOP-20
(TOP VIEW)



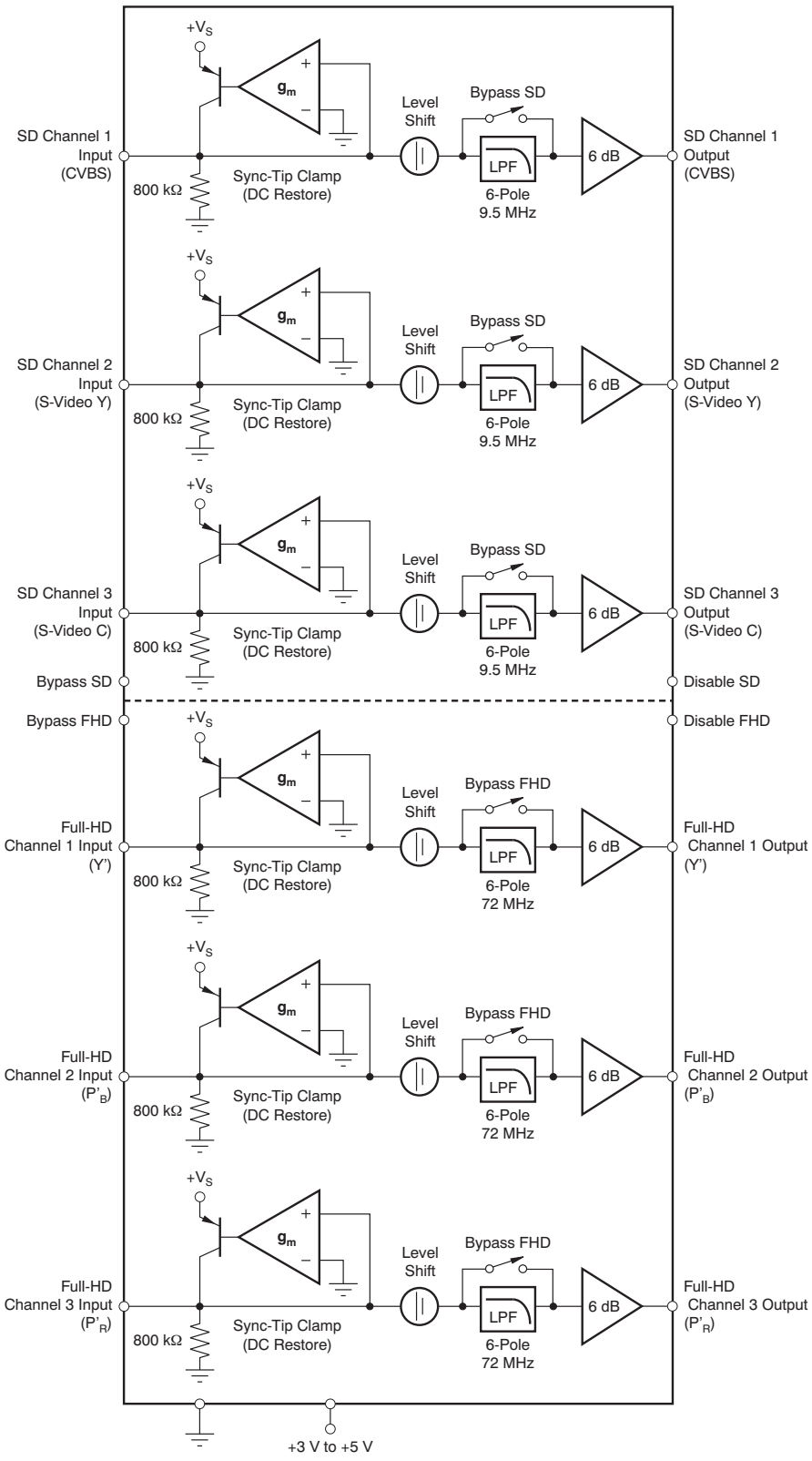
(1) NC = No connection.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SD1 IN	1	I	Standard-definition video input, channel 1; LPF = 9.5 MHz
SD2 IN	2	I	Standard-definition video input, channel 2; LPF = 9.5 MHz
SD3 IN	3	I	Standard-definition video input, channel 3; LPF = 9.5 MHz
NC	4	—	No internal connection
V_{S+}	5	I	Positive power-supply pin; connect to +2.7 V up to +5 V
NC	6	—	No internal connection
FHD1 IN	7	I	Full high-definition video input, channel 1; LPF = 72 MHz
FHD2 IN	8	I	Full high-definition video input, channel 2; LPF = 72 MHz
FHD3 IN	9	I	Full high-definition video input, channel 3; LPF = 72 MHz
Bypass SD	10	I	Bypass all SD channel filters. Logic high bypasses the internal filters and logic low engages the internal filters.
Bypass FHD	11	I	Bypass all FHD channel filters. Logic high bypasses the internal filters and logic low engages the internal filters.
FHD3 OUT	12	O	Full high-definition video output, channel 3; LPF = 72 MHz
FHD2 OUT	13	O	Full high-definition video output, channel 2; LPF = 72 MHz
FHD1 OUT	14	O	Full high-definition video output, channel 1; LPF = 72 MHz
Disable FHD	15	I	Disable full high-definition channels. Logic high disables the FHD channels and logic low enables the FHD channels.
GND	16	I	Ground pin for all internal circuitry
Disable SD	17	I	Disable standard definition channels. Logic high disables the SD channels and logic low enables the SD channels.
SD3 OUT	18	O	Standard-definition video output, channel 3; LPF = 9.5 MHz
SD2 OUT	19	O	Standard-definition video output, channel 2; LPF = 9.5 MHz
SD1 OUT	20	O	Standard-definition video output, channel 1; LPF = 9.5 MHz

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FUNCTIONAL BLOCK DIAGRAM



(1)

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TYPICAL CHARACTERISTICS

Table 1. Table of Graphs: 3.3 V, Standard-Definition (SD) Channels

TITLE	FIGURE
SD Channels Small-Signal Gain vs Frequency Response	Figure 2, Figure 3, Figure 4, Figure 9, Figure 10, Figure 19, Figure 20
SD Channels Phase vs Frequency Response	Figure 5
SD Channels Group Delay vs Frequency Response	Figure 6
SD Channels Large-Signal Gain vs Frequency Response	Figure 7, Figure 8
SD Channels Bypass Mode Response vs Time	Figure 11
SD Channels Disable Mode Response vs Time	Figure 12, Figure 13
SD Channels Slew Rate vs Output Voltage	Figure 14
SD Channels Large-Signal Pulse Response vs Time	Figure 15, Figure 16
SD Channels Small-Signal Pulse Response vs Time	Figure 17, Figure 18
SD Channels THD vs Frequency	Figure 21, Figure 22

Table 2. Table of Graphs: 3.3 V, Full High-Definition (FHD) Channels

TITLE	FIGURE
FHD Channels Small-Signal Gain vs Frequency Response	Figure 23, Figure 24, Figure 29, Figure 30, Figure 35, Figure 36
FHD Channels Phase vs Frequency Response	Figure 25
FHD Channels Group Delay vs Frequency Response	Figure 26
FHD Channels Large-Signal Gain vs Frequency Response	Figure 27, Figure 28
FHD Channels Slew Rate vs Output Voltage	Figure 31
FHD Channels Bypass Mode Response vs Time	Figure 32
FHD Channels Disable Mode Response vs Time	Figure 33, Figure 34
FHD Channels THD vs Frequency	Figure 37, Figure 38

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Table 3. Table of Graphs: 5 V, Standard-Definition (SD) Channels

TITLE	FIGURE
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SD Channels Phase vs Frequency Response	Figure 42
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SD Channels Large-Signal Gain vs Frequency Response	Figure 44, Figure 45
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FHD Channels Phase vs Frequency Response	Figure 62
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TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

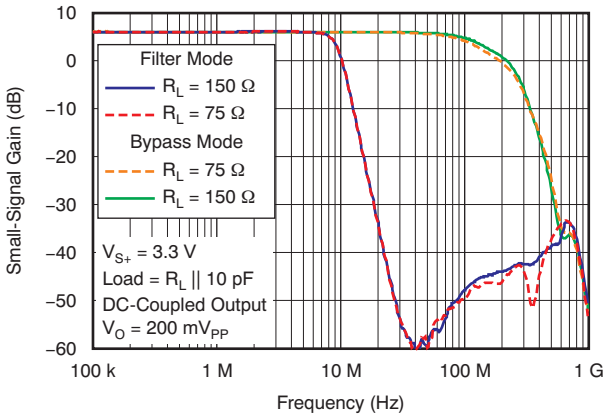


Figure 2.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

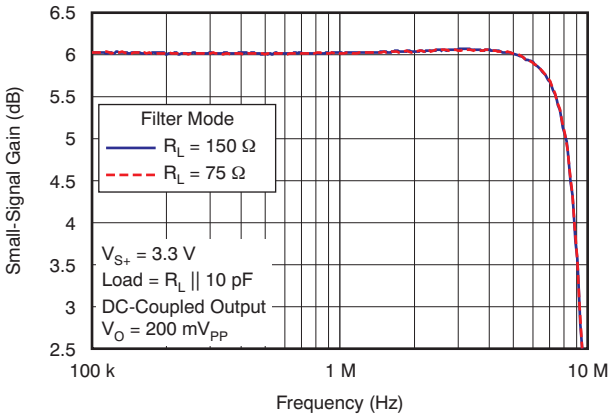


Figure 3.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

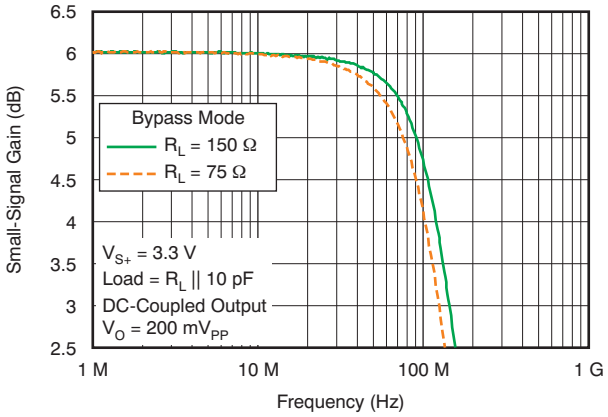


Figure 4.

SD CHANNELS PHASE vs FREQUENCY RESPONSE

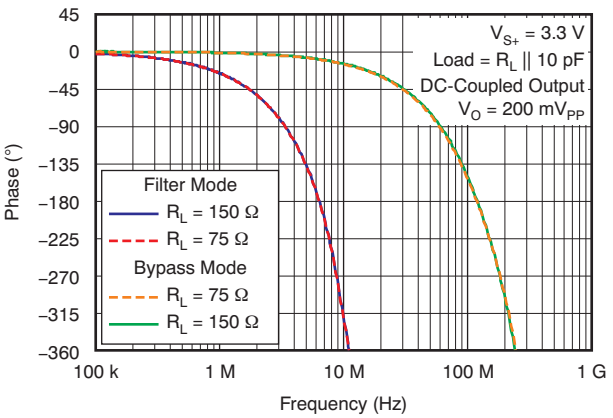


Figure 5.

SD CHANNELS GROUP DELAY vs FREQUENCY RESPONSE

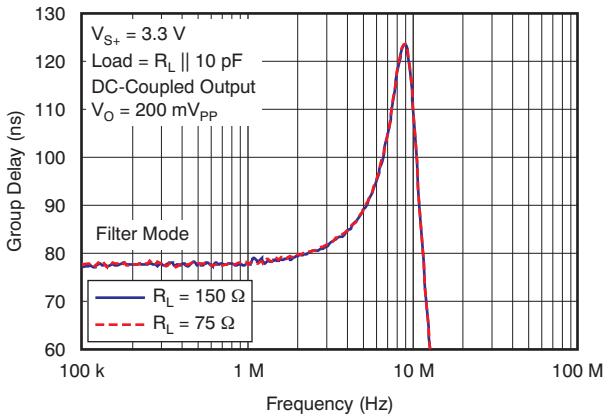


Figure 6.

SD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

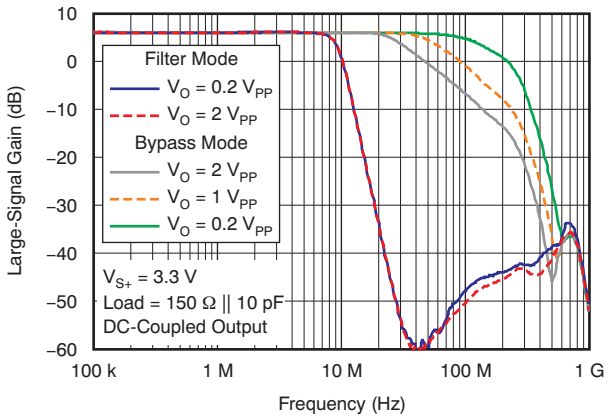


Figure 7.

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TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

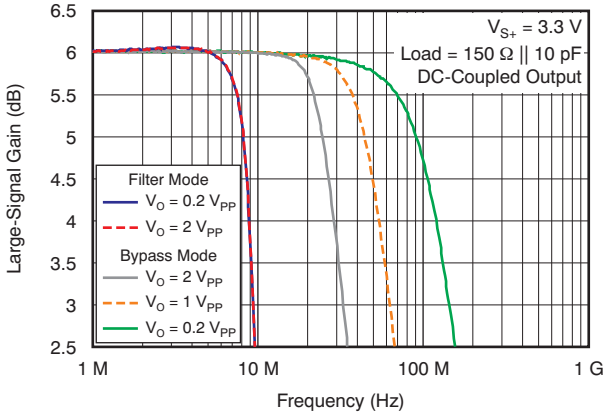


Figure 8.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

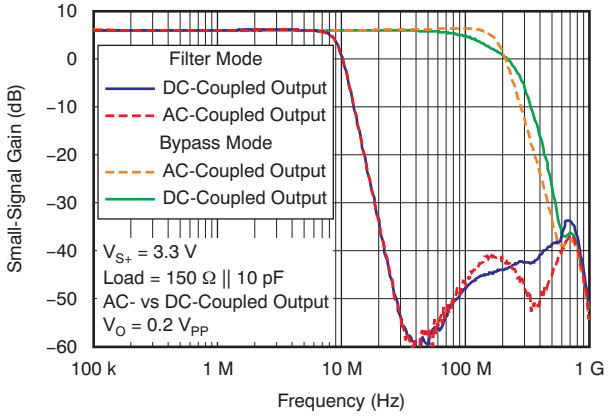


Figure 9.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

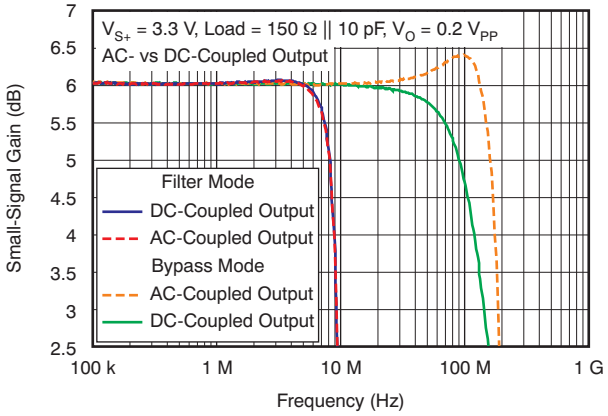


Figure 10.

SD CHANNELS BYPASS MODE RESPONSE vs TIME

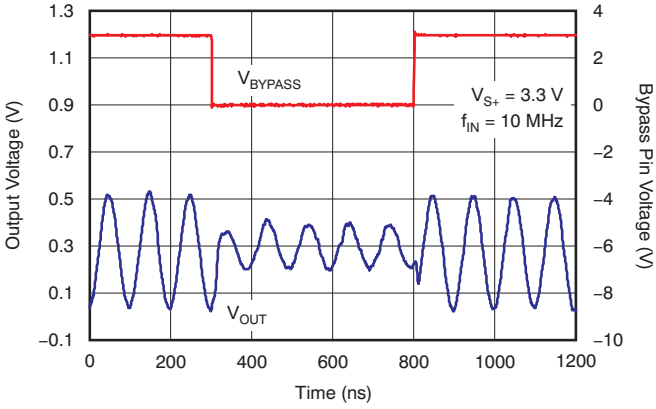


Figure 11.

SD CHANNELS DISABLE MODE RESPONSE vs TIME

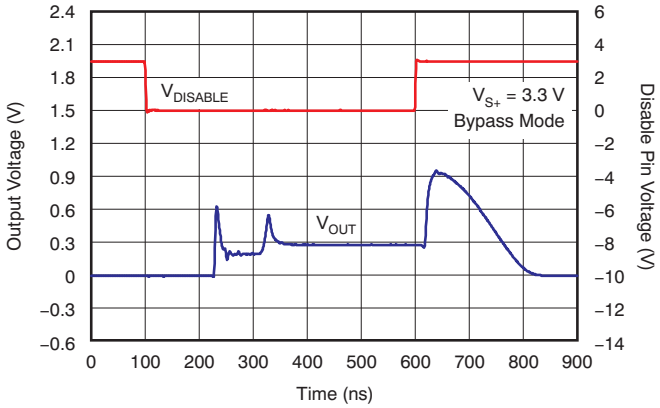


Figure 12.

SD CHANNELS DISABLE MODE RESPONSE vs TIME

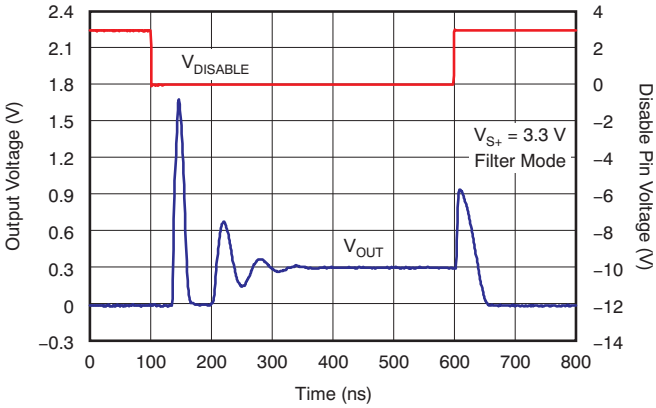


Figure 13.

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TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS SLEW RATE vs OUTPUT VOLTAGE

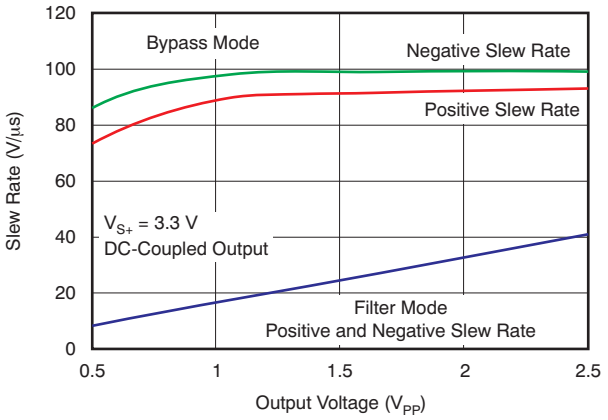


Figure 14.

SD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

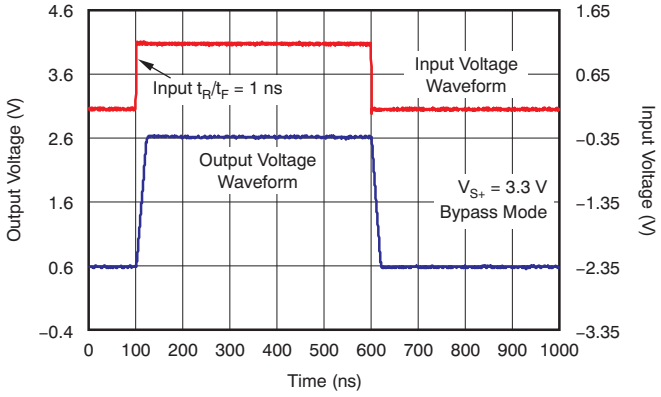


Figure 15.

SD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

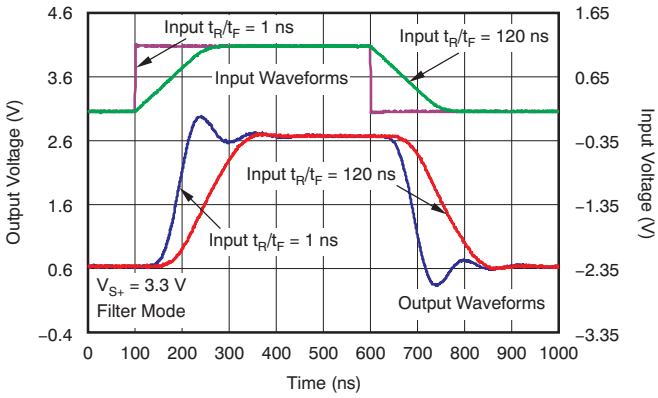


Figure 16.

SD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

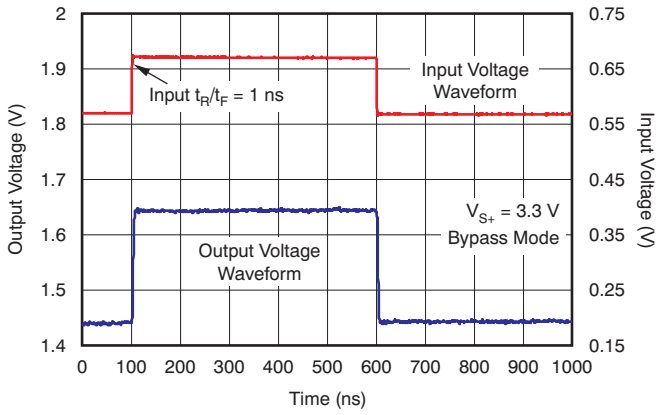


Figure 17.

SD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

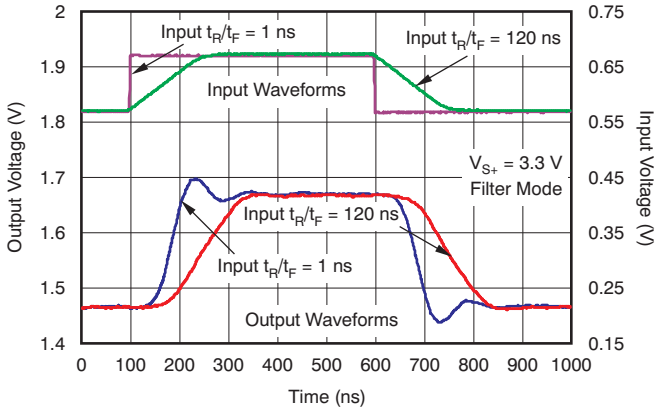


Figure 18.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

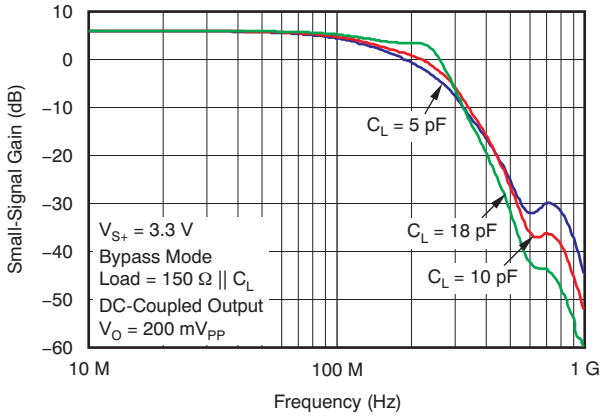


Figure 19.

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TYPICAL CHARACTERISTICS: 3.3 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

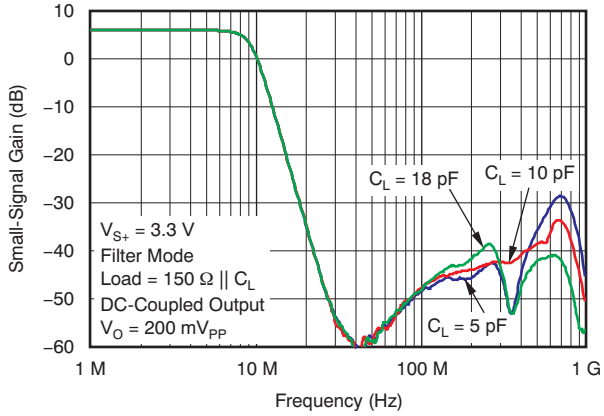


Figure 20.

SD CHANNELS THD vs FREQUENCY

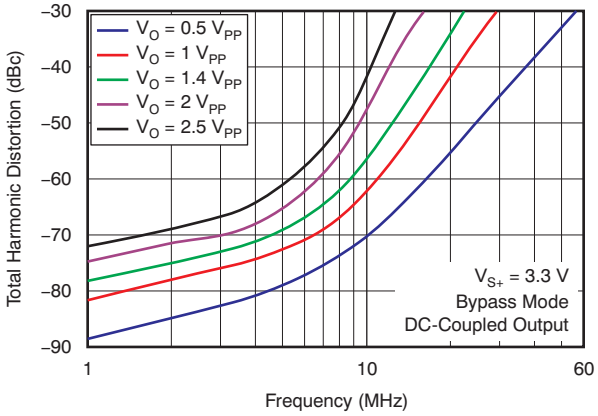


Figure 21.

SD CHANNELS THD vs FREQUENCY

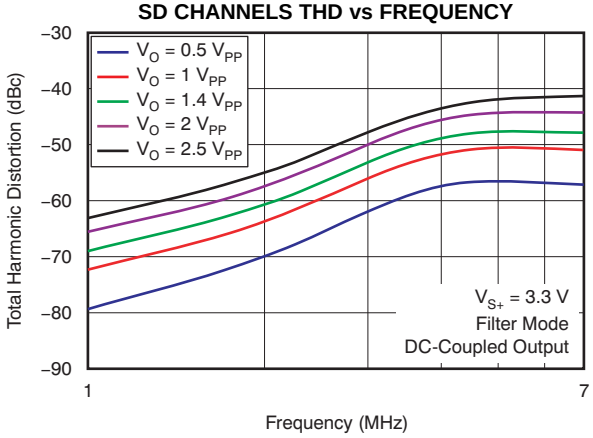


Figure 22.

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TYPICAL CHARACTERISTICS: 3.3 V, Full HD (FHD) Channels

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

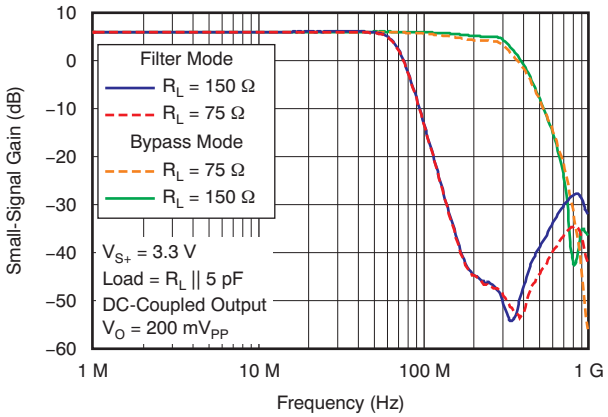


Figure 23.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

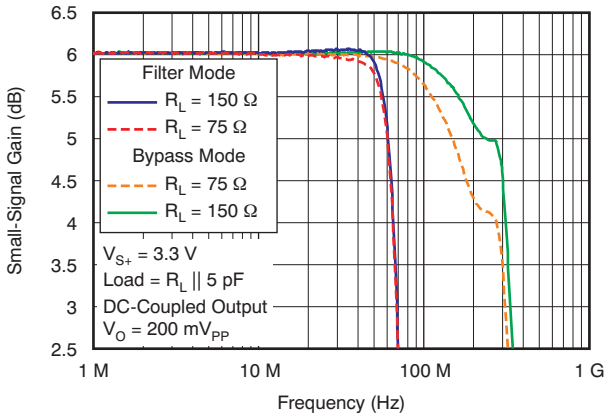


Figure 24.

FHD CHANNELS PHASE vs FREQUENCY RESPONSE

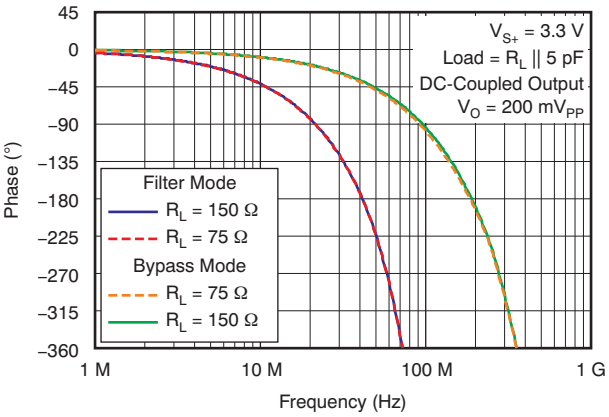


Figure 25.

FHD CHANNELS GROUP DELAY vs FREQUENCY RESPONSE

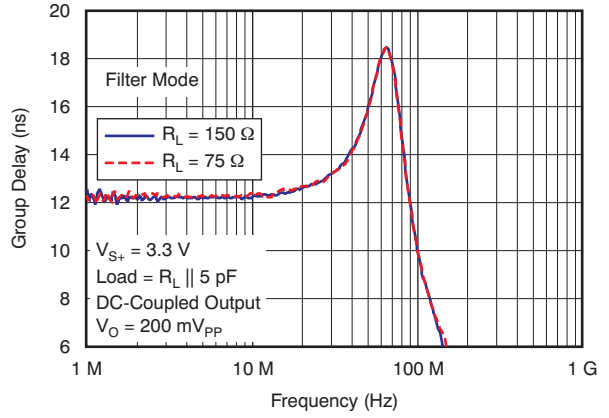


Figure 26.

FHD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

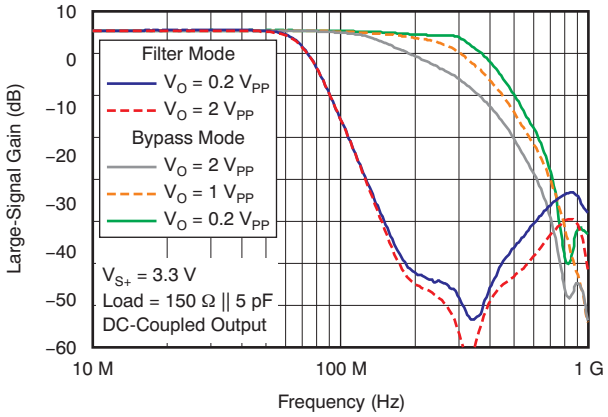


Figure 27.

FHD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

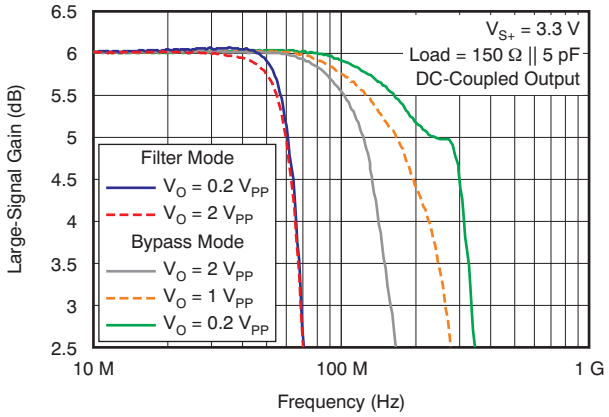


Figure 28.

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TYPICAL CHARACTERISTICS: 3.3 V, Full HD (FHD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

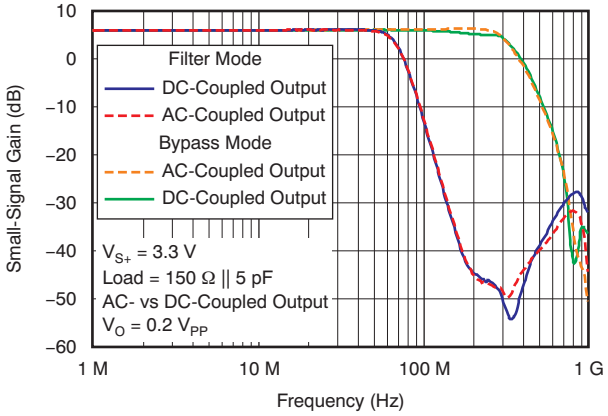


Figure 29.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

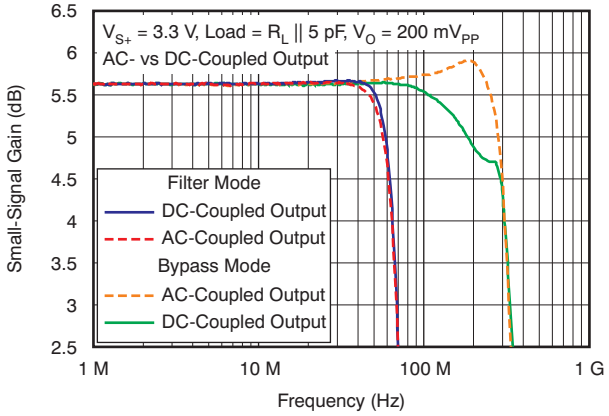


Figure 30.

FHD CHANNELS SLEW RATE vs OUTPUT VOLTAGE

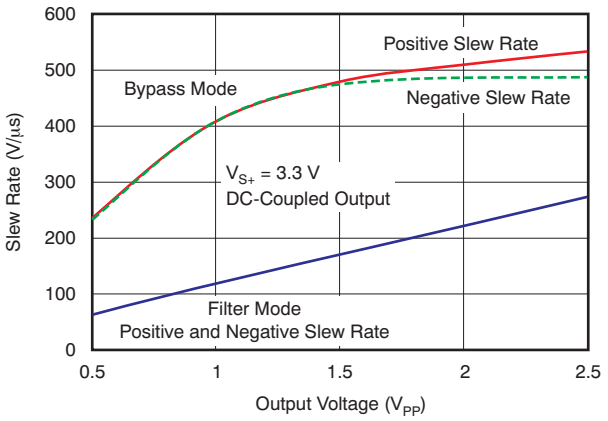


Figure 31.

FHD CHANNELS BYPASS MODE RESPONSE vs TIME

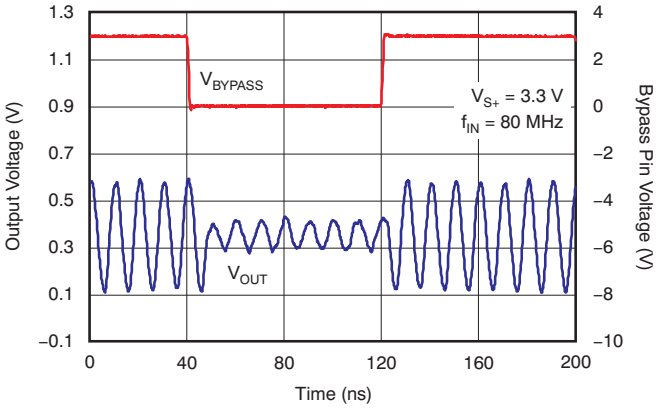


Figure 32.

FHD CHANNELS DISABLE MODE RESPONSE vs TIME

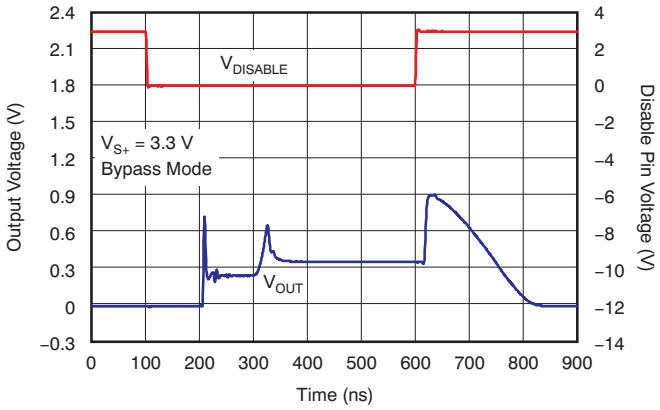


Figure 33.

FHD CHANNELS DISABLE MODE RESPONSE vs TIME

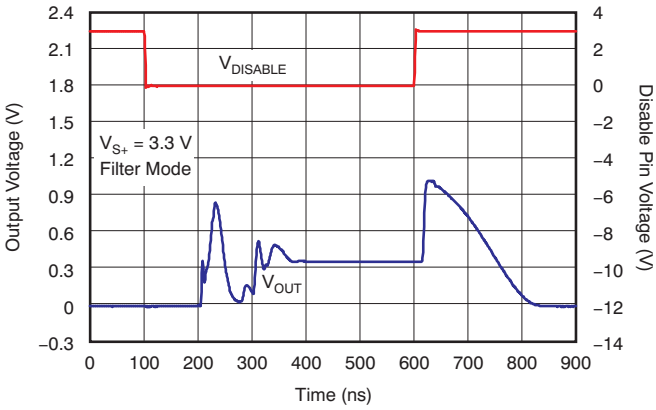


Figure 34.

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TYPICAL CHARACTERISTICS: 3.3 V, Full HD (FHD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

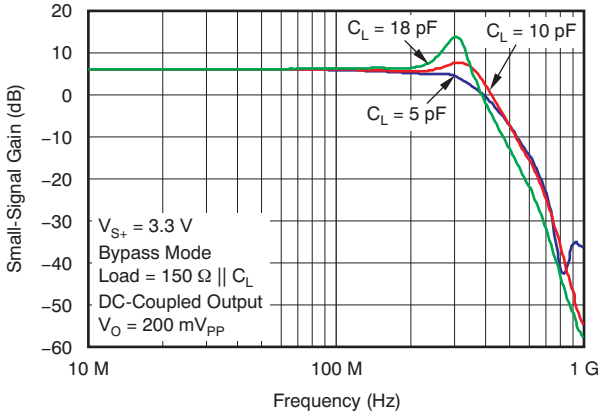


Figure 35.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

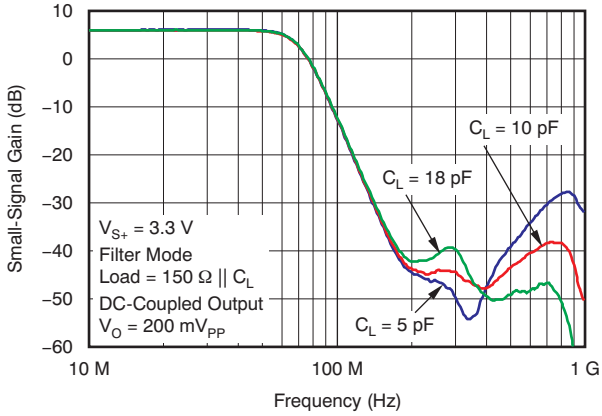


Figure 36.

FHD CHANNELS THD vs FREQUENCY

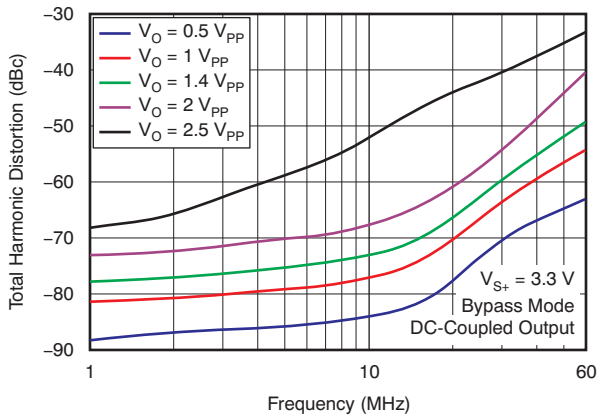


Figure 37.

FHD CHANNELS THD vs FREQUENCY

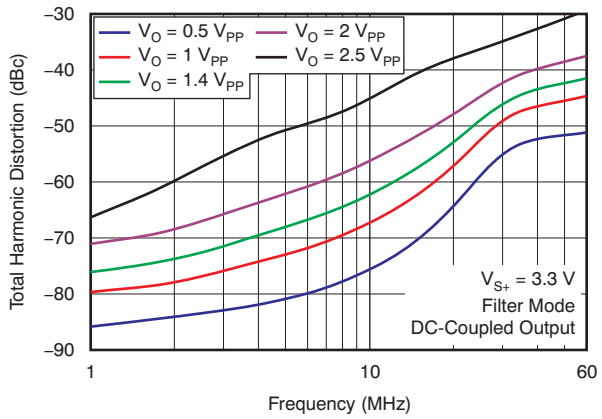


Figure 38.

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TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

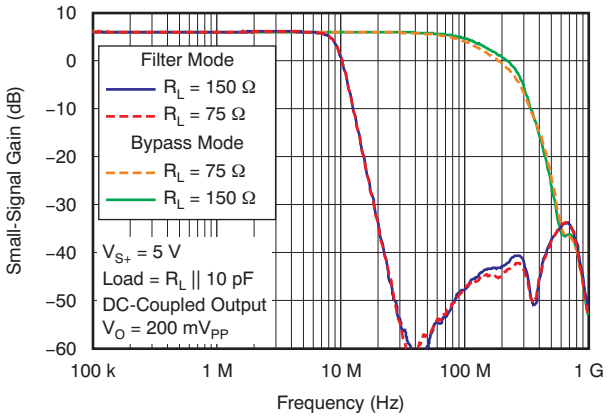


Figure 39.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

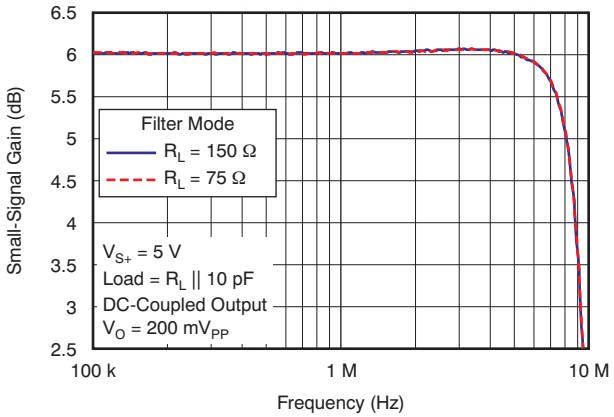


Figure 40.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

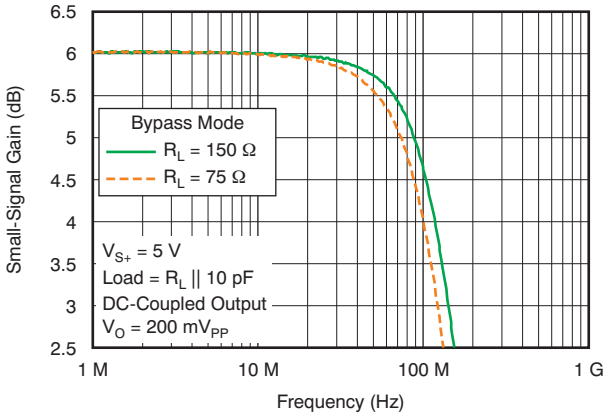


Figure 41.

SD CHANNELS PHASE vs FREQUENCY RESPONSE

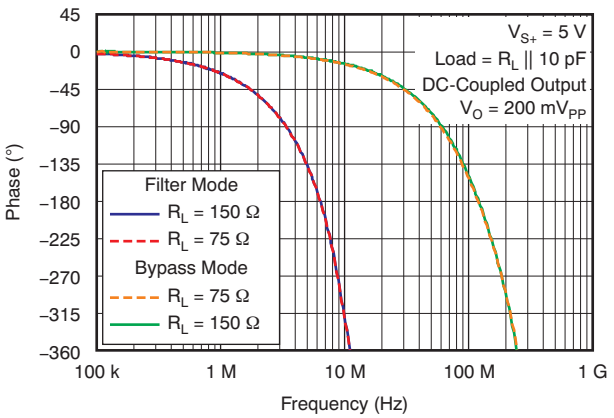


Figure 42.

SD CHANNELS GROUP DELAY vs FREQUENCY RESPONSE

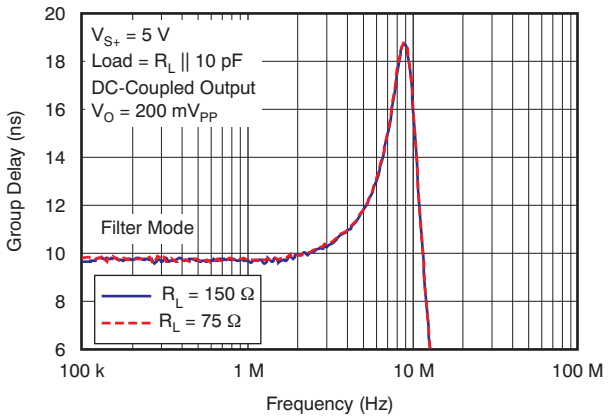


Figure 43.

SD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

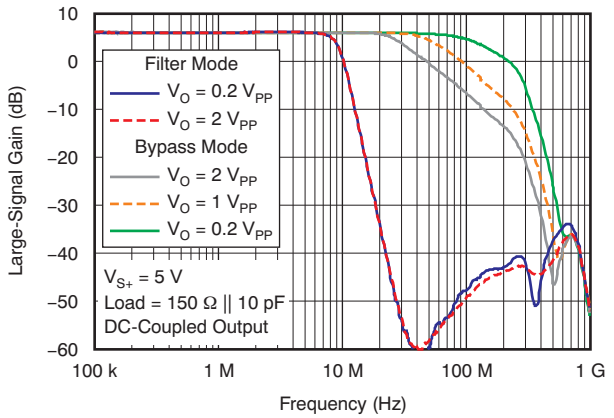


Figure 44.

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TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

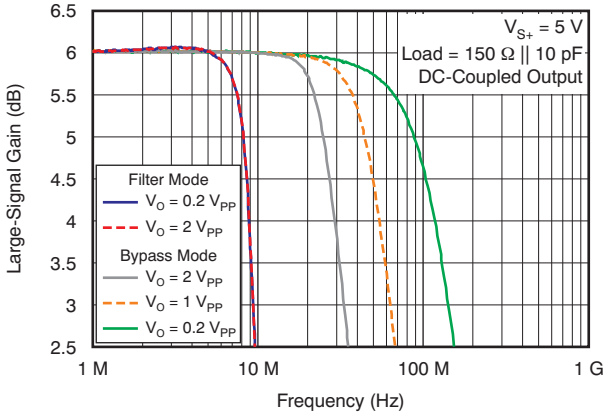


Figure 45.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

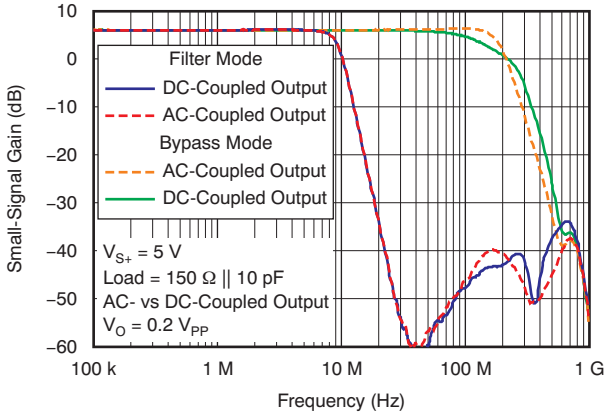


Figure 46.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

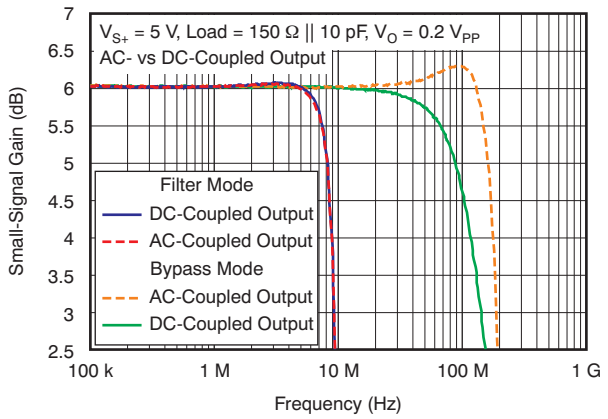


Figure 47.

SD CHANNELS BYPASS MODE RESPONSE vs TIME

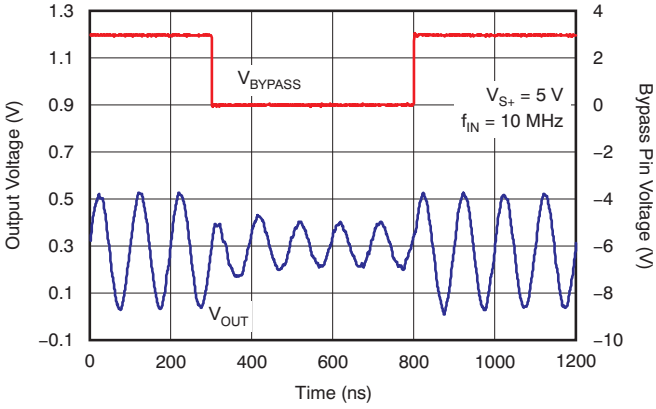


Figure 48.

SD CHANNELS DISABLE MODE RESPONSE vs TIME

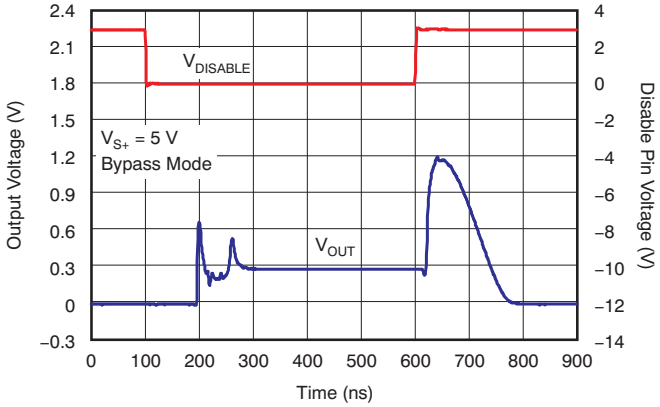


Figure 49.

SD CHANNELS DISABLE MODE RESPONSE vs TIME

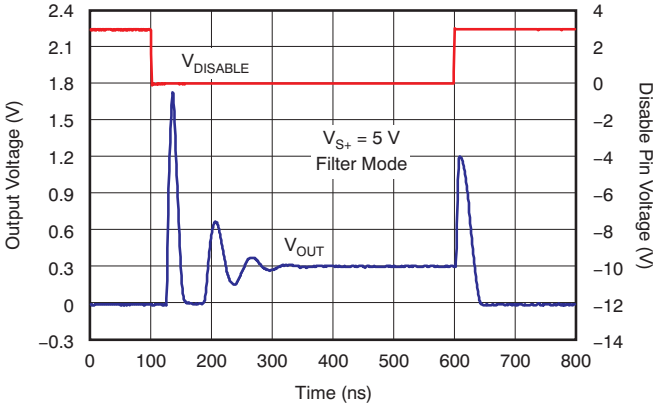


Figure 50.

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TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS SLEW RATE vs OUTPUT VOLTAGE

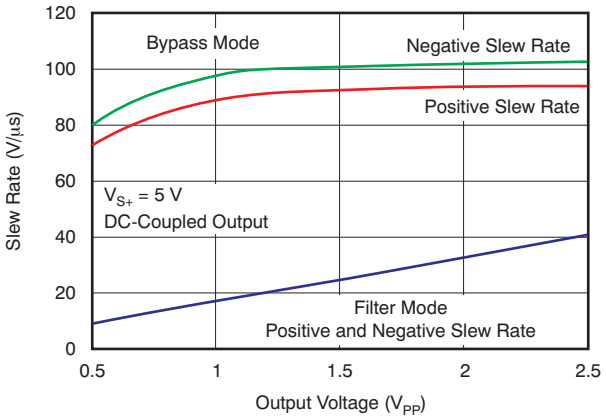


Figure 51.

SD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

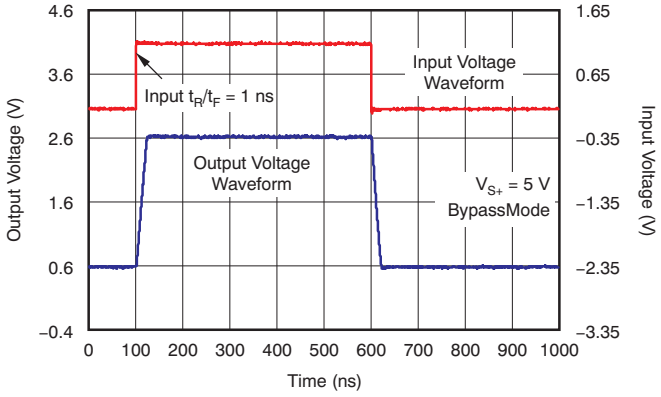


Figure 52.

SD CHANNELS LARGE-SIGNAL PULSE RESPONSE vs TIME

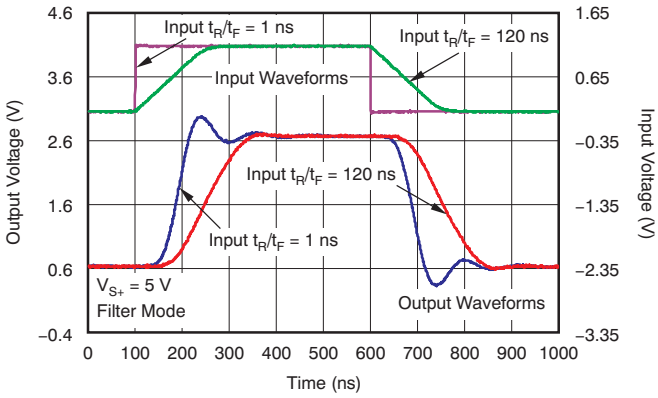


Figure 53.

SD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

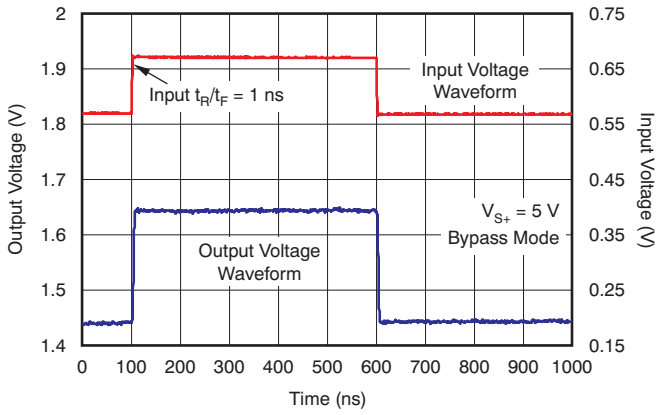


Figure 54.

SD CHANNELS SMALL-SIGNAL PULSE RESPONSE vs TIME

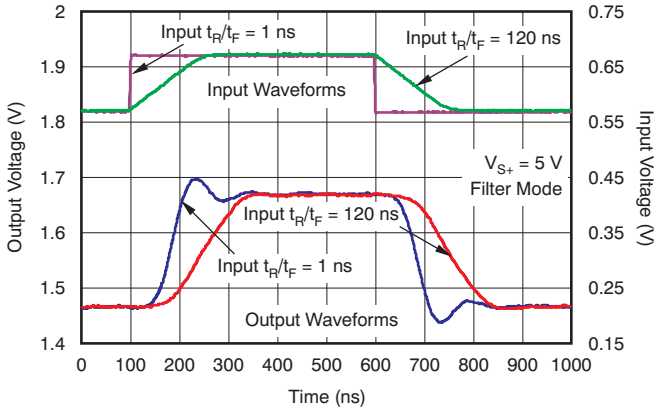


Figure 55.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

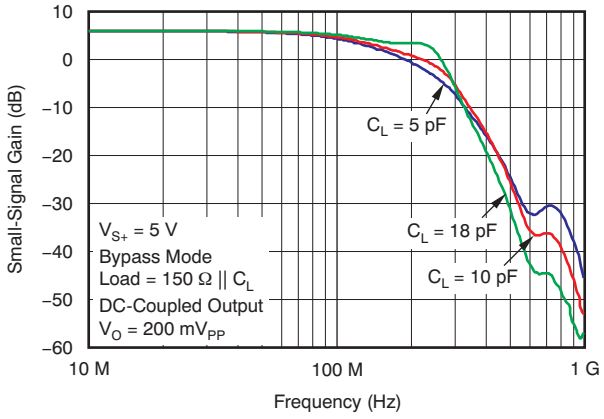


Figure 56.

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TYPICAL CHARACTERISTICS: 5 V, Standard-Definition (SD) Channels (continued)

With load = 150 Ω || 10 pF, dc-coupled input and output, unless otherwise noted.

SD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

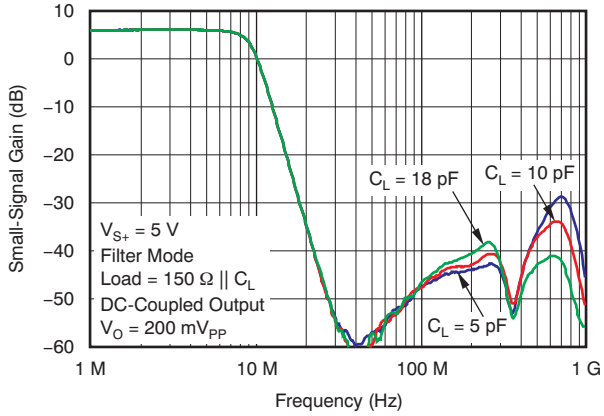


Figure 57.

SD CHANNELS THD vs FREQUENCY

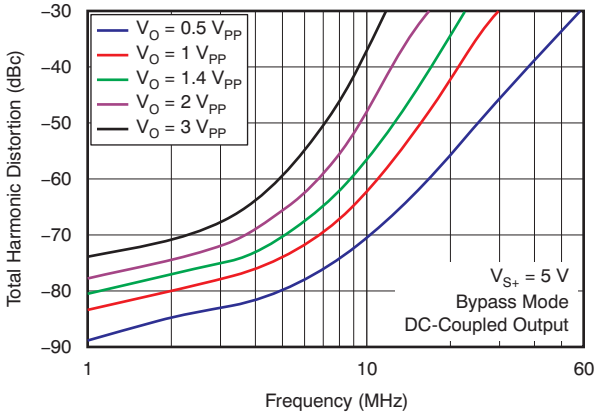


Figure 58.

SD CHANNELS THD vs FREQUENCY

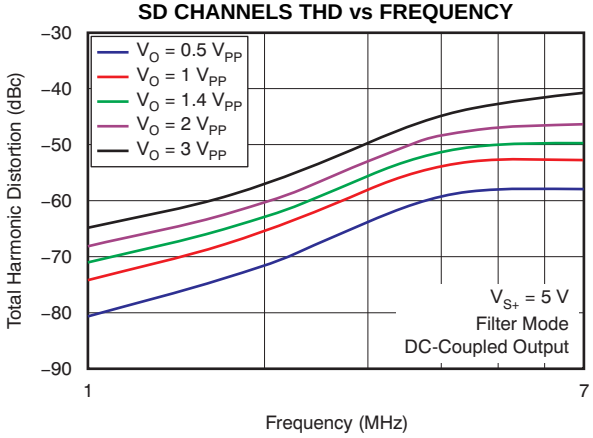


Figure 59.

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TYPICAL CHARACTERISTICS: 5 V, Full HD (FHD) Channels

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

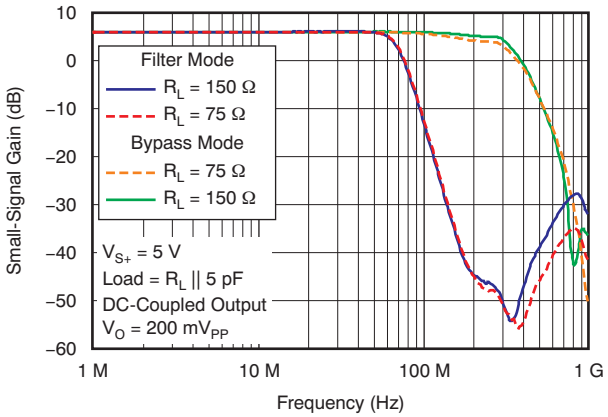


Figure 60.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

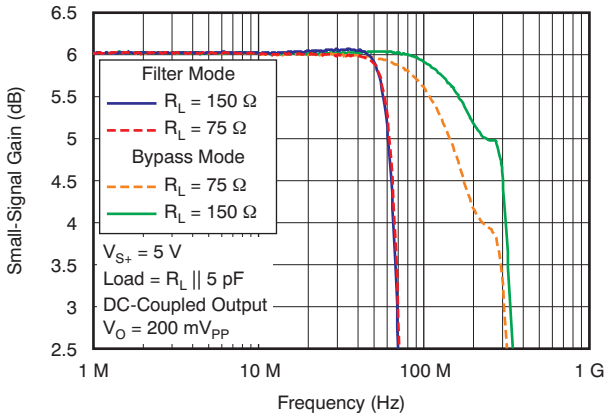


Figure 61.

FHD CHANNELS PHASE vs FREQUENCY RESPONSE

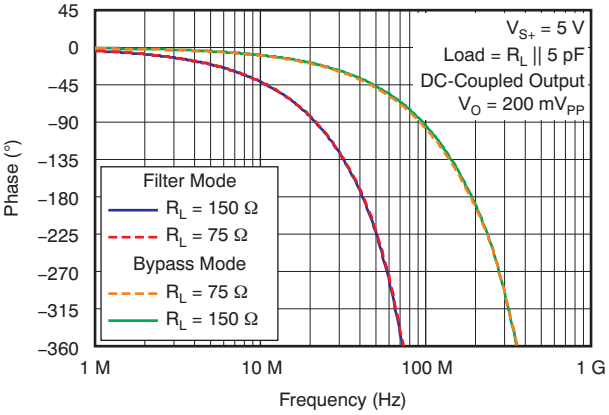


Figure 62.

FHD CHANNELS GROUP DELAY vs FREQUENCY RESPONSE

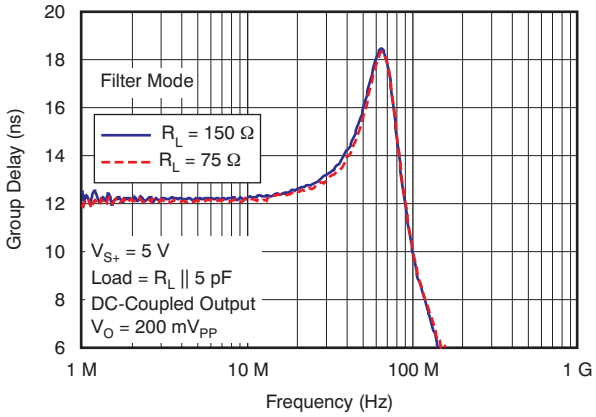


Figure 63.

FHD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

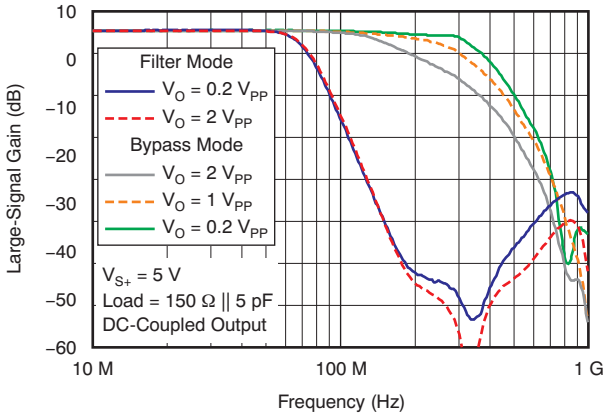


Figure 64.

FHD CHANNELS LARGE-SIGNAL GAIN vs FREQUENCY RESPONSE

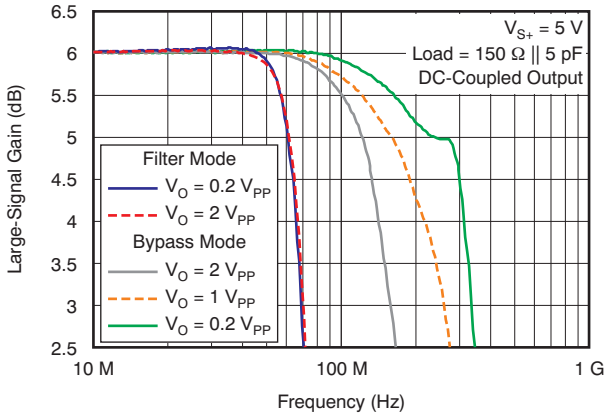


Figure 65.

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TYPICAL CHARACTERISTICS: 5 V, Full HD (FHD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

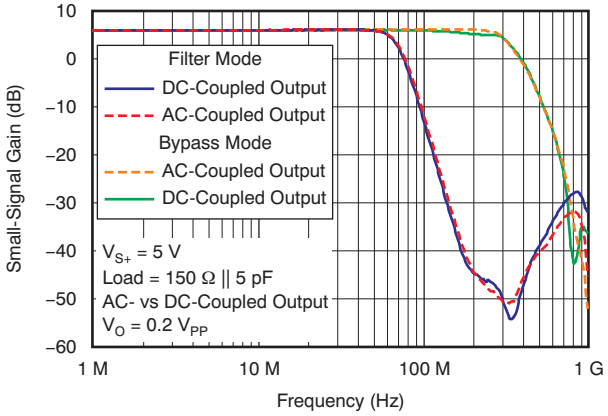


Figure 66.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

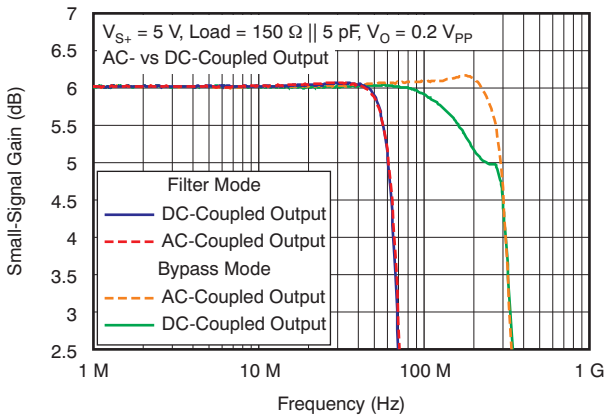


Figure 67.

FHD CHANNELS SLEW RATE vs OUTPUT VOLTAGE

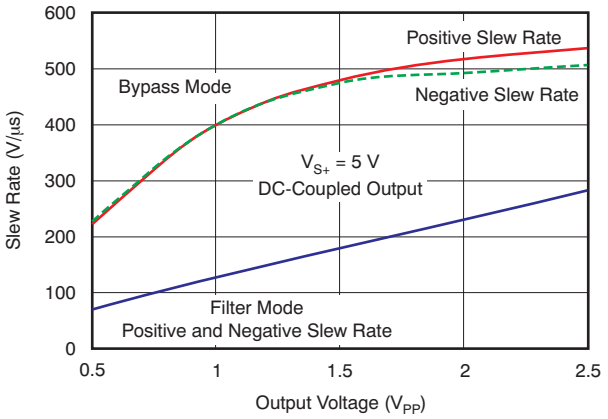


Figure 68.

FHD CHANNELS BYPASS MODE RESPONSE vs TIME

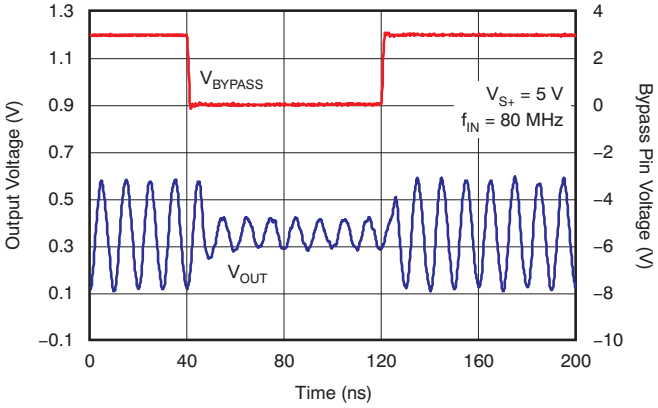


Figure 69.

FHD CHANNELS DISABLE MODE RESPONSE vs TIME

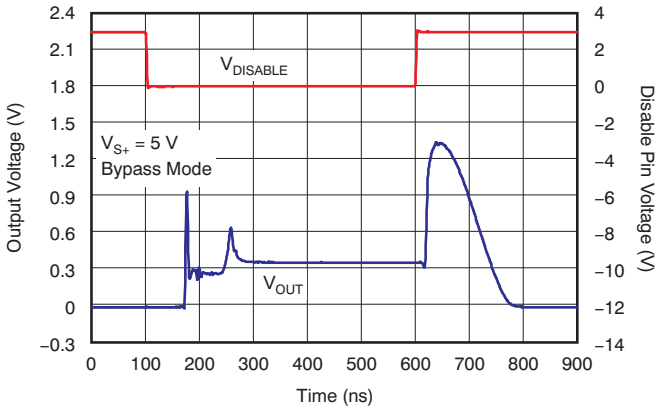


Figure 70.

FHD CHANNELS DISABLE MODE RESPONSE vs TIME

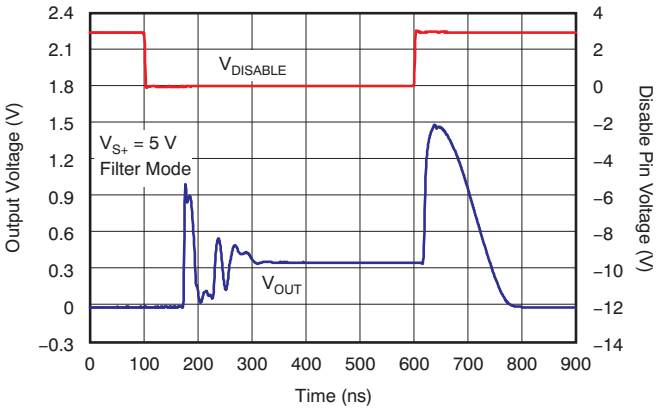


Figure 71.

TYPICAL CHARACTERISTICS: 5 V, Full HD (FHD) Channels (continued)

With load = 150 Ω || 5 pF, dc-coupled input and output, unless otherwise noted.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

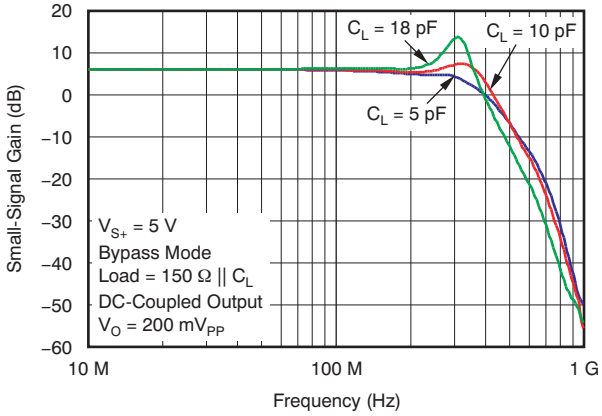


Figure 72.

FHD CHANNELS SMALL-SIGNAL GAIN vs FREQUENCY RESPONSE

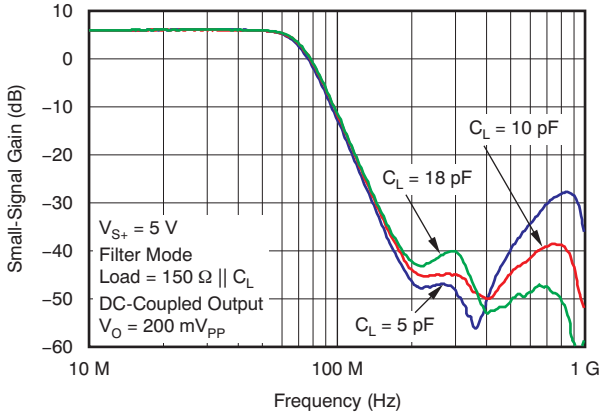


Figure 73.

FHD CHANNELS THD vs FREQUENCY

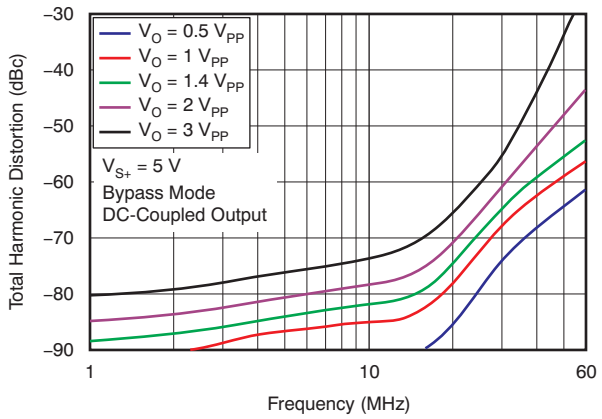


Figure 74.

FHD CHANNELS THD vs FREQUENCY

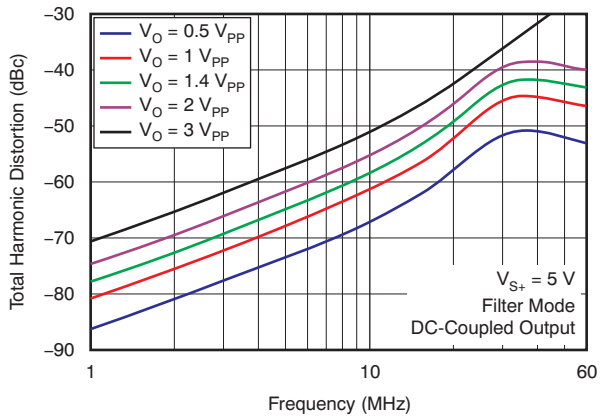


Figure 75.

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APPLICATION INFORMATION

The THS7364 is targeted for six-channel video output applications that require three standard-definition (SD) video output buffers and three full-high definition (FHD) video output buffers. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7364. Built on the revolutionary, complementary Silicon Germanium (SiGe) BiCom3X process, the THS7364 incorporates many features not typically found in integrated video parts while consuming very low power. The THS7364 includes the following features:

- Single-supply 2.7-V to 5-V operation with low total quiescent current of 23.4 mA at 3.3 V and 24.5 mA at 5 V
- Disable mode allows for shutting down individual SD/FHD blocks of amplifiers to save system power in power-sensitive applications
- Input configuration accepting dc + level shift, ac sync-tip clamp, or ac-bias
  - AC-biasing is allowed with the use of external pull-up resistors to the positive power supply
- Sixth-order, low-pass filter for DAC reconstruction or ADC image rejection:
  - 9.5 MHz for NTSC, PAL, SECAM, composite video (CVBS), S-Video Y'/C', 480i/576i, Y'/P'$_B$/P'$_R$, and G'B'R' (R'G'B') signals
  - 72-MHz for 1080p60 Y'/P' $_B$/P'$_R$ or G'B'R' signals; also allows up to QXGA (1600 × 1200 at 60 Hz) R'G'B' video in filter bypass mode
- Individually-controlled Bypass mode bypasses the low-pass filters for each SD/FHD block of amplifiers
  - SD bypass mode features 150-MHz and 100-V/μs performance
  - FHD bypass mode features 350-MHz and 500-V/μs performance
- Individually-controlled Disable mode shuts down all amplifiers in each SD/FHD block to reduce quiescent current to 0.1 μA
- Internally-fixed gain of 2-V/V (+6-dB) buffer that can drive two video lines with dc-coupling or traditional ac-coupling
- Flow-through configuration using a TSSOP-20 package that complies with the latest lead-free (RoHS-compatible) and green manufacturing requirements

OPERATING VOLTAGE

The THS7364 is designed to operate from 2.7 V to 5 V over the –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high-quality, low-temperature coefficient capacitors. The design of the THS7364 allows operation down to 2.6 V, but it is recommended to use at least a 3-V supply to ensure that no issues arise with headroom or clipping with 100% color-saturated CVBS signals. If only 75% color saturated CVBS is supported, then the output voltage requirements are reduced to 2 V_{PP} on the output, allowing a 2.7-V supply to be utilized without issues.

A 0.1-μF to 0.01-μF capacitor should be placed as close as possible to the power-supply pins. Failure to do so may result in the THS7364 outputs ringing or oscillating. Additionally, a large capacitor (such as 22 μF to 100 μF) should be placed on the power-supply line to minimize interference with 50-/60-Hz line frequencies.

INPUT VOLTAGE

The THS7364 input range allows for an input signal range from –0.2 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 2 V/V (+6 dB) and the internal input level shift of 150 mV (typical), the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.2 V to 3.5 V. However, because of the gain and level shift, the linear output range limits the allowable linear input range to approximately –0.1 V to 2.3 V.

INPUT OVERVOLTAGE PROTECTION

The THS7364 is built using a very high-speed, complementary, bipolar, and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 76.

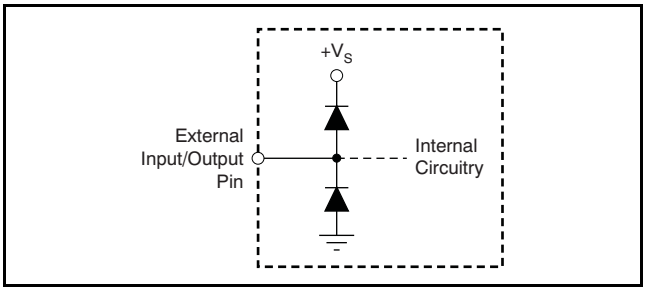


Figure 76. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

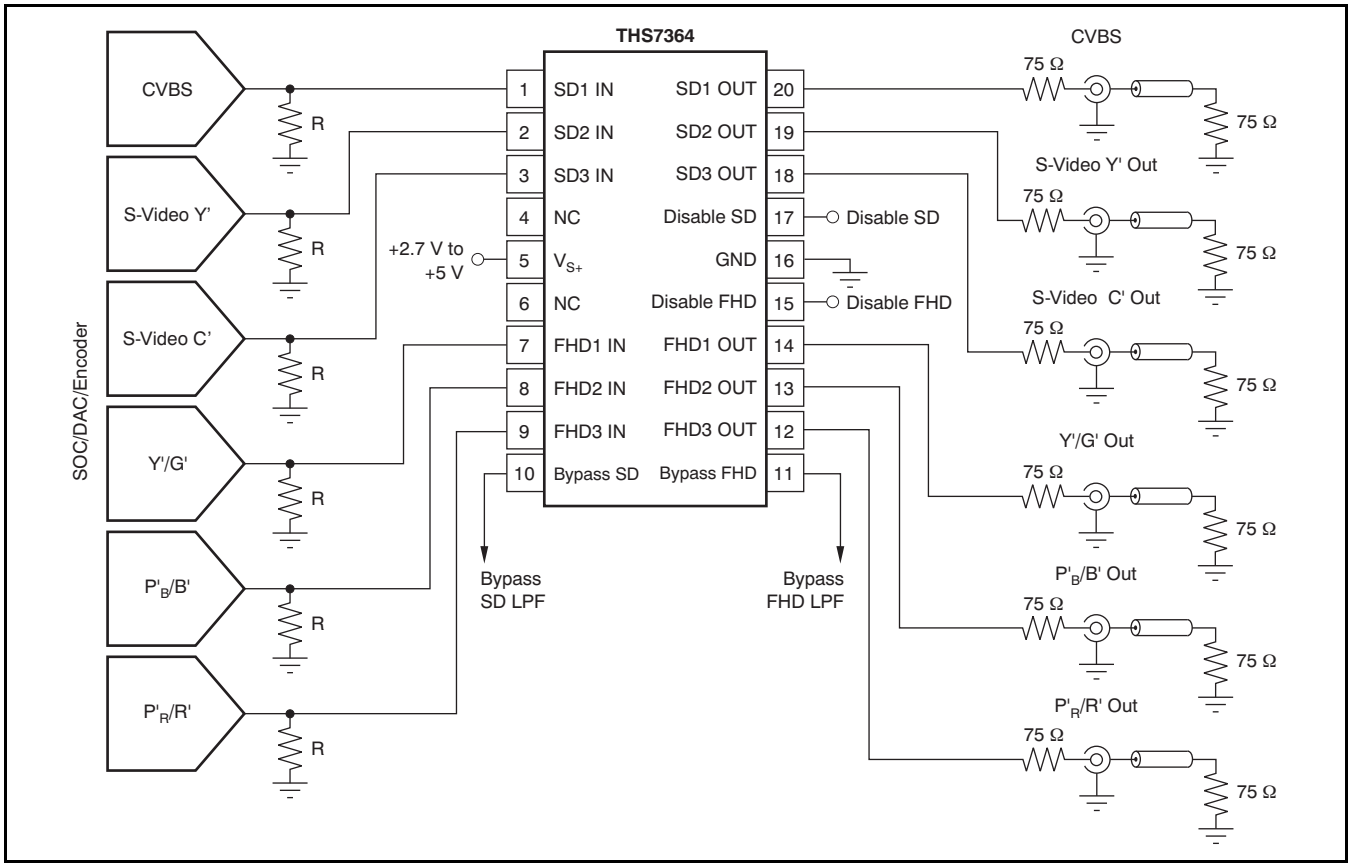
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TYPICAL CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit using the THS7364 as a video buffer is shown in Figure 77. It shows a DAC or encoder driving the input channels of the THS7364. One channel is a CVBS connection while two other channels are for the S-Video Y'/C' signals of an SD video system. These signals can be NTSC, PAL, or SECAM signals. The other three channels are the component video Y'/P'$_B$/P'$_R$ (sometimes labeled Y'U'V' or incorrectly labeled Y'/C'$_B$/C'$_R$) signals. These signals are typically 480i, 576i, 480p, 576p, 720p, 1080i, or up to 1080p60 signals. Because the filters can be bypassed, other formats such as R'G'B' video up to QXGA or UWXGA can also be supported with the THS7364.

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (*Y*) term. This usage accounts for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, *gamma*, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

This rationale is also used for the chroma (*C'*) term. Chroma is derived from the nonlinear R'G'B' terms and, thus, it is nonlinear. Chominance (*C*) is derived from linear RGB, giving the difference between chroma (C') and chrominance (C). The color difference signals (P'$_B$/P'$_R$/U'/V') are also referenced in this manner to denote the nonlinear (gamma corrected) signals.



(1) **Figure 77. Typical Six-Channel System Inputs from DC-Coupled Encoder/DAC with DC-Coupled Line Driving**

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R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The Society of Motion Picture and Television Engineers (SMPTE) component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This practice is consistent with the Y'/P'$_B$/P'$_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Because the blue color difference channel (P'$_B$) is next and the red color difference channel (P'$_R$) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

INPUT MODE OF OPERATION: DC

The inputs to the THS7364 allow for both ac- and dc-coupled inputs. Many DACs or video encoders can be dc-connected to the THS7364. One of the drawbacks to dc-coupling arises when 0 V is applied to the input. Although the input of the THS7364 allows for a 0-V input signal without issue, the output swing of a traditional amplifier cannot yield a 0-V signal, resulting in possible clipping. This limitation is true for any single-supply amplifier because of the characteristics of the output transistors. Neither CMOS nor bipolar transistors can achieve 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the video signal receiver uses an automatic gain control (AGC) loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This correction may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control; reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation or clipping problems, the THS7364 has a 150-mV input level shift feature. This feature takes the input voltage and adds an internal +150-mV shift to the signal. Because the THS7364 also has a gain of 6 dB (2 V/V), the resulting output with a 0-V applied input signal is approximately 300 mV. The THS7364 rail-to-rail output stage can create this output level while connected to a typical video load. This configuration ensures that no saturation or clipping of the sync signals occur. This shift is constant, regardless of the input signal. For example, if a 1-V input is applied, the output is 2.3 V.

Because the internal gain is fixed at +6 dB, the gain dictates what the allowable linear input voltage range can be without clipping concerns. For example, if the power supply is set to 3 V, the maximum output is approximately 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ([2.9 V/2] – 0.15 V) = 1.3 V. This range is valid for up to the maximum recommended 5-V power supply that allows approximately a ([4.9 V/2] – 0.15 V) = 2.3 V input range while avoiding clipping on the output.

The input impedance of the THS7364 in this mode of operation is dictated by the internal, 800-kΩ pull-down resistor, as shown in Figure 78. Note that the internal voltage shift does not appear at the input pin; it only shows at the output pin.

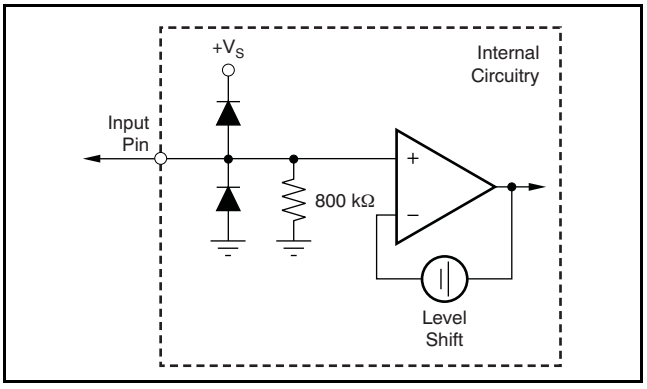


Figure 78. Equivalent DC Input Mode Circuit

INPUT MODE OF OPERATION: AC SYNC TIP CLAMP

Some video DACs or encoders are not referenced to ground but rather to the positive power supply. The resulting video signals are generally at too great a voltage for a dc-coupled video buffer to function properly. To account for this scenario, the THS7364 incorporates a sync-tip clamp circuit. This function requires a capacitor (nominally 0.1 μF) to be in series with the input. Although the term *sync-tip-clamp* is used throughout this document, it should be noted that the THS7364 would probably be better termed as a *dc restoration circuit* based on how this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function.

The input to the THS7364 has an internal control loop that sets the lowest input applied voltage to clamp at ground (0 V). By setting the reference at 0 V, the THS7364 allows a dc-coupled input to also function. Therefore, the sync-tip-clamp (STC) is considered transparent because it does not operate unless the input signal goes below ground. The signal then goes through the same 150-mV level shifter, resulting in an output voltage low level of 300 mV. If the input signal tries to go below 0 V, the THS7364 internal control loop sources up to 6 mA of current to increase the input voltage level on the THS7364 input side of the coupling capacitor. As soon as the voltage goes above the 0-V level, the loop stops sourcing current and becomes very high impedance.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot—common in VCR signals, noise, DAC overshoot, or reflections found in poor printed circuit board (PCB) layouts. Ideally, the STC should not react to the overshoot voltage of the input signal. Otherwise, this response could result in clipping on the rest of the video signal because it may raise the bias voltage too much.

To help minimize this input signal overshoot problem, the control loop in the THS7364 has an internal low-pass filter, as shown in Figure 79. This filter reduces the response time of the STC circuit. This delay is a function of how far the voltage is below ground, but in general it is approximately a 400-ns delay for the SD channel filters and approximately a 150-ns delay for the FHD filters. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage but rather the flat portion of the sync signal.

As a result of this delay, sync may have an apparent voltage shift. The amount of shift depends on the amount of droop in the signal as dictated by the input capacitor and the STC current flow. Because sync is used primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems.

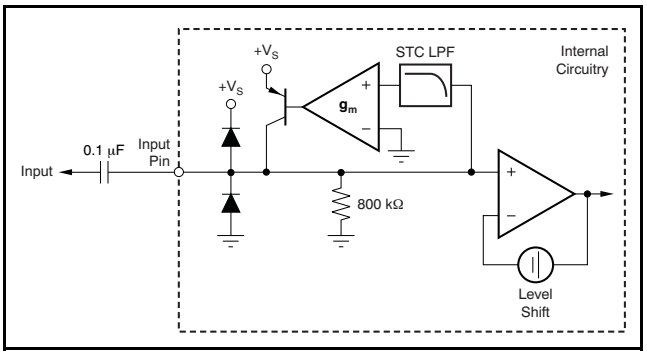


Figure 79. Equivalent AC Sync-Tip-Clamp Input Circuit

While this feature may not fully eliminate overshoot issues on the input signal, in cases of extreme overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (for example, 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage that appears at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This architecture helps ensure a very robust STC system.

When the ac STC operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 0-V clamp level, the internal loop of the THS7364 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 0-V reference level increases, the amount of source current increases proportionally—supplying up to 6 mA of current. Thus, the time to re-establish the proper STC voltage can be very fast. If the difference is very small, then the source current is also very small to account for minor voltage droop.

However, what happens if the input signal goes above the 0-V input level? The problem is the video signal is always above this level and must not be altered in any way. Thus, if the sync level of the input signal is above this 0-V level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 0-V level.

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This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This effect is often seen by looking at the tilt (droop) of a constant luma signal being applied and the resulting output level. The associated change in luma level from the beginning and end of the video line is the amount of line tilt (droop).

If the discharge current is very small, the amount of tilt is very low, which is a generally a good thing. However, the amount of time for the system to capture the sync signal could be too long. This effect is also termed *hum rejection*. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

To allow for both dc- and ac-coupling in the same part, the THS7364 incorporates an 800-kΩ resistor to ground. Although a true constant current sink is preferred over a resistor, there can be issues when the voltage is near ground. This configuration can cause the current sink transistor to saturate and cause potential problems with the signal. The 800-kΩ resistor is large enough to not impact a dc-coupled DAC termination. For discharging an ac-coupled source, Ohm's Law is used. If the video signal is 1 V, then there is 1 V/800 kΩ = 1.25-μA of discharge current. If more hum rejection is desired or there is a loss of sync occurring, then simply decrease the 0.1-μF input coupling capacitor. A decrease from 0.1 μF to 0.047 μF increases the hum rejection by a factor of 2.1. Alternatively, an external pull-down resistor to ground may be added that decreases the overall resistance and ultimately increases the discharge current.

To ensure proper stability of the ac STC control loop, the source impedance must be less than 1-kΩ with the input capacitor in place. Otherwise, there is a possibility of the control loop ringing, which may appear on the output of the THS7364. Because most DACs or encoders use resistors to establish the voltage, which are typically less than 300-Ω, meeting the less than 1-kΩ requirement is easily done. However, if the source impedance looking from the THS7364 input perspective is very high, then simply adding a 1-kΩ resistor to GND ensures proper operation of the THS7364.

INPUT MODE OF OPERATION: AC BIAS

Sync-tip clamps work very well for signals that have horizontal and/or vertical syncs associated with them; however, some video signals do not have a sync embedded within the signal. If ac-coupling of these signals is desired, then a dc bias is required to properly set the dc operating point within the THS7364. This function is easily accomplished with the THS7364 by simply adding an external pull-up resistor to the positive power supply, as shown in Figure 80.

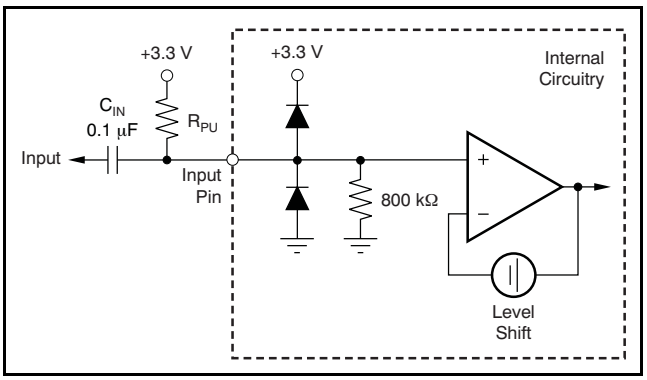


Figure 80. AC-Bias Input Mode Circuit Configuration

The dc voltage appearing at the input pin is equal to Equation 1:

$$V_{DC} = V_S \left(\frac{800\ k\Omega}{800\ k\Omega + R_{PU}} \right) \quad (1)$$

The THS7364 allowable input range is approximately 0 V to (V_{S+} – 1.5 V), allowing for a very wide input voltage range. As such, the input dc bias point is very flexible, with the output dc bias point being the primary factor. For example, if the output dc bias point is desired to be 1.6 V on a 3.3-V supply, then the input dc bias point should be (1.6 V – 300 mV)/2 = 0.65 V. Thus, the pull-up resistor calculates to approximately 3.3 MΩ, resulting in 0.644 V. If the output dc-bias point is desired to be 1.6 V with a 5-V power supply, then the pull-up resistor calculates to approximately 5.36 MΩ.

Keep in mind that the internal 800-kΩ resistor has approximately a ±20% variance. As such, the calculations should take this variance into account. For the 0.644-V example above, using an ideal 3.3-MΩ resistor, the input dc bias voltage is approximately 0.644 V ± 0.1 V.

The value of the output bias voltage is very flexible and is left to each individual design. It is important to ensure that the signal does not clip or saturate the video signal. Thus, it is recommended to ensure the output bias voltage is between 0.9 V and (V_{S+} – 1 V). For 100% color saturated CVBS or signals with Macrovision®, the CVBS signal can reach up to 1.23 V_{PP} at the input, or 2.46 V_{PP} at the output of the THS7364. In contrast, other signals are typically 1 V_{PP} or 0.7 V_{PP} at the input which translate to an output voltage of 2 V_{PP} or 1.4 V_{PP}. The output bias voltage must account for a worst-case situation, depending on the signals involved.

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One other issue that must be taken into account is the dc-bias point is a function of the power supply. As such, there is an impact on system PSRR. To help reduce this impact, the input capacitor combines with the pull-up resistance to function as a low-pass filter. Additionally, the time to charge the capacitor to the final dc bias point is a function of the pull-up resistor and the input capacitor size. Lastly, the input capacitor forms a high-pass filter with the parallel impedance of the pull-up resistor and the 800-kΩ resistor. In general, it is good to have this high-pass filter at approximately 3 Hz to minimize any potential droop on a P'_B or P'_R signal. A 0.1-μF input capacitor with a 3.3-MΩ pull-up resistor equates to approximately a 2.5-Hz high-pass corner frequency.

This mode of operation is recommended for use with chroma (C'), P'_B, P'_R, U', and V' signals. This method can also be used with sync signals if desired. The benefit of using the STC function over the ac-bias configuration on embedded sync signals is that the STC maintains a constant *back-porch* voltage as opposed to a back-porch voltage that fluctuates depending on the video content. Because the high-pass corner frequency is a very low 2.5 Hz, the impact on the video signal is negligible relative to the STC configuration.

One question may arise over the P'_B and P'_R channels. For 480i, 576i, 480p, and 576p signals, a sync may or may not be present. If no sync exists within the signal, then it is obvious that ac-bias is the preferred method of ac-coupling the signal.

For 720p, 1080i, and 1080p signals, or for the the 480i, 576i, 480p, and 576p signals with sync present on the P'_B and P'_R channels, the lowest voltage of the sync is –300 mV below the midpoint reference voltage of 0 V. The P'_B and P'_R signals allow a signal to be as low as –350 mV below the midpoint reference voltage of 0 V. This allowance corresponds to 100% yellow for P'_B signal or 100% cyan for P'_R signal . Because the P'_B and P'_R signal voltage can be lower than the sync voltage, there exists a potential for clipping of the signal for a short period of time if the signals drop below the sync voltage.

The THS7364 does include a 150-mV input level shift, or 300 mV at the output, that should mitigate any clipping issues. For example, if a STC is used, then the bottom of the sync is 300 mV at the output. If the signal does go the lowest level, or 50 mV lower than the sync at the input, then the instantaneous output is (–50 mV + 150 mV) × 2 = 200 mV at the output.

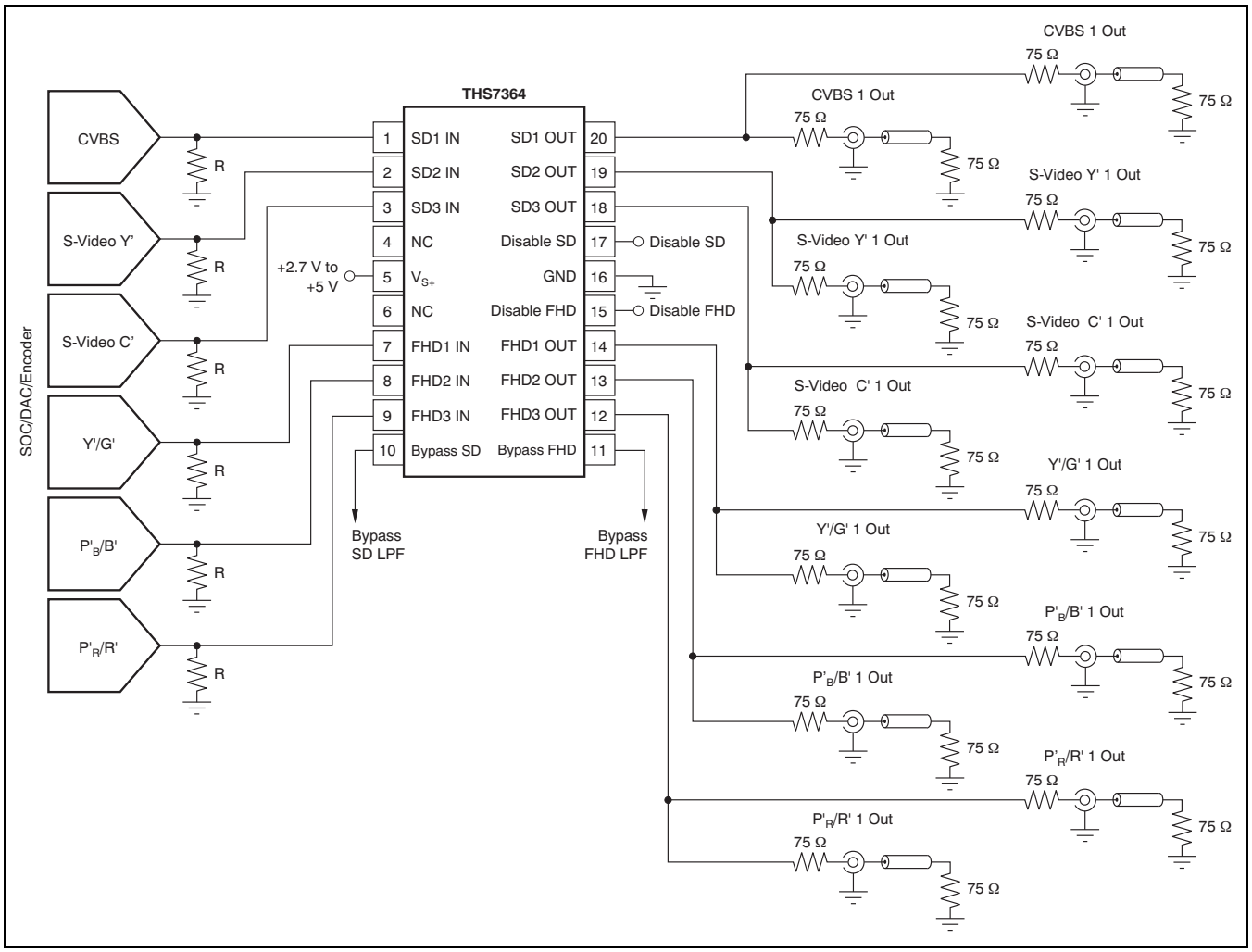
Another potential risk is that if this signal (100% yellow for P'_B or 100% cyan for P'_R) exists for several pixels, then the STC circuit engages to raise the voltage back to 0 V at the input. This function can cause a 50-mV level shift at the input midway through the active video signal. This effect is undesirable and can cause errors in the decoding of the signal.

It is therefore recommended to use ac bias mode for component P'_B and P'_R signals when ac-coupling is desired.

OUTPUT MODE OF OPERATION: DC-COUPLED

The THS7364 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This design offers the best line tilt and field tilt (droop) performance because no ac-coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt as a result of the input ac-coupling continues to be seen on the output, regardless of the output coupling. The 80-mA output current drive capability of the THS7364 is designed to drive two video lines simultaneously—essentially, a 75-Ω load—while keeping the output dynamic range as wide as possible. Figure 81 shows the THS7364 driving two video lines while keeping the output dc-coupled.

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(1) **Figure 81. Typical Six-Channel System with DC-Coupled Line Driving and Two Outputs Per Channel**

One concern of dc-coupling, however, arises if the line is terminated to ground. If the ac-bias input configuration is used, the output of the THS7364 has a dc bias on the output, such as 1.6 V. With two lines terminated to ground, this configuration allows a dc current path to flow, such as 1.6 V/75-Ω = 21.3 mA. The result of this configuration is a slightly decreased high output voltage swing and an increase in power dissipation of the THS7364. While the THS7364 was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer. Using a 5-V supply, this configuration can result in an additional dc power dissipation of (5 V – 1.6 V) × 21.3 mA = 72.5 mW per channel. With a 3.3-V supply, this dissipation reduces to 36.2 mW per channel. The overall low quiescent current of the THS7364 design minimizes potential thermal issues even when using the TSSOP package at high ambient temperatures, but power and thermal analysis should always be examined in any system to ensure that no issues arise. Be sure to use RMS power and not instantaneous power when evaluating the thermal performance.

Note that the THS7364 can drive the line with dc-coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output (typically 75 Ω). This requirement helps isolate capacitive loading effects from the THS7364 output. Failure to isolate capacitive loads may result in instabilities with the output buffer, potentially causing ringing or oscillations to appear. The stray capacitance appearing directly at the THS7364 output pins should be kept below 20 pF for the fixed SD filter channels and below 15 pF for the FHD filter channels. One way to help ensure this condition is satisfied is to make sure the 75-Ω source resistor is placed within 0.5 inches, or 12.7 mm, of the THS7364 output pin. If a large ac-coupling capacitor is used, the capacitor should be placed after this resistor.

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There are many reasons dc-coupling is desirable, including reduced costs, PCB area, and no line tilt. A common question is whether or not there are any drawbacks to using dc-coupling. There are some potential issues that must be examined, such as the dc current bias as discussed above. Another potential risk is whether this configuration meets industry standards. EIA/CEA-770 stipulates that the back-porch shall be 0 V ± 1 V as measured at the receiver. With a double-terminated load system, this requirement implies a 0 V ± 2 V level at the video amplifier output. The THS7364 can easily meet this requirement without issue. However, in Japan, the EIAJ CP-1203 specification stipulates a 0 V ± 0.1 V level with no signal. This requirement can be met with the THS7364 in shutdown mode, but while active it cannot meet this specification without output ac-coupling. AC-coupling the output essentially ensures that the video signal works with any system and any specification. For many modern systems, however, dc-coupling can satisfy most needs.

OUTPUT MODE OF OPERATION: AC-COUPLED

A very common method of coupling the video signal to the line is with a large capacitor. This capacitor is typically between 220 μF and 1000 μF, although 470 μF is very typical. The value of this capacitor must be large enough to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document. AC-coupling is performed for several reasons, but the most common is to ensure full interoperability with the receiving video system. This approach ensures that regardless of the reference dc voltage used on the transmitting side, the receiving side re-establishes the dc reference voltage to its own requirements.

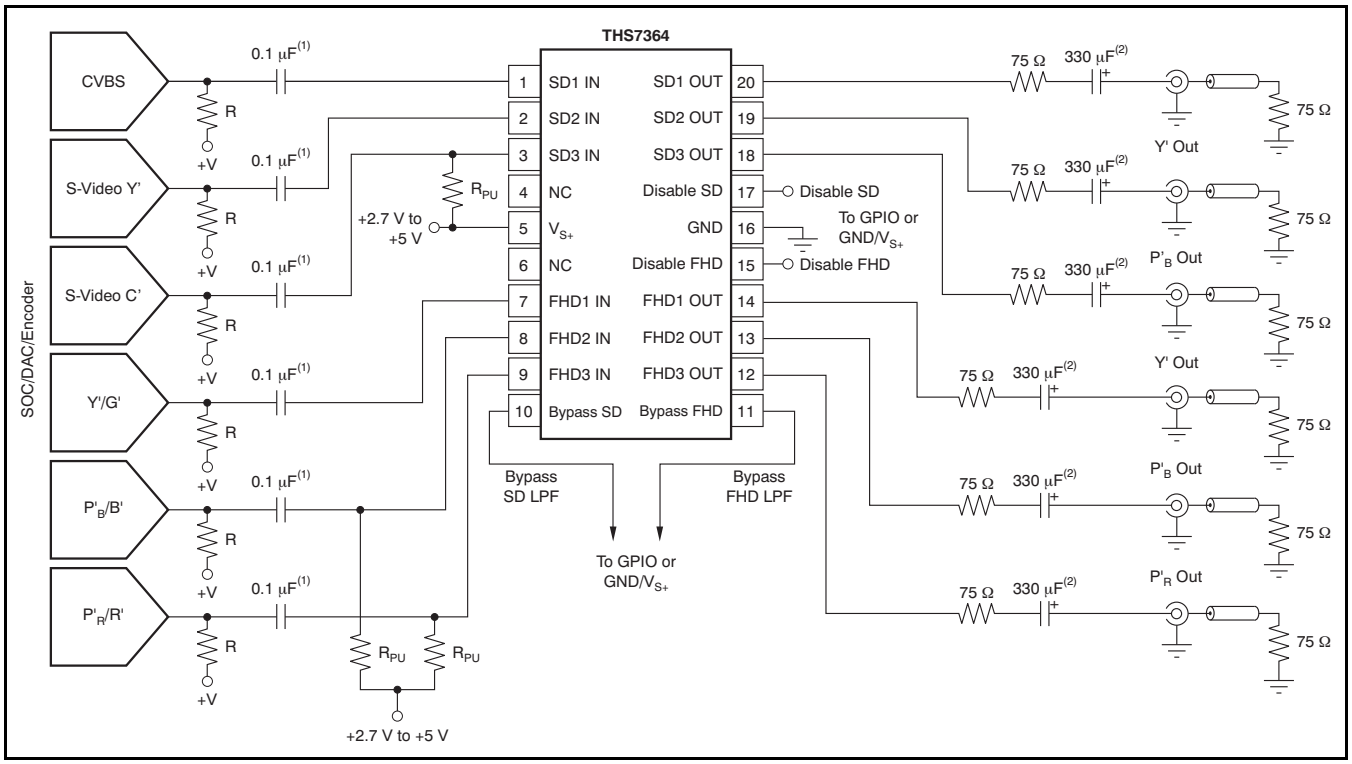
In the same way as the dc output mode of operation discussed previously, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. This 75-Ω resistor should be placed next to the THS7364 output to minimize capacitive loading effects. If two lines are to be driven, it is best to have each line use its own capacitor and resistor rather than sharing these components. This configuration helps ensure line-to-line dc isolation and eliminates the potential problems as described previously. Using a single, 1000-μF capacitor for two lines is permissible, but there is a chance for interference between the two receivers.

Lastly, because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-μF to 0.01-μF capacitor in parallel with the large 220-μF to 1000-μF capacitor. These large value capacitors are most commonly aluminum electrolytic. It is well-known that these capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-μF to 0.01-μF capacitors help pass these high-frequency signals (greater than 1 MHz) with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system is not required to go as low (or as high of a frequency) as the luma channels. Thus, the capacitor values of the chroma line(s) can be smaller, such as 0.1 μF.

Figure 82 shows a typical configuration where the input is ac-coupled and the output is also ac-coupled. AC-coupled inputs are generally required when current-sink DACs are used or the input is connected to an unknown source, such as when the THS7364 is used as an input device.

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(1) AC-coupled input is shown in this example. DC-coupling is also allowed as long as the DAC output voltage is within the allowable linear input and output voltage range of the THS7364. To apply dc-coupling, remove the 0.1-µF input capacitors and the R_{PU} pull-up resistors along with connecting the DAC termination resistors (R) to ground.

(2) This example shows an ac-coupled output. DC-coupling is also allowed by simply removing these capacitors.

Figure 82. Typical AC Input System Driving AC-Coupled Video Lines

LOW-PASS FILTER

Each channel of the THS7364 incorporates a sixth-order, low-pass filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems because of aliasing of the ADC in the receiver. Another benefit of the filter is to smooth out aberrations in the signal that some DACs can have if the internal filtering is not very good. This benefit helps with picture quality and ensures that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem with this characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of the very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. Considering this delay with the fact that video can go from a white pixel to a black pixel over and over again, it is easy to see that ringing can occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is an acceptable compromise for both attenuation and group delay.

The THS7364 SD filters have a nominal corner (–3 dB) frequency at 9.5 MHz and a –1-dB passband typically at 8.2 MHz. This 9.5-MHz filter is ideal for SD NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'C'), 480i/576i Y'/P'_B/P'_R, Y'U'V', broadcast G'B'R' signals, and computer R'G'B' video signals. The 9.5-MHz, –3-dB corner frequency was designed to

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achieve
54 dB of attenuation at 27 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as a result of aliasing effects of an ADC found in a receiver.

The THS7364 FHD filters have a nominal corner (–3 dB) frequency at 72 MHz and a –1-dB passband typically at 60 MHz. This 72-MHz filter is ideal for 1080p50 or 1080p60 component video. It is also ideal for oversampling systems where the video DAC upsamples the video signal such as 720p or 1080i upsampled to 148.5 MHz. The benefit is an extremely flat passband response along with almost no group delay within the HD video passband. In bypass mode, these filters can also be used for some computer R'G'B' video signals including VGA, SVGA, XGA, SXGA, and QXGA.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 27 MHz for traditional SD DACs); they continue around the sampling frequencies of 2x f_S, 3x f_S, 4x f_S, and so on (that is, 54 MHz, 81 MHz, 108 MHz, etc.). Because of these multiple images, an ADC can fold down into the baseband signal, meaning that the low-pass filter must also eliminate these higher-order images. The THS7364 filters are Butterworth filters and, as such, do not *bounce* at higher frequencies, thus maintaining good attenuation performance.

The filter frequencies were chosen to account for process variations in the THS7364. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering is sufficient to meet the system demands. Thus, the selection of the filter frequencies was not arbitrarily selected and is a good compromise that should meet the demands of most systems.

One of the features of the THS7364 is that these filters can be bypassed. Bypassing the SD filters results in an amplifier with 150-MHz bandwidth and 100-V/μs slew rate. This configuration can be helpful when diagnosing potential system issues or when simply wishing to pass higher frequency signals through the system.

Bypassing the FHD filters results in a amplifier supporting 350-MHz bandwidth and 500-V/μs slew rate. This configuration supports computer R'G'B' signals up to UWXGA resolution.

BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system, such as the THS7364, over a passive system are PCB area and filter variations. The small TSSOP-20 package for six video channels is much smaller over a passive RLC network, especially a six-pole passive network. Additionally, consider that inductors have at best ±10% tolerances (normally, ±15% to ±20% is common) and capacitors typically have ±10% tolerances. Using a Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay have wide variations. These variances can lead to potential performance and quality issues in mass-production environments. The THS7364 solves most of these problems with the corner frequency being essentially the only variable.

Another concern about passive filters is the use of inductors. Inductors are magnetic components, and are therefore susceptible to electromagnetic coupling/interference (EMC/EMI). Some common coupling can occur because of other video channels nearby using inductors for filtering, or it can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation and can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature changes. To minimize temperature effects, the THS7364 uses low-temperature coefficient resistors and high-quality, low-temperature coefficient capacitors found in the BiCom3X process. These filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This approach maintains a low channel-to-channel time delay that is required for proper video signal performance.

Another benefit of the THS7364 over a passive RLC filter is the input and output impedance. The input impedance presented to the DAC varies significantly, from 35 Ω to over 1.5 kΩ with a passive network, and may cause voltage variations over frequency. The THS7364 input impedance is 800 kΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impact the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7364.

On the output side of the filter, a passive filter again has a large impedance variation over frequency. The EIA/CEA-770 specifications require the return loss to be at least 25 dB over the video frequency range of usage. For a video system, this requirement implies the source impedance (which includes the source,

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series resistor, and the filter) must be better than 75 Ω, +/-9 Ω. The THS7364 is an operational amplifier that approximates an ideal voltage source, which is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss meeting EIA/CEA specifications, this output impedance must maintain a 75-Ω impedance. A wide impedance variation of a passive filter cannot ensure this level of performance. On the other hand, the THS7364 has approximately 0.9 Ω of output impedance, or a return loss of 44 dB, at 6.75 MHz for the SD filters and approximately 9 Ω of output impedance, or a return loss of 25 dB, at 60 MHz for the FHD filters. Thus, the system is matched significantly better with a THS7364 compared to a passive filter.

One final benefit of the THS7364 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load: the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This requirement forces the DAC to drive at least 1.25 V_P (100% saturation CVBS)/37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when six channels are being driven. Using the THS7364 with a high input impedance and the capability to drive up to two video lines per channel can reduce DAC power dissipation significantly. This outcome is possible because the resistance that the DAC drives can be substantially increased. It is common to set this resistance in a DAC by a current-setting resistor on the DAC itself. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving significant amounts of power. For example, a 3.3-V, six-channel DAC dissipates 660 mW alone for the steering current capability (six channels × 33.3 mA × 3.3 V) if it must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 82 mW (six channels × 4.16 mA × 3.3 V).

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EVALUATION MODULE

To evaluate the THS7364, an evaluation module (EVM) is available. The THS7364EVM allows for testing the THS7364 in many different configurations. Inputs and outputs include BNC connectors and RCA connectors commonly found in video systems, along with 75-Ω input termination resistors, 75-Ω series source termination resistors, and 75-Ω characteristic impedance traces. Several unpopulated component pads are found on the EVM to allow for different input and output configurations as dictated by the user. This EVM is designed to be used with a single supply from 2.6 V up to 5 V.

The EVM default input configuration sets all channels for dc input coupling. The input signal must be within 0 V to approximately 1.4 V for proper operation. Failure to be within this range saturates and/or clips the output signal. If the input range is beyond this, if the signal voltage is unknown, or if coming from a current sink DAC, then ac input configuration is desired. This option is easily accomplished with the EVM by simply replacing the Z_1 through Z_6 0-Ω resistors with 0.1-μF capacitors.

For an ac-coupled input and sync-tip clamp (STC) functionality commonly used for CVBS, s-video Y', component Y' signals, and R'G'B' signals, no other changes are needed. However, if a bias voltage is needed after the input capacitor which is commonly needed for s-video C', component $P'_{B,}$ and P'_R, then a pull-up resistor should be added to the signal on the EVM. This configuration is easily achieved by simply adding a resistor to any of the following resistor pads; RX7 to RX12. A common value to use is 3.3 MΩ. Note that even signals with embedded sync can also use bias mode if desired.

The EVM default output configuration sets all channels for ac output coupling. The 470-μF and 0.1-μF capacitors work well for most ac-coupled systems. However, if dc-coupled output is desired, then replacing the 0.1-μF capacitors (C20, C22, C24, C26, C28, and/or C30) with 0-Ω resistors works well. Removing the 470-μF capacitors is optional, but removing them from the EVM eliminates a few picofarads of stray capacitance on each signal path which may be desirable.

The THS7364 incorporates an easy method to configure the bypass modes and the disable modes. The use of JP4 controls the SD channels disable feature; JP6 controls the FHD channels disable feature; JP3 controls the SD channels filter/bypass mode; and JP5 controls the FHD channels filter/bypass mode.

Connection of JP4 and JP6 to GND applies 0 V to the disable pins and the THS7364 operates normally. Moving JP4 to $+V_S$ causes the THS7364 SD channels to be in disable mode, while moving JP6 to $+V_S$ causes the THS7364 FHD channels to be in disable mode.

Connection of JP3 to GND places the THS7364 SD channels in filter mode while moving JP3 to $+V_S$ places the THS7364 SD channels in bypass mode. Connection of JP5 to GND places the THS7364 FHD channels in filter mode while moving JP5 to $+V_S$ places the THS7364 FHD channels in bypass mode.

Figure 83 shows the THS7364EVM schematic. Figure 84 and Figure 85 illustrate the two layers of the EVM PCB, incorporating standard high-speed layout practices. Table 5 lists the bill of materials as the board comes supplied from Texas Instruments.

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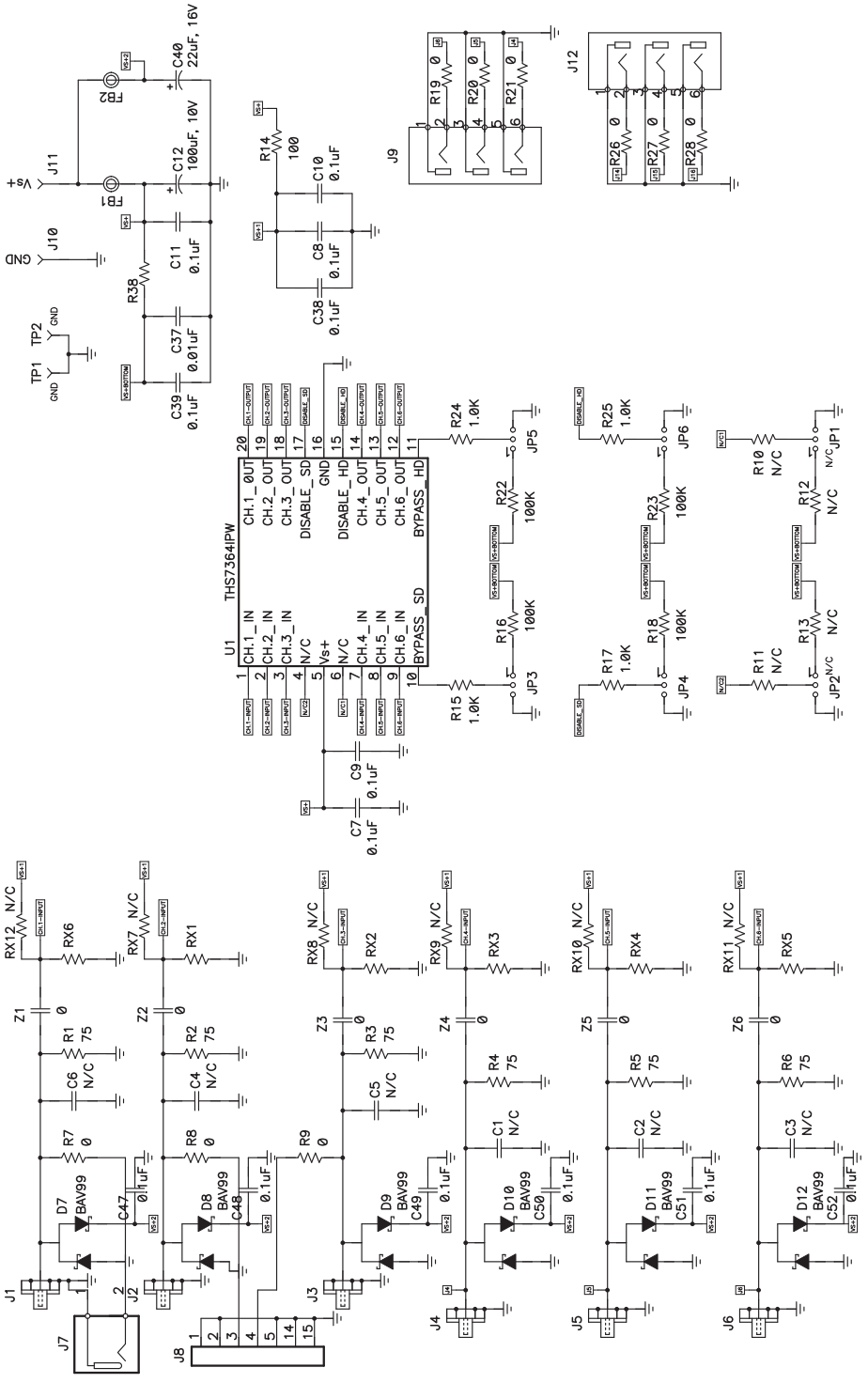


Figure 83. THS7364EVM Schematic

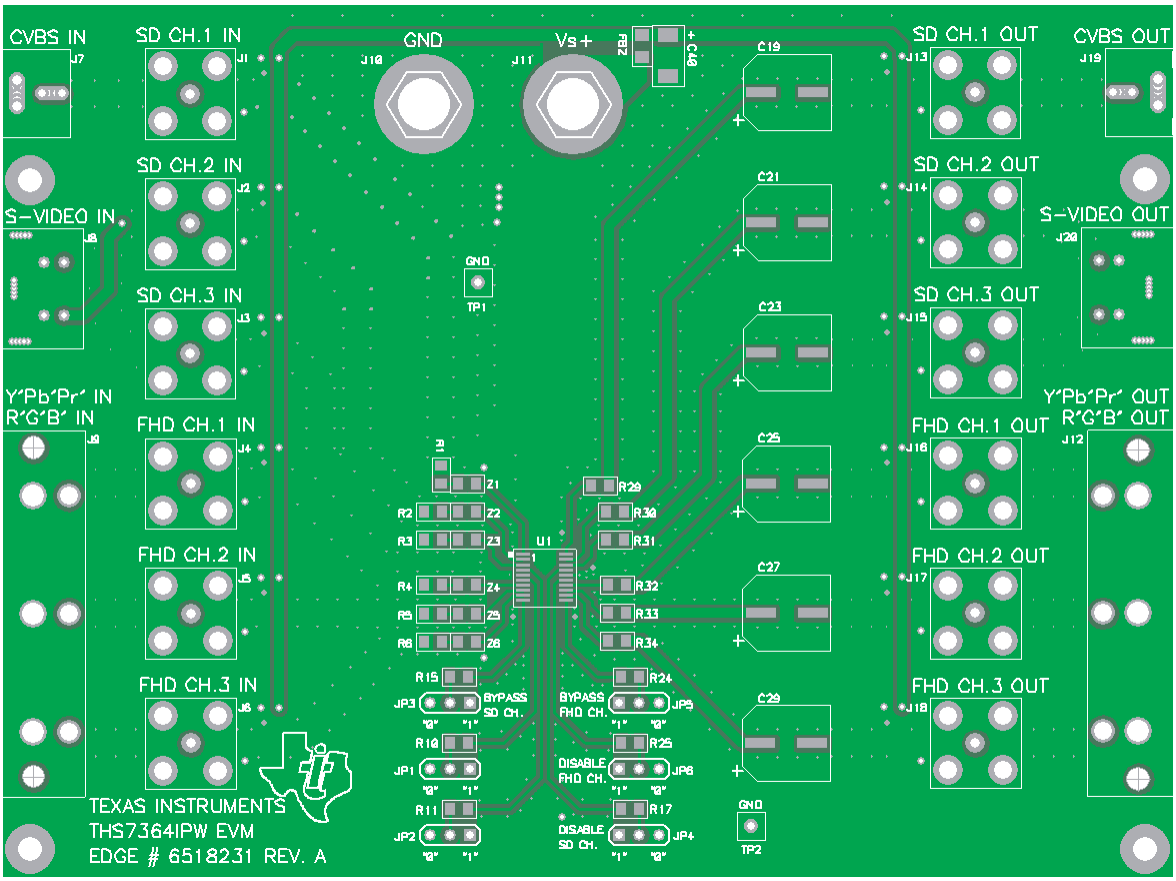


Figure 84. THS7364EVM PCB Top Layer

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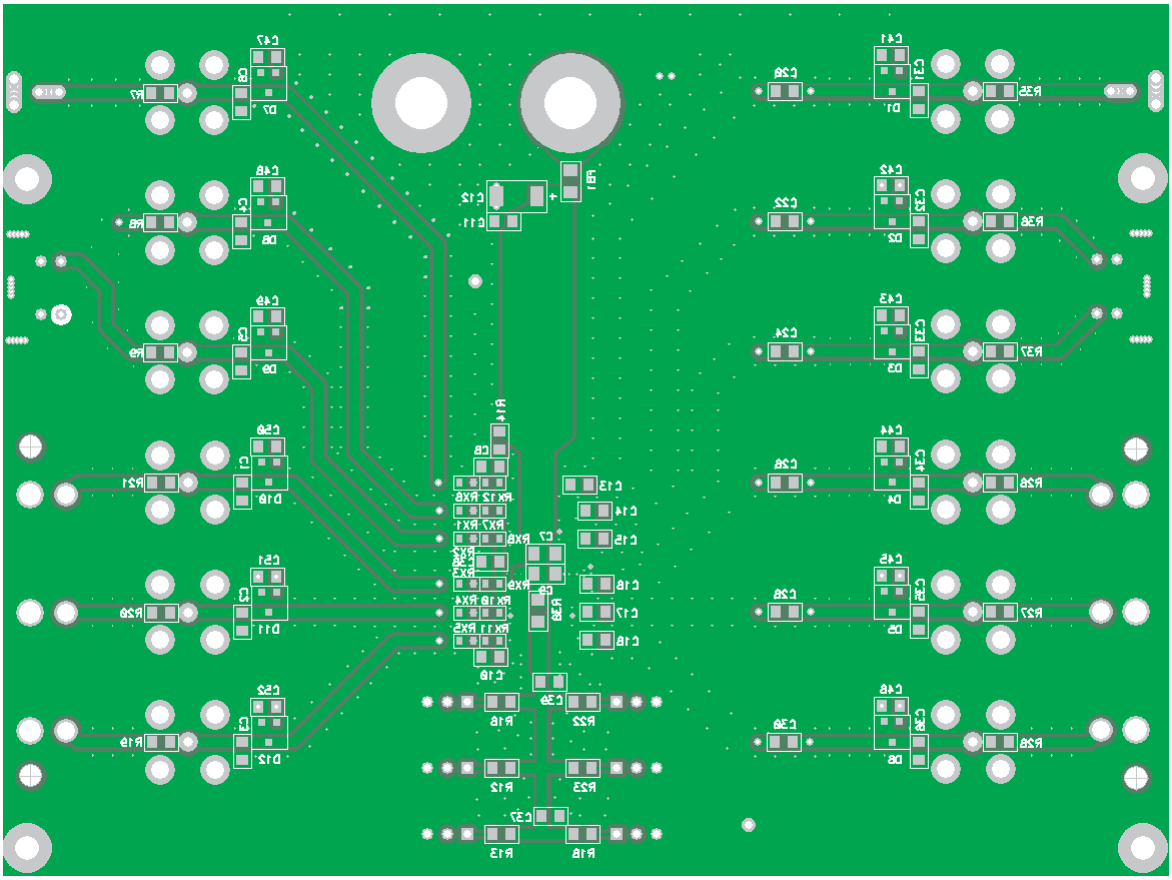


Figure 85. THS7364EVM PCB Bottom Layer

THS7364EVM Bill of Materials

Table 5. THS7364EVM Parts List

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1, FB2	2	Bead, ferrite, 2.5 A, 330 Ω	805	(TDK) MPZ2012S331A	(DIGI-KEY) 445-1569-1-ND
2	C12	1	Capacitor, 100 µF, tantalum, 10 V, 10%, low ESR	C	(AVX) TPSC107K010R0100	(DIGI-KEY) 478-1765-1-ND
3	C40	1	Capacitor, 22 µF, tantalum, 16 V, 10%, low ESR	C	(AVX) TPSC226K016R0375	(DIGI-KEY) 478-1767-1-ND
4	C1-C6, C13-C18, C3-C36	18	OPEN	0805	—	—
5	C37	1	Capacitor, 0.01 µF, ceramic, 100 V, X7R	0805	(AVX) 08051C103KAT2A	(DIGI-KEY) 478-1358-1-ND
6	C8, C10, C11, C20, C22, C24, C26, C28, C30, C38, C39, C41-C52	23	Capacitor, 0.1 µF, ceramic, 50 V, X7R	0805	(AVX) 08055C104KAT2A	(DIGI-KEY) 478-1395-1-ND
7	C9	1	Capacitor, 0.1 µF, ceramic, 50 V, X7R	1206	(AVX) 12065C104KAT2A	(DIGI-KEY) 478-1556-1-ND
8	C7	1	Capacitor, 3.3 µF, ceramic, 25 V, X7R	1206	(TDK) C3216X7R1E335K	(DIGI-KEY) 445-4029-1-ND
9	C19, C21, C23, C25, C27, C29	6	Capacitor, aluminum, 470 µF, 10 V, 20%	F	(PANASONIC) EEE-FP1A471AP	(DIGI-KEY) PCE4526CT-ND
10	RX1-RX12	12	Open	0603	—	—
11	R10-R13	4	Open	0805	—	—
12	Z1-R9, R19-R21, R26-R28, R35-R37	18	Resistor, 0 Ω	0805	(ROHM) MCR10EZHJ000	(DIGI-KEY) RHM0.0ACT-ND
13	R1-R6, R29-R34	12	Resistor, 75 Ω, 1/8 W, 1%	0805	(ROHM) MCR10EZHF75.0	(DIGI-KEY) RHM75.0CCT-ND
14	R14	1	Resistor, 100 Ω, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1000	(DIGI-KEY) RHM100CCT-ND
15	R15, R17, R24, R25	4	Resistor, 1 kΩ, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1001	(DIGI-KEY) RHM1.00KCCT-ND
16	R16, R18, R22, R23	4	Resistor, 100 kΩ, 1/8 W, 1%	0805	(ROHM) MCR10EZHF1003	(DIGI-KEY) RHM100KCCT-ND
17	R38	1	Resistor, 1 kΩ, 1/4 W, 1%	1206	(ROHM) MCR18EZHF1001	(DIGI-KEY) RHM1.00KFCT-ND
18	D1-D12	12	Diode, ultrafast		(FAIRCHILD) BAV99	(DIGI-KEY) BAV99FSCT-ND
19	J10, J11	2	Jack, banana receptance, 0.25" diameter hole		(SPC) 15459	(NEWARK) 79K5034
20	J1-J6, J13-J17, J18	12	Connector, BNC, jack, 75 Ω		(AMPHENOL) 31-5329-72RFX	(NEWARK) 93F7554
21	J8, J20	2	Connector, mini circular DIN		(CUI) MD-40SM	(DIGI-KEY) CP-2240-ND
22	J7, J19	2	Connector, RCA jack, yellow		(CUI) RCJ-044	(DIGI-KEY) CP-1421-ND
23	J9, J12	2	Connector, RCA, jack, R/A		(CUI) RCJ-32265	(DIGI-KEY) CP-1446-ND
24	TP1, TP2	2	Test point, black		(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
25	JP1, JP2	2	Open		—	—
26	JP3-JP6	4	Header, 0.1" CTRS, 0.025" square pins	3 pos.	(SULLINS) PBC36SAAN	(DIGI-KEY) S1011E-36-ND
27	JP3-JP6	4	Shunts		(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
28	U1	1	IC, THS7364	PW	(TI) THS7364IPW	—
29		4	Standoff, 4-40 hex, 0.625" length		(KEYSTONE) 1808	(DIGI-KEY) 1808K-ND
30		4	Screw, Phillips, 4-40, .250"		PMSSS 440 0025 PH	(DIGI-KEY) H703-ND
31		1	Board, printed circuit		EDGE # 6518231 REV.A	—

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.6 V to 5.5 V single-supply and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS7364IPW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7364
THS7364IPW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7364
THS7364IPWR	Active	Production	TSSOP (PW) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7364
THS7364IPWR.B	Active	Production	TSSOP (PW) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7364

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

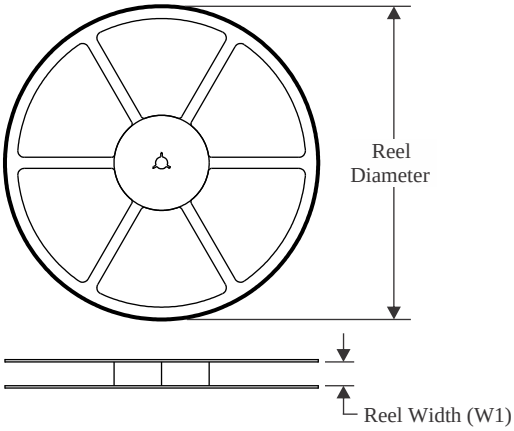
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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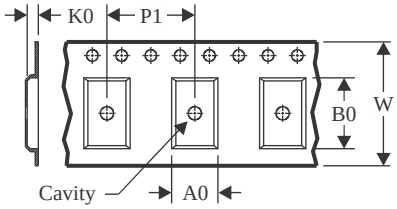
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

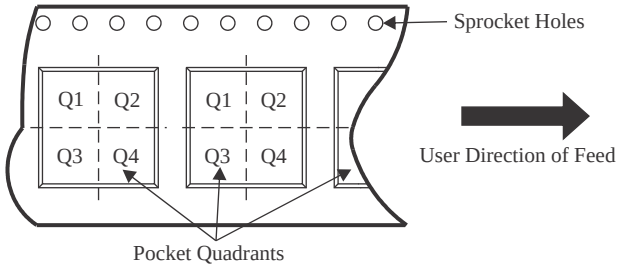


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

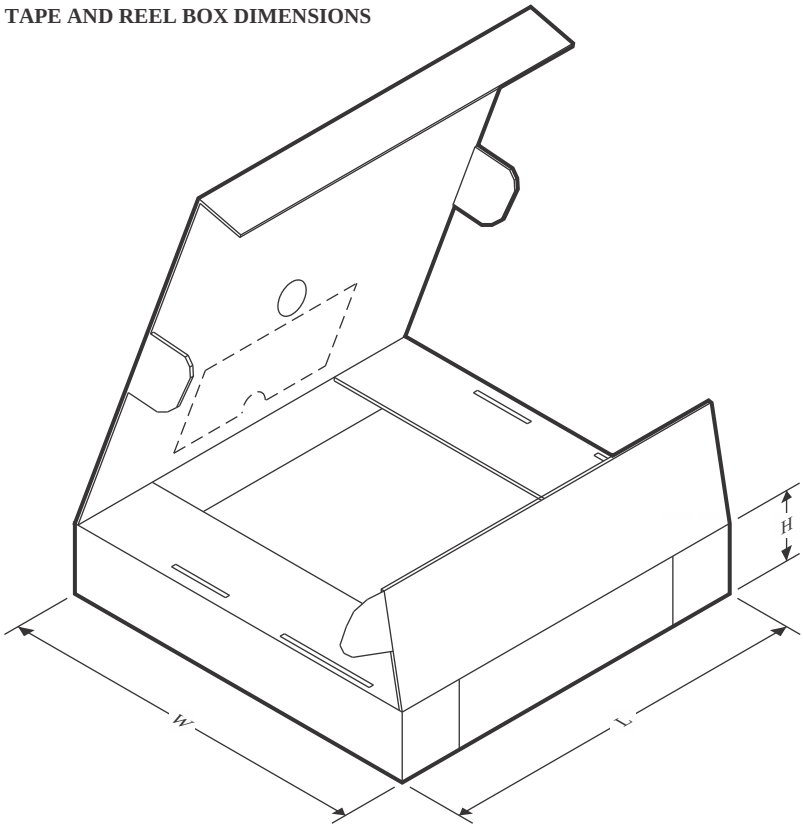
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7364IPWR	TSSOP	PW	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

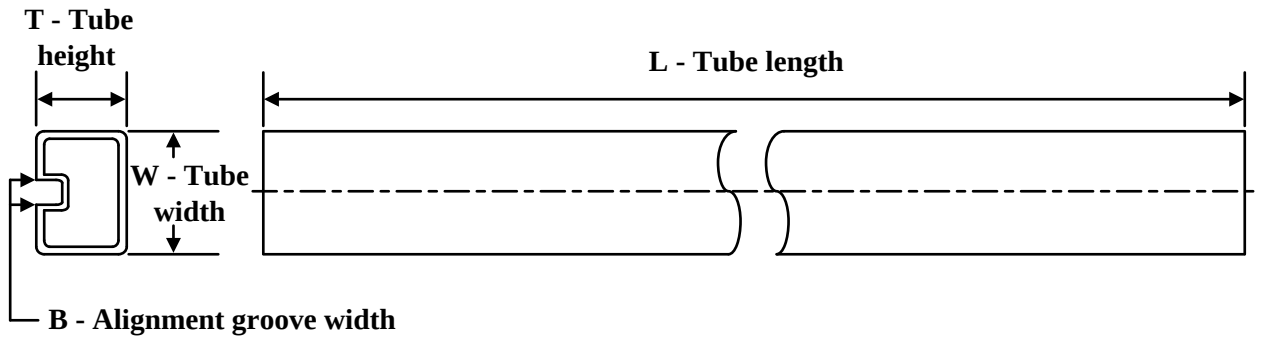
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7364IPWR	TSSOP	PW	20	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

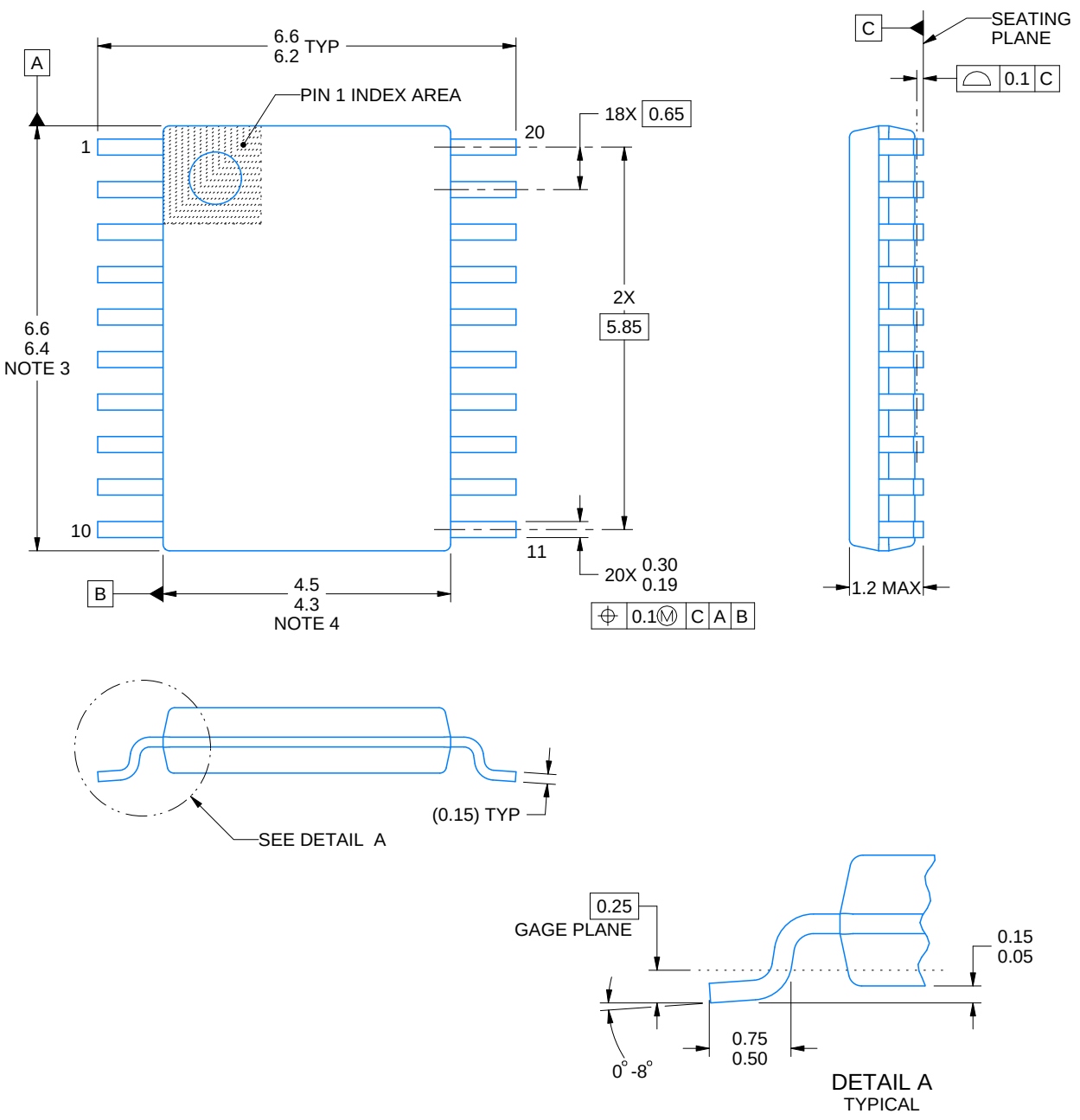
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS7364IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
THS7364IPW.B	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

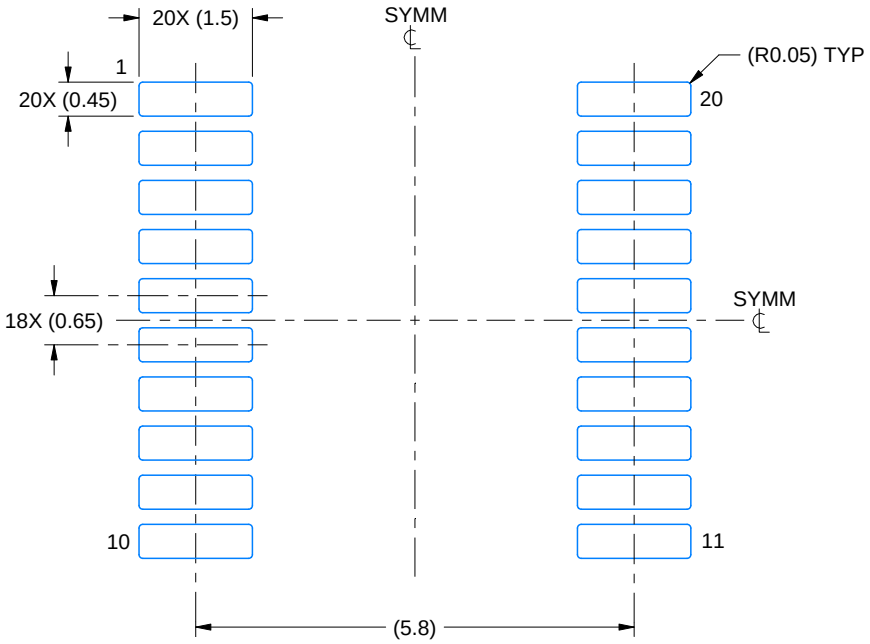
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

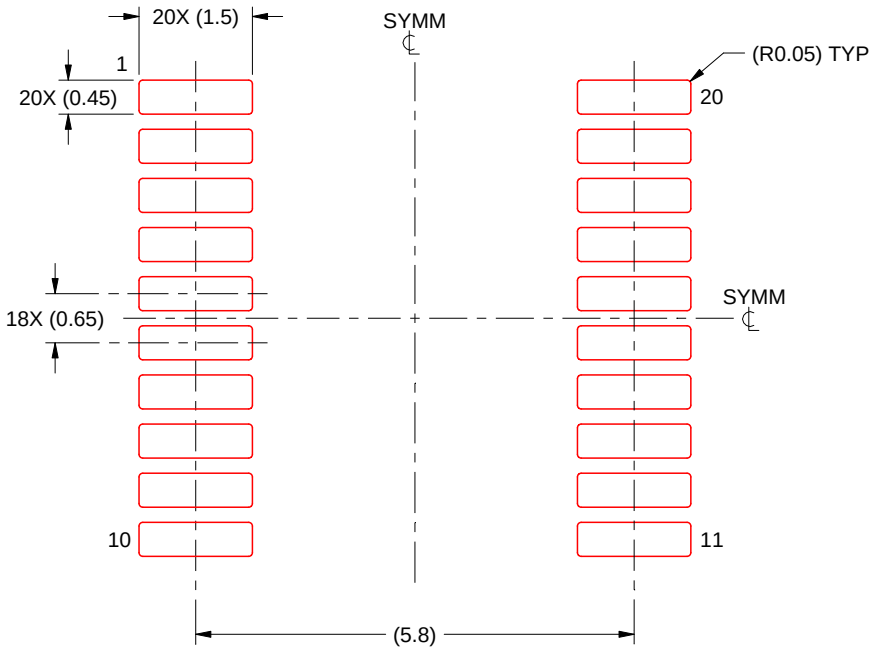


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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