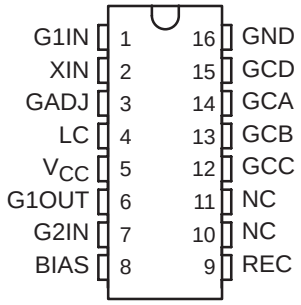
SLSS003 − SEPTEMBER 1983 − REVISED MARCH 1988

- **Designed for Use With the TL851 in Sonar Ranging Modules Like the SN28827**
- **Digitally Controlled Variable-Gain Variable-Bandwidth Amplifier**
- **Operational Frequency Range of 20 kHz to 90 kHz**
- **TTL-Compatible**
- **Operates From Power Sources of 4.5 V to 6.8 V**
- **Interfaces to Electrostatic or Piezoelectric Transducers**
- **Overall Gain Adjustable With One External Resistor**

N PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TL852 is an economical sonar ranging receiver integrated circuit for use with the TL851 control integrated circuit. A minimum of external components is required for operation, and this amplifier easily interfaces to Polaroid's 50-kHz electrostatic transducer. An external 68-kΩ ±5% resistor from BIAS to GND provides the internal biasing reference. Amplifier gain can be set with a resistor from G1IN to GADJ. Required amplifier gain will vary for different applications. Using the detect-level measurement circuit of Figure 1, a nominal peak-to-peak value of 230 mV input during gain step 2 is recommended for most applications. For reliable operation, a level no lower than 50 mV should be used. The recommended detect level of 230 mV can be obtained for most amplifiers with an R1 value between 5 kΩ and 20 kΩ

Digital control of amplifier gain is provided with gain control inputs GCA, GCB, GCC, and GCD. These inputs must be driven synchronously (all inputs stable within 0.1 μs) to avoid false receive output signals due to invalid logic counts. This can be done easily with the TL851 control integrated circuit. A plot showing relative gain for the various gain steps versus time can be seen in Figure 2. To dampen ringing of the 50-kHz electrostatic transducer, a 5-kΩ resistor from G1IN to XIN is recommended.

An external parallel combination of inductance and capacitance between LC and V_{CC} provides an amplifier with an externally controlled gain and Q. This not only allows control of gain to compensate for attenuation of signal with distance, but also maximizes noise and sidelobe rejection. Care must be taken to accurately tune the L-C combination at operating frequency or gain and Q will be greatly reduced at higher gain steps.

AC coupling between stages of the amplifier is accomplished with a 0.01-mF capacitor for proper biasing.

The receive output is normally held at a low level by an internal 1-μA current source. When an input of sufficient amplitude is received, the output is driven alternately by the 1-μA discharge current and a 50-μA charging current. A 1000-pF capacitor is required from REC to GND to integrate the received signal so that one or two noise pulses will not be recognized.

XIN provides clamping for the transformer secondary when used for transducer transmit drive as shown in Figure 4 of the SN28827 data sheet.

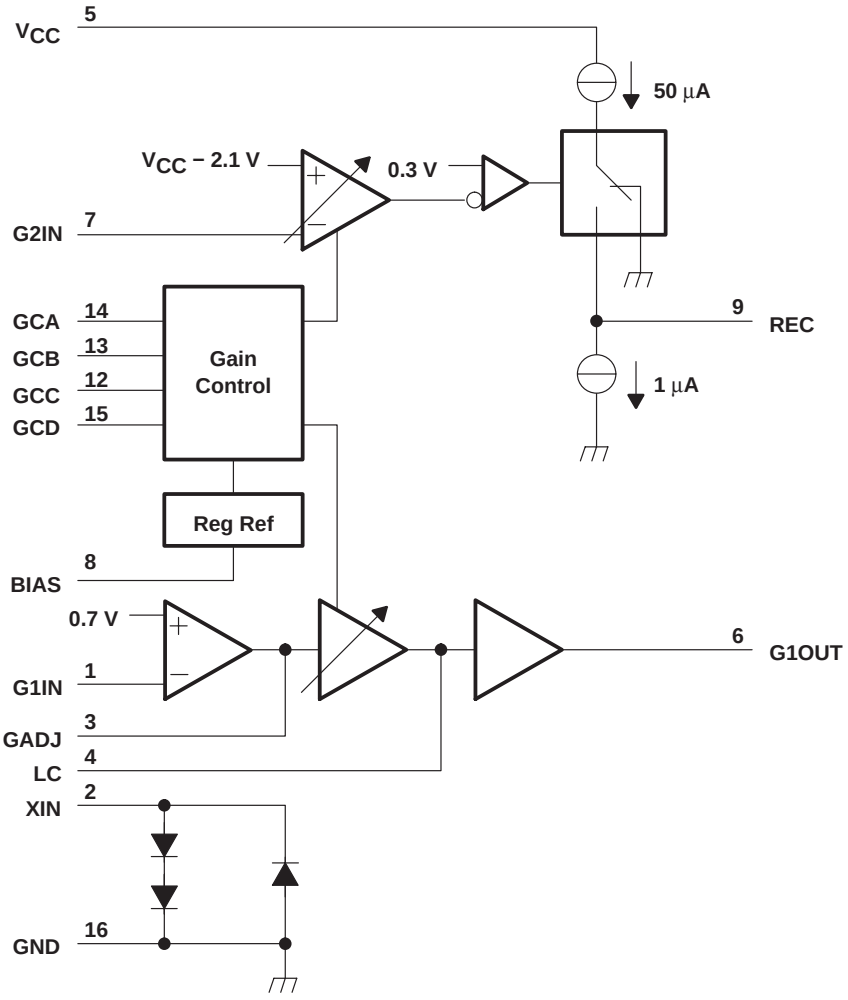
The TL852 is characterized for operation from 0°C to 40°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

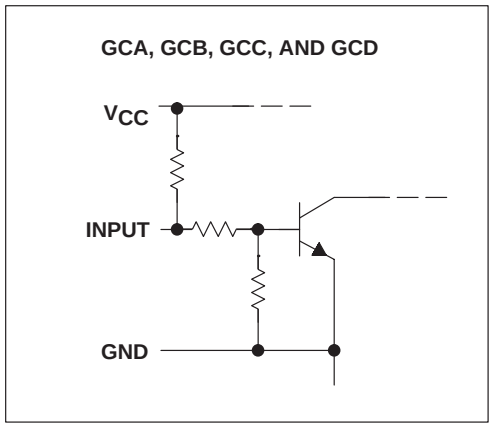
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TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

functional block diagram



schematic of gain control inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage at any pin with respect to GND . . . . . − 0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . − 7 V to 0.5 V
XIN input current (50% duty cycle) . . . . . ±60 mA
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . − 40°C to 85°C
Storage temperature range . . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	GCA, GCB, GCC, GCD	2.1		V
Low-level input voltage, V_{IL}	GCA, GCB, GCC, GCD		0.6	V
Bias resistor between BIAS and GND		64	72	kΩ
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
Input clamp voltage at XIN	I_I = 40 mA				2.5	V
	I_I = − 40 mA				− 1.5	V
Open-circuit input voltage at GCA, GCB, GCC, GCD	V_{CC} = 5 V,	I_I = 0		2.5		V
High-level input current, I_{IH}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IH} = 2 V		− 0.5		mA
Low-level input current, I_{IL}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IL} = 0			− 3	mA
Raceive output current	I_{G2IN} = − 100 μA,	V_O = 0.3 V		1		μA
	I_{G2IN} = 100 μA,	V_O = 0.1 V		− 50		μA
Supply current, I_{CC}					45	mA

‡ Typical values are at V_{CC} = 5 V and T_A = 25°C.

APPLICATION INFORMATION

detect level versus gain step

Detect level is measured by applying a 15-cycle burst of 49.4 kHz square wave just after the beginning of the gain step to be tested. The least burst amplitude that makes REC reach the trip level is defined to be the detect level. System gain is then inversely proportional to detect level. See the test circuit in Figure 1.

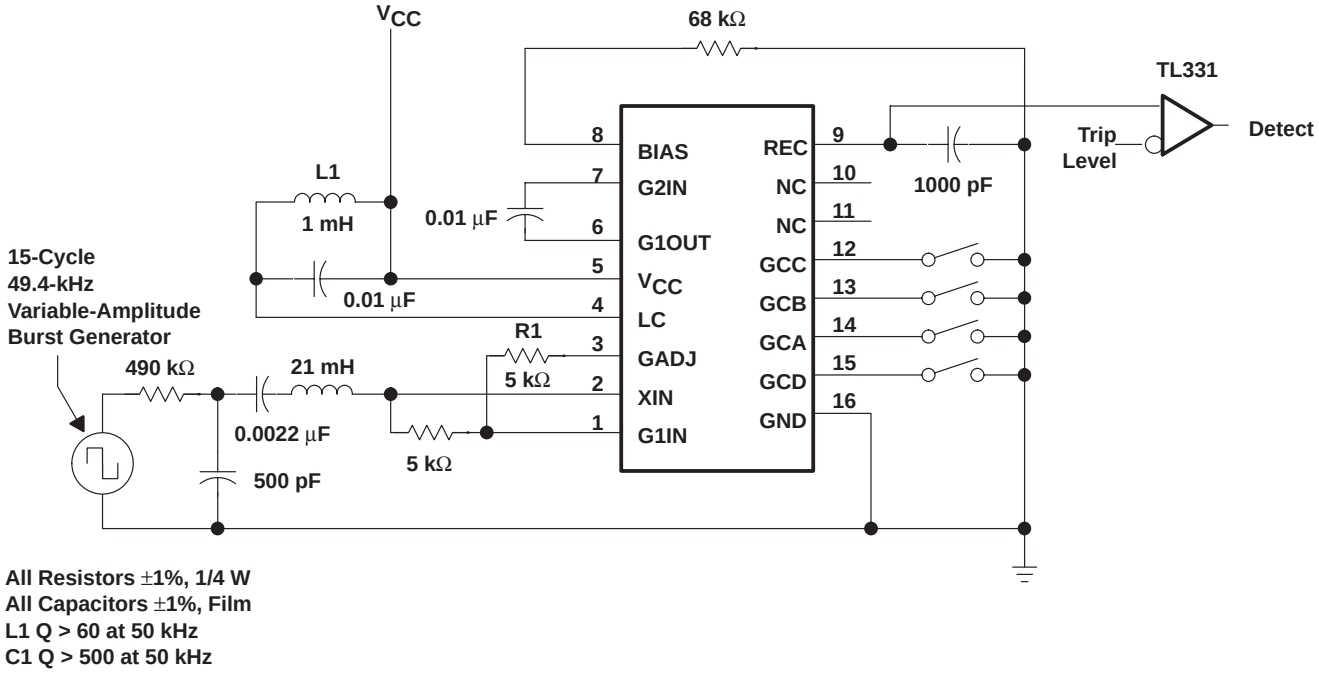


Figure 1. Detect-Level Measurement Circuit and Waveforms

APPLICATION INFORMATION

GAIN STEP TABLE

GCD	GCC	GCB	GCA	STEP NUMBER
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11

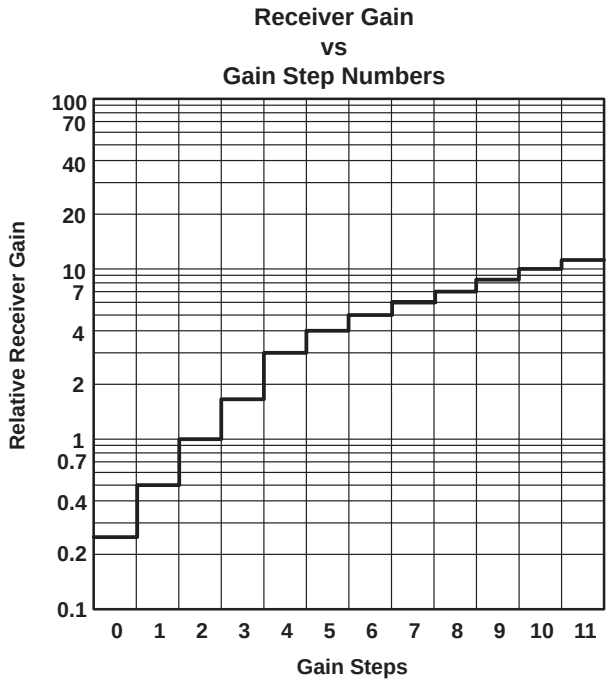


Figure 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL852CDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TL852C
TL852CDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See TL852CDR	TL852C
TL852CN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TL852CN
TL852CN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	See TL852CN	TL852CN
TL852CNE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	See TL852CN	TL852CN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

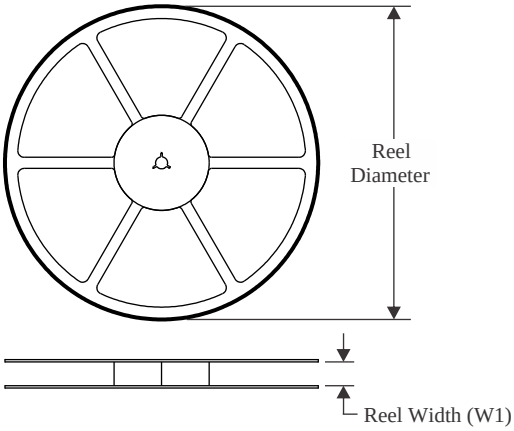
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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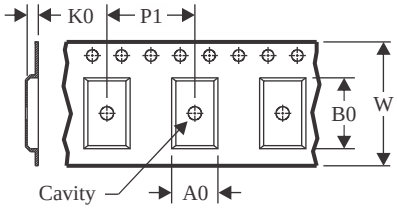
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

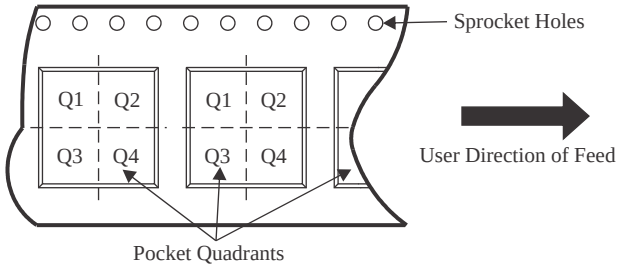


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

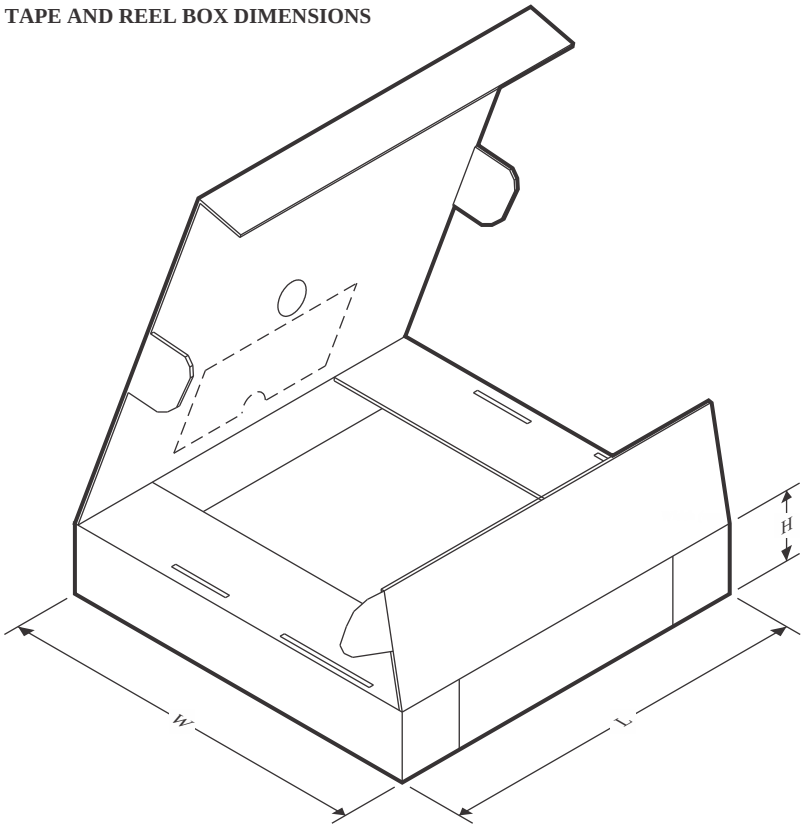
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL852CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

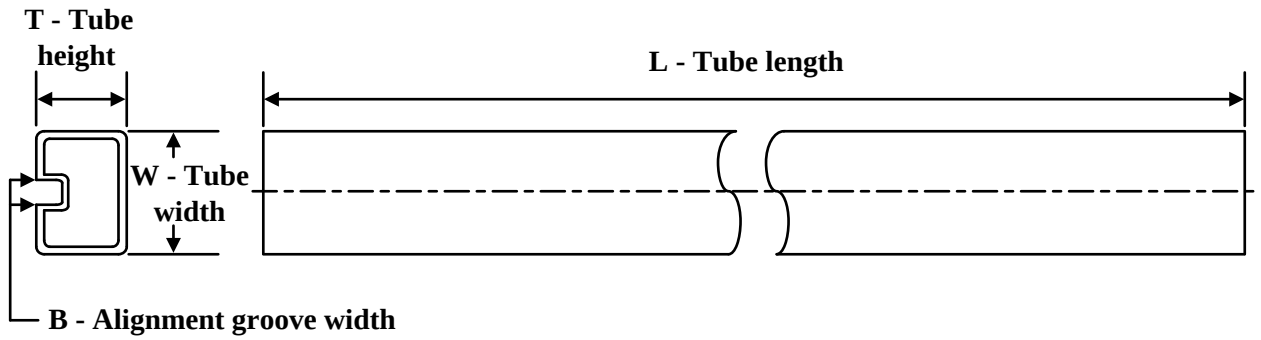
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL852CDR	SOIC	D	16	2500	350.0	350.0	43.0

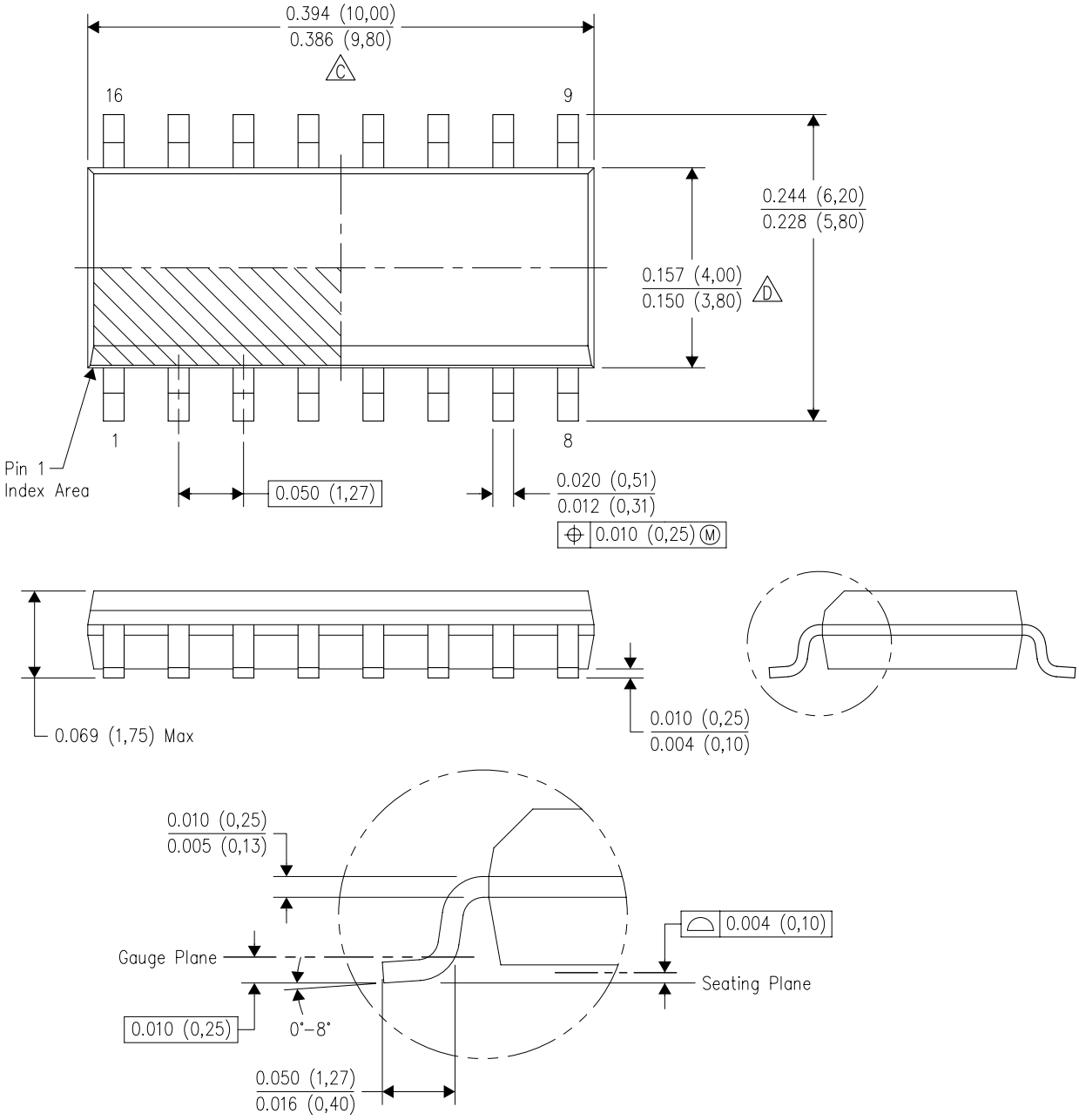
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL852CN	N	PDIP	16	25	506	13.97	11230	4.32
TL852CN.A	N	PDIP	16	25	506	13.97	11230	4.32
TL852CNE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

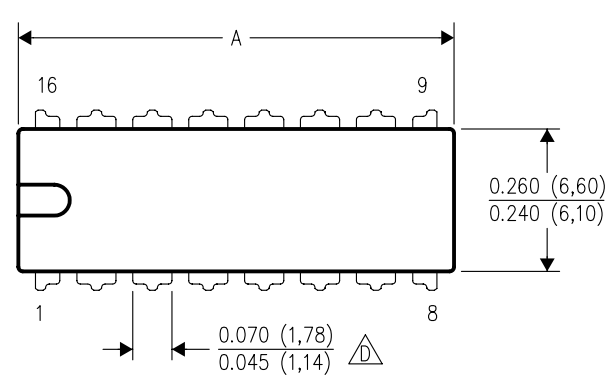


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

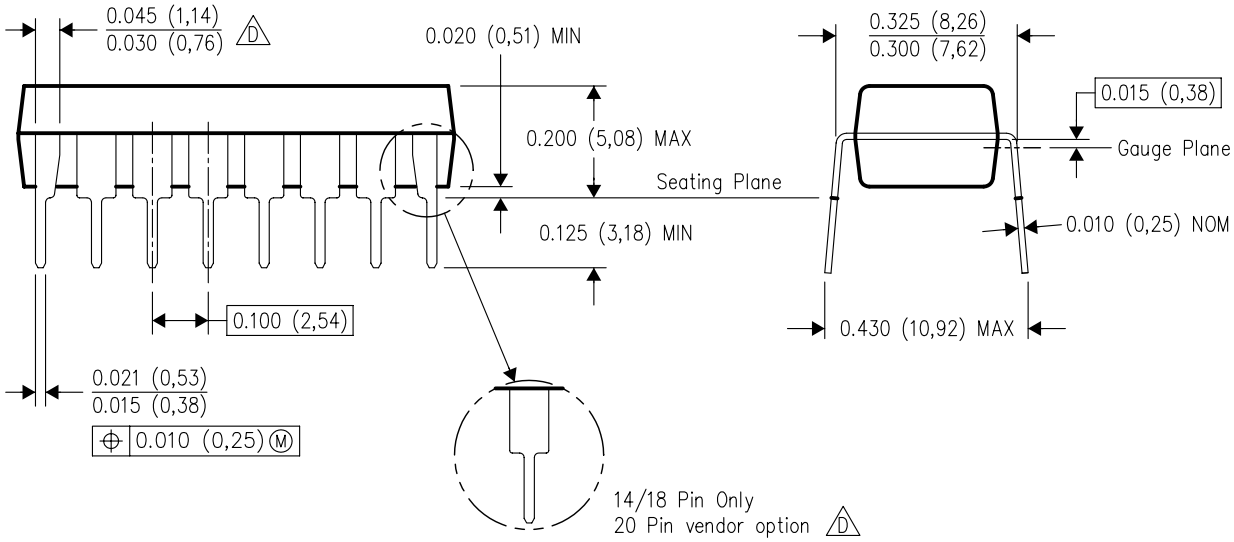
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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