- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Output Swing includes Both Supply Rails**
- **Low Noise . . . 12 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C (TLC2262A)**
- **Macromodel Included**
- **Performance Upgrade for the TS27M2/M4 and TLC27M2/M4**

description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

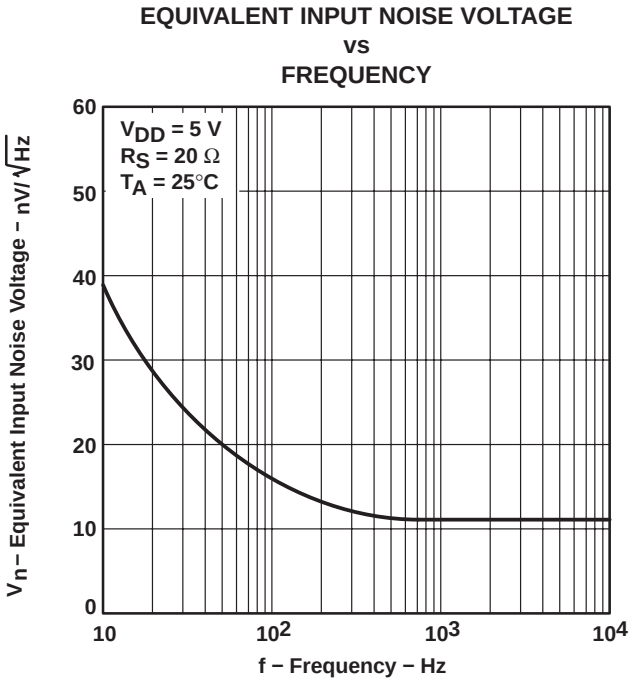


Figure 1

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Advanced LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

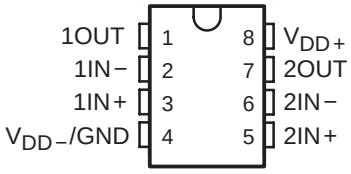
Copyright © 2008 Texas Instruments Incorporated

ORDERING INFORMATION†

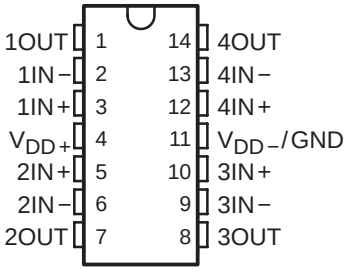
T_A	V_{IO}max AT 25°C	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	950 μV	SOIC (D)	Tape and reel	TLC2262AQDRQ1§	2262AQ1
	2.5 mV	SOIC (D)	Tape and reel	TLC2262QDRQ1§	2262Q1
	950 μV	TSSOP (PW)	Tape and reel	TLC2262AQPWRQ1§	2262AQ1
	2.5 mV	TSSOP (PW)	Tape and reel	TLC2262QPWRQ1§	2262Q1
	950 μV	SOIC (D)	Tape and reel	TLC2264AQDRQ1	2264AQ1
	2.5 mV	SOIC (D)	Tape and reel	TLC2264QDRQ1	2264Q1
	950 μV	TSSOP (PW)	Tape and reel	TLC2264AQPWRQ1	2264AQ1
	2.5 mV	TSSOP (PW)	Tape and reel	TLC2264QPWRQ1	2264Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ Product Preview.

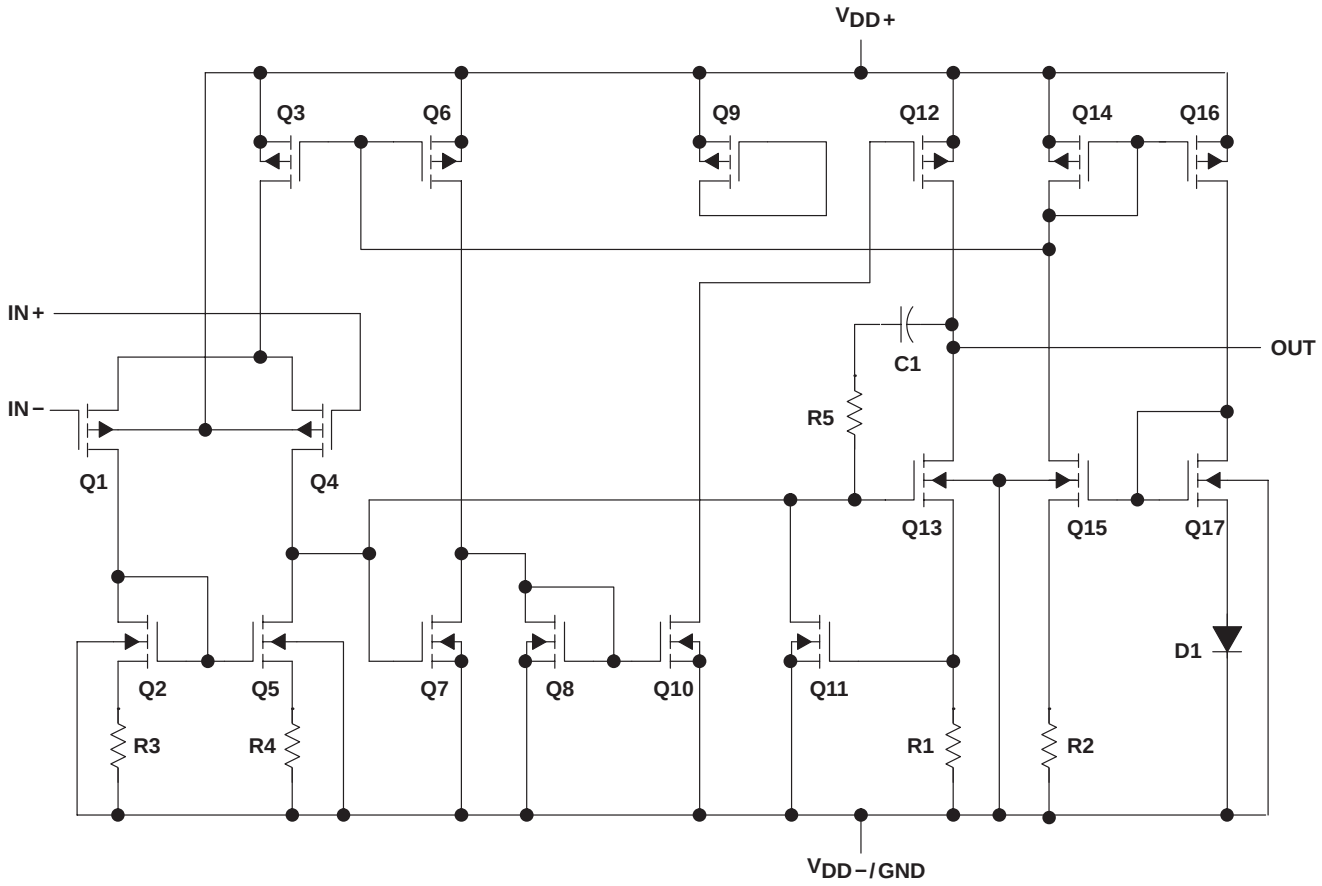
TLC2262, TLC2262A
D OR PW PACKAGE
(TOP VIEW)



TLC2264, TLC2264A
D OR PW PACKAGE
(TOP VIEW)



equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	**TLC2262**	**TLC2264**
Transistors	38	76
Resistors	28	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . −8 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±16 V
Input voltage, V_I (any input, see Note 1) . . . . . V_{DD-} − 0.3 V to V_{DD+}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: Q suffix . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or PW package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D−8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D−14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
PW−14	750 mW	6.0 mW/°C	480 mW	389 mW	150 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} −1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.5	V
Operating free-air temperature, T_A	−40	125	°C

TLC2262 electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		5			5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		400	500		400	500	μA
				Full range			500			500	

† Full range is −40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262 operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.82			0.82		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V

TLC2262 electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		5			5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	−5 to 4	−5.3 to 4		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_O = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 μA	25°C		−4.99			−4.99		V
		V_{IC} = 0,	I_O = 500 μA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0,	I_O = 4 mA	25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ	25°C	80	200		80	200		V/mV
				Full range	50			50			
			R_L = 1 MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0,	R_S = 50 Ω	25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0,	No load	25°C		425	500		425	500	μA
				Full range			500			500	

† Full range is −40°C to 125°C for Q suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2262 operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2262-Q1			TLC2262A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		85			85		kHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q suffix.

TLC2264 electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 4 mA	25°C		0.8	1		0.7	1	
				Full range			1.2			1.2	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	100		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V,		25°C	80	95		80	95		dB
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is −40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264 operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q suffix.
‡ Referenced to 2.5 V

TLC2264 electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1			1		pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_O = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0,	I_O = 50 μA	25°C		−4.99			−4.99		V
		V_{IC} = 0,	I_O = 500 μA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0,	I_O = 4 mA	25°C	−4	−4.3		−4	−4.3		
				Full range	−3.8			−3.8			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 50 kΩ	25°C	80	200		80	200		V/mV
				Full range	50			50			
			R_L = 1 MΩ	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0,	R_S = 50 Ω	25°C	75	88		75	88		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 0,	No load	25°C		0.85	1		0.85	1	mA
				Full range			1			1	

† Full range is −40°C to 125°C for Q suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2264 operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2264-Q1			TLC2264A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2 V, C_L = 100 pF	R_L = 50 kΩ,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.8			0.8		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 50 kΩ, f = 20 kHz	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.024%			0.024%		
	Gain-bandwidth product	f =10 kHz, C_L = 100 pF	R_L = 50 kΩ,	25°C		0.73			0.73		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 50 kΩ,	A_V = 1, C_L = 100 pF	25°C		70			70		kHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 50 kΩ, C_L = 100 pF	To 0.1%	25°C		7.1			7.1		μs
			To 0.01%			16.5			16.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ,	C_L = 100 pF	25°C		57°			57°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	2 − 5 6, 7
α_{VIO}	Input offset voltage temperature coefficient	Distribution	8 − 11
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	12
V_I	Input voltage range	vs Supply voltage vs Free-air temperature	13 14
V_{OH}	High-level output voltage	vs High-level output current	15
V_{OL}	Low-level output voltage	vs Low-level output current	16, 17
V_{OM+}	Maximum positive output voltage	vs Output current	18
V_{OM-}	Maximum negative output voltage	vs Output current	19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	21 22
V_O	Output voltage	vs Differential input voltage	23, 24
	Differential gain	vs Load resistance	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26, 27 28, 29
z_o	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	32 33
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	37, 38 39, 40
SR	Slew rate	vs Load capacitance vs Free-air temperature	41 42
V_O	Inverting large-signal pulse response		43, 44
	Voltage-follower large-signal pulse response		45, 46
	Inverting small-signal pulse response		47, 48
	Voltage-follower small-signal pulse response		49, 50
V_n	Equivalent input noise voltage	vs Frequency	51, 52
	Noise voltage (referred to input)	Over a 10-second period	53
	Integrated noise voltage	vs Frequency	54
THD + N	Total harmonic distortion plus noise	vs Frequency	55
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	56 57
ϕ_m	Phase margin	vs Frequency vs Load capacitance	26, 27 58
	Gain margin	vs Load capacitance	59
B_1	Unity-gain bandwidth	vs Load capacitance	60
	Overestimation of phase margin	vs Load capacitance	61

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC2262
INPUT OFFSET VOLTAGE**

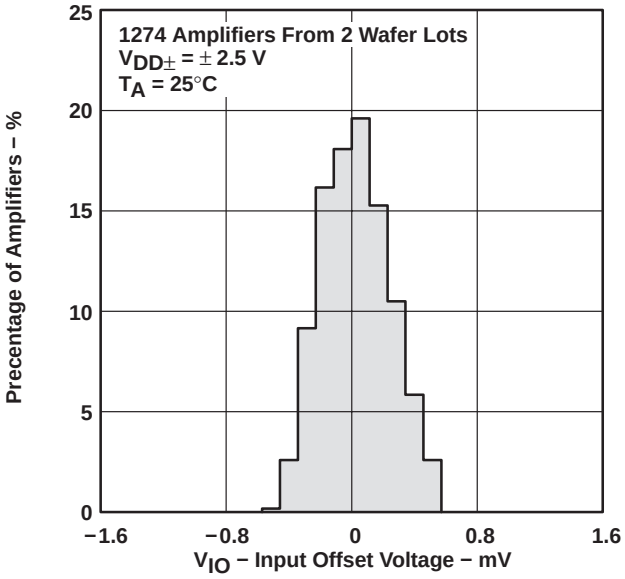


Figure 2

**DISTRIBUTION OF TLC2262
INPUT OFFSET VOLTAGE**

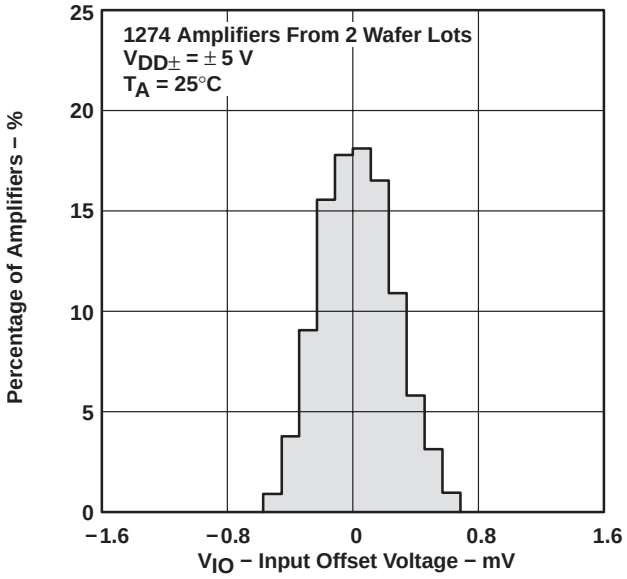


Figure 3

**DISTRIBUTION OF TLC2264
INPUT OFFSET VOLTAGE**

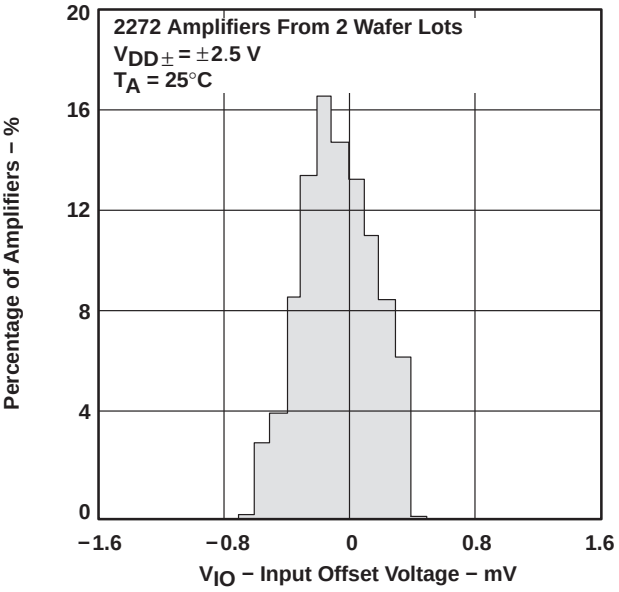


Figure 4

**DISTRIBUTION OF TLC2264
INPUT OFFSET VOLTAGE**

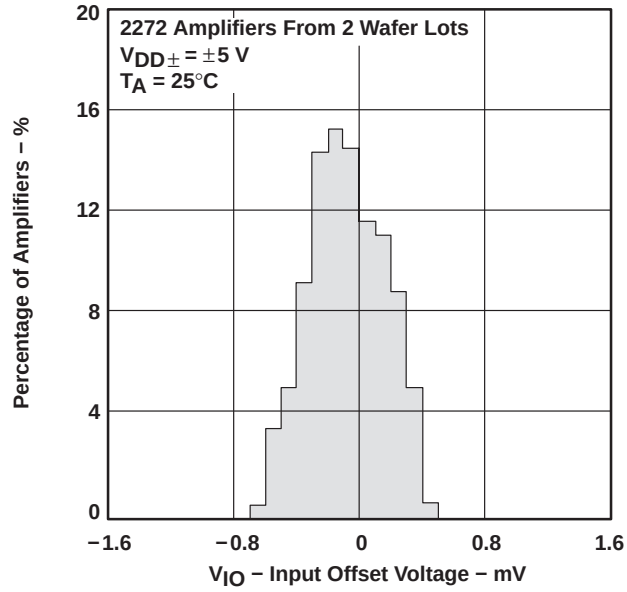
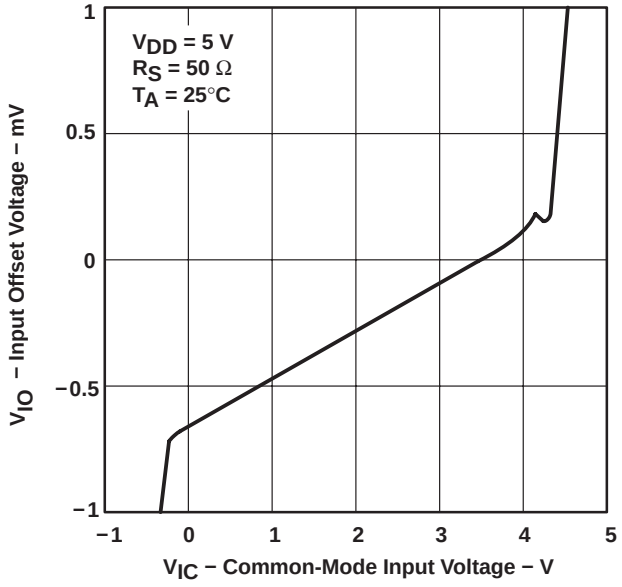


Figure 5

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 6

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

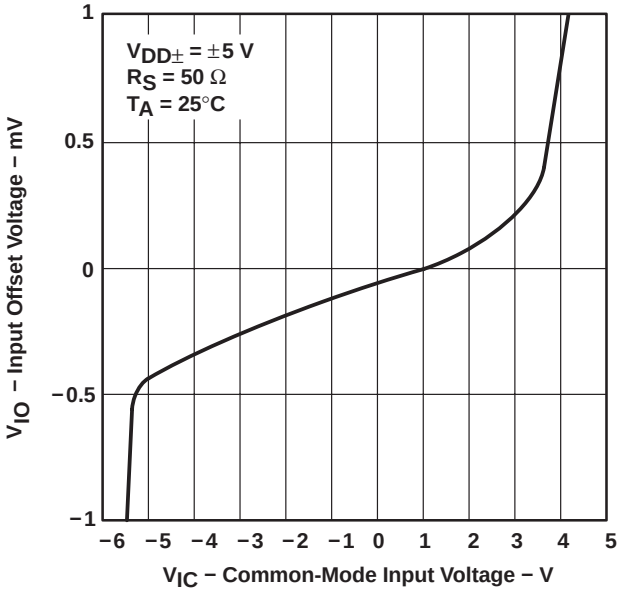


Figure 7

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

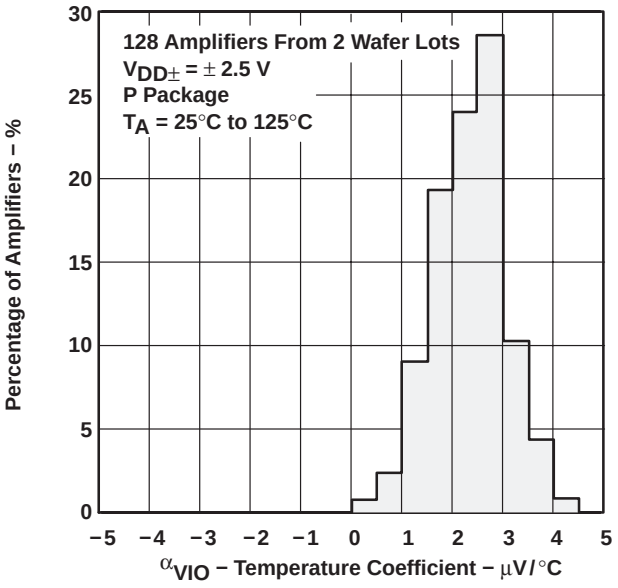


Figure 8

DISTRIBUTION OF TLC2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

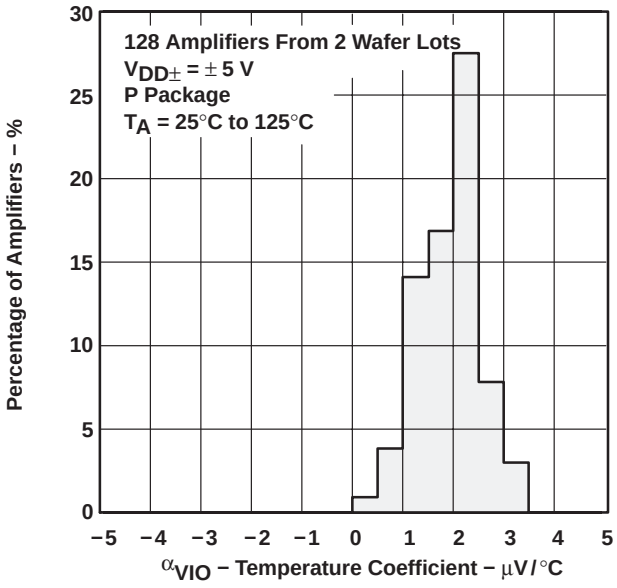


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

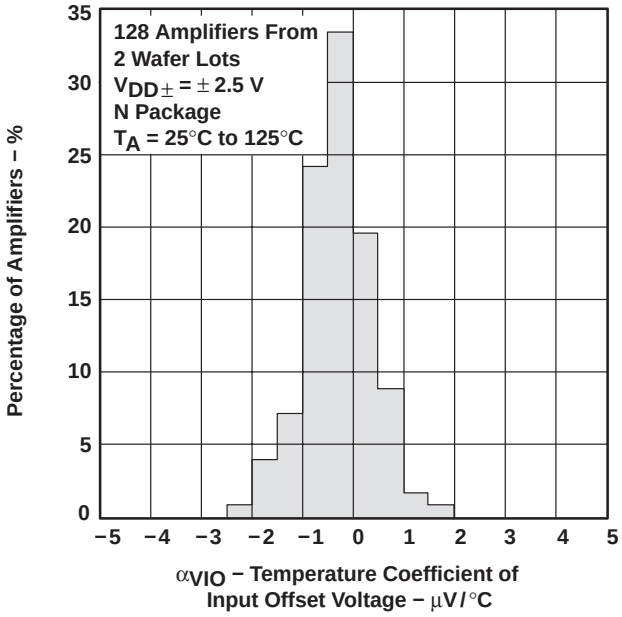


Figure 10

DISTRIBUTION OF TLC2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

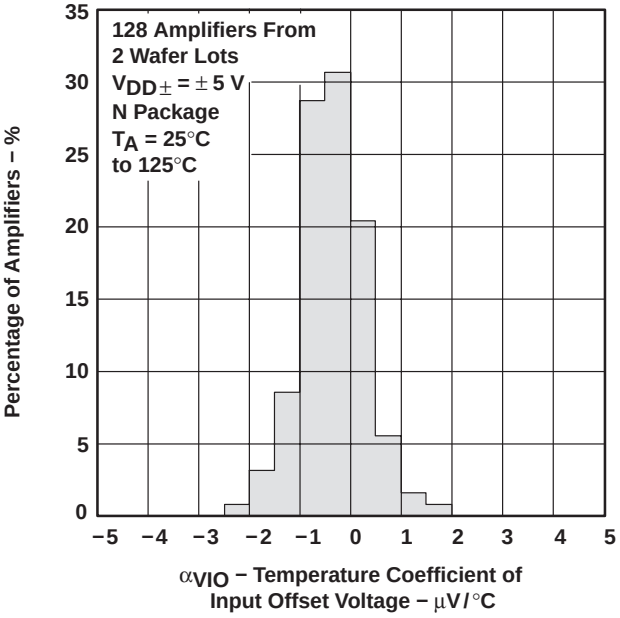


Figure 11

INPUT BIAS AND INPUT OFFSET CURRENTS† vs FREE-AIR TEMPERATURE

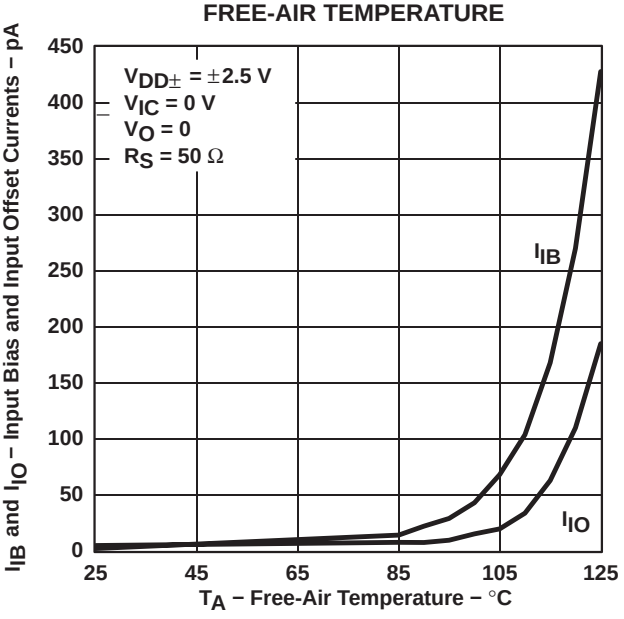


Figure 12

INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

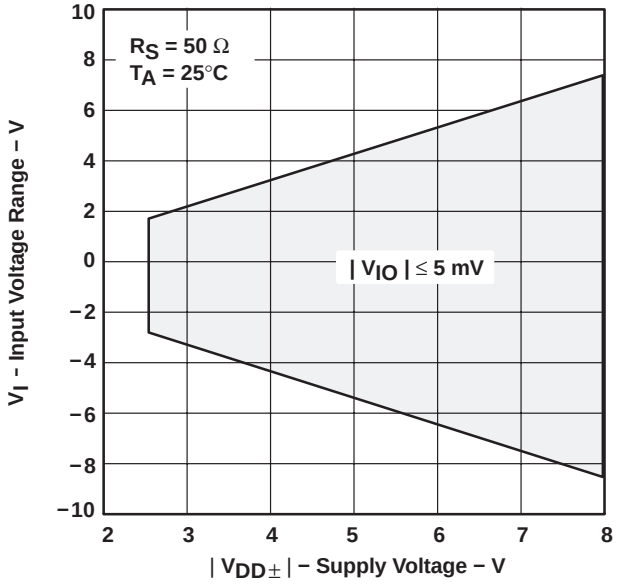


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE†‡ vs FREE-AIR TEMPERATURE

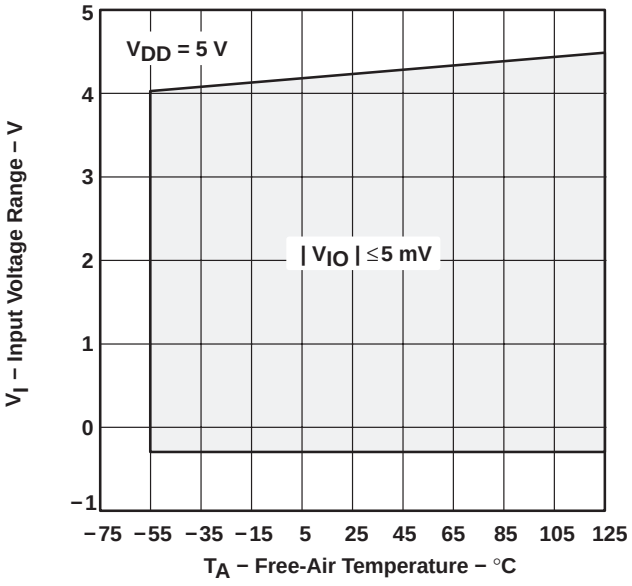


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

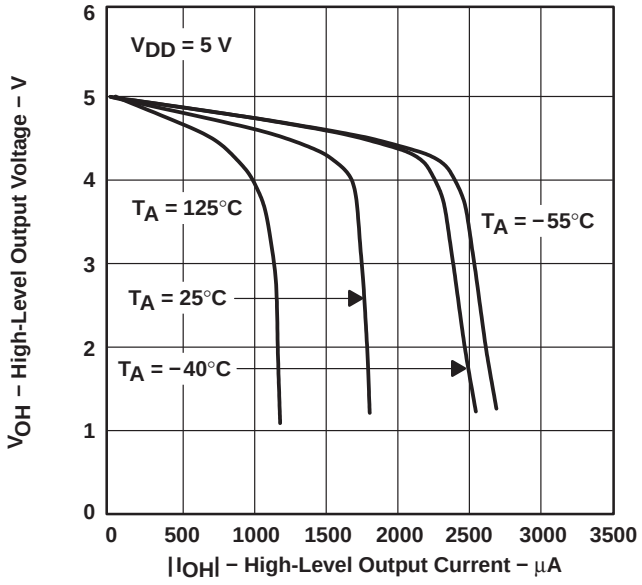


Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡ vs LOW-LEVEL OUTPUT CURRENT

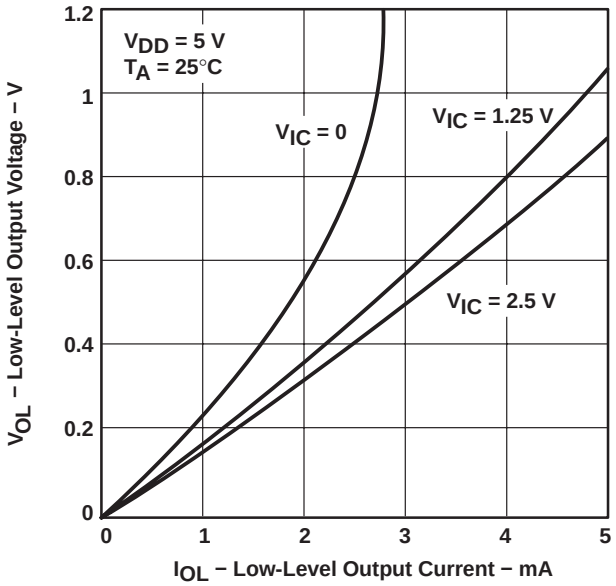


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT

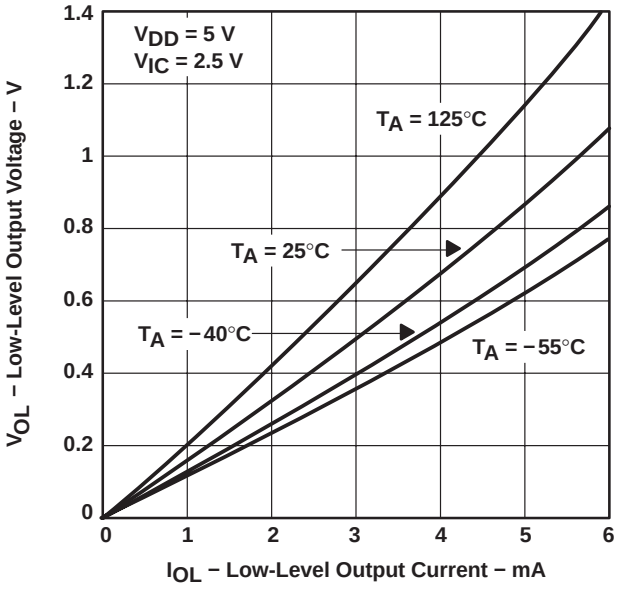


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE† vs OUTPUT CURRENT

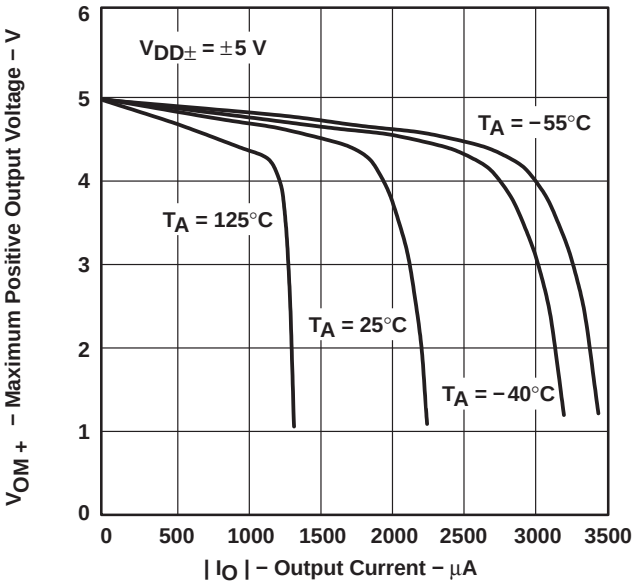


Figure 18

MAXIMUM NEGATIVE OUTPUT VOLTAGE† vs OUTPUT CURRENT

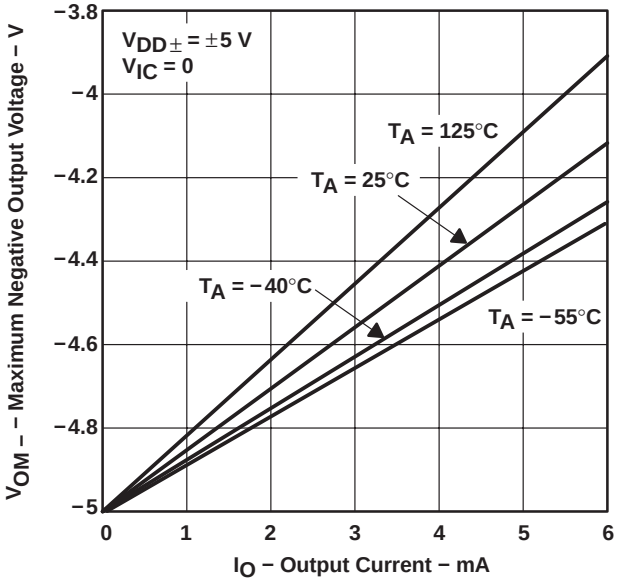
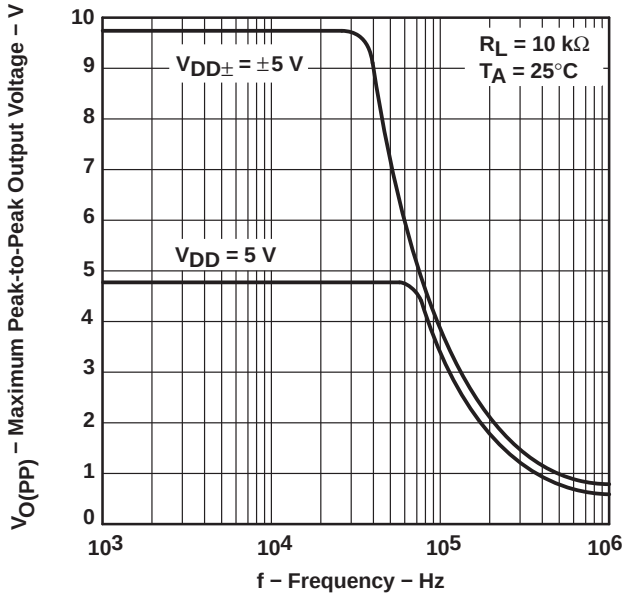


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†‡ vs FREQUENCY



‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

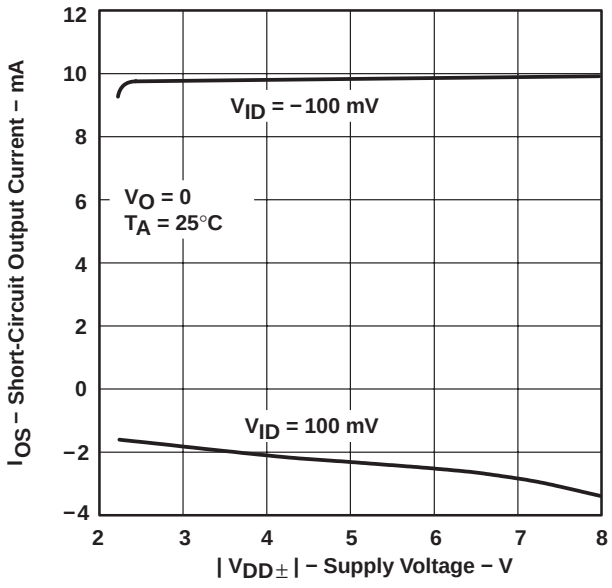


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

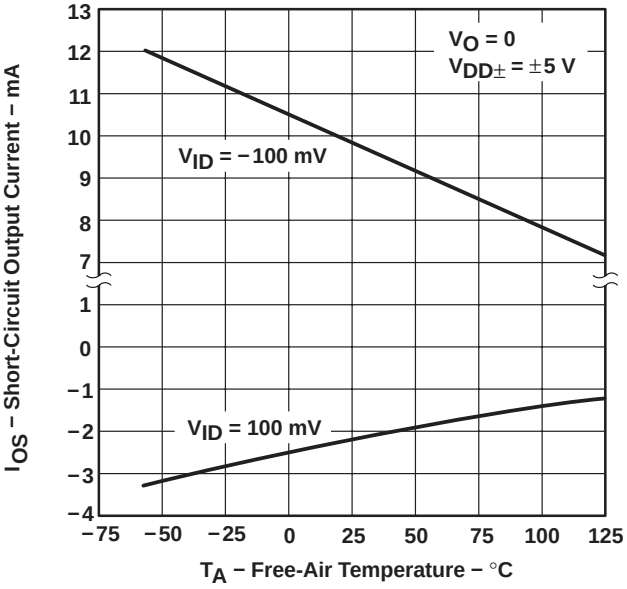


Figure 22

OUTPUT VOLTAGE‡ vs DIFFERENTIAL INPUT VOLTAGE

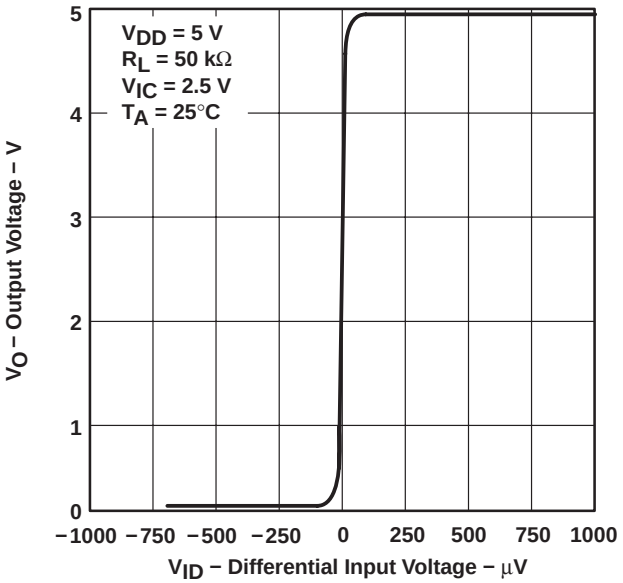


Figure 23

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

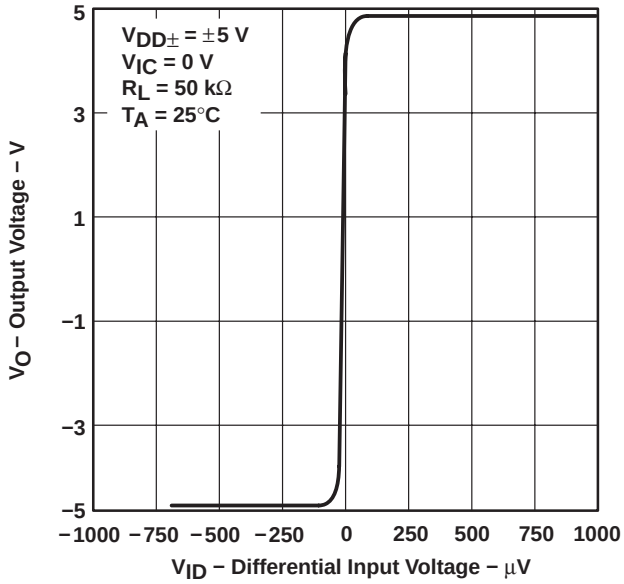


Figure 24

DIFFERENTIAL GAIN‡ vs LOAD RESISTANCE

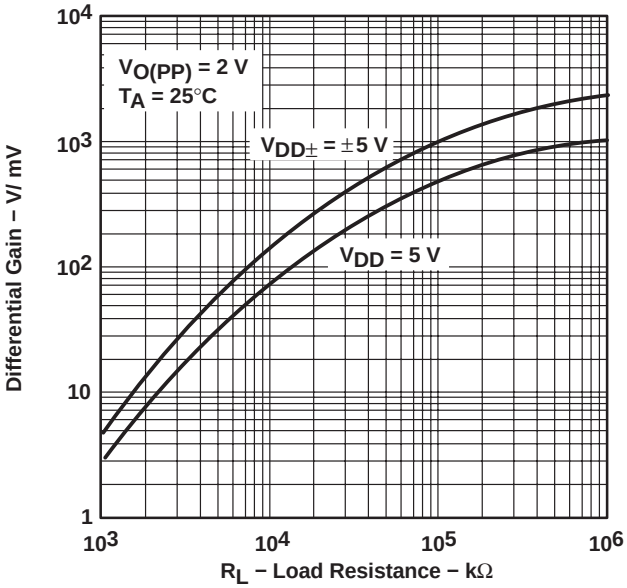
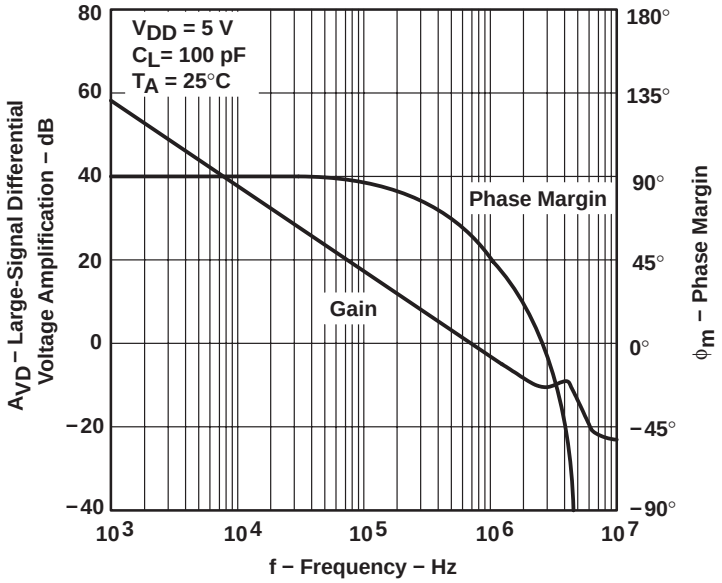


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE† AMPLIFICATION AND PHASE MARGIN vs FREQUENCY



† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

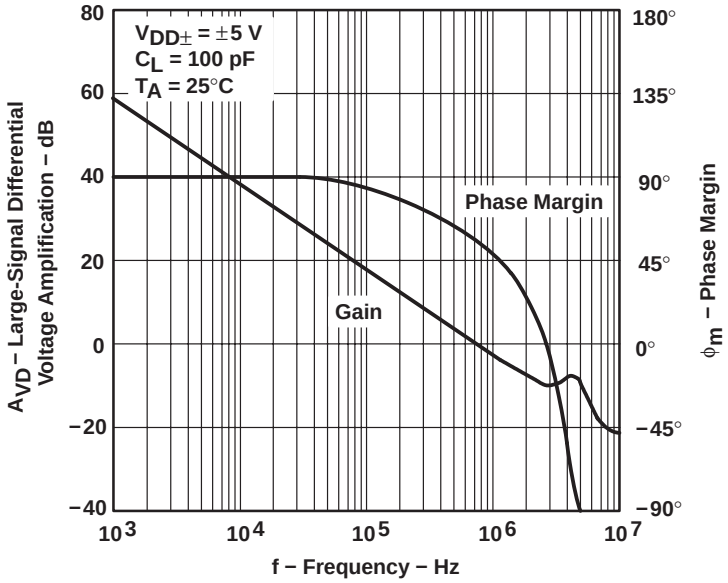


Figure 27

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

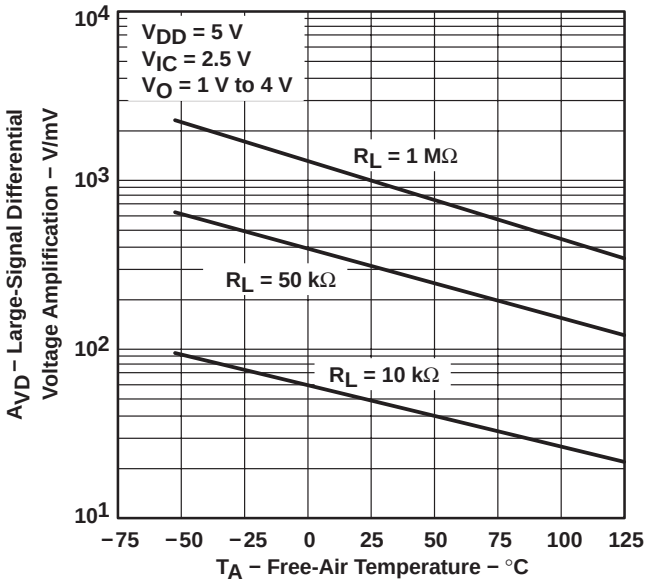


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

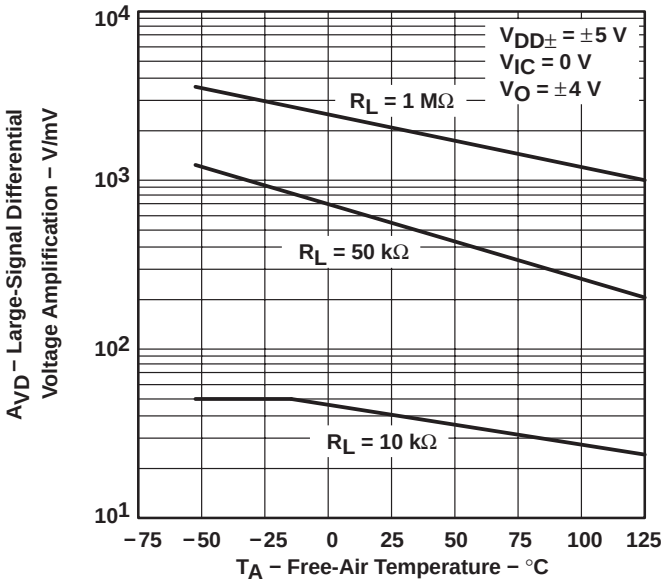


Figure 29

OUTPUT IMPEDANCE‡ vs FREQUENCY

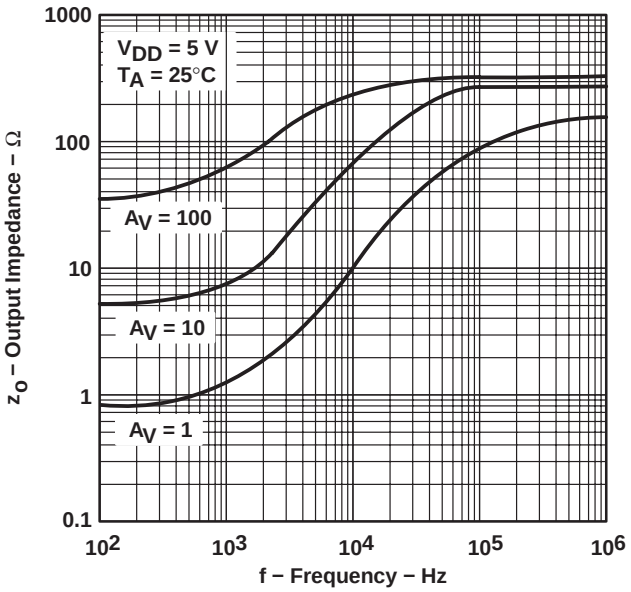


Figure 30

OUTPUT IMPEDANCE vs FREQUENCY

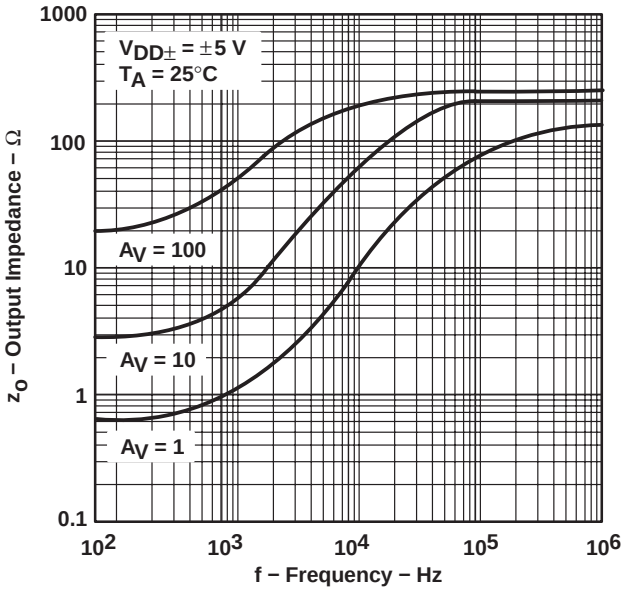


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO† vs FREQUENCY

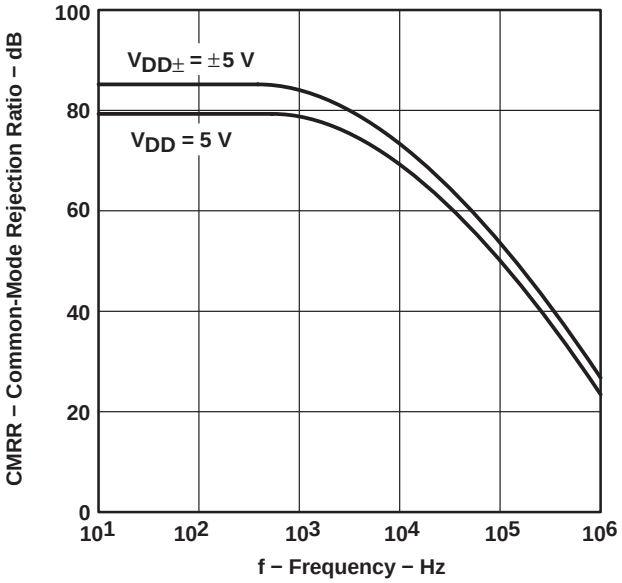


Figure 32

COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

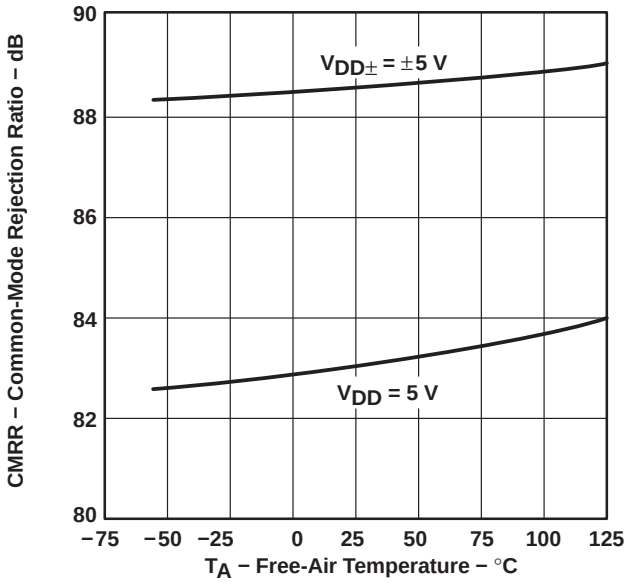


Figure 33

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

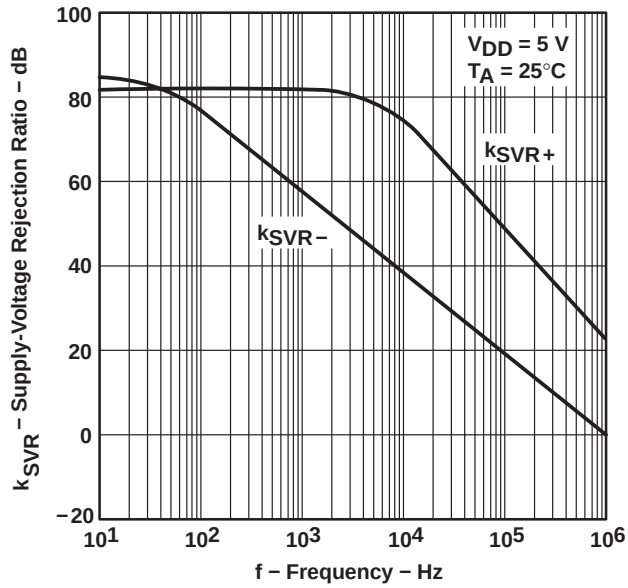


Figure 34

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

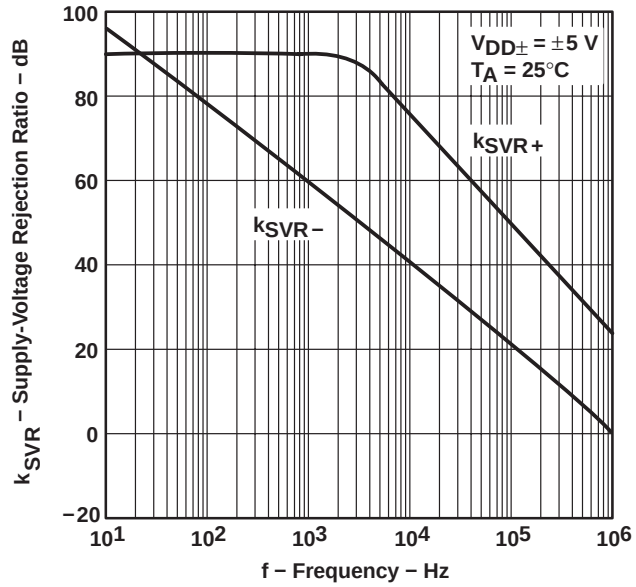


Figure 35

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO† vs FREE-AIR TEMPERATURE

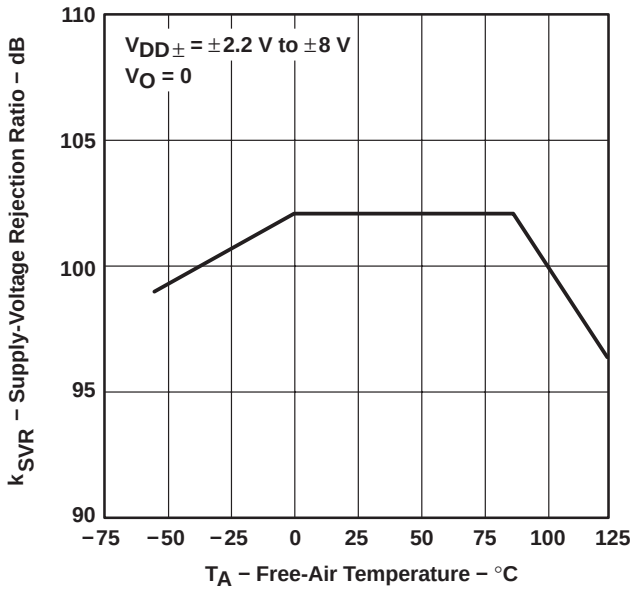


Figure 36

TLC2262 SUPPLY CURRENT† vs SUPPLY VOLTAGE

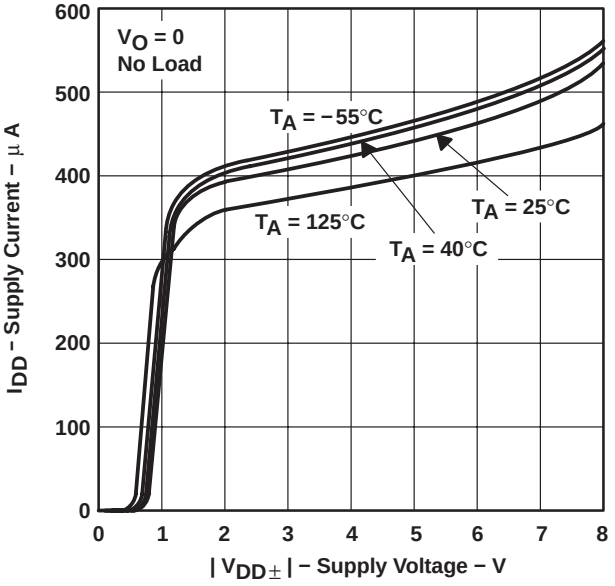


Figure 37

TLC2264 SUPPLY CURRENT† vs SUPPLY VOLTAGE

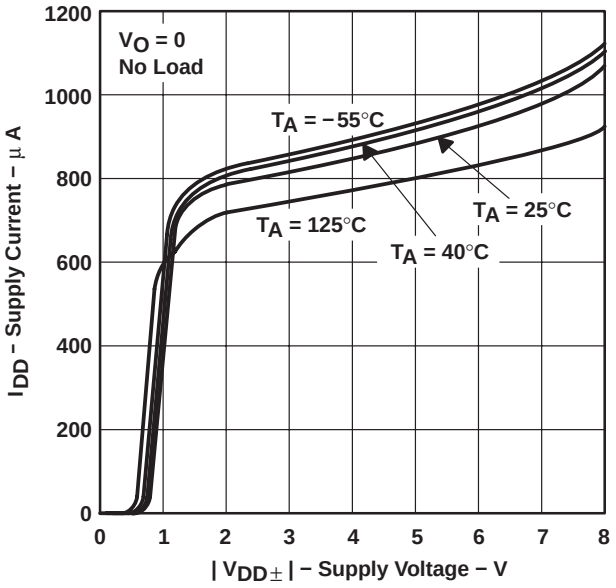


Figure 38

TLC2262 SUPPLY CURRENT†‡ vs FREE-AIR TEMPERATURE

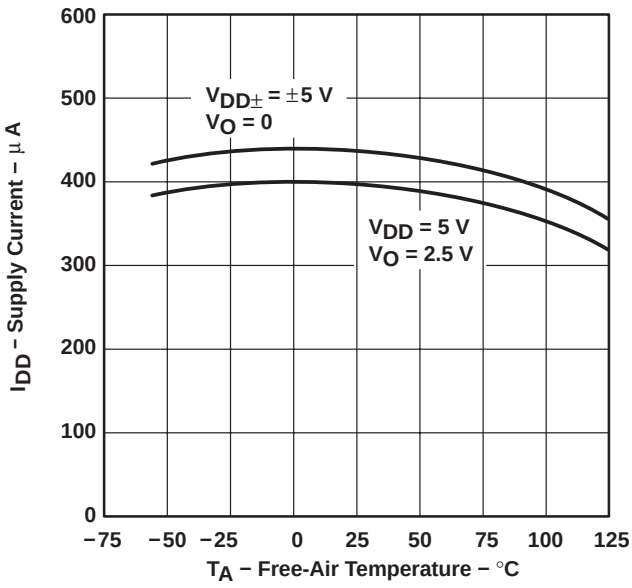


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

TLC2264
SUPPLY CURRENT†‡
vs
FREE-AIR TEMPERATURE

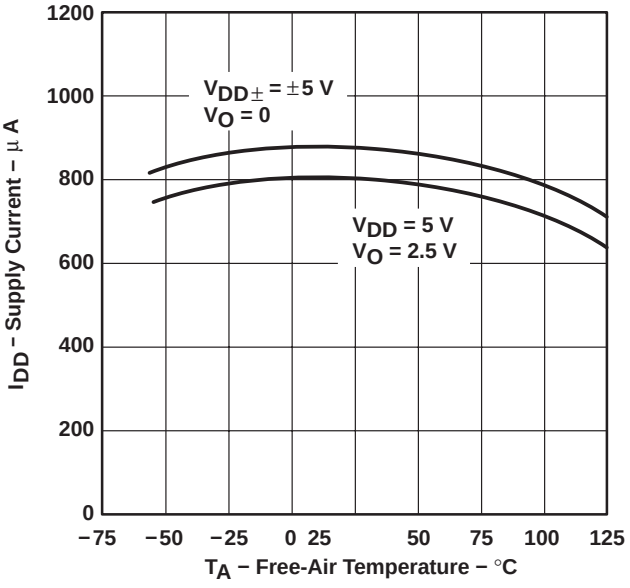


Figure 40

SLEW RATE‡
vs
LOAD CAPACITANCE

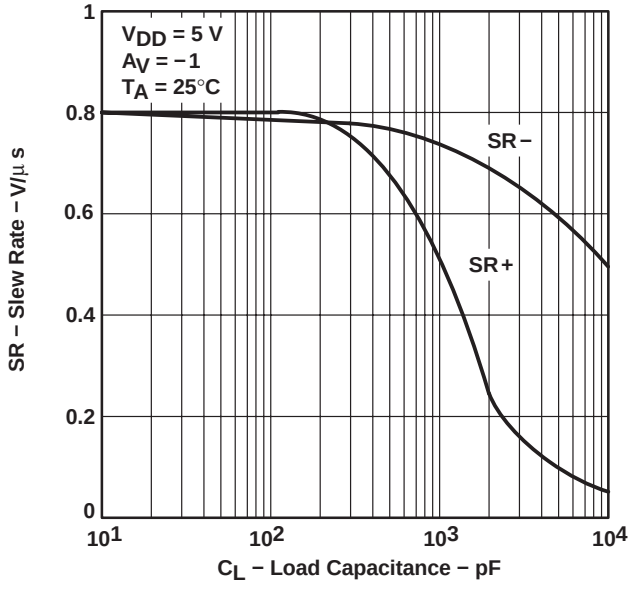


Figure 41

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

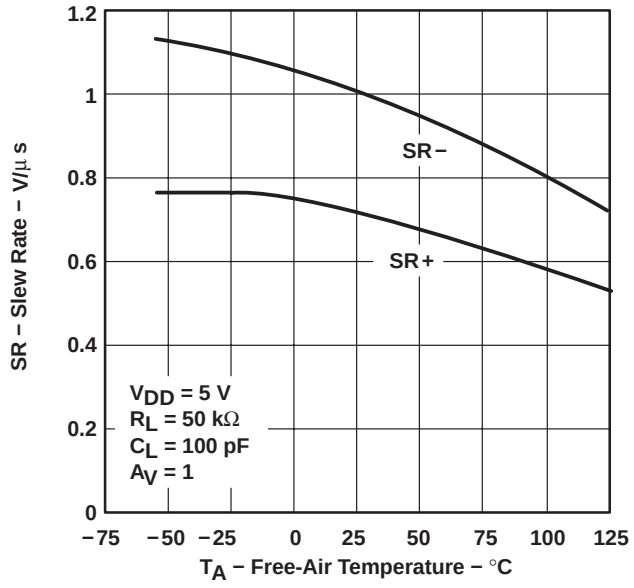


Figure 42

INVERTING LARGE-SIGNAL PULSE
RESPONSE‡

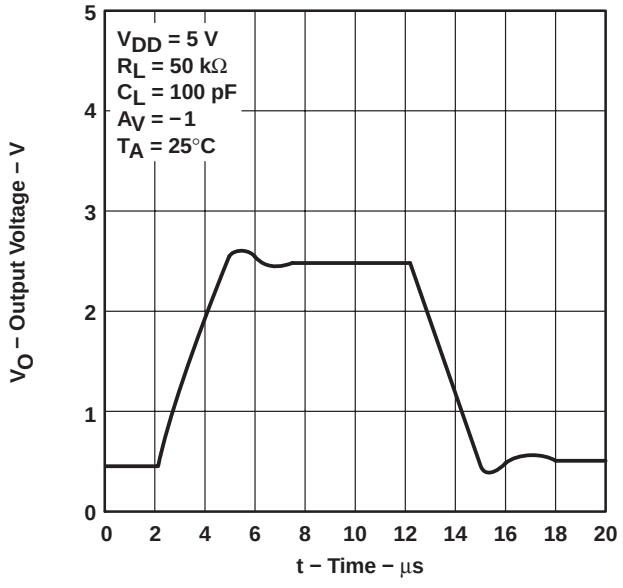


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

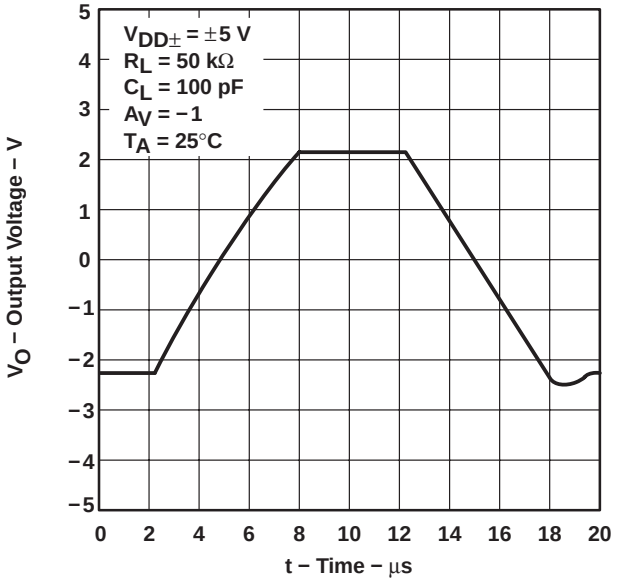


Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

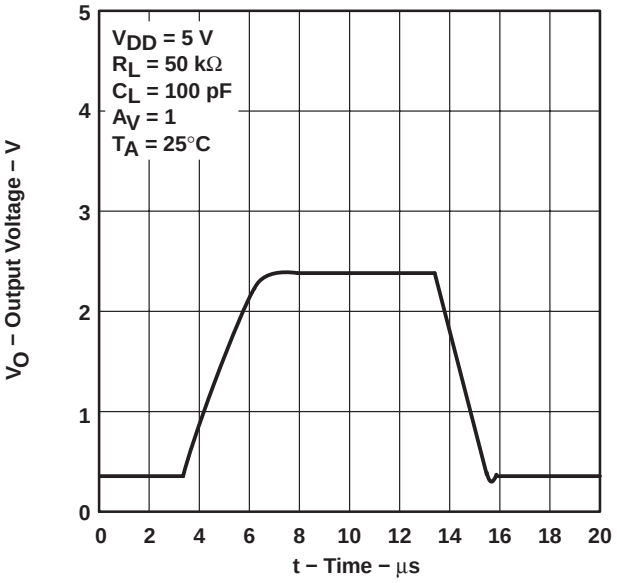


Figure 45

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

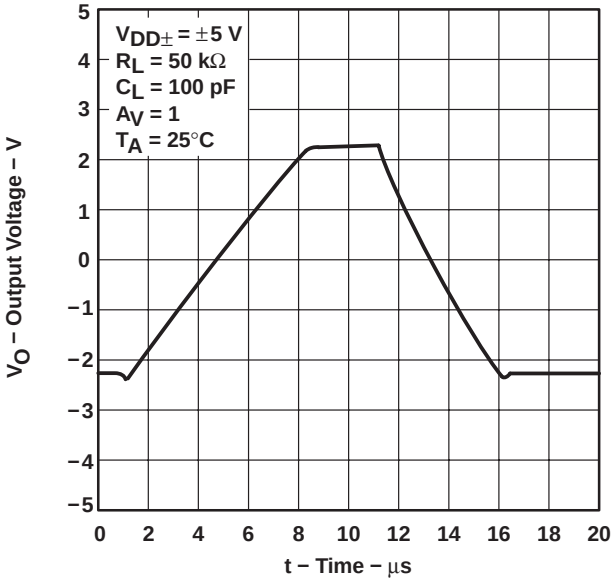


Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

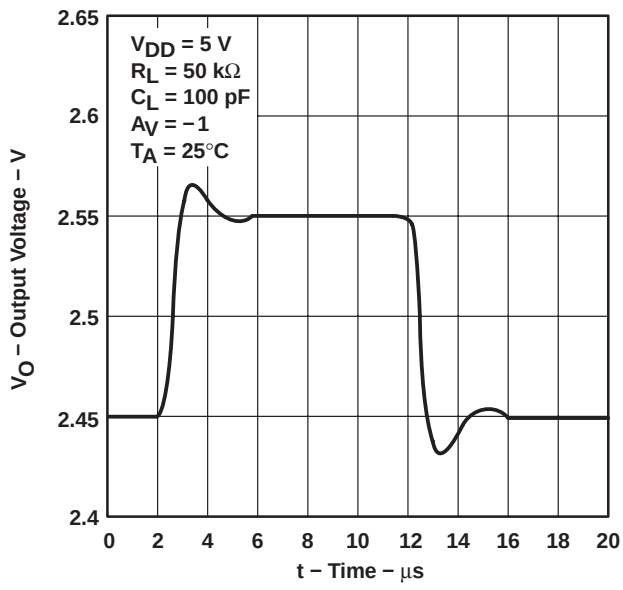


Figure 47

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

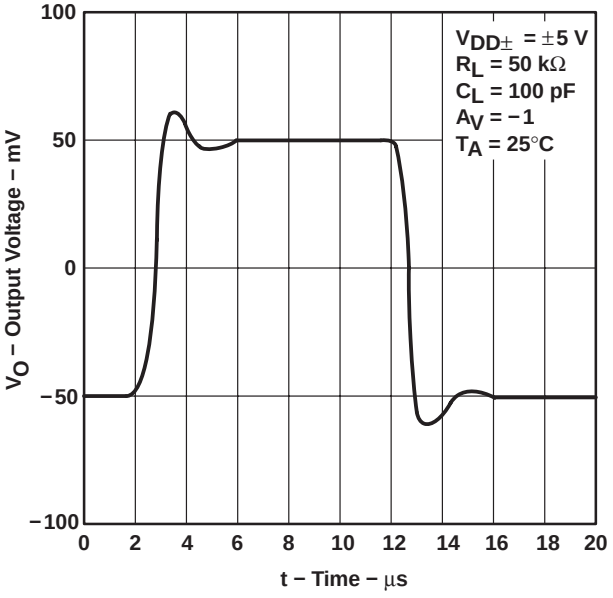


Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

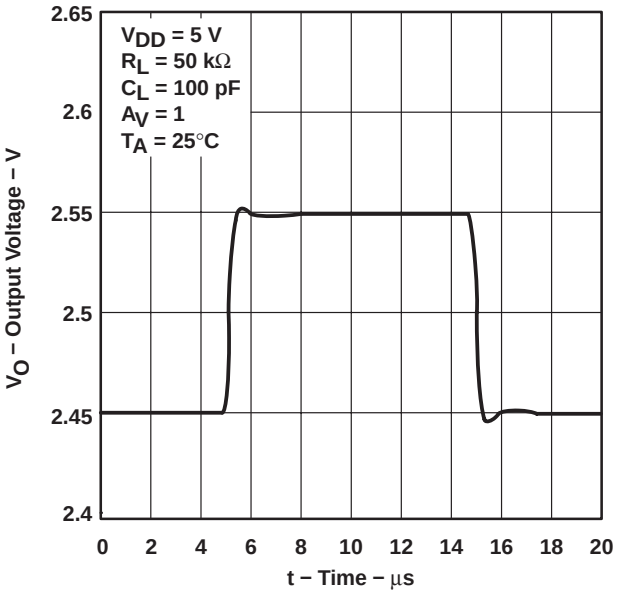


Figure 49

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

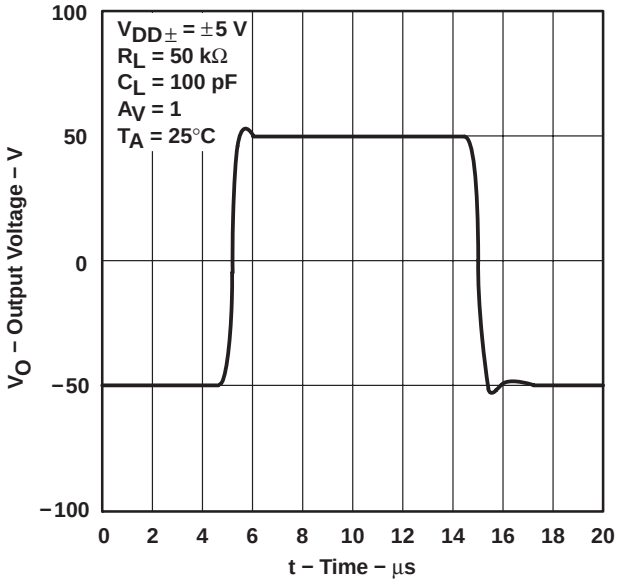


Figure 50

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

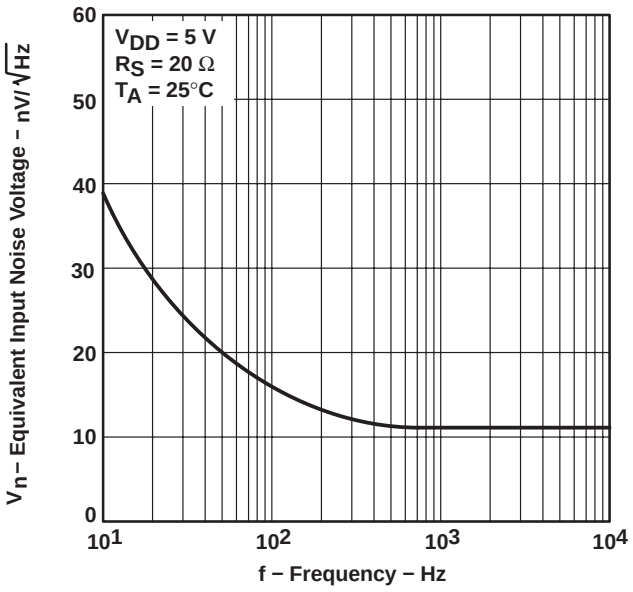


Figure 51

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

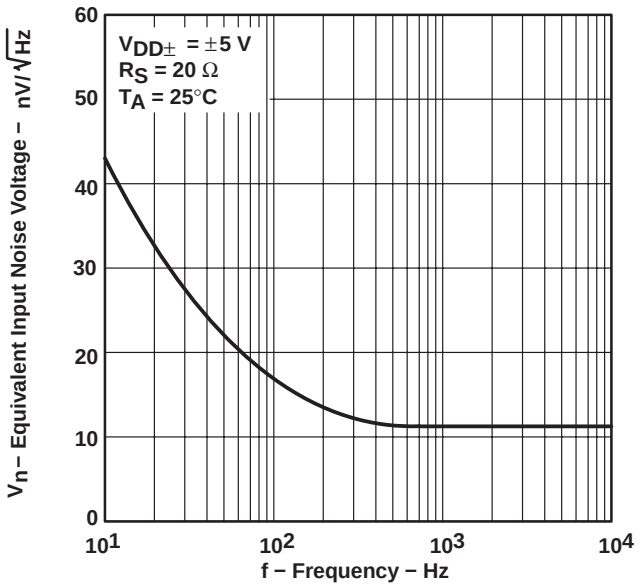


Figure 52

EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD†

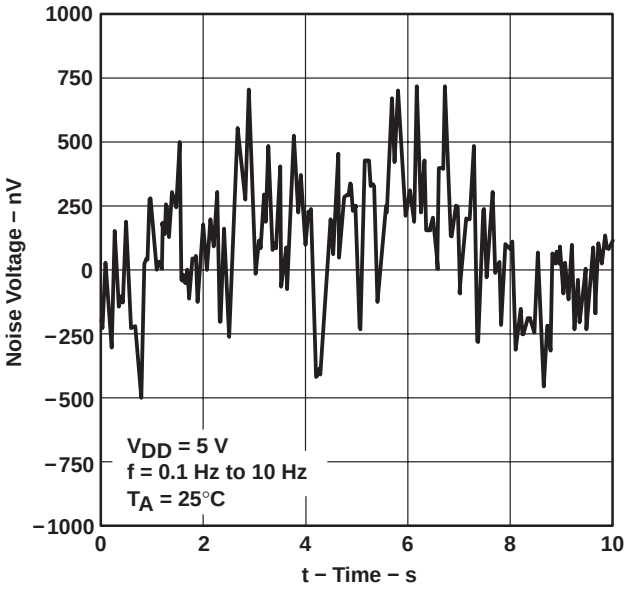


Figure 53

INTEGRATED NOISE VOLTAGE vs FREQUENCY

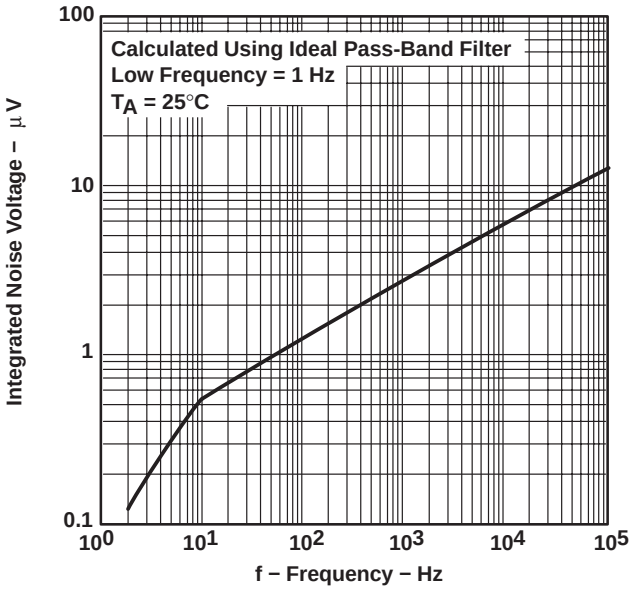


Figure 54

TOTAL HARMONIC DISTORTION PLUS NOISE† vs FREQUENCY

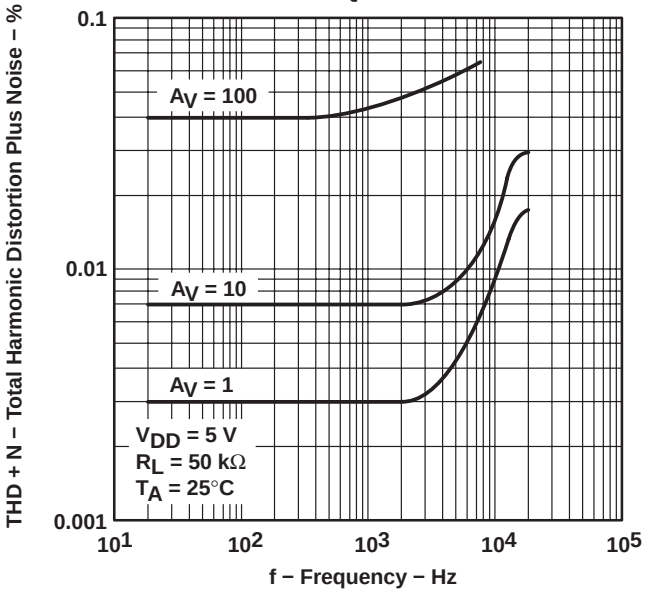


Figure 55

† For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

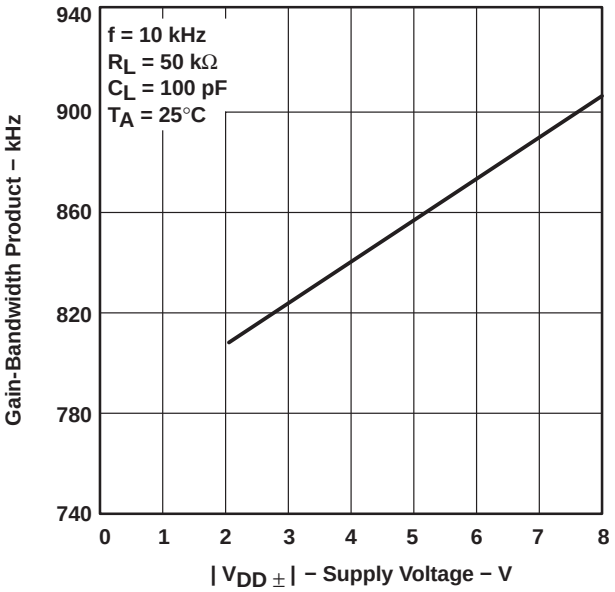


Figure 56

GAIN-BANDWIDTH PRODUCT†‡ vs FREE-AIR TEMPERATURE

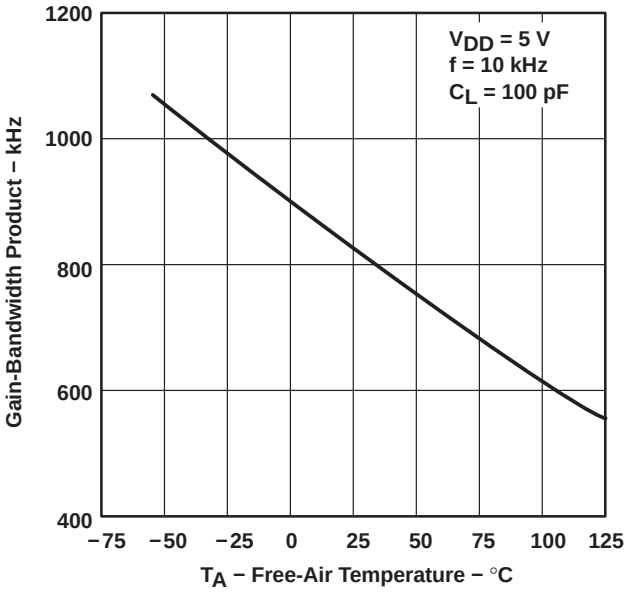


Figure 57

PHASE MARGIN vs LOAD CAPACITANCE

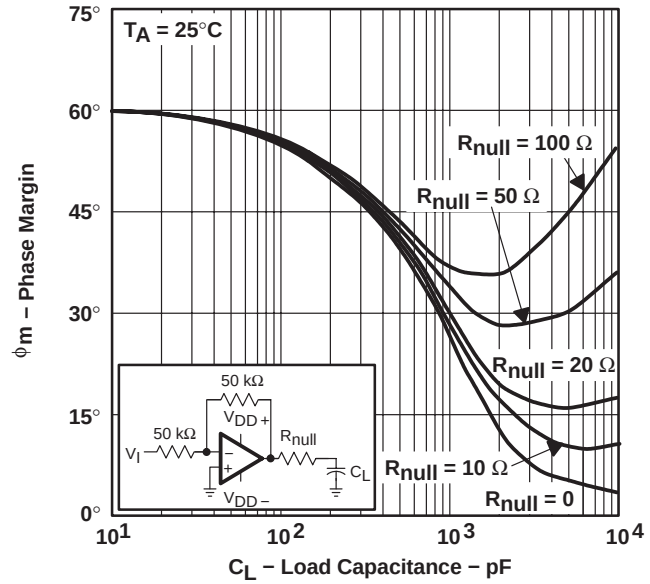


Figure 58

GAIN MARGIN vs LOAD CAPACITANCE

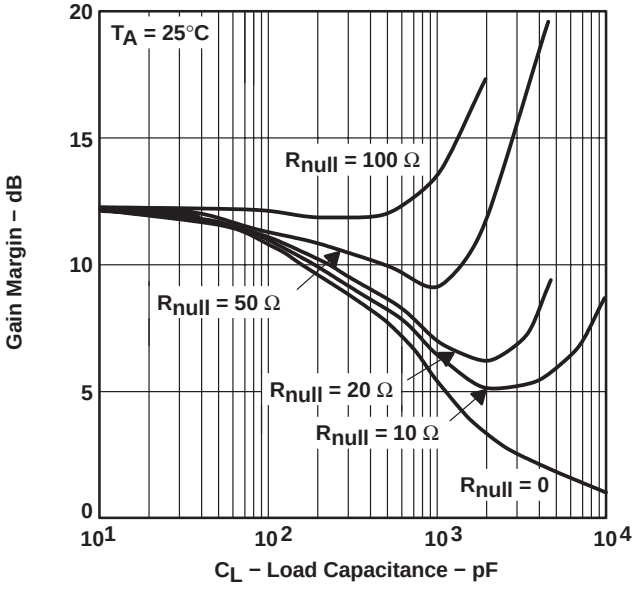


Figure 59

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For curves where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH† vs LOAD CAPACITANCE

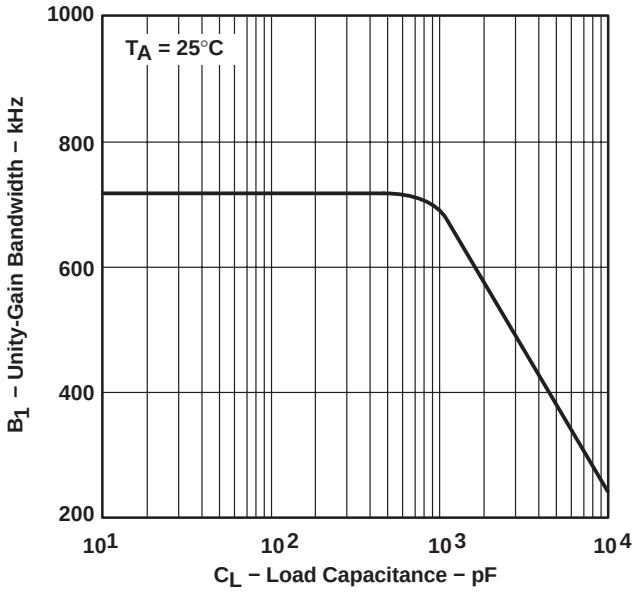


Figure 60

OVERESTIMATION OF PHASE MARGIN† vs LOAD CAPACITANCE

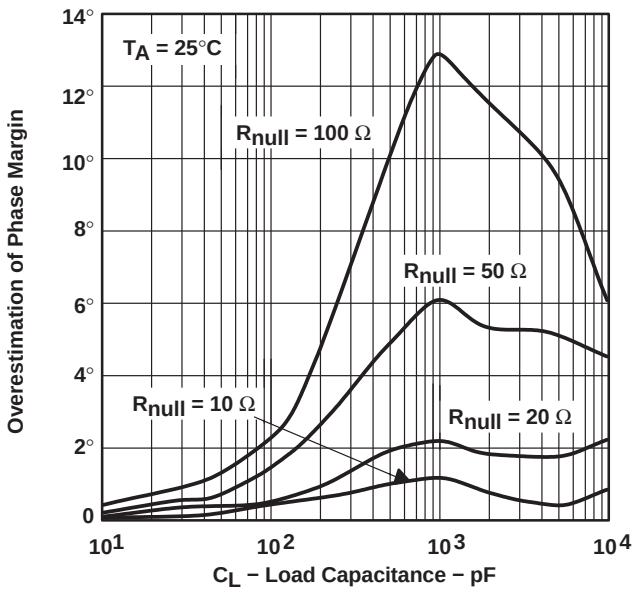


Figure 61

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 58 and Figure 59 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 62) improves the gain and phase margins when driving large capacitive loads. Figure 58 and Figure 59 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\Theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

Where :

$\Delta\Theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 60). To use equation 1, UGBW must be approximated from Figure 60.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 61. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

Where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 70 MHz, at C_L = 1000 pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\Theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

Where :

$\Delta\Theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation 2

P_2 = unadjusted pole (70 MHz@10 pF, 7 MHz@100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

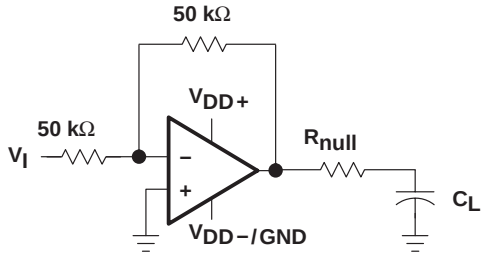


Figure 62. Series-Resistance Circuit

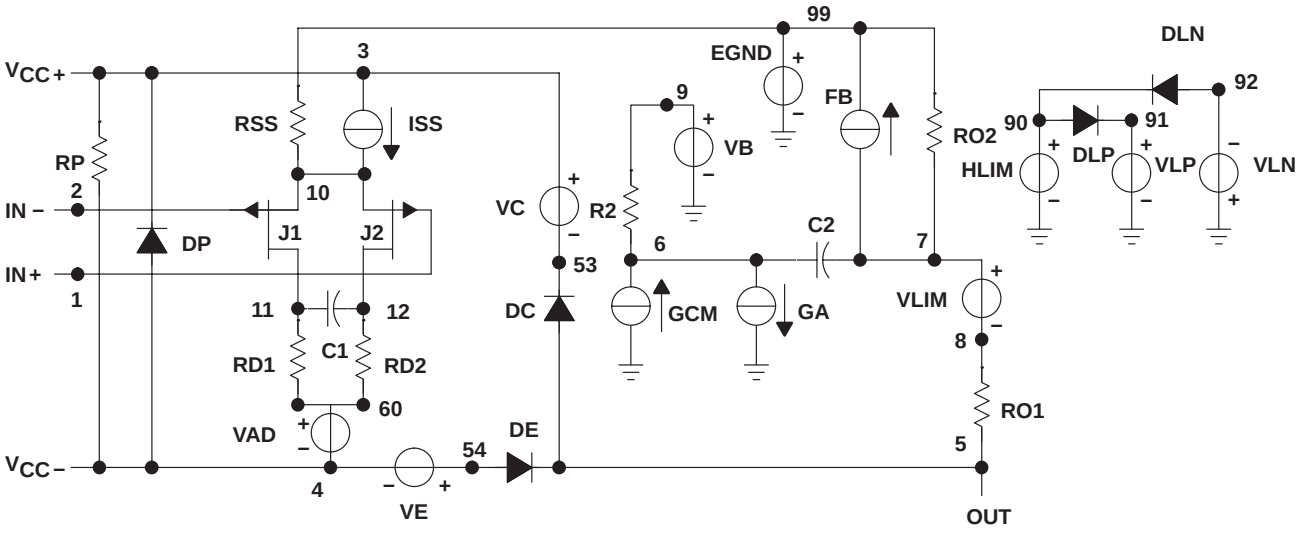
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 63 are generated using the TLC226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLC226x 1 2 3 4 5
C1      11      12      3.560E−12
C2      6       7       15.00E−12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB      7       99      POLY (5) VB VC VE VLP
+ VLN 0 21.04E6 −30E6 30E6 30E6 −30E6
GA      6       0       11      12 47.12E−6
GCM     0       6       10      99 4.9E−9
ISS     3       10      DC 8.250E−6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.0E3
RD1     60      11      21.22E3
RD2     60      12      21.22E3
R01     8       5       120
R02     7       99      120
RP      3       4       26.04E3
RSS     10      99      24.24E6
VAD     60      4       −.6
VB      9       0       DC 0
VC      3       53      DC .65
VE      54      4       DC .65
VLIM    7       8       DC 0
VLP     91      0       DC 1.4
VLN     0       92      DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=500.0E−15 BETA=281E−6
+ VTO= −.065)
.ENDS
```

Figure 63. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2264AQPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQPWRG4Q1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ
TLC2264AQPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2264A-Q1 :

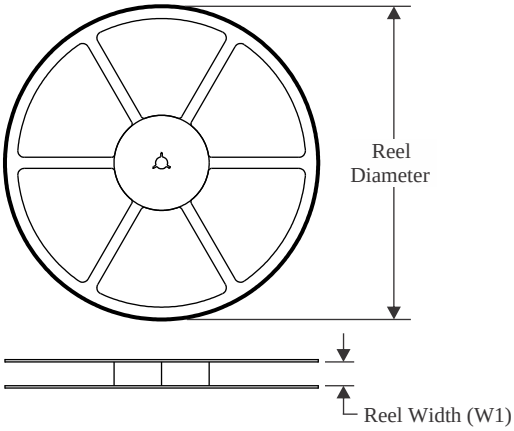
- Catalog : TLC2264A
- Military : TLC2264AM

NOTE: Qualified Version Definitions:

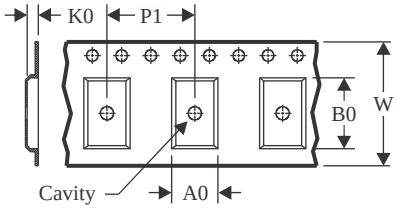
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

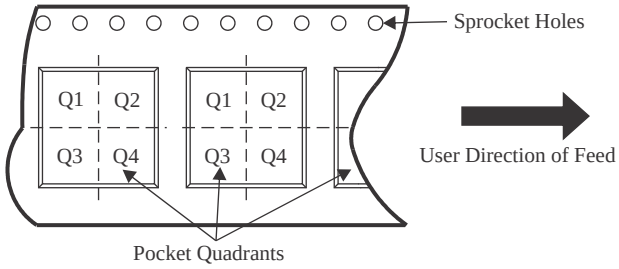


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

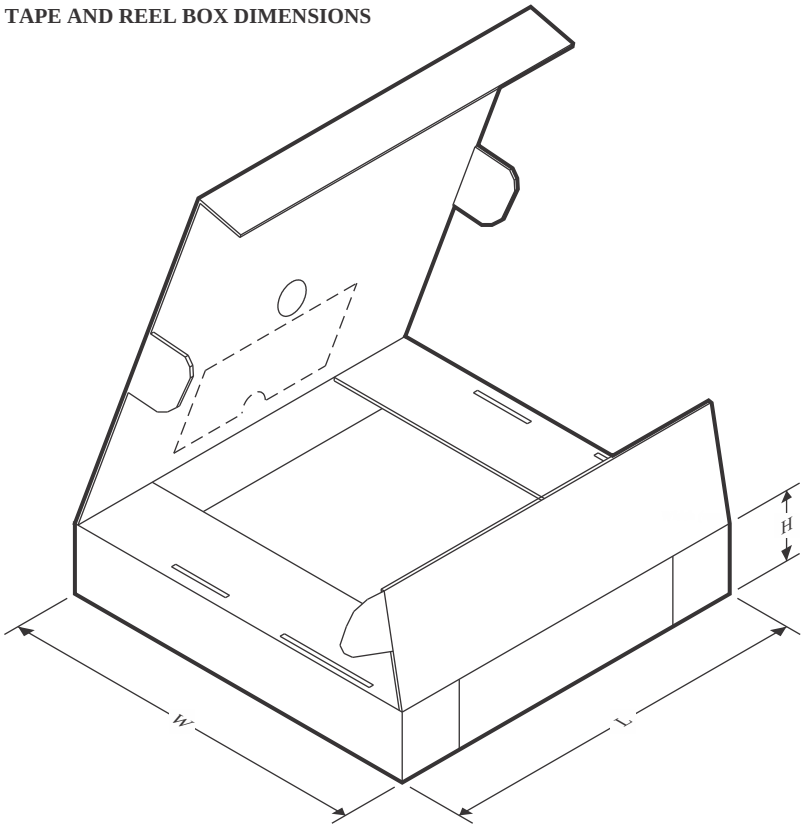
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2264AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

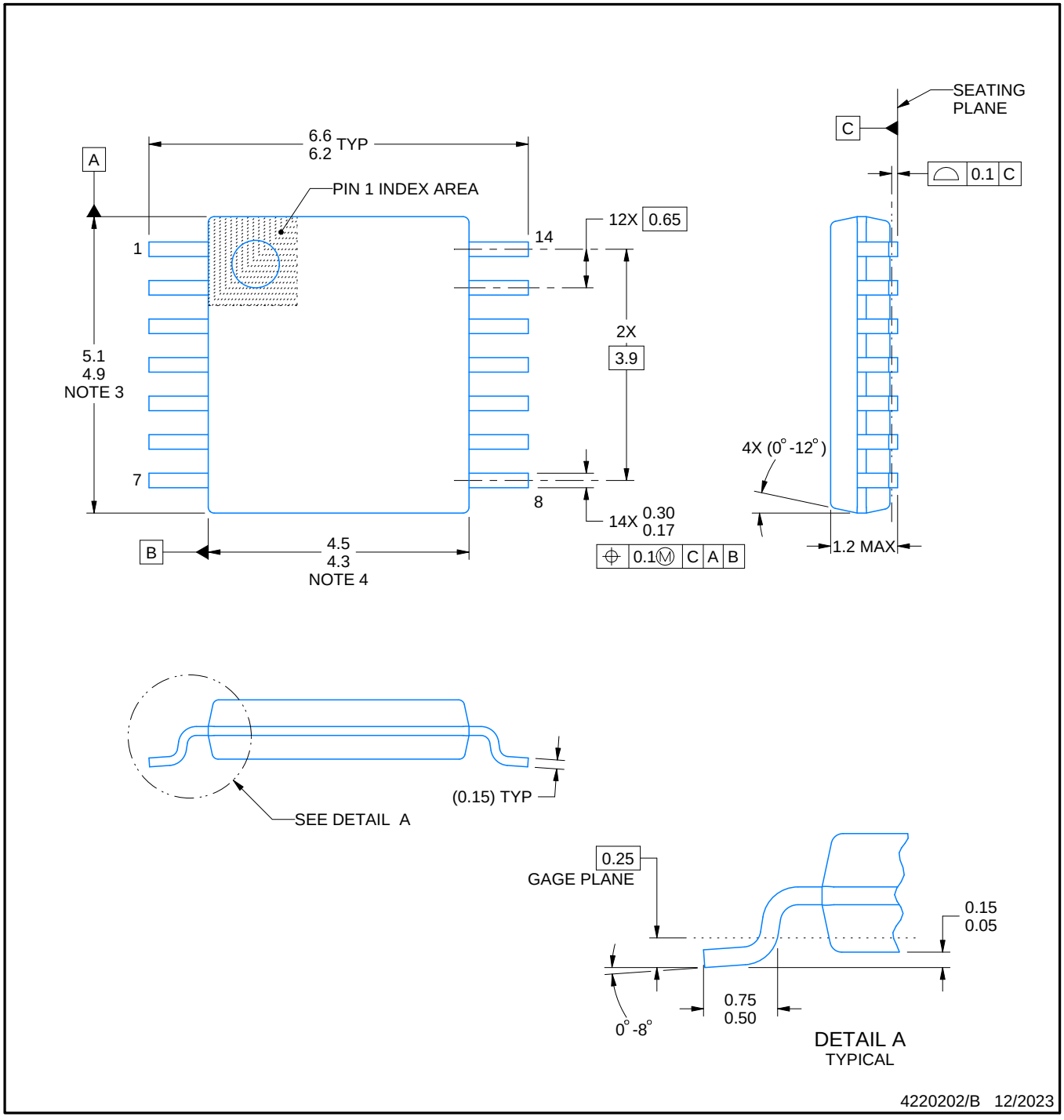
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2264AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2264AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0014A

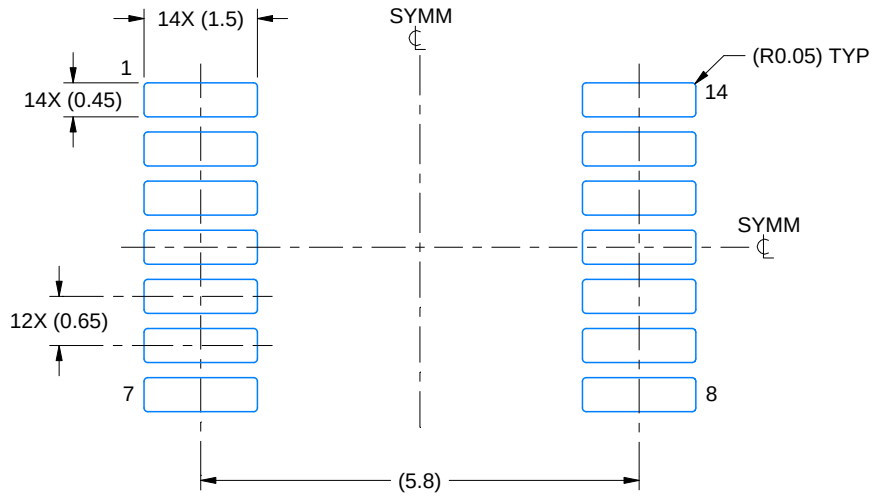
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

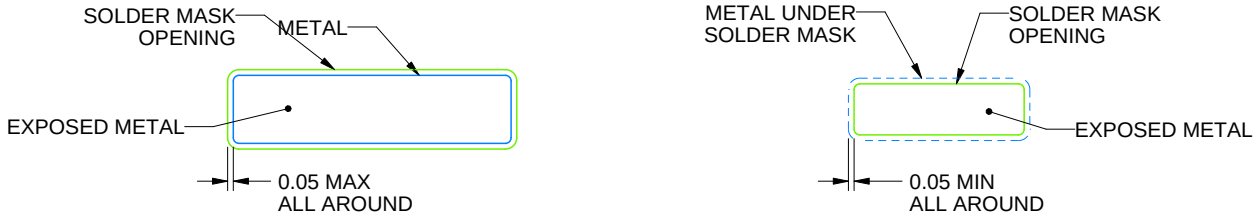


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

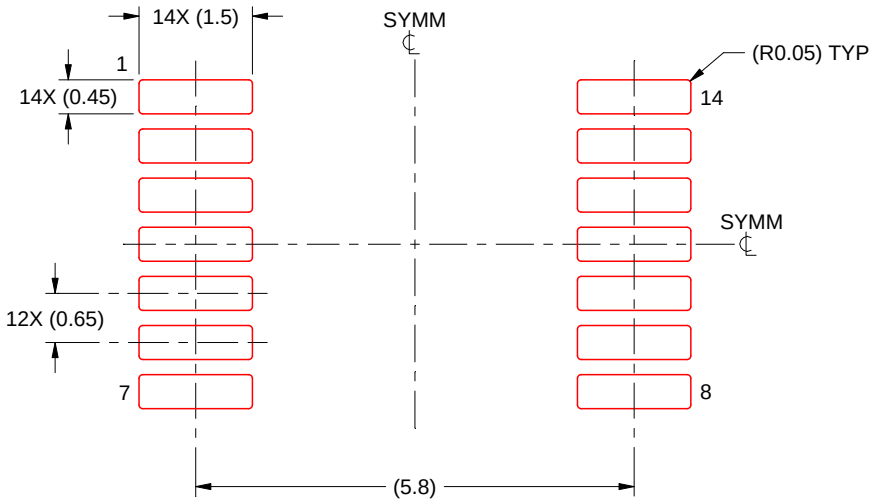


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025