

TLC227x-EP, TLC227xA-EP Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SGLS131B – JULY 2002 – REVISED DECEMBER 2003

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Output Swing Includes Both Supply Rails**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description

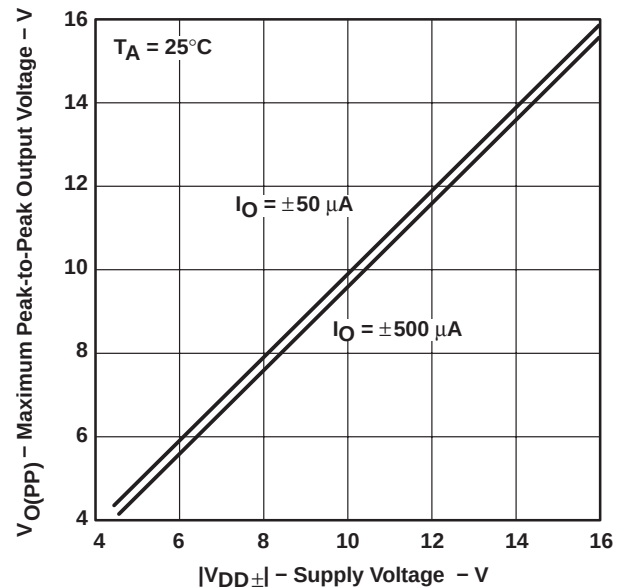
The TLC2272A and TLC2274A are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227xA family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227xA has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC227xA, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications.

- **Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage**
950 μV Max at T_A = 25°C
- **Macromodel Included**
- **Performance Upgrades for the TS272, TS274, TLC272, and TLC274**

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
VS
SUPPLY VOLTAGE



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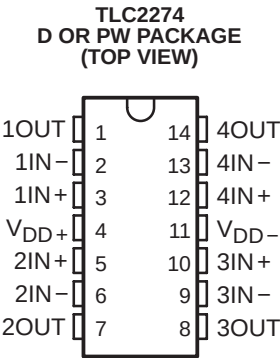
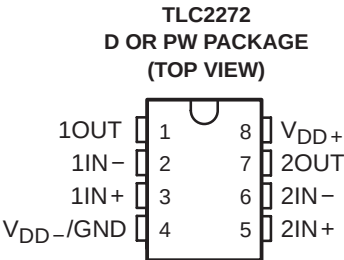
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AVAILABLE OPTIONS

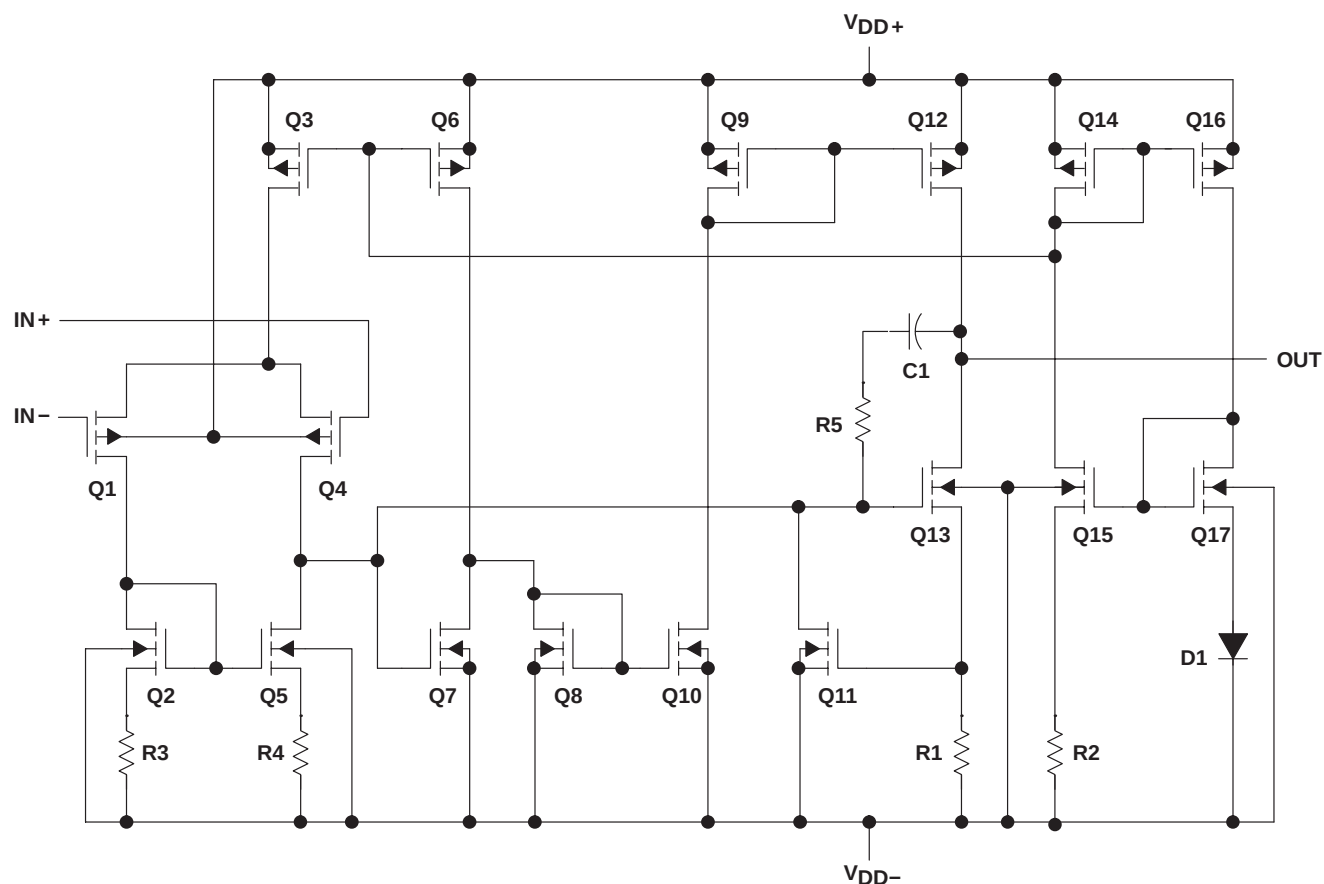
T _A	V _{IO} max At 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
-55°C to 125°C	950 µV 2.5 mV	TLC2272AMDREP TLC2272MDREP	TLC2272AMPWREP TLC2272MPWREP
-55°C to 125°C	950 µV 2.5 mV	TLC2274AMDREP TLC2274MDREP	TLC2274AMPWREP TLC2274MPWREP



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equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2272	TLC2274
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage range, V_I (any input, see Note 1)	$V_{DD-} - 0.3 \text{ V}$ to V_{DD+}
Input current, I_I (any input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range (see Note 4)	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or PW package	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current will flow if input is brought below $V_{DD-} - 0.3 \text{ V}$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	337 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
PW-8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	448 mW	364 mW	—

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage, V_I	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	–55	125	°C



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TLC2272-EP electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272-EP			TLC2272A-EP			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, V _{DD±} = ±2.5 V, R _S = 50 Ω		25°C	300	2500		300	950		μV
	Full range				3000		1500				
α _{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C	2			2			μV/°C
	Input offset voltage long-term drift (see Note 5)			25°C	0.002			0.002			μV/mo
I _{IO}	Input offset current			25°C	0.5	60		0.5	60		pA
				Full range		800		800			
I _{IB}	Input bias current			25°C	1	60		1	60		pA
				Full range		800		800			
V _{ICR}	Common-mode input voltage	R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V _{OH}	High-level output voltage	I _{OH} = -20 μA		25°C	4.99			4.99			V
		I _{OH} = -200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I _{OH} = -1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 50 μA		25°C	0.01			0.01			V
		V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	0.09	0.15		0.09	0.15		
				Full range		0.15			0.15		
		V _{IC} = 2.5 V, I _{OL} = 5 mA		25°C	0.9	1.5		0.9	1.5		
				Full range		1.5			1.5		
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 10 kΩ [‡]	25°C	10	35		10	35		V/mV
				Full range	10			10			
			R _L = 1 mΩ [‡]	25°C	175			175			
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²		Ω	
r _i	Common-mode input resistance			25°C	10 ¹²			10 ¹²		Ω	
c _i	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8			8		pF	
z _o	Closed-loop output impedance	f = 1 MHz,	A _V = 10	25°C	140			140		Ω	
CMRR	Common-mode rejection ratio	V _{IC} = 0 V to 2.7 V, V _O = 2.5 V, R _S = 50 Ω		25°C	70	75		70	75		dB
				Full range	70			70			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 16 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	2.2	3		2.2	3		mA
				Full range		3			3		

[†] Full range is -55°C to 125°C for M level part.

[‡] Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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TLC2272-EP operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2272-EP			TLC2272A-EP			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.25 V to 2.75 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	50			50			nV/√Hz
		f = 1 kHz		25°C	9			9			
V _{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1			1			μV
		f = 0.1 Hz to 10 Hz		25°C	1.4			1.4			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 10 kΩ [‡] ,	A _V = 1	25°C	0.0013%			0.0013%			
			A _V = 10		0.004%			0.004%			
			A _V = 100		0.03%			0.03%			
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF [‡] , R _L = 10 kΩ [‡] ,		25°C	2.18			2.18			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 10 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	1			1			MHz
t _s	Settling time	A _V = −1, Step = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]	To 0.1%	25°C	1.5			1.5			μs
			To 0.01%		2.6			2.6			
ϕ _m	Phase margin at unity gain	R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	50°			50°			
	Gain margin			25°C	10			10			dB

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

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TLC2272-EP electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2272-EP			TLC2272A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C		300	2500		300	950	μV
		Full range			3000			1500	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C		2			2		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 5)		25°C		0.002			0.002		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		Full range			800			800	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		Full range			800			800	
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_O = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_O = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V}, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99		V
		25°C	-4.85	-4.91		-4.85	-4.91		
	$V_{IC} = 0\text{ V}, I_O = 500\ \mu\text{A}$	Full range	-4.85			-4.85			
		25°C	-3.5	-4.1		-3.5	-4.1		
	$V_{IC} = 0\text{ V}, I_O = 5\text{ mA}$	Full range	-3.5			-3.5			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	25°C	20	50	20	50		V/mV
			Full range	20		20			
		$R_L = 1\text{ m}\Omega$	25°C	300		300			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ P package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		130			130		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	75	80		75	80		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0\text{ V}, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C		2.4	3		2.4	3	mA
		Full range			3			3	

† Full range is -55°C to 125°C for M level part.

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2272-EP operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2272-EP			TLC2272A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 1\text{ V}$, $C_L = 100\text{ pF}$ $R_L = 10\text{ k}\Omega$	25°C	2.3	3.6		2.3	3.6		V/ μs
		Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		50			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		1			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		1.4			1.4		
I_n	Equivalent input noise current			0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$ $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$		0.0011%			0.0011%		
		$A_V = 10$		0.004%			0.004%		
		$A_V = 100$		0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$ $R_L = 10\text{ k}\Omega$	25°C	2.25			2.25		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C	0.54			0.54		MHz
t_s	Settling time $A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C	1.5			1.5		μs
		To 0.01%		3.2			3.2		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	52°			52°		
	Gain margin		25°C	10			10		dB

† Full range is -55°C to 125°C for M level part.

TLC2274-EP electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2274-EP			TLC2274A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 2.5\text{ V}, V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range		3000			1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 5)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		800			800		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		800			800		
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99		V
	$I_{OH} = -200\ \mu\text{A}$	25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
	$I_{OH} = -1\text{ mA}$	25°C	4.25	4.65		4.25	4.65		
		Full range	4.25			4.25			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
		25°C	0.09	0.15		0.09	0.15		
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	Full range		0.15			0.15		
		25°C	0.9	1.5		0.9	1.5		
	$V_{IC} = 2.5\text{ V}, I_{OL} = 5\text{ mA}$	Full range		1.5			1.5		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega^\ddagger$	25°C	10	35	10	35		V/mV
			Full range	10		10			
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C	175		175			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_i Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C		140			140		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	75		70	75		dB
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	4.4	6		4.4	6		mA
		Full range		6			6		

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2274-EP operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274-EP			TLC2274A-EP			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain	V _O = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]	25°C	2.3	3.6		2.3	3.6		V/μs		
			Full range	1.7			1.7					
V _n	Equivalent input noise voltage	f = 10 Hz	25°C	50			50			nV/√Hz		
		f = 1 kHz	25°C	9			9					
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C	1			1			μV		
		f = 0.1 Hz to 10 Hz	25°C	1.4			1.4					
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz	
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 20 kHz, R _L = 10 kΩ [‡]	A _V = 1	25°C	0.0013%			0.0013%				
					A _V = 10	0.004%			0.004%			
						A _V = 100	0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF [‡]	R _L = 10 kΩ [‡]	25°C	2.18			2.18			MHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 10 kΩ [‡]	A _V = 1, C _L = 100 pF [‡]	25°C	1			1			MHz	
t _s	Settling time	A _V = −1, Step = 0.5 V to 2.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]	To 0.1%	25°C	1.5			1.5			μs	
			To 0.01%		2.6			2.6				
ϕ _m	Phase margin at unity gain	R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	50°			50°				
	Gain margin			25°C	10			10			dB	

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

TLC2274-EP electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2274-EP			TLC2274A-EP			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	V _{IC} = 0 V, V _O = 0 V, R _S = 50 Ω		25°C	300	2500		300	950	μV		
	Full range				3000		1500					
αV _{IO}	Temperature coefficient of input offset voltage			25°C to 125°C	2			2		μV/°C		
	Input offset voltage long-term drift (see Note 5)			25°C	0.002			0.002		μV/mo		
I _{IO}	Input offset current			25°C	0.5	60		0.5	60	pA		
				Full range		800		800				
I _{IB}	Input bias current			25°C	1	60		1	60	pA		
				Full range		800		800				
V _{ICR}	Common-mode input voltage			R _S = 50 Ω, V _{IO} ≤ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2	V
						Full range		−5 to 3.5		−5 to 3.5		
V _{OM+}	Maximum positive peak output voltage	I _O = −20 μA		25°C	4.99			4.99	V			
		I _O = −200 μA		25°C	4.85	4.93		4.85		4.93		
				Full range	4.85			4.85				
		I _O = −1 mA	25°C	4.25	4.65		4.25	4.65				
Full range	4.25				4.25							
V _{OM−}	Maximum negative peak output voltage	V _{IC} = 0 V, I _O = 50 μA		25°C	−4.99			−4.99	V			
		V _{IC} = 0 V, I _O = 500 μA		25°C	−4.85	−4.91		−4.85		−4.91		
				Full range	−4.85			−4.85				
		V _{IC} = 0 V, I _O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1				
			Full range	−3.5			−3.5					
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V	R _L = 10 kΩ	25°C	20	50		20	50	V/mV		
				Full range	20			20				
			R _L = 1 MΩ	25°C	300			300				
r _{id}	Differential input resistance			25°C	10 ¹²			10 ¹²		Ω		
r _i	Common-mode input resistance			25°C	10 ¹²			10 ¹²		Ω		
c _i	Common-mode input capacitance	f = 10 kHz, N package		25°C	8			8		pF		
z _o	Closed-loop output impedance	f = 1 MHz, A _V = 10		25°C	130			130		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = −5 V to 2.7 V V _O = 0 V, R _S = 50 Ω		25°C	75	80		75	80	dB		
				Full range	75			75				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ± 2.2 V to ±8 V, V _{IC} = 0 V, No load		25°C	80	95		80	95	dB		
				Full range	80			80				
I _{DD}	Supply current	V _O = 0 V, No load		25°C	4.8	6		4.8	6	mA		
				Full range		6			6			

† Full range is -55°C to 125°C for M level part.

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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TLC2274-EP operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2274-EP			TLC2274A-EP			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C	2.3	3.6		2.3	3.6		V/ μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		50			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		1			1		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C		0.0011%			0.0011%		
			$A_V = 10$			0.004%			0.004%		
			$A_V = 100$			0.03%			0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C		2.25			2.25		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54			0.54		MHz
t_s	Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unit gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is -55°C to 125°C for M level part.

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NOTE: For all graphs where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

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**DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE**

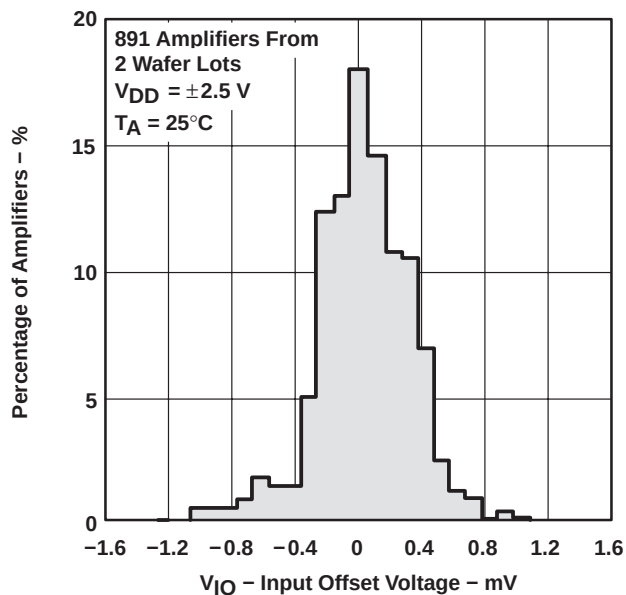


Figure 1

**DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE**

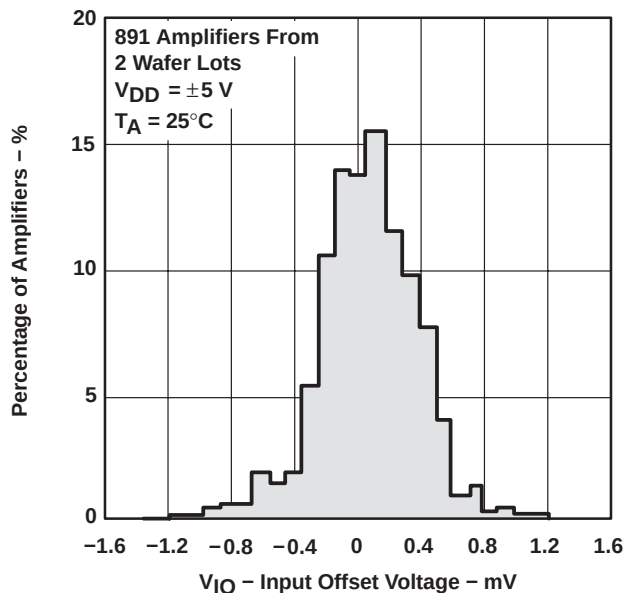


Figure 2

**DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE**

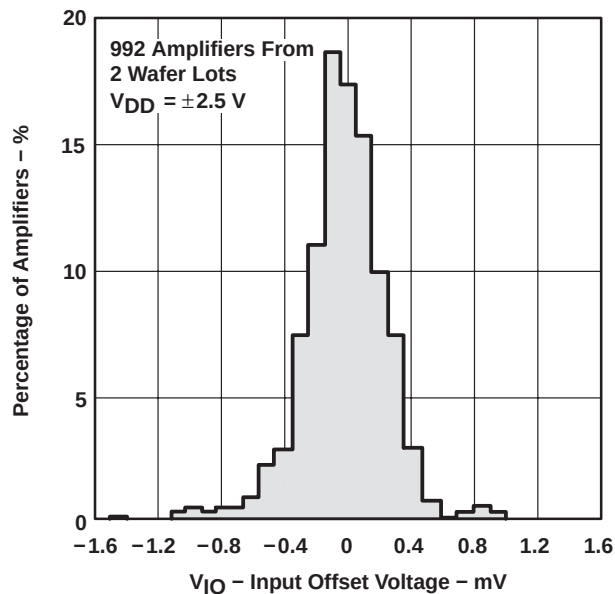


Figure 3

**DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE**

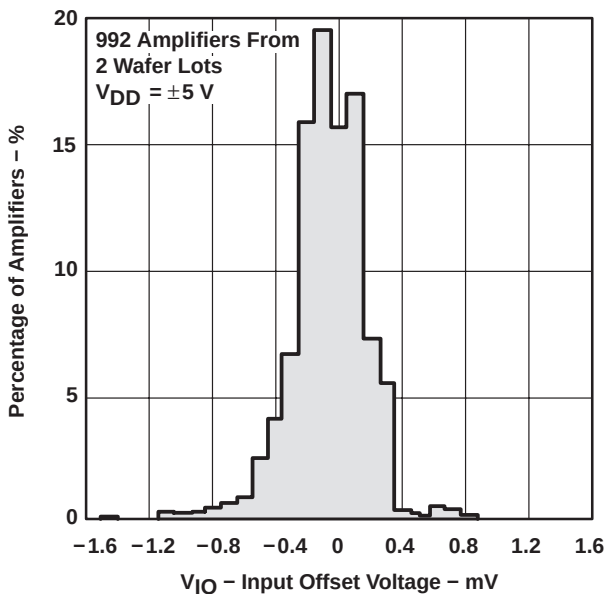
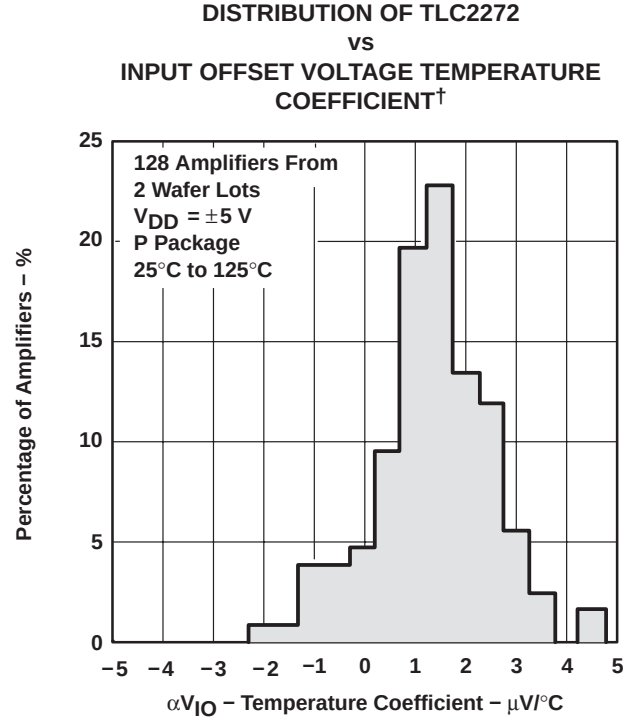
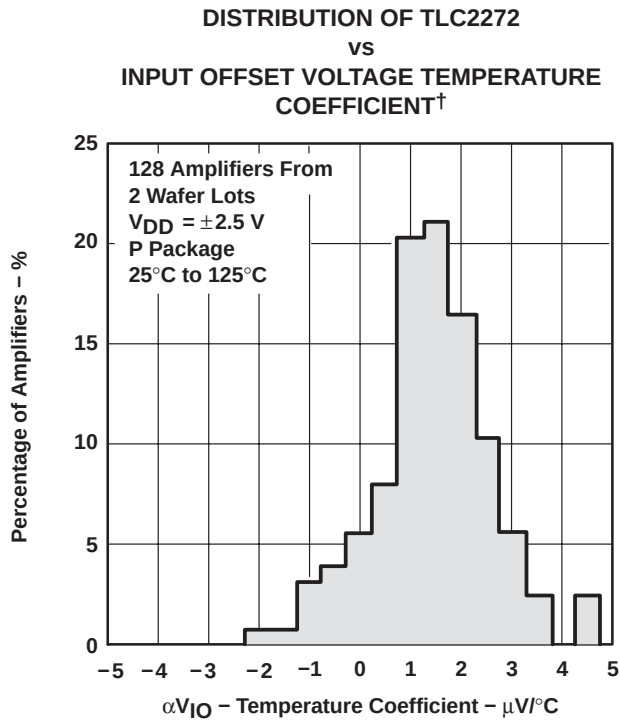
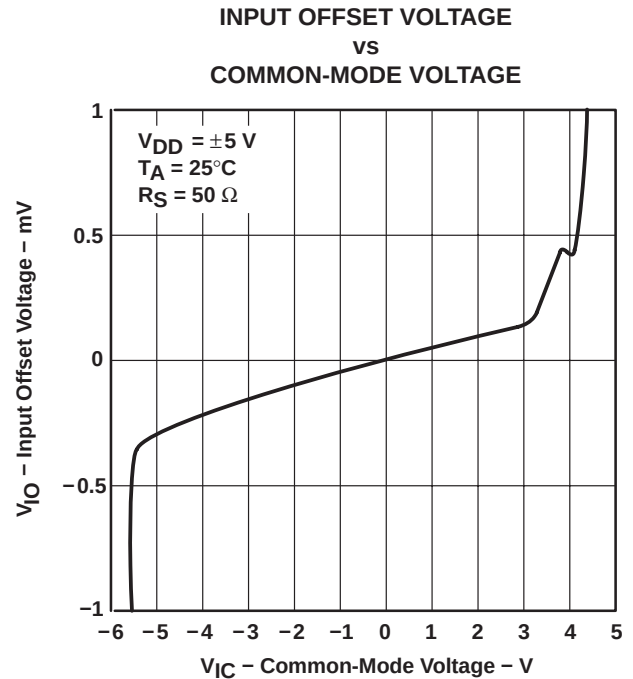
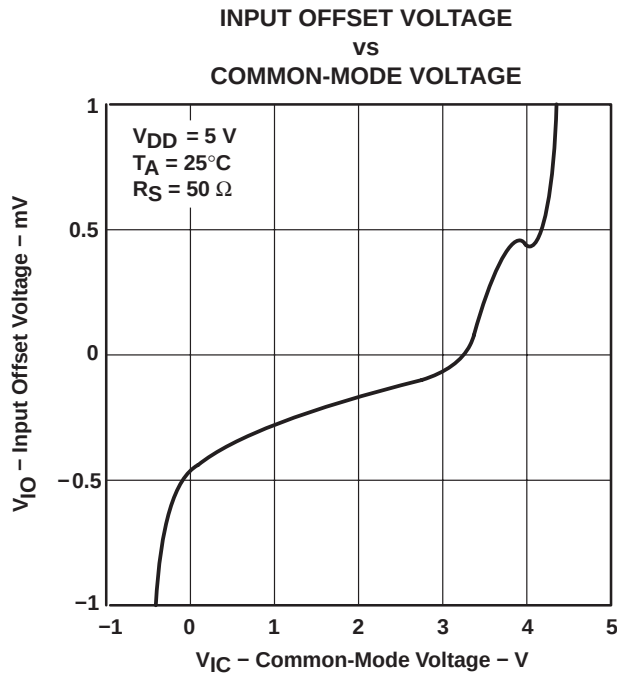


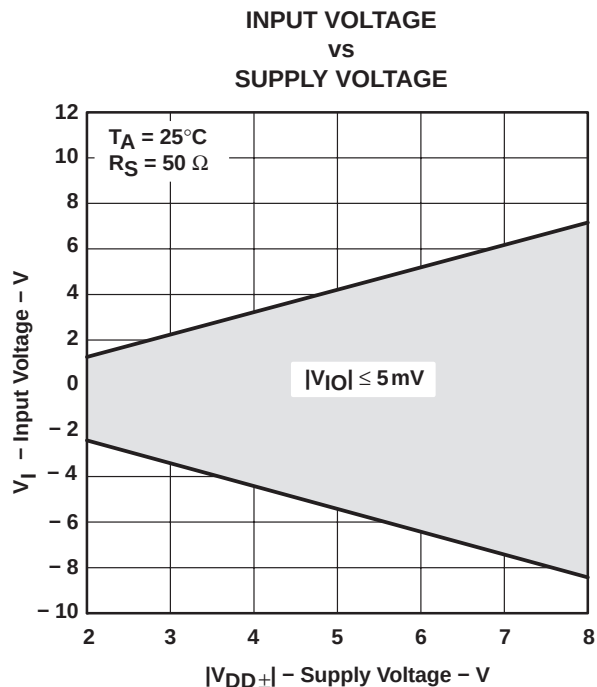
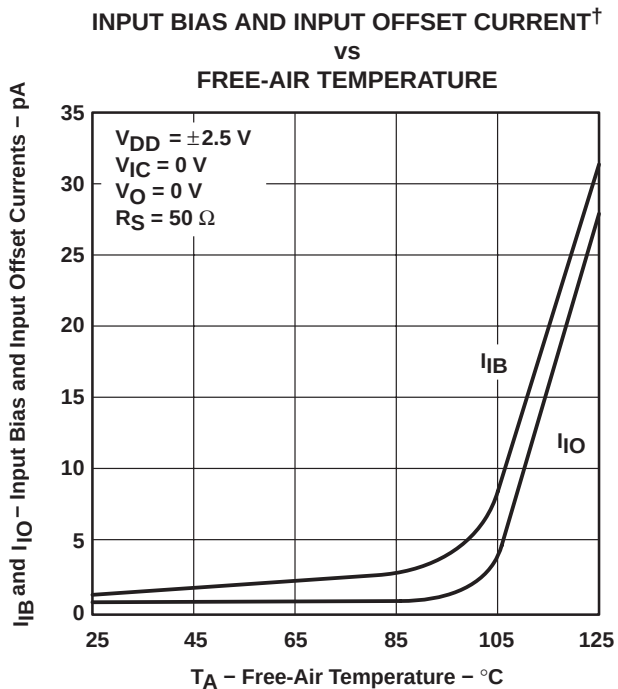
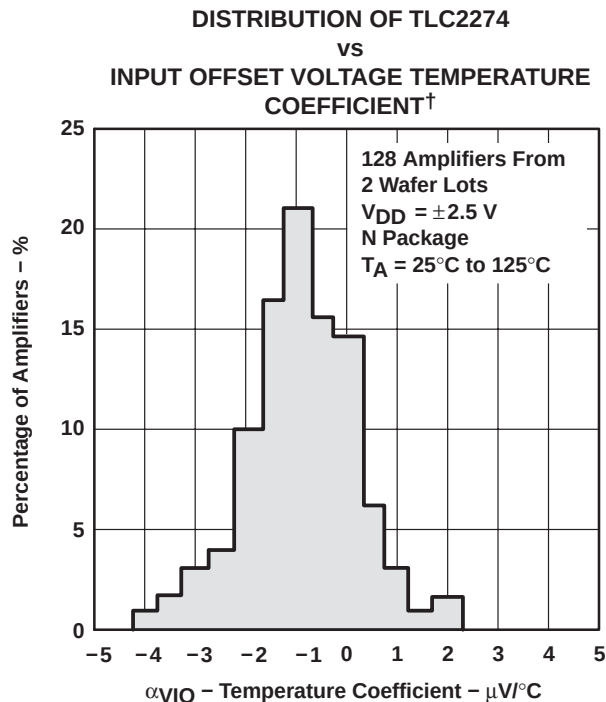
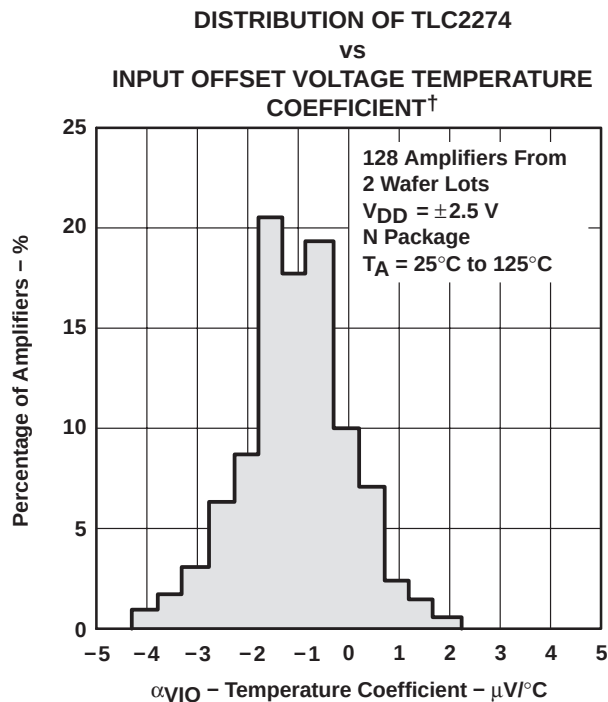
Figure 4

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

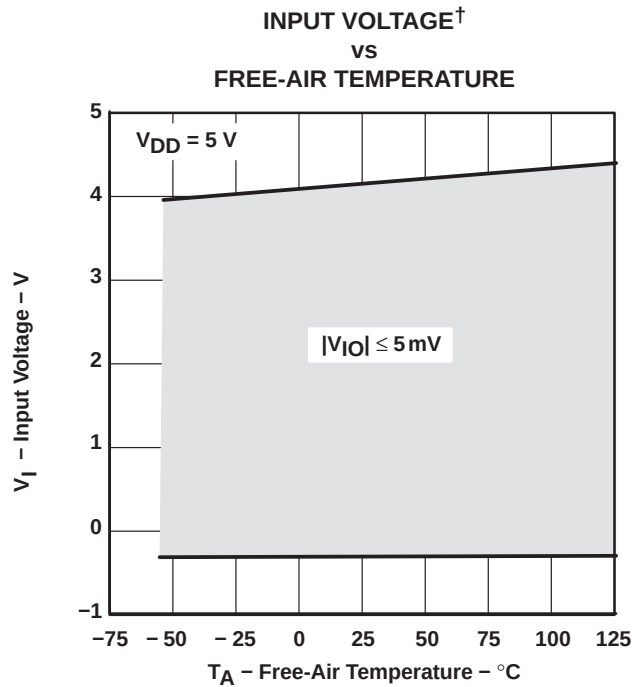


Figure 13

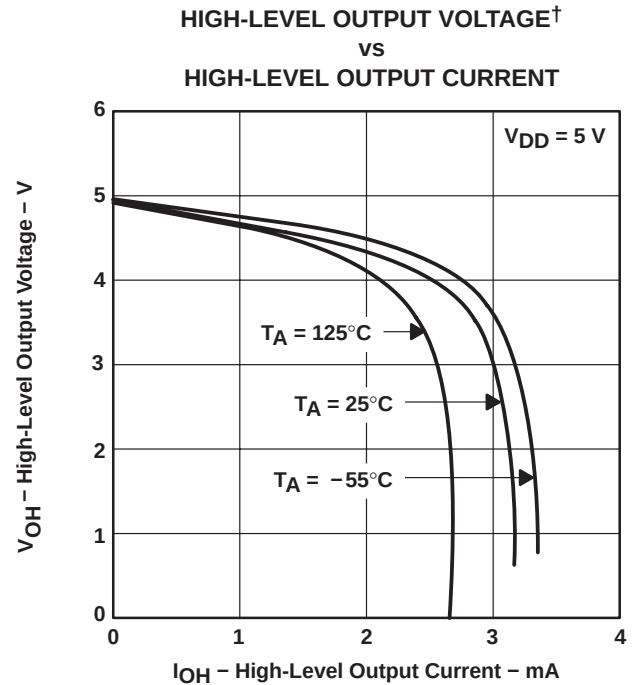


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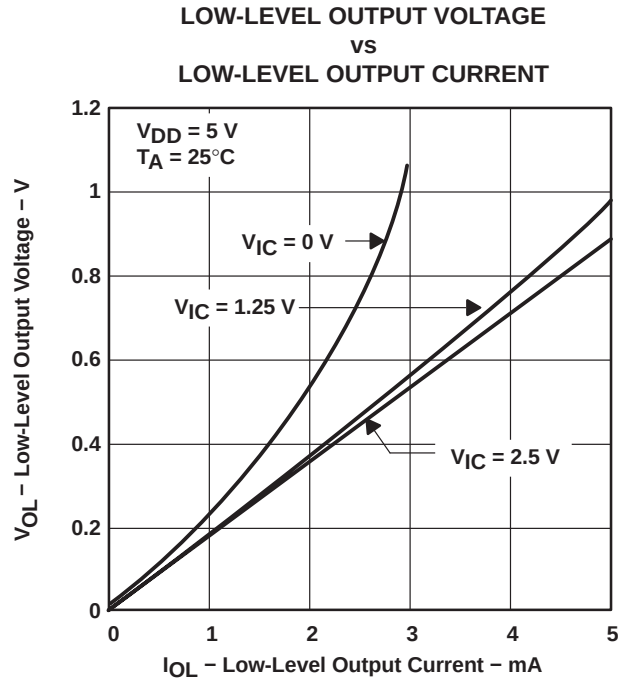


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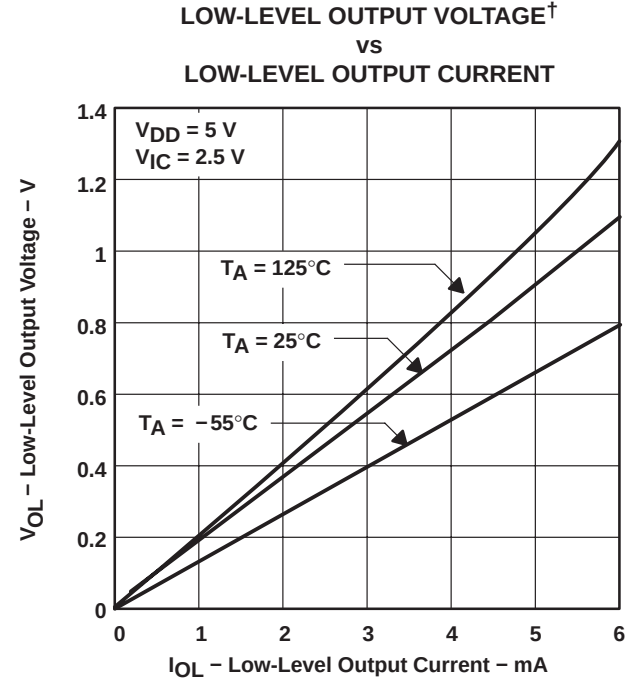


Figure 16

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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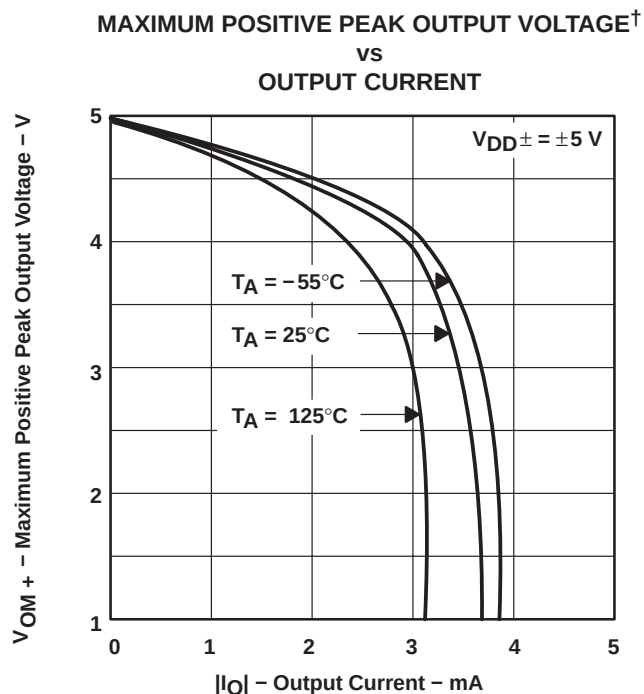


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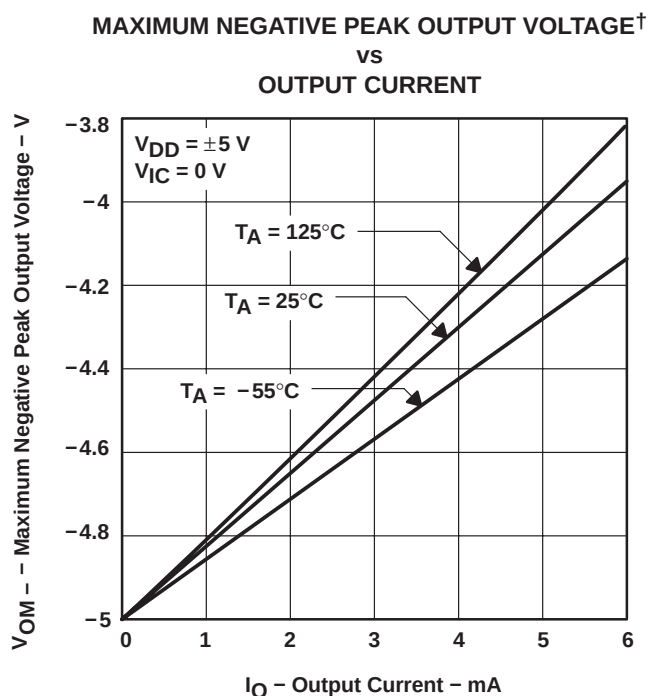


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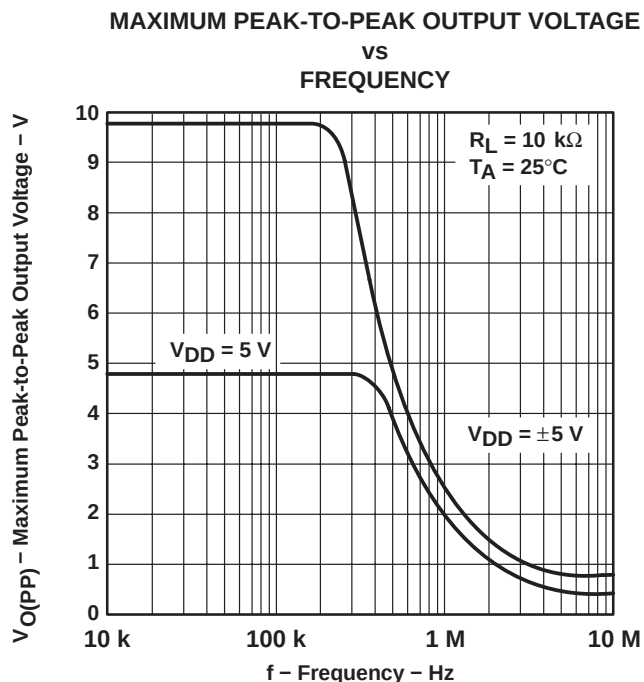


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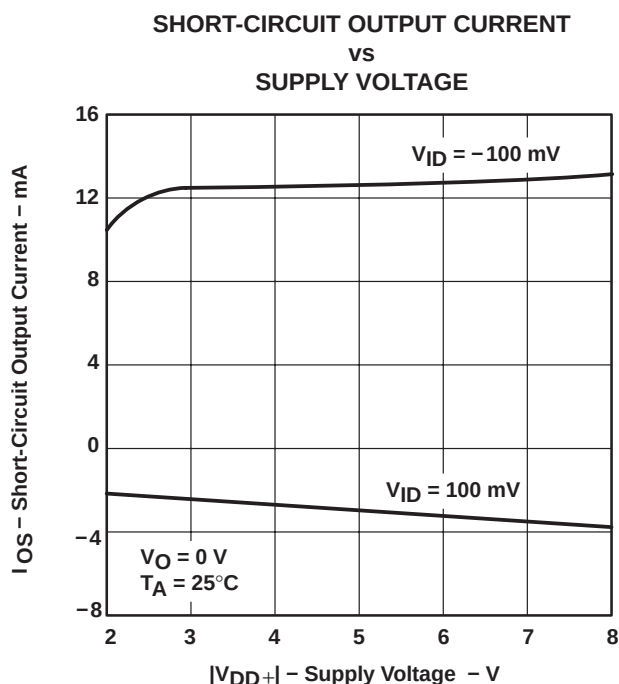


Figure 20

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

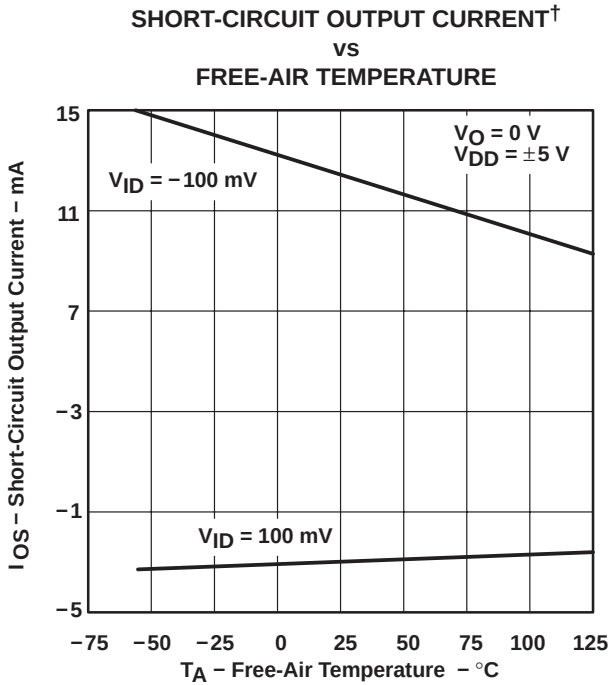


Figure 21

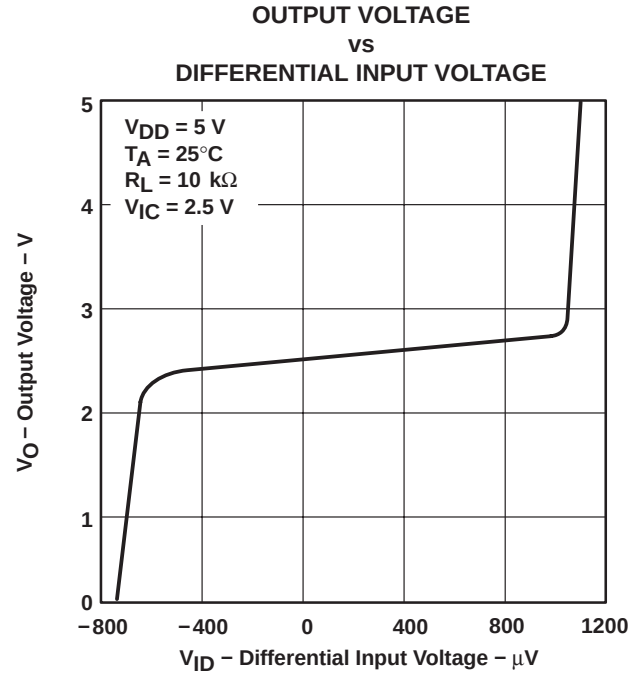


Figure 22

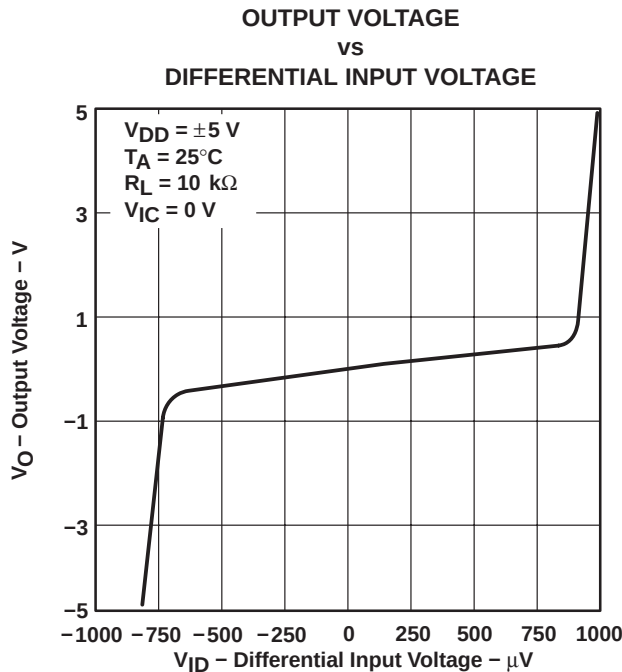


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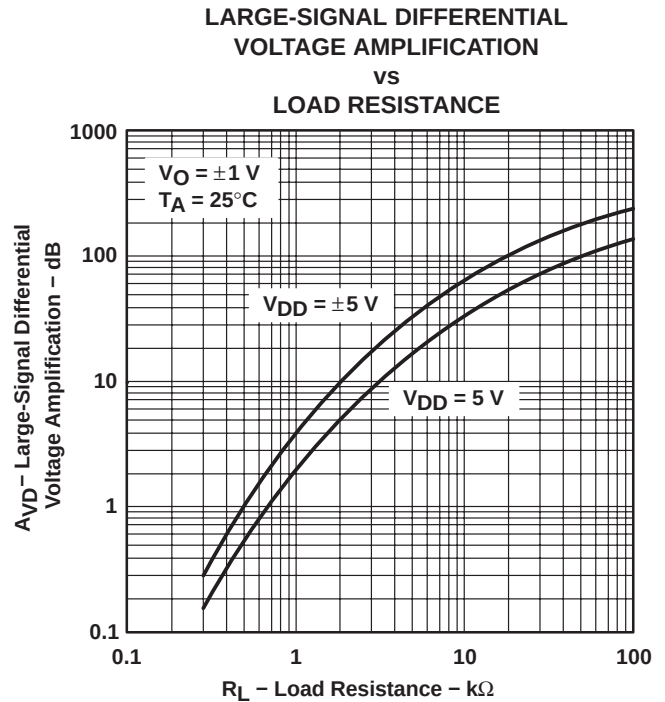


Figure 24

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

vs
FREQUENCY

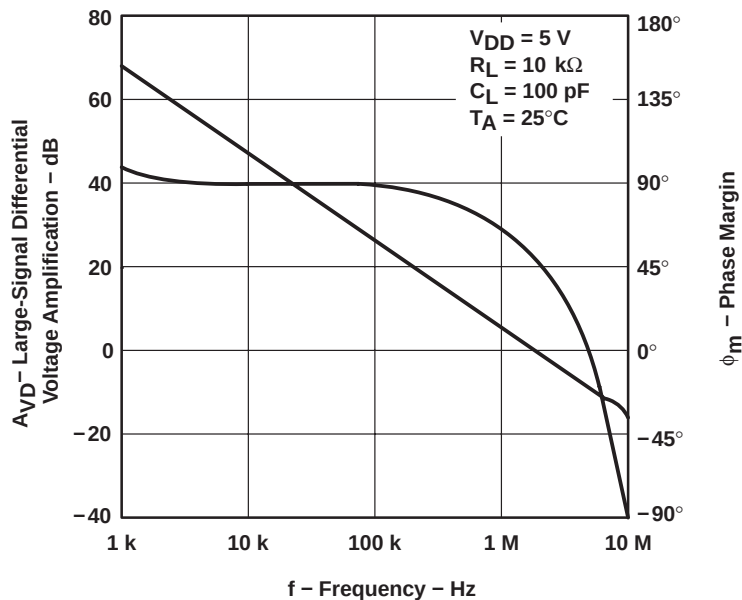


Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

vs
FREQUENCY

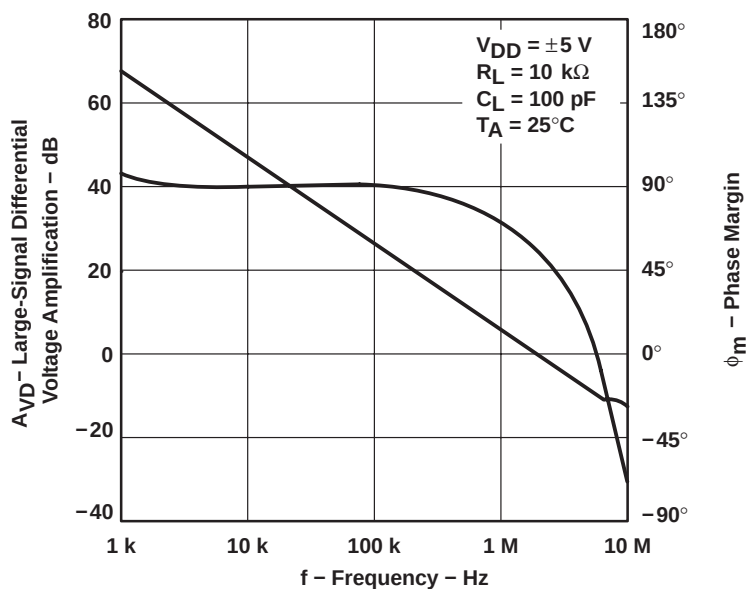


Figure 26

TYPICAL CHARACTERISTICS

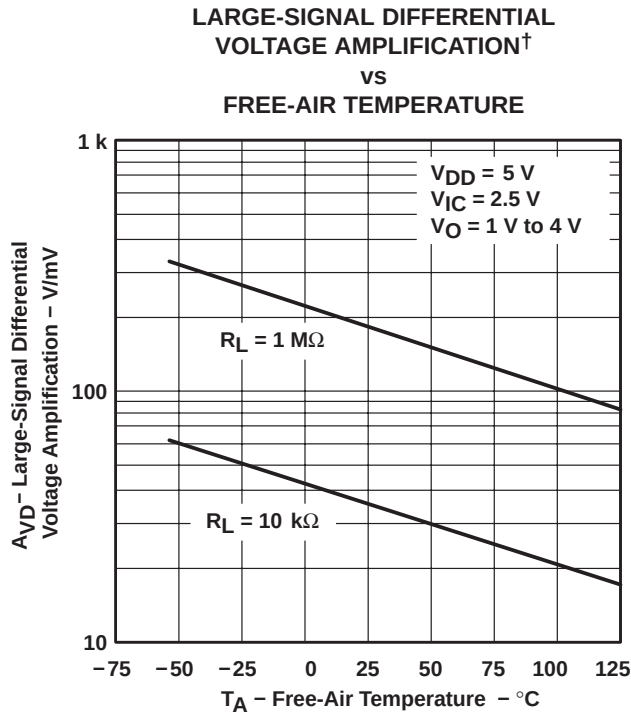


Figure 27

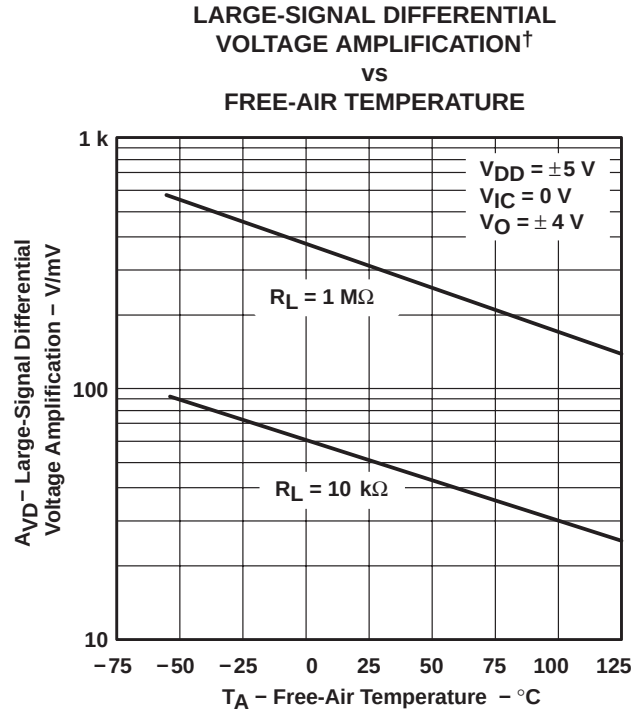


Figure 28

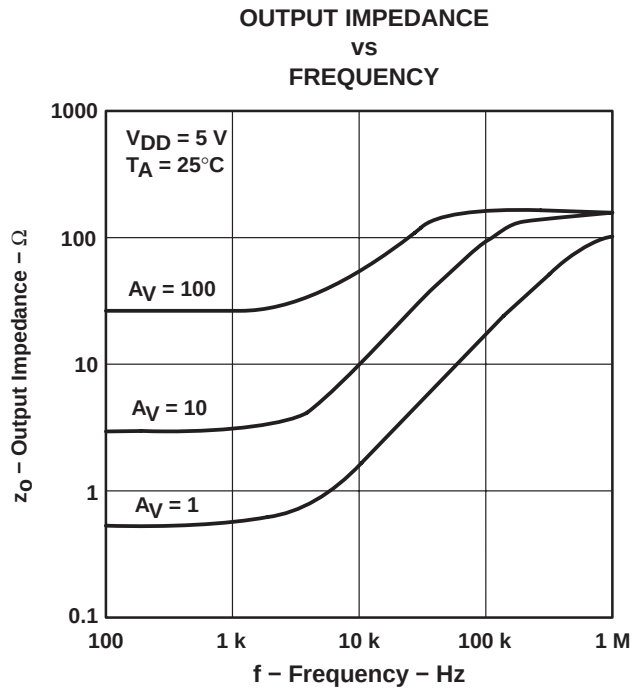


Figure 29

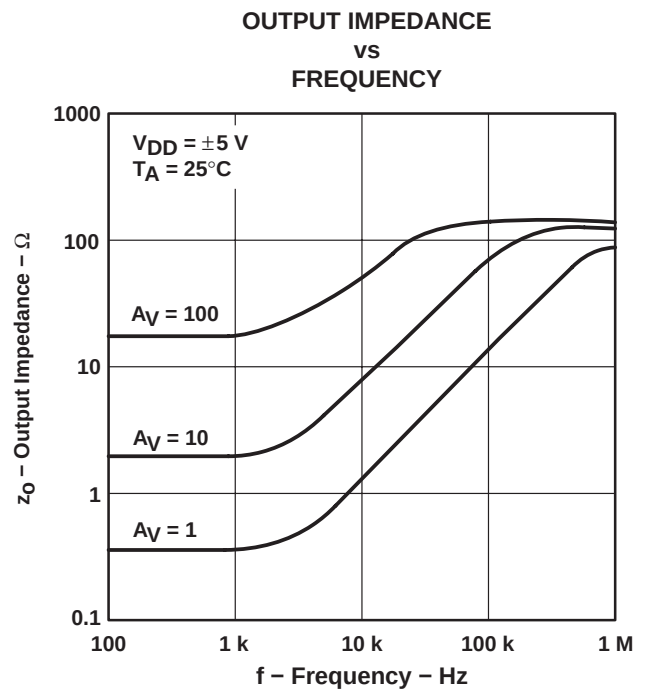


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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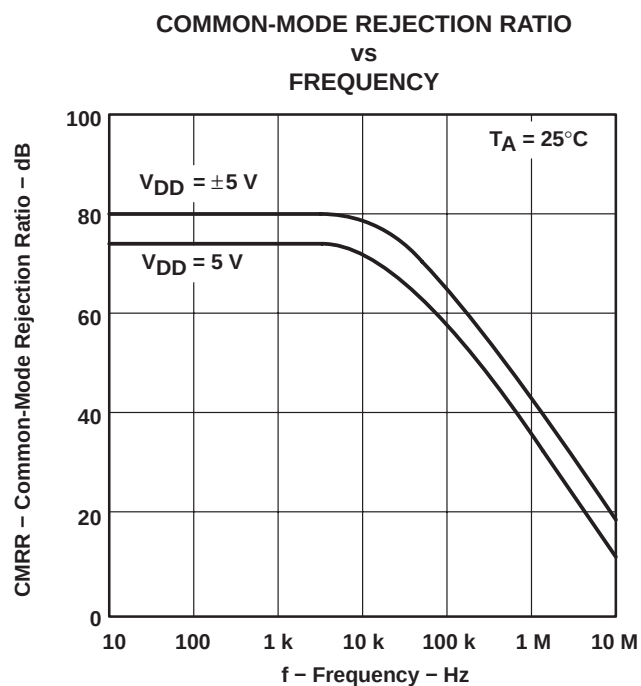


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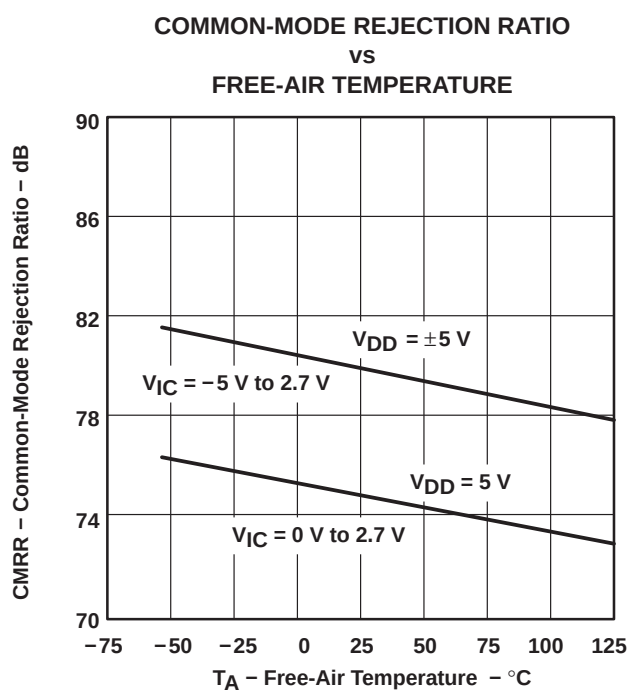


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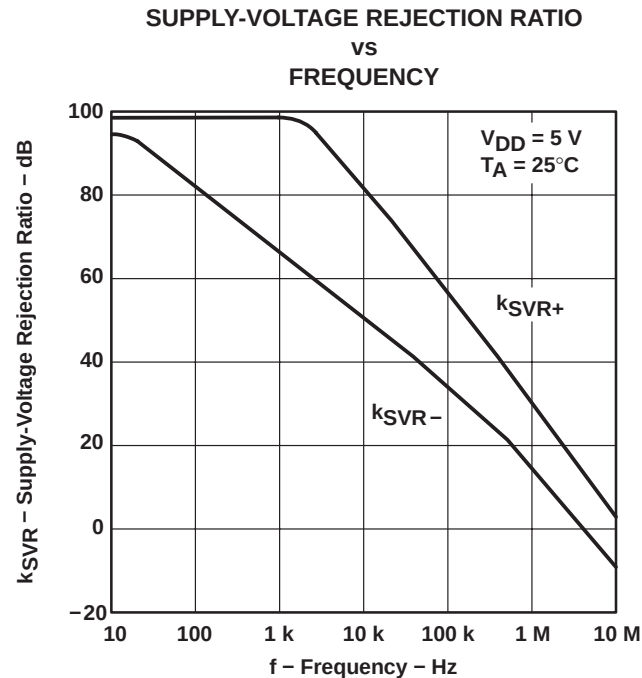


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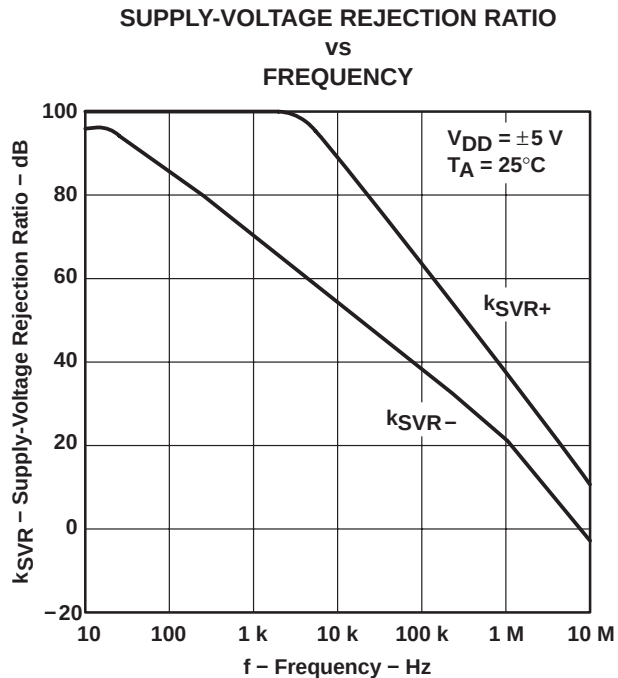


Figure 34

TYPICAL CHARACTERISTICS

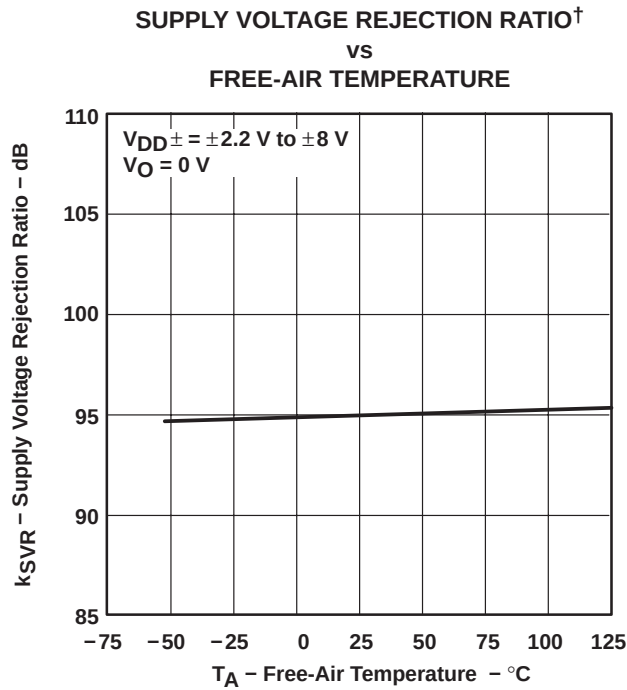


Figure 35

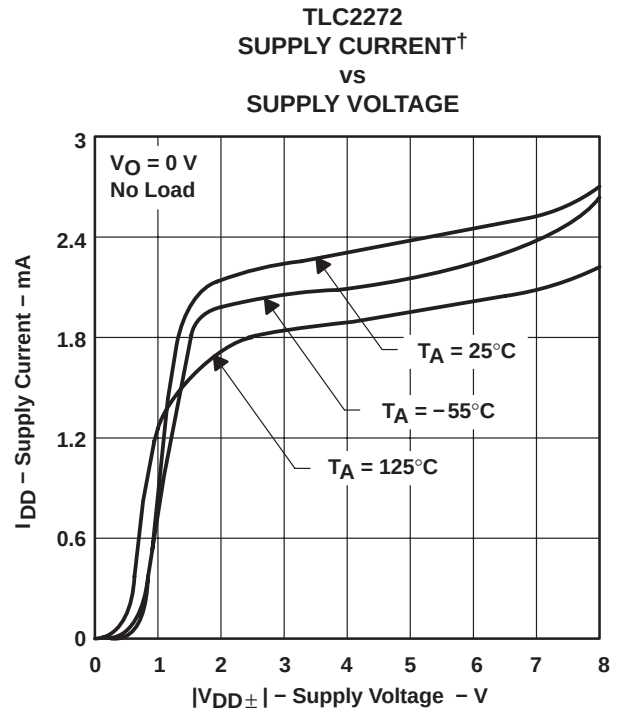


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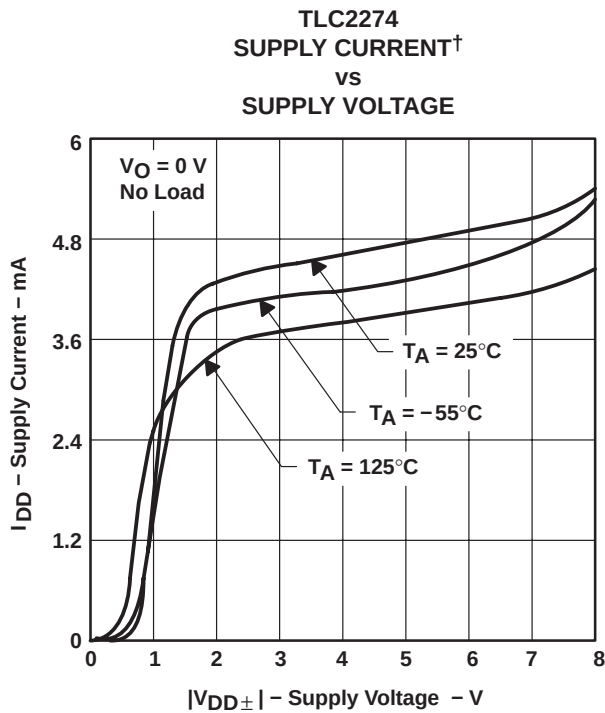


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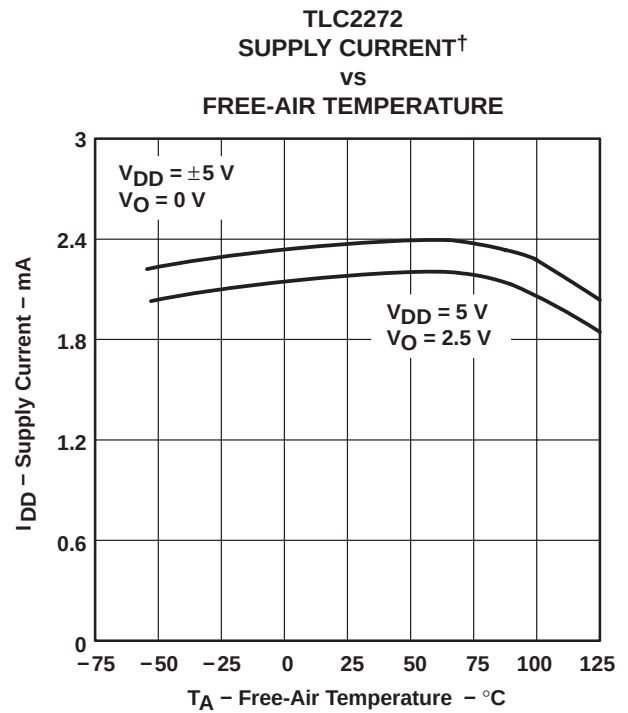


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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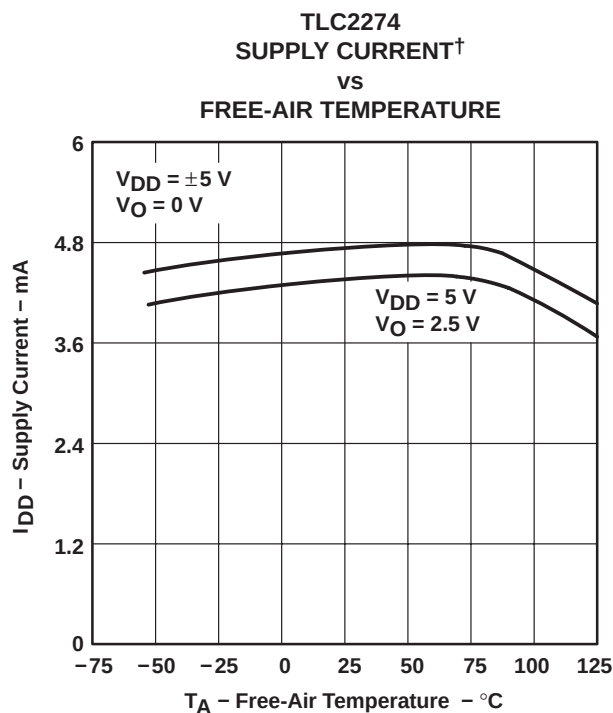


Figure 39

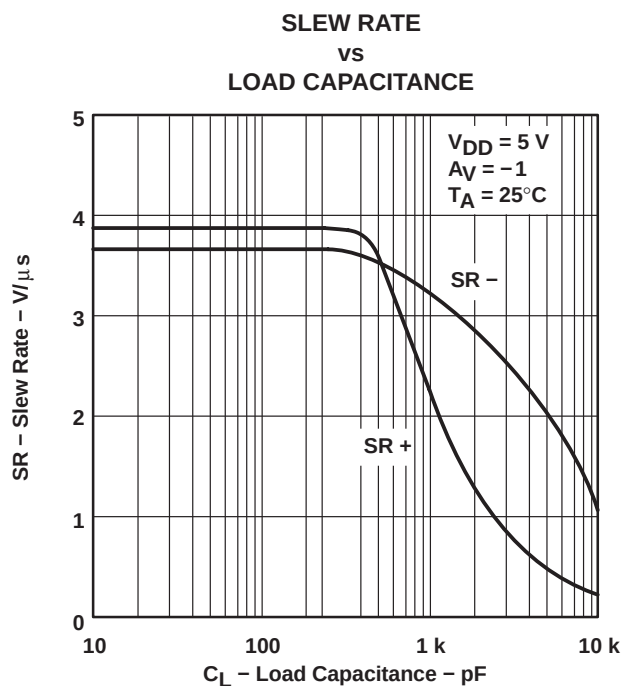


Figure 40

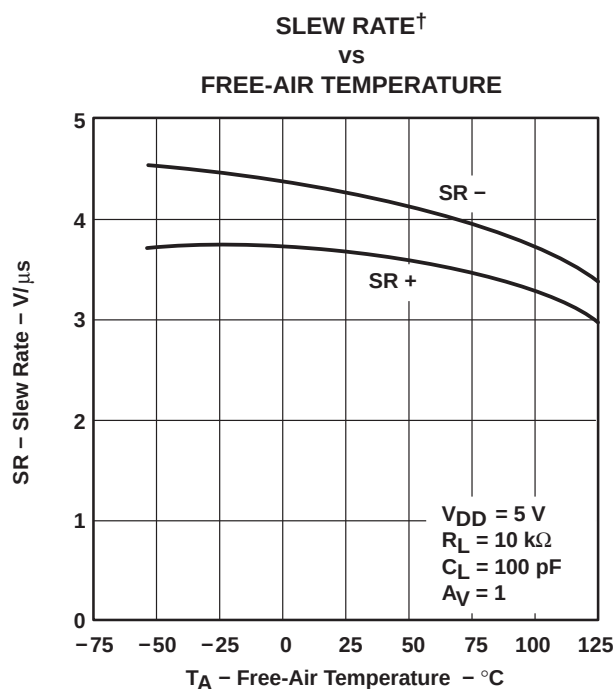


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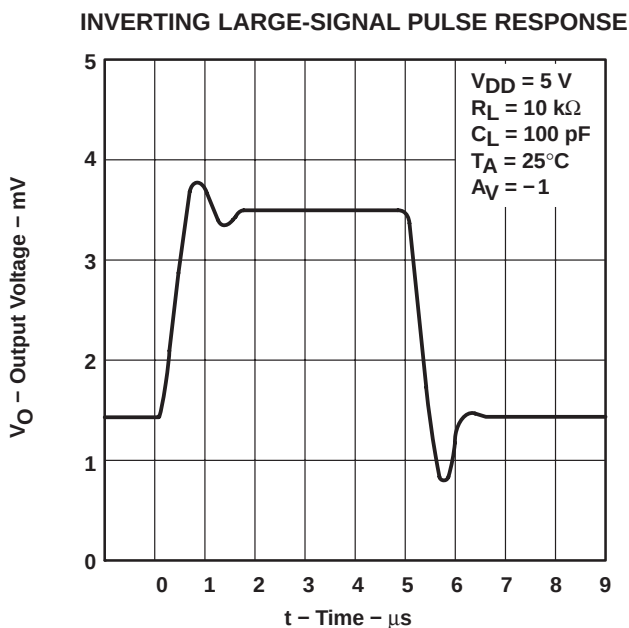


Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

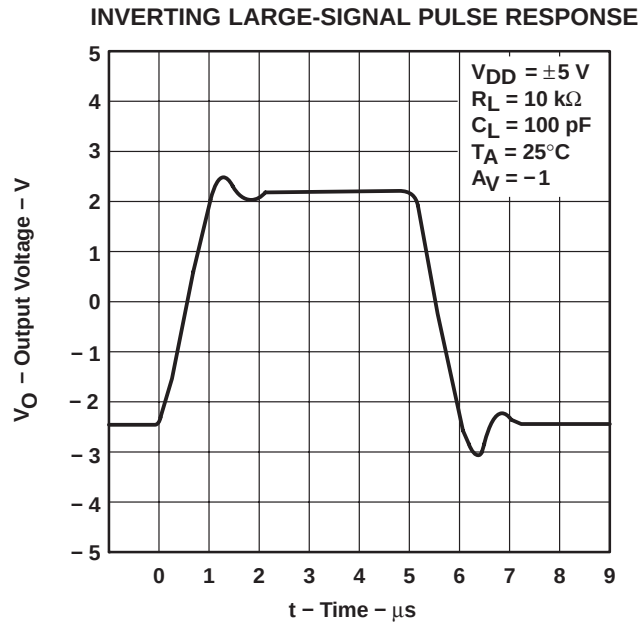


Figure 43

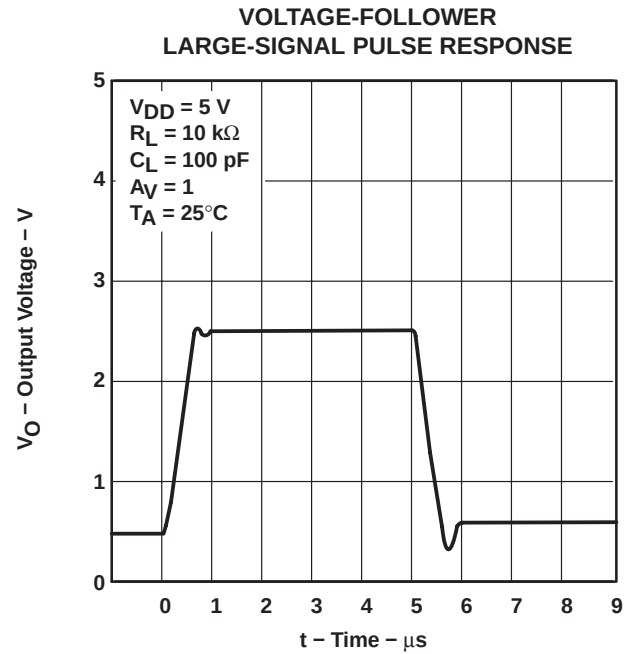


Figure 44

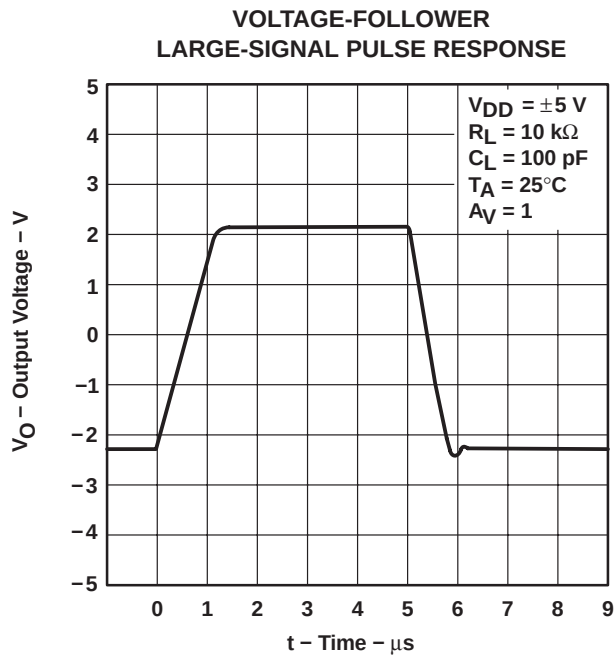


Figure 45

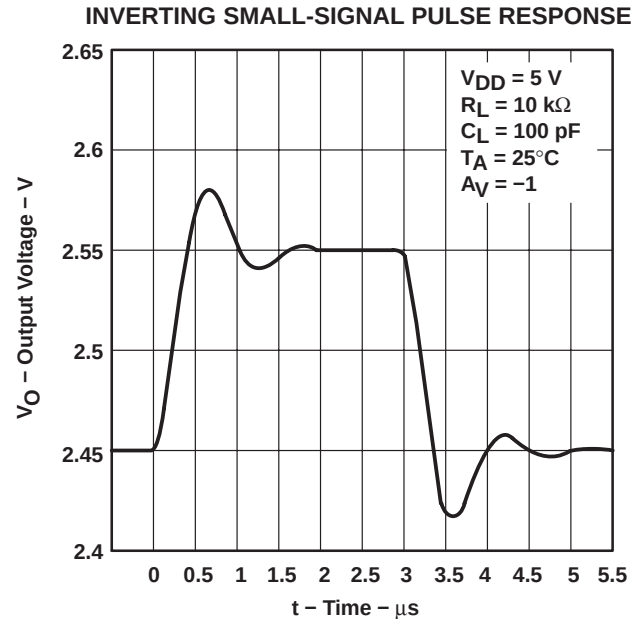


Figure 46

TLC227x-EP, TLC227xA-EP

Advanced LinCMOS™ RAIL-TO-RAIL

OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

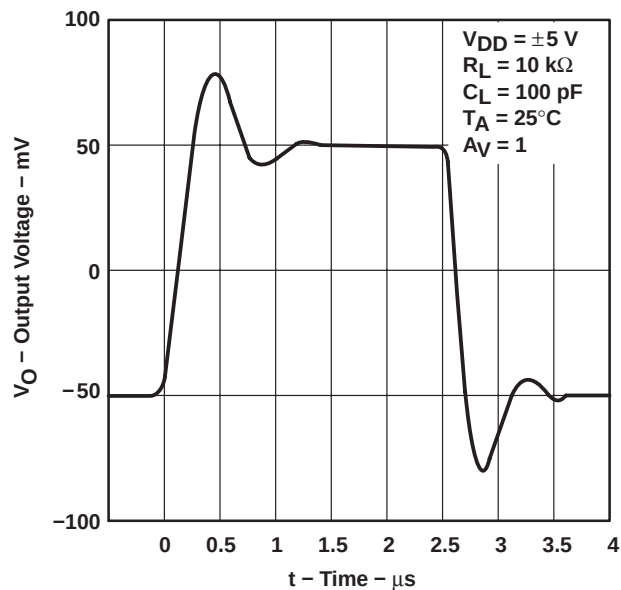


Figure 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

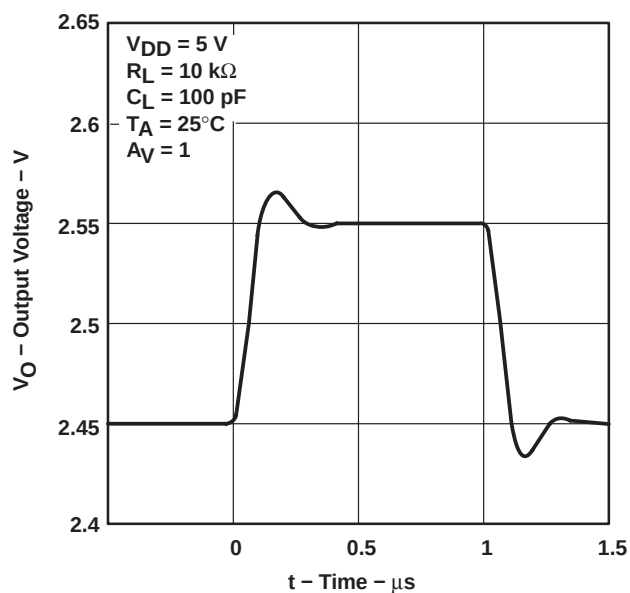


Figure 48

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

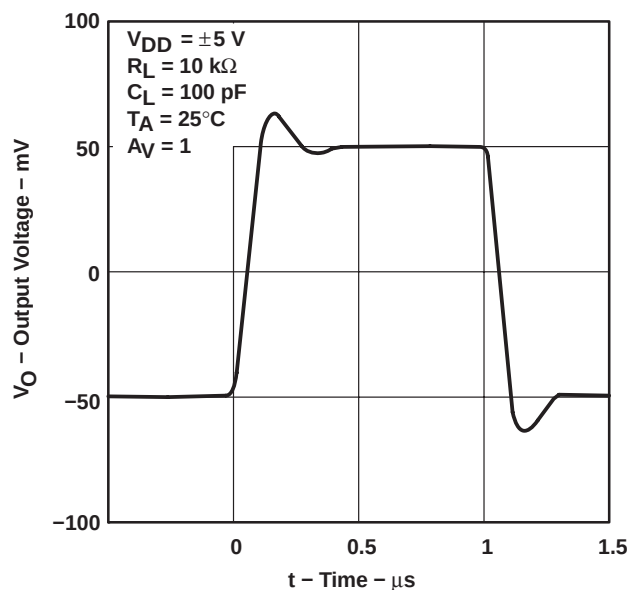


Figure 49

EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY

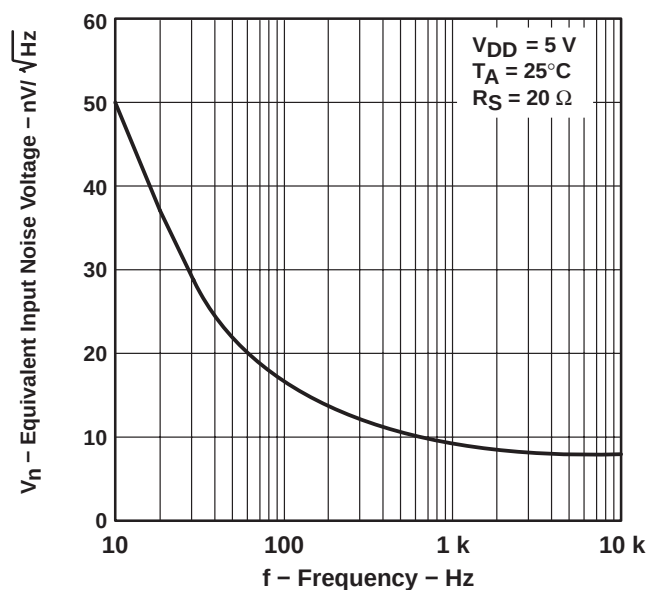


Figure 50

TYPICAL CHARACTERISTICS

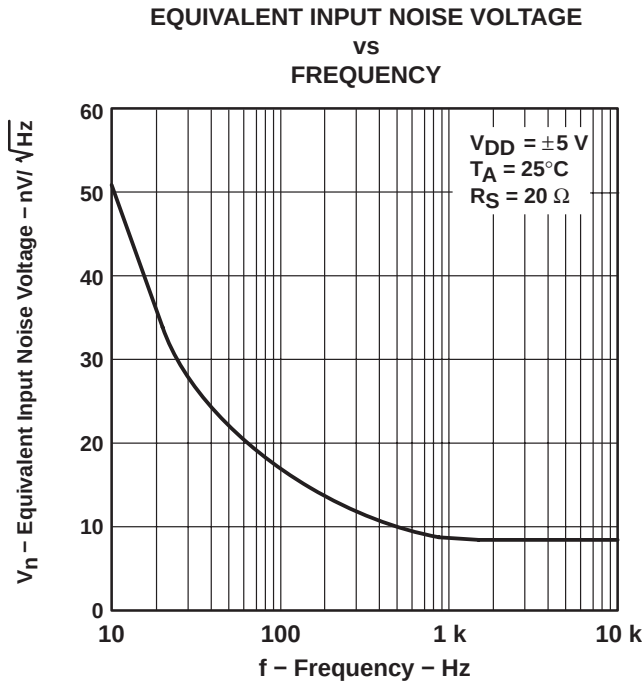


Figure 51

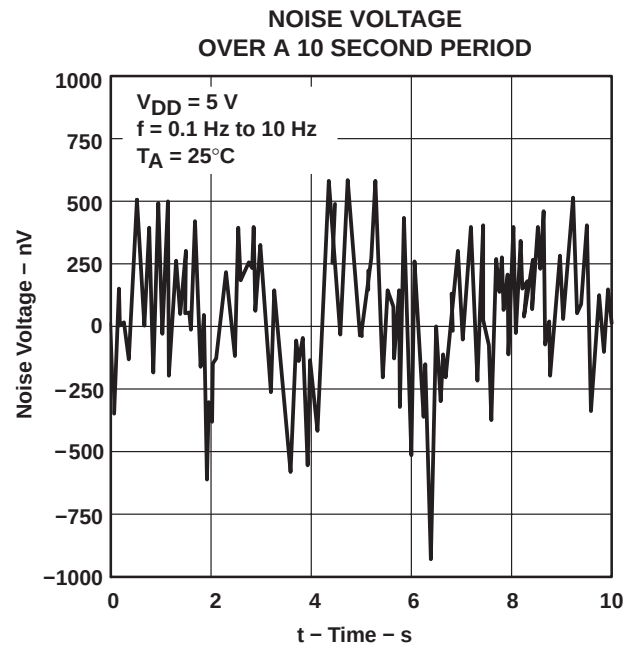


Figure 52

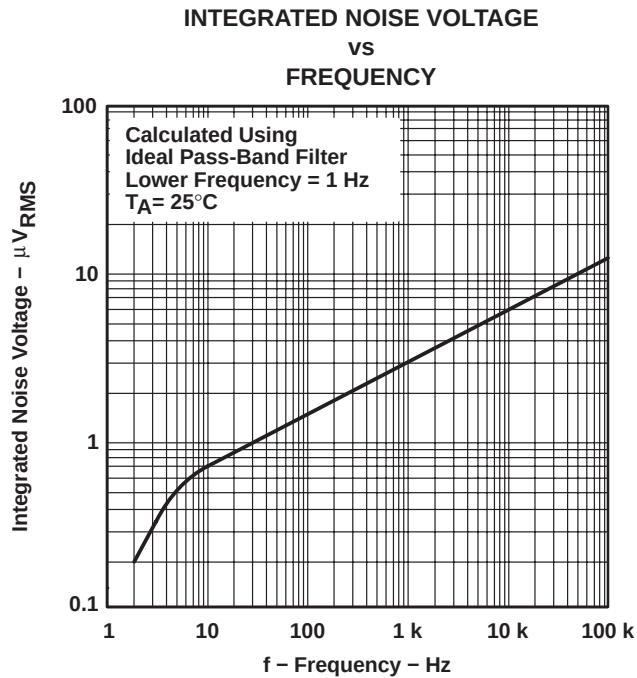


Figure 53

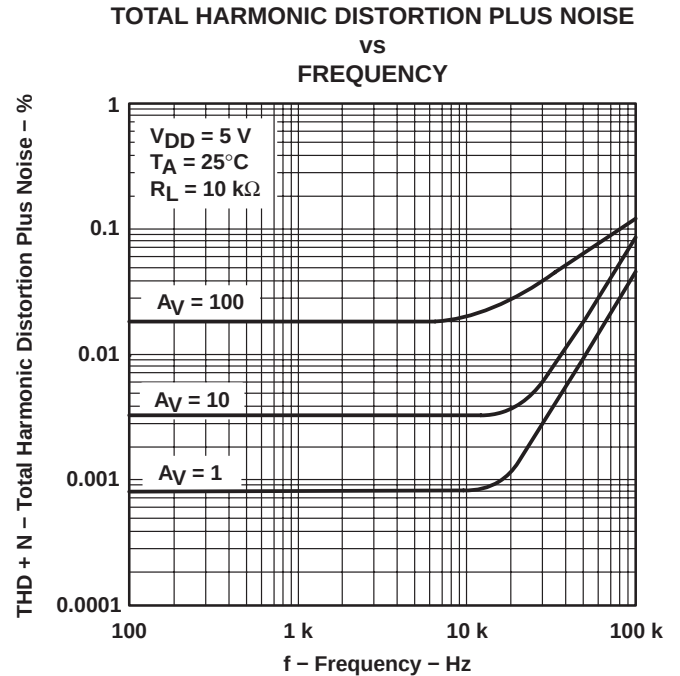


Figure 54

TLC227x-EP, TLC227xA-EP

Advanced LinCMOS™ RAIL-TO-RAIL

OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TYPICAL CHARACTERISTICS

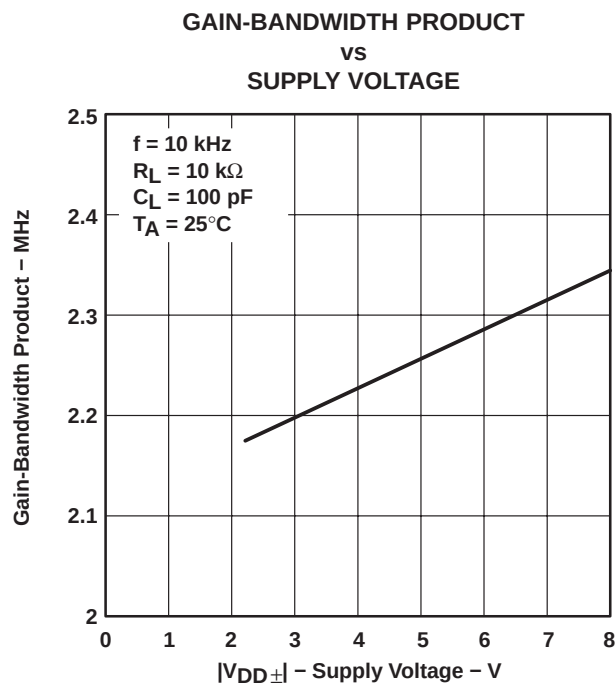


Figure 55

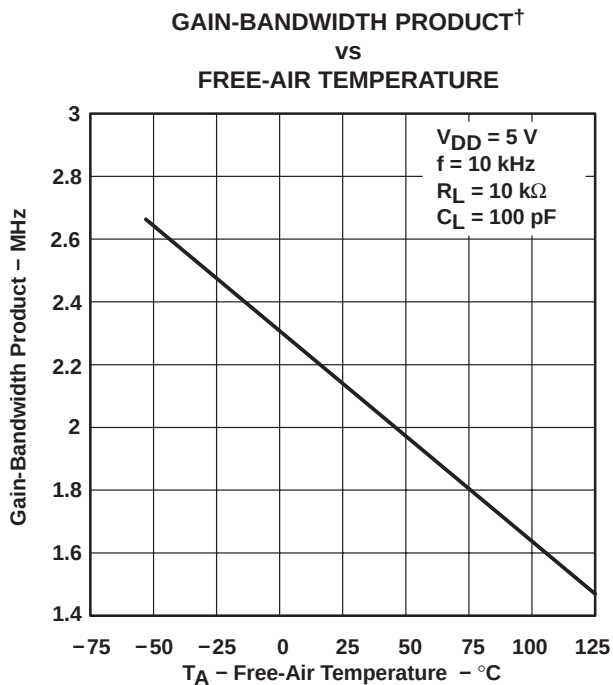


Figure 56

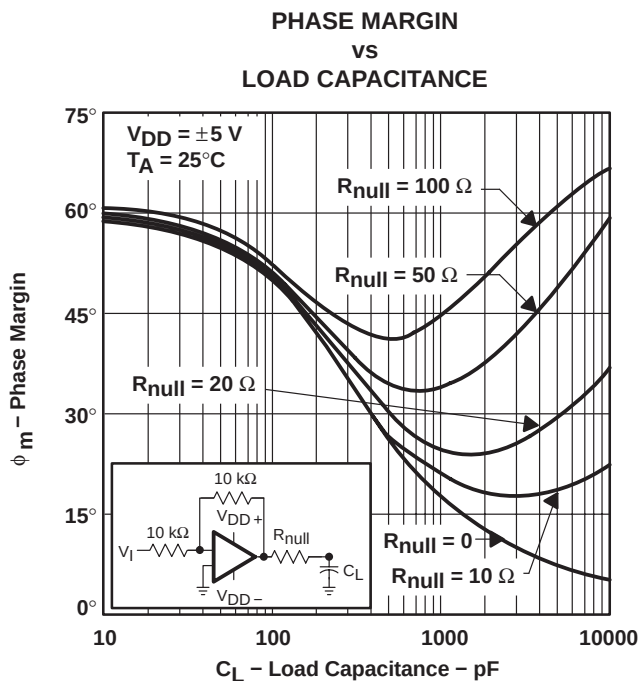


Figure 57

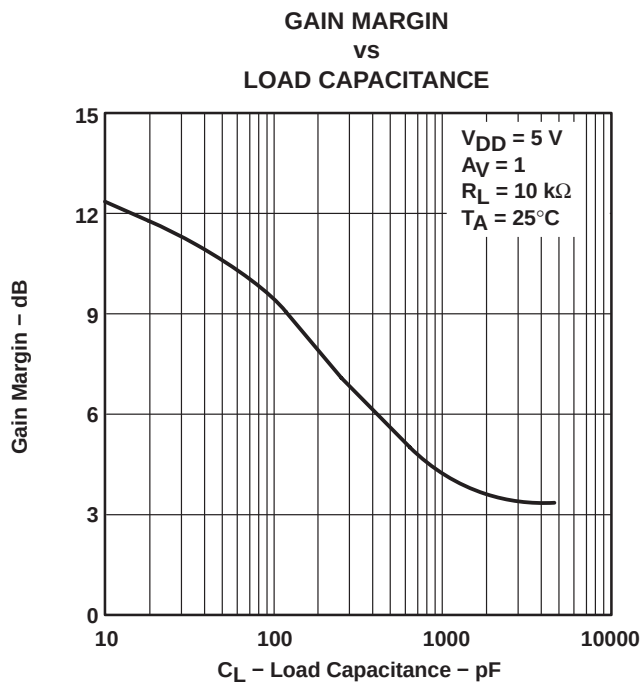


Figure 58

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 59 were generated using the TLC227x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

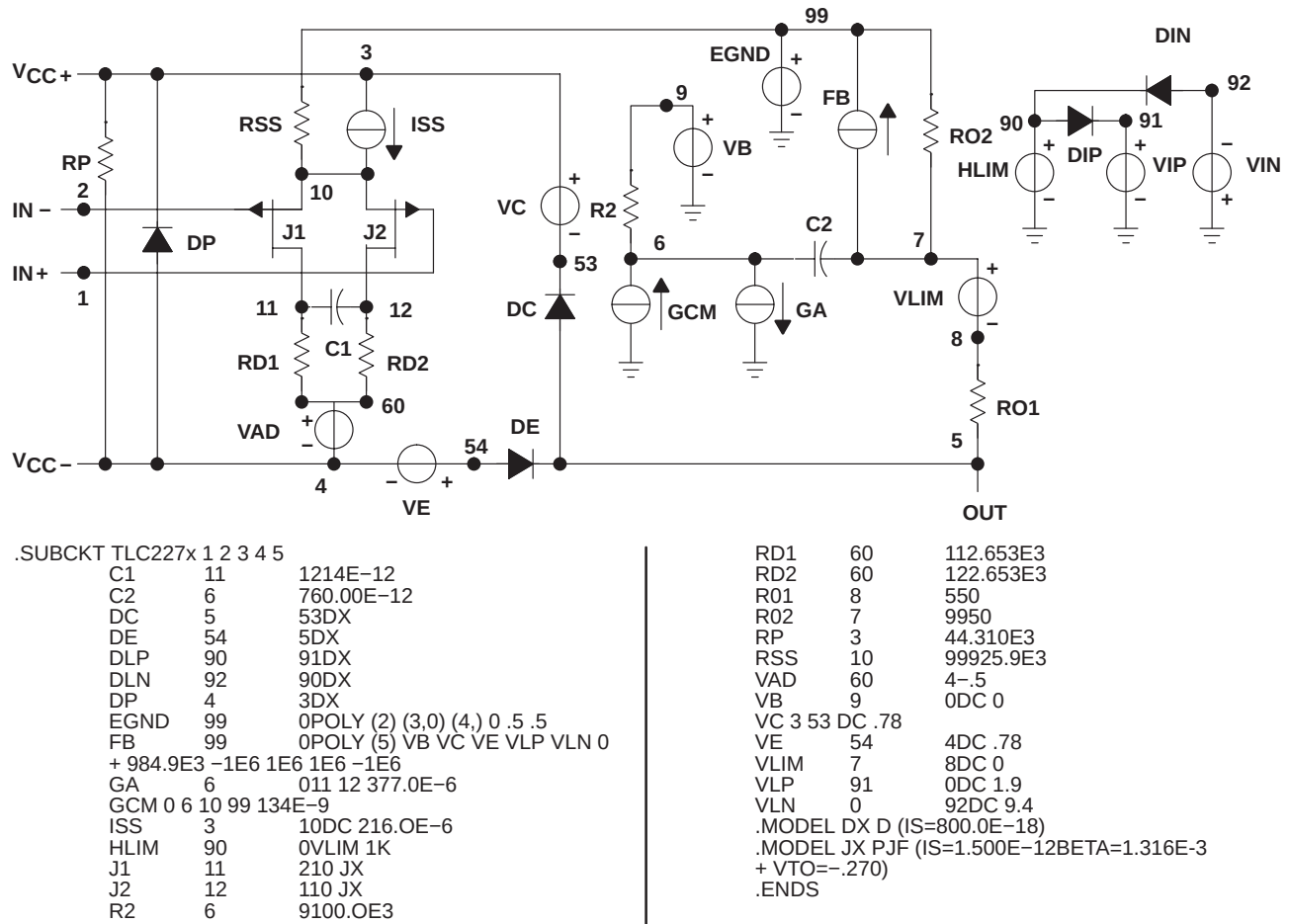


Figure 59. Boyle Macromodel and Subcircuit

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Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specification and operating characteristics of the semiconductor product to which the model relates.



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2272AMDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE
TLC2272AMDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE
TLC2272AMDREPG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE
TLC2274AMDREP	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME
TLC2274AMDREP.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME
TLC2274AMPWREP	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME
TLC2274AMPWREP.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME
TLC2274MDREP	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274ME
TLC2274MDREP.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274ME
V62/03618-01XE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE
V62/03618-02UE	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME
V62/03618-02YE	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME
V62/03618-04YE	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274ME

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

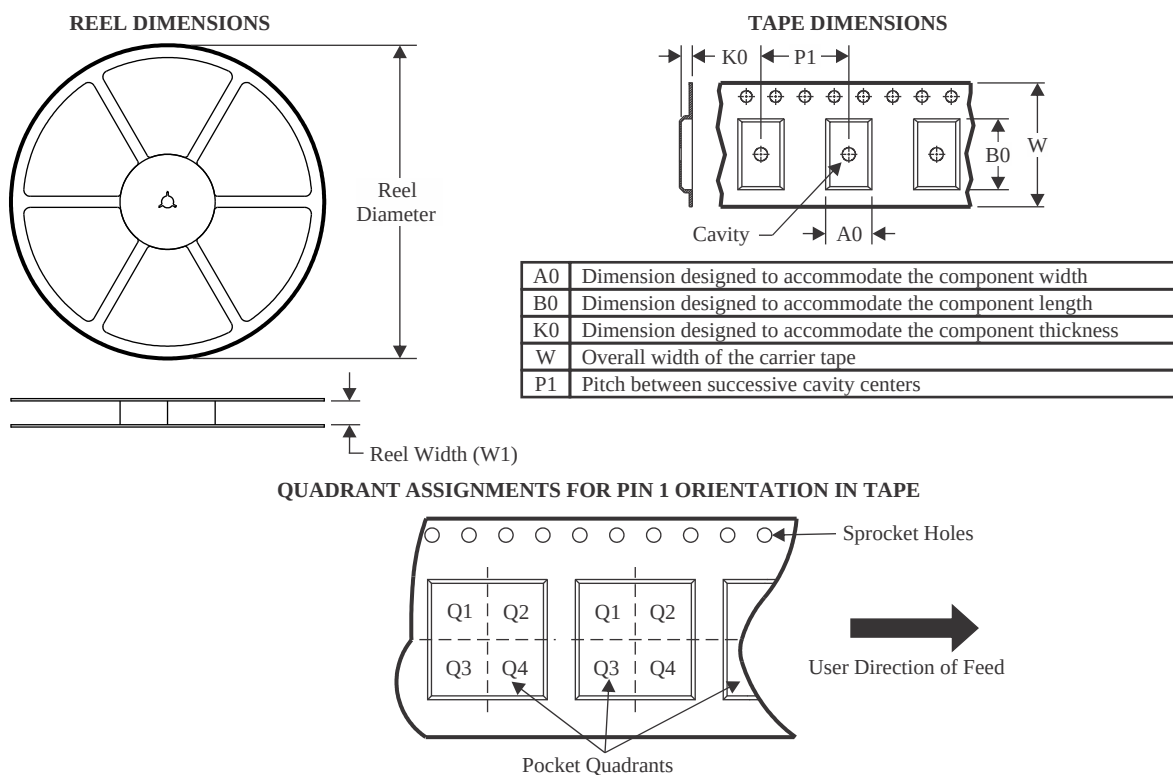
OTHER QUALIFIED VERSIONS OF TLC2272A-EP, TLC2274-EP, TLC2274A-EP :

- Catalog : [TLC2272A](#), [TLC2274](#), [TLC2274A](#)
- Automotive : [TLC2272A-Q1](#), [TLC2274-Q1](#), [TLC2274A-Q1](#)
- Military : [TLC2272AM](#), [TLC2274AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

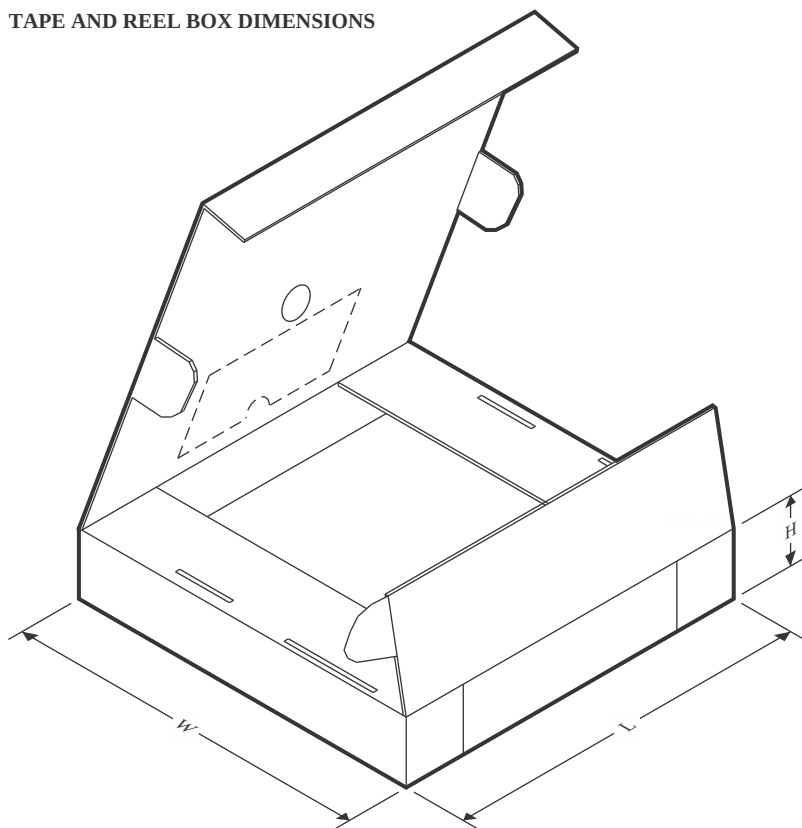
TAPE AND REEL INFORMATION



*All dimensions are nominal

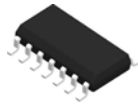
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2272AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2274AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274AMPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

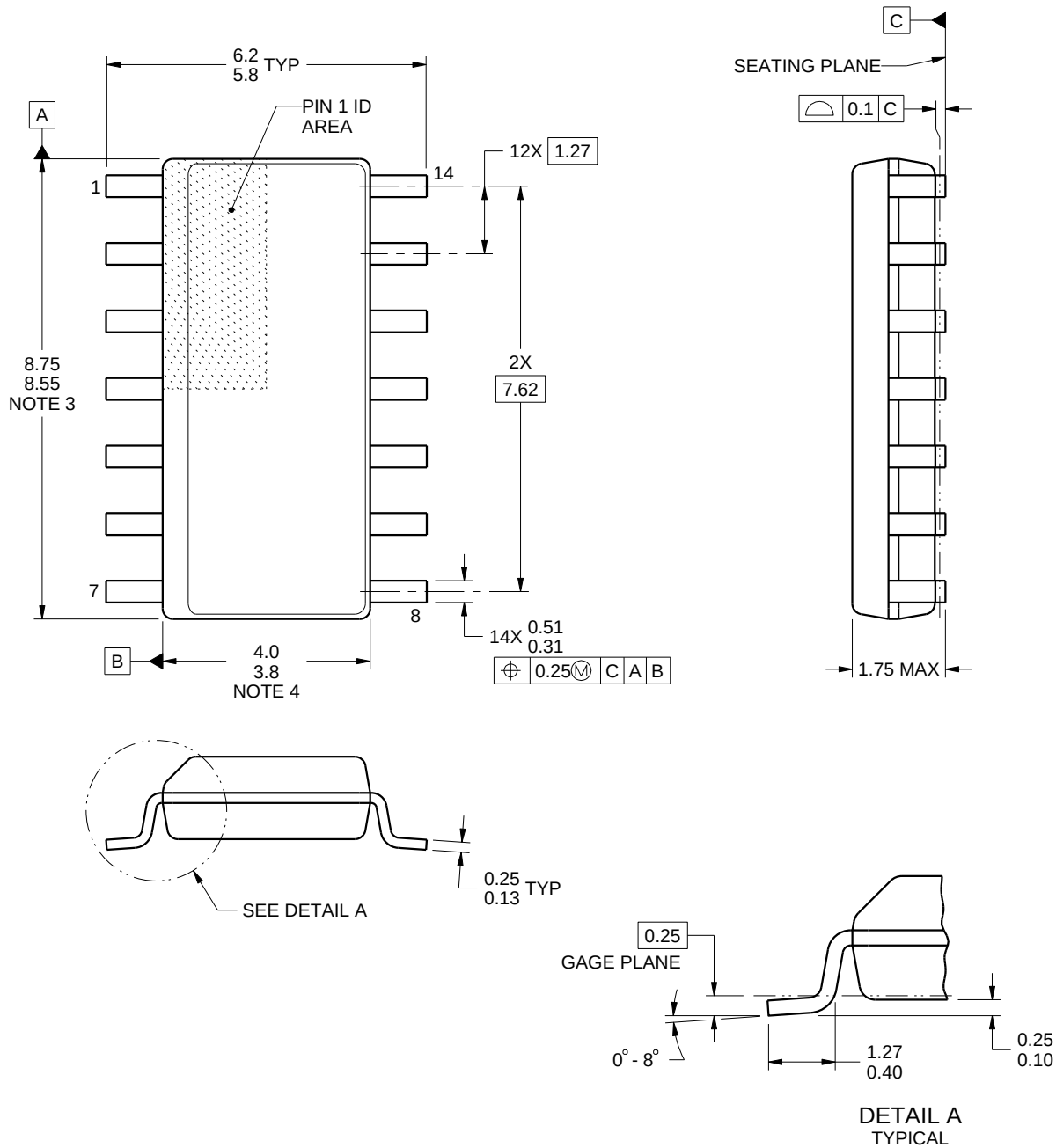


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2272AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
TLC2274AMDREP	SOIC	D	14	2500	353.0	353.0	32.0
TLC2274AMPWREP	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2274MDREP	SOIC	D	14	2500	340.5	336.1	32.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

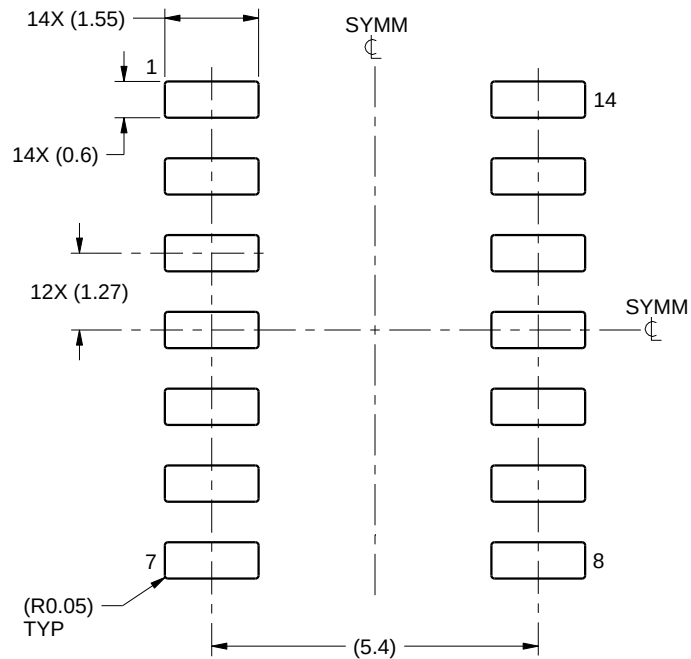
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

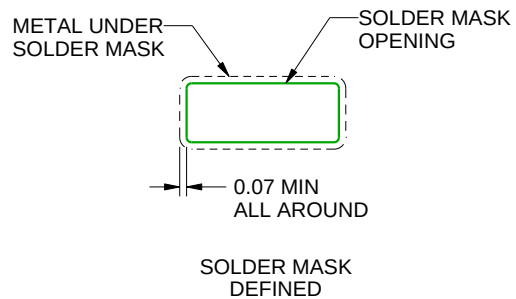
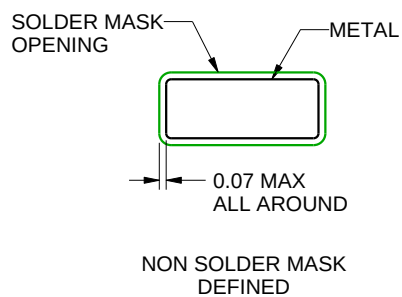
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

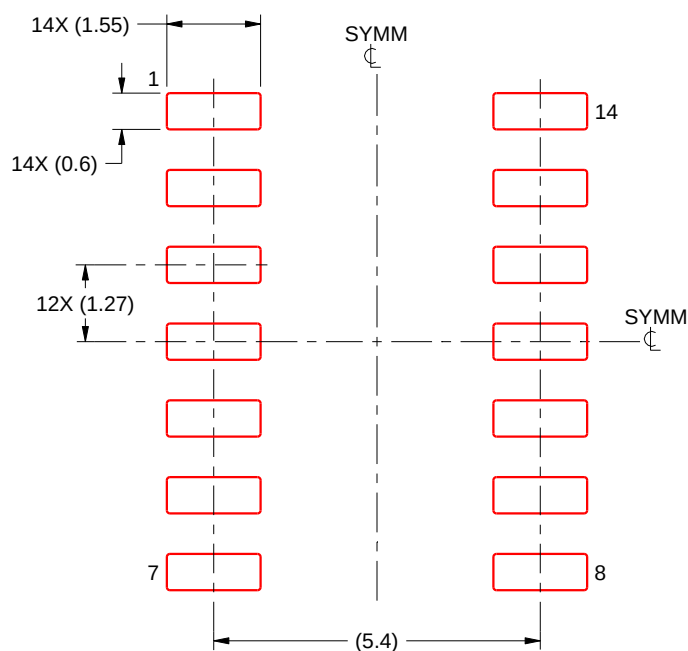
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

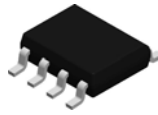


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

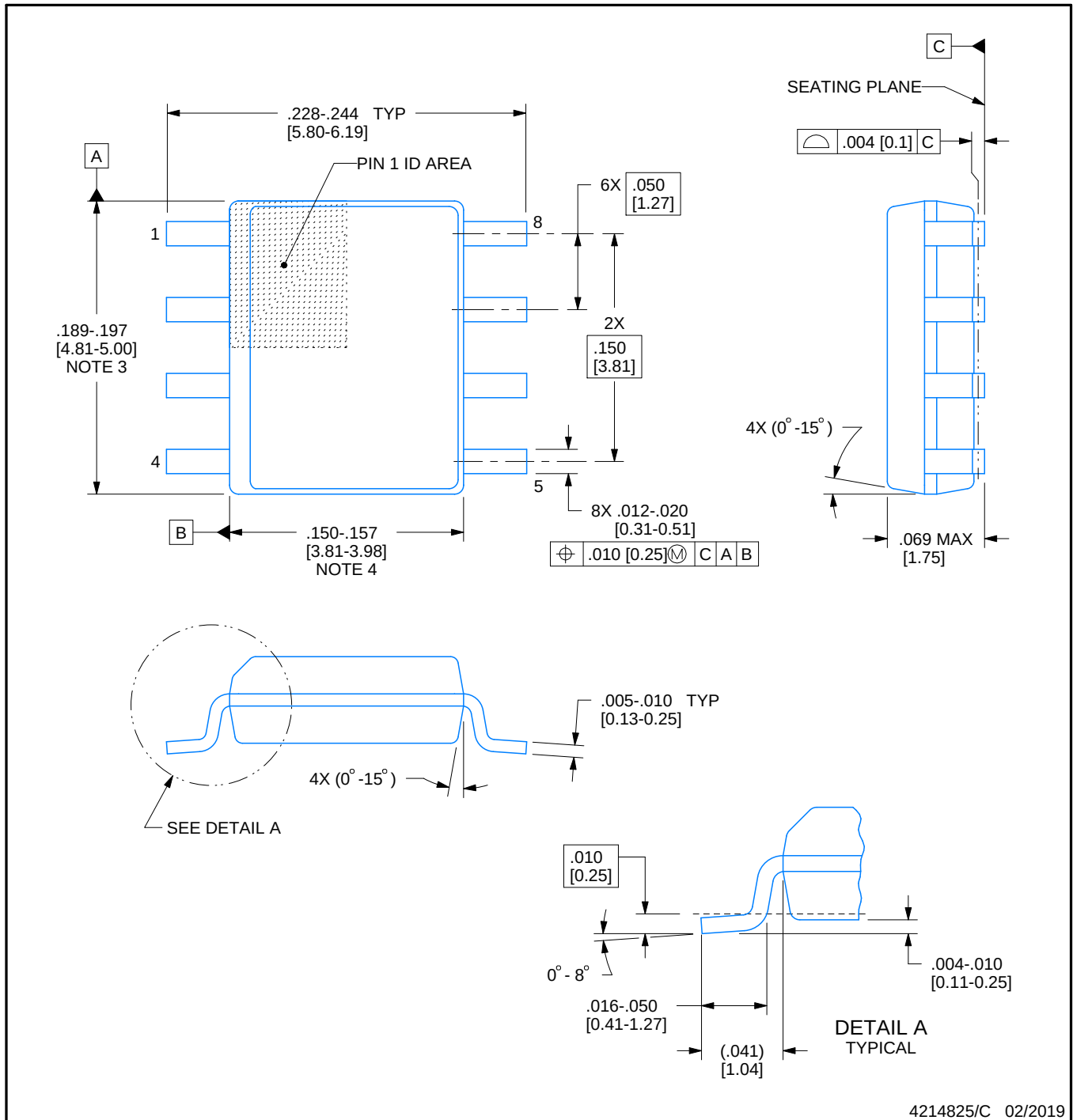


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

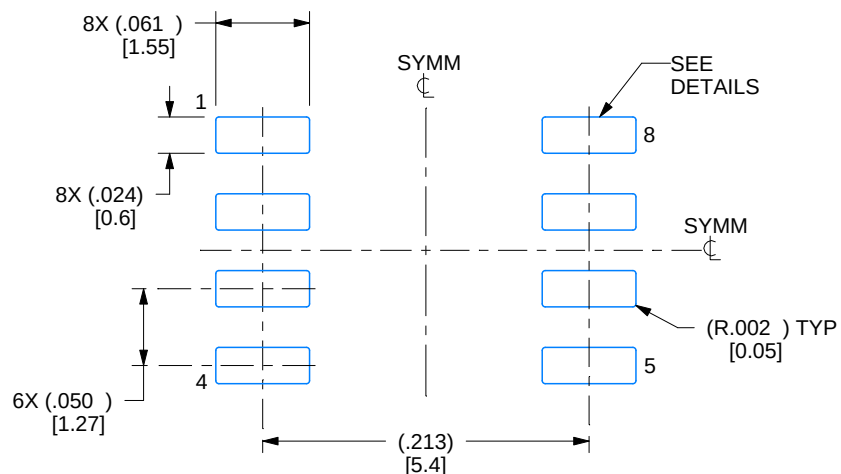
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

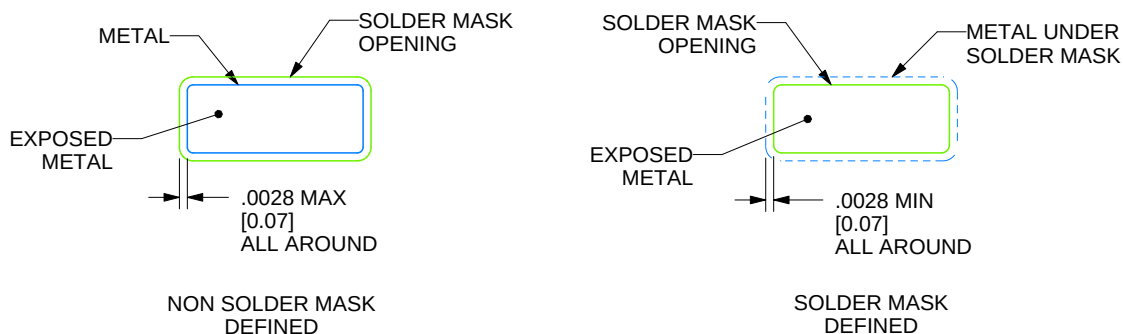
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

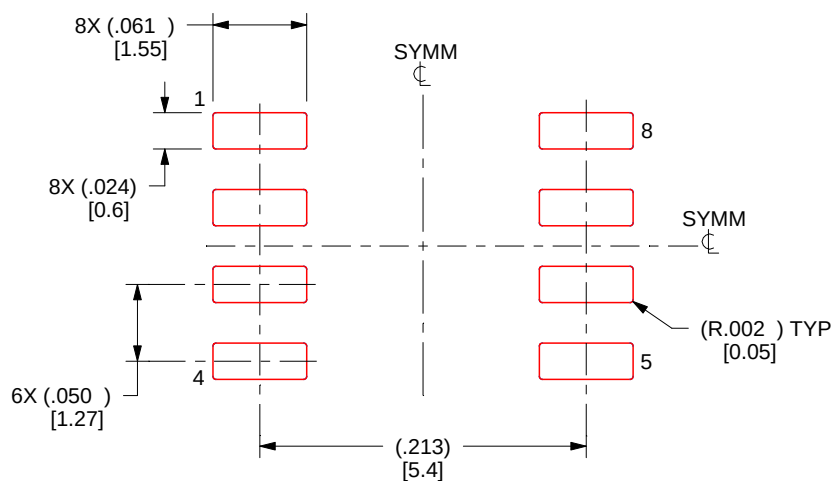
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

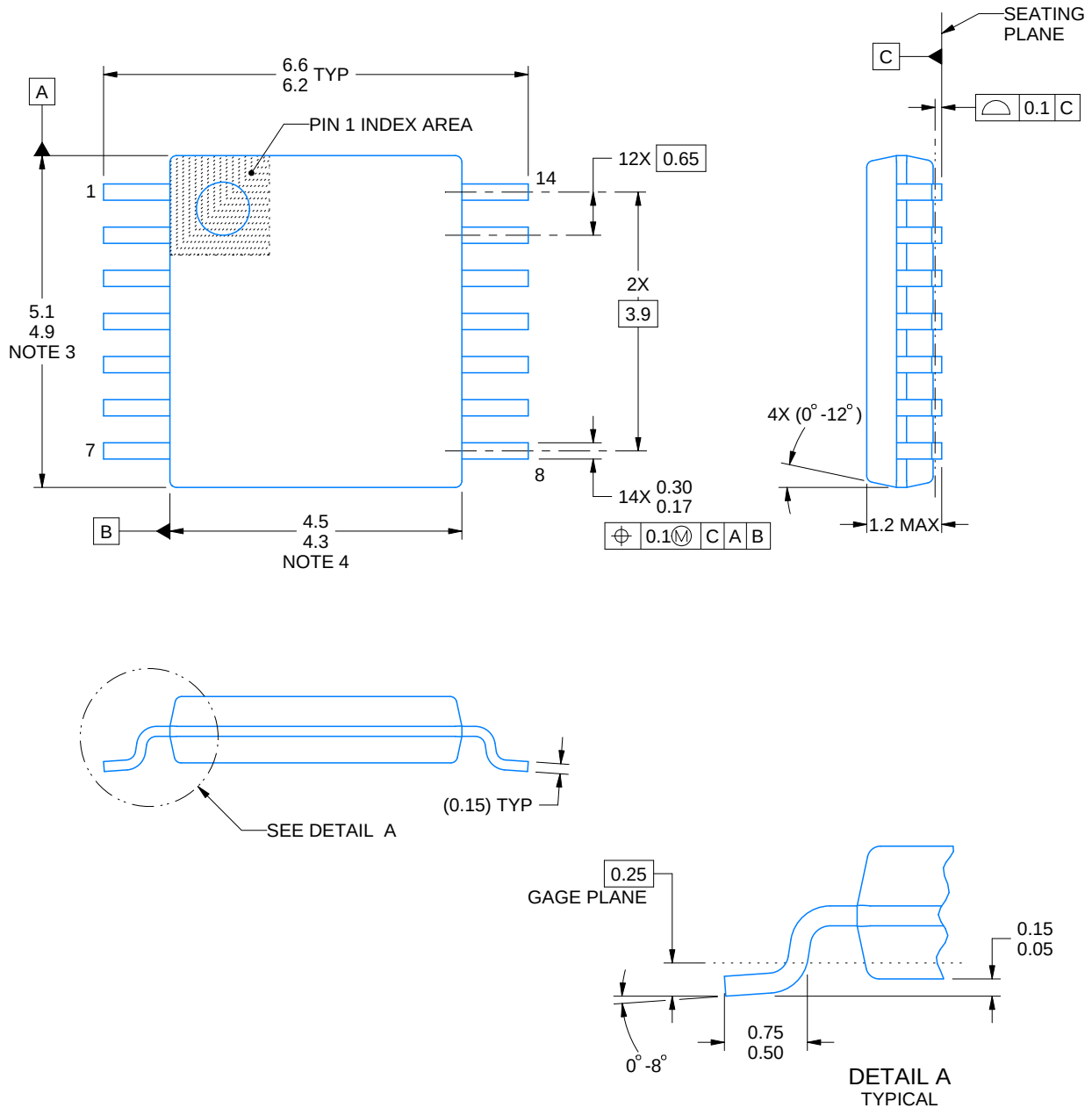
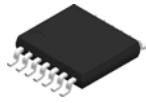


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

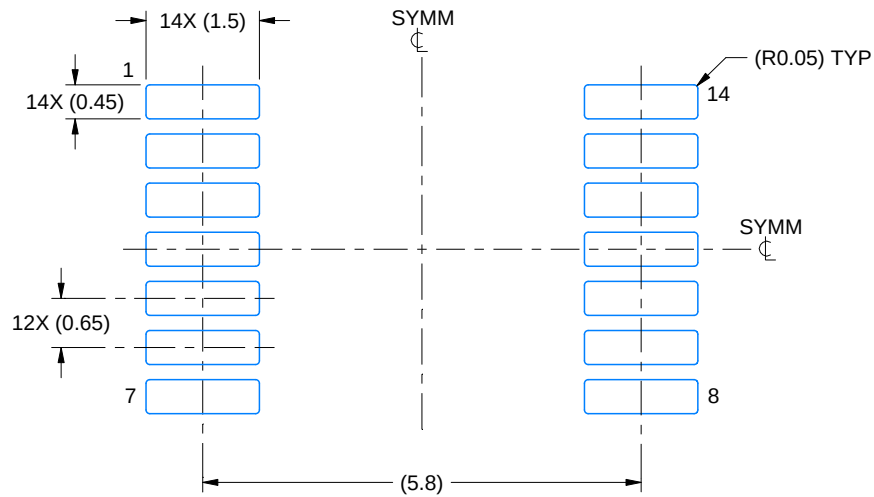
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

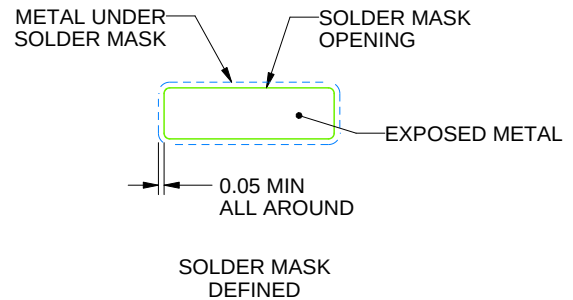
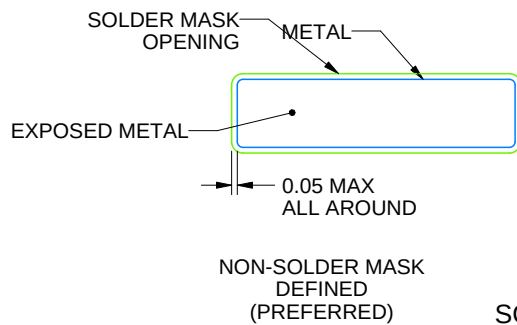
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

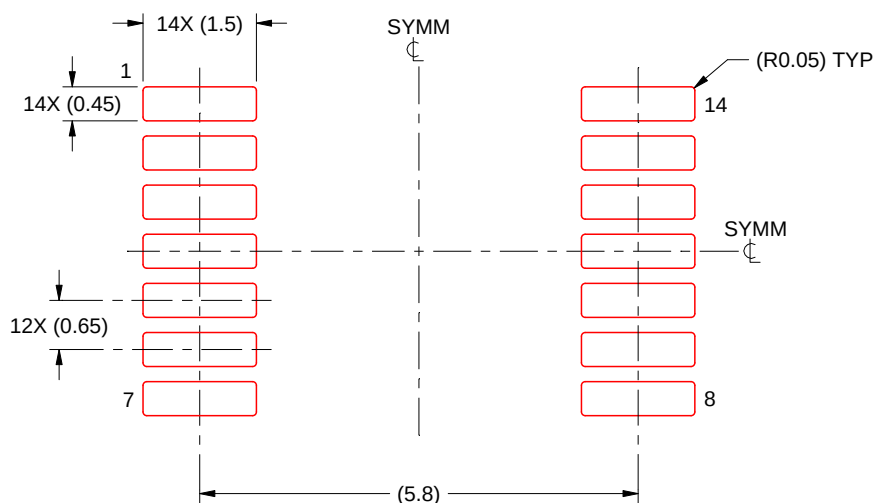
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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