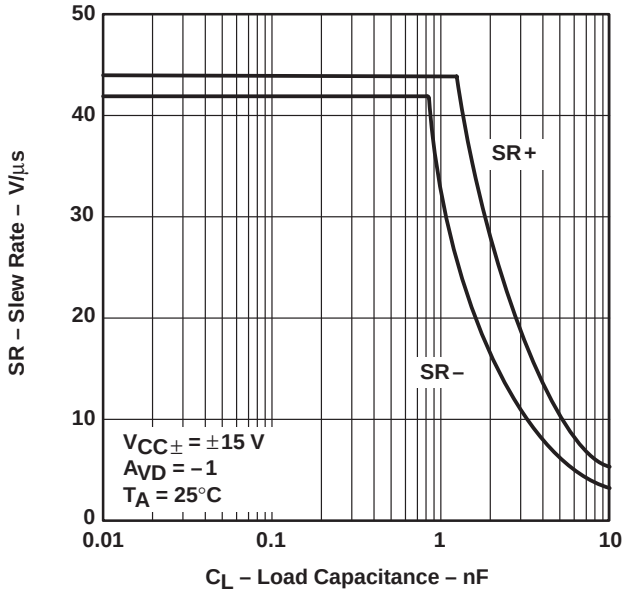
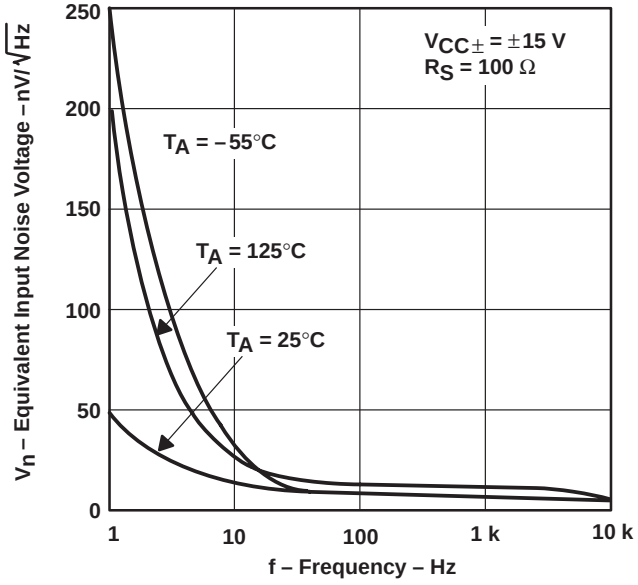
## available features

- **Low Noise:**
  **10 Hz . . . 15 nV/√Hz**
  **1 kHz . . . 10.5 nV/√Hz**
- **10000-pF Load Capability**
- **20-mA Min Short-Circuit Output Current**
- **30-V/μs Min Slew Rate**
- **High Gain-Bandwidth Product . . . 5.9 MHz**
- **Low $V_{IO}$ . . . 500 μV Max at 25°C**
- **Single or Split Supply . . . 4 V to 44 V**
- **Fast Settling Time**
  **340 ns to 0.1%**
  **400 ns to 0.01%**
- **Saturation Recovery . . . 150 ns**
- **Large Output Swing . . . $V_{CC-}$ +0.1 V to $V_{CC+}$ – 1 V**

**SLEW RATE vs LOAD CAPACITANCE**




**EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY**




## description

The TLE2141M and TLE2141AM are high-performance, internally compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2141AM is a tighter offset voltage grade of the TLE2141M. Both are pin-compatible upgrades to standard industry products.

The design incorporates a patent-pending input stage that simultaneously achieves low audio band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

**AVAILABLE OPTIONS**

| $T_A$ | $V_{IO}$ max AT 25°C | PACKAGE | | CHIP FORM (Y) |
|---|---|---|---|---|
| | | CHIP CARRIER (FK) | CERAMIC DIP (JG) | |
| –55°C to 125°C | 500 μV<br>900 μV | TLE2141AMFK<br>TLE2141MFK | TLE2141AMJG<br>TLE2141MJG | TLE2141Y |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description (continued)

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2141M and TLE2141AM are useful for low-droop sample and holds and direct buffering of long cables, including four 20-mA current loops.

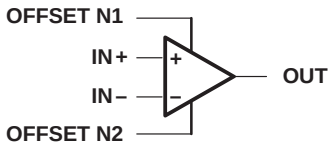
The special design also exhibits an improved insensitivity to inherent IC component mismatches as is evidenced by a 500-μV maximum offset voltage and 1.7-μV/°C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the ±2-V to ±22-V range. Inputs can operate between $V_{CC-}$ −0.3 to $V_{CC+}$ −1.8 V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all NPN output stage provides a nearly rail-to-rail output swing of $V_{CC-}$ +0.1 to $V_{CC+}$ −1 V under light current loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

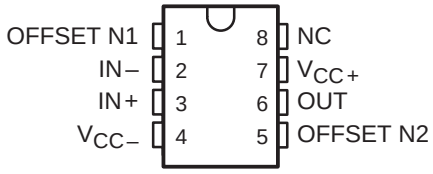
Both versions can also be used as comparators. Differential inputs of $V_{CC\pm}$ can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is overdriven beyond the limits of recommended output swing.

Both the TLE2141M and TLE2141AM are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The M-suffix is characterized for operation over the full military temperature range of −55°C to 125°C.

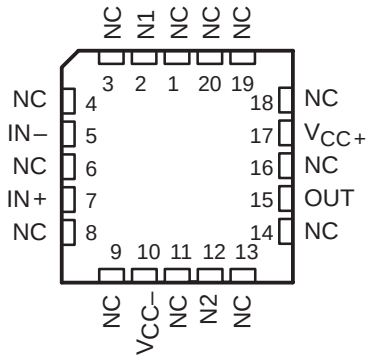
## symbol




**JG PACKAGE**
**(TOP VIEW)**




**FK PACKAGE**
**(TOP VIEW)**

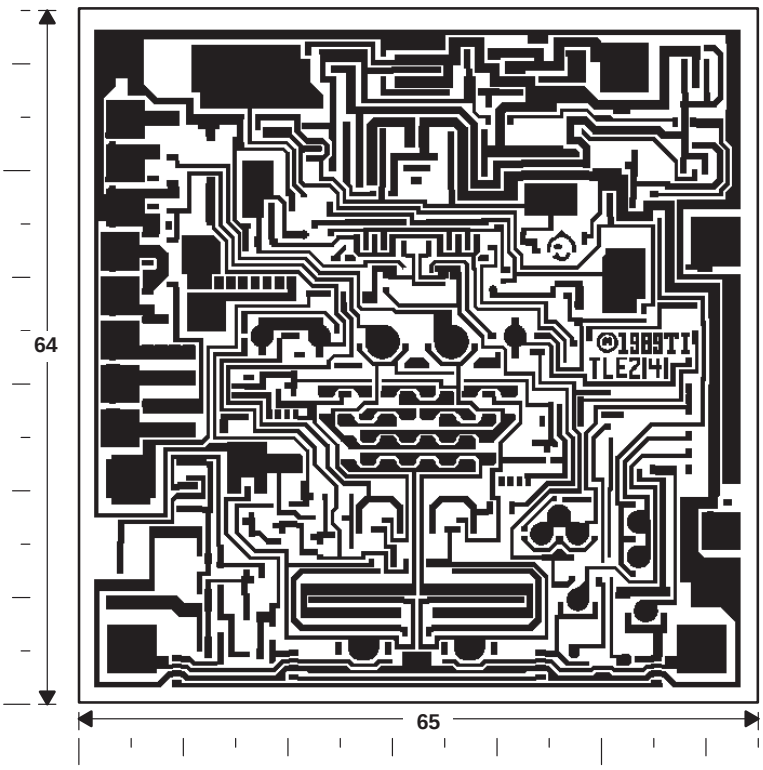


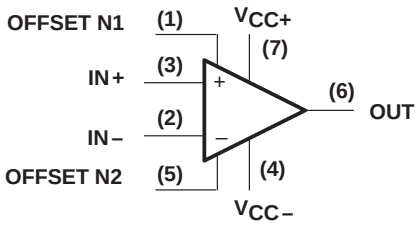

NC – No internal connection

## chip information

These chips, when properly assembled, display characteristics similar to the TLE2141M. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

**BONDING PAD ASSIGNMENTS**




**CHIP THICKNESS: 15 TYPICAL**

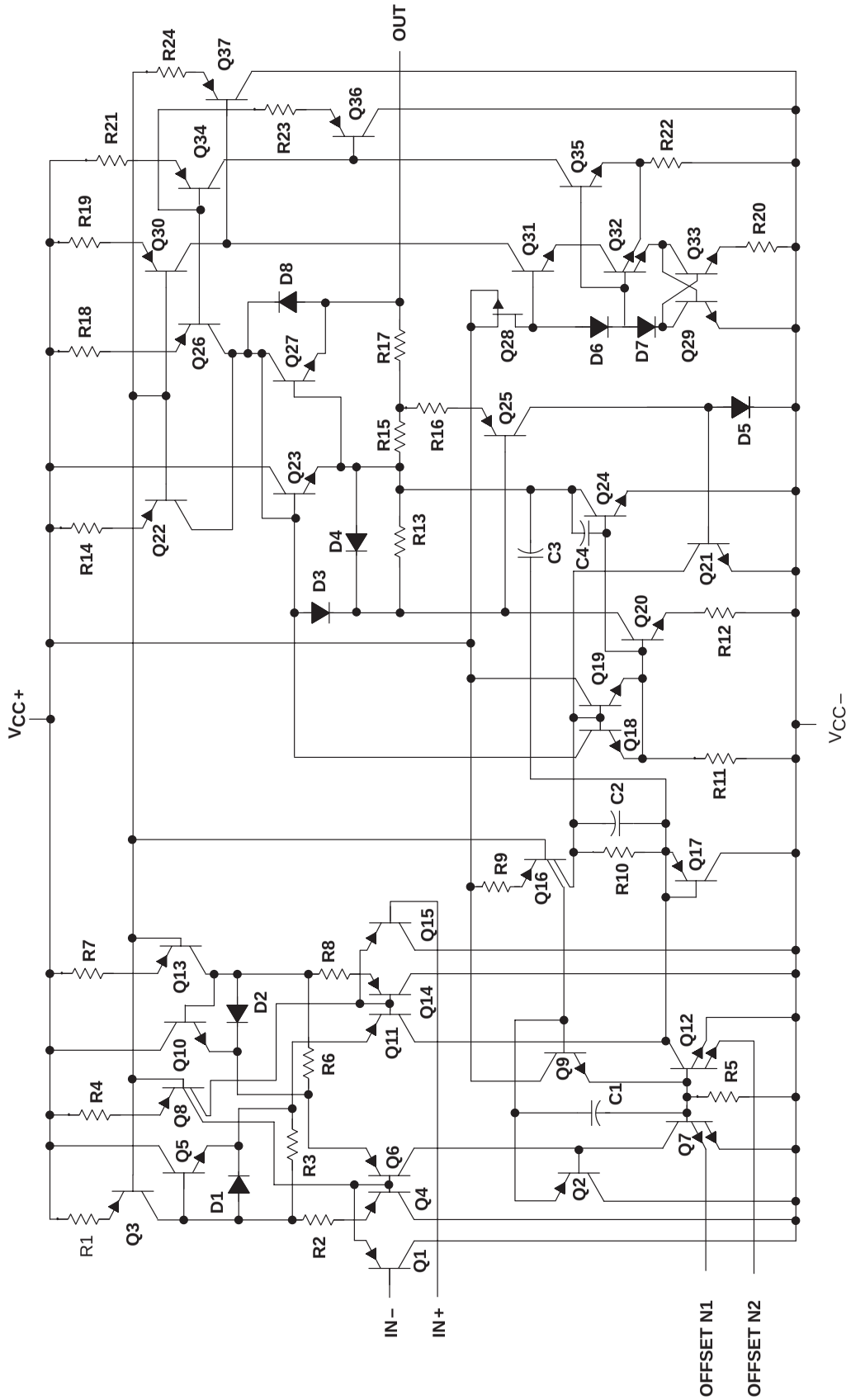
**BONDING PADS: 4 × 4 MINIMUM**

**$T_{Jmax}$ = 150°C**

**TOLERANCES ARE ±10%**

**ALL DIMENSIONS ARE IN MILS**

## equivalent schematic



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC+}$ (see Note 1) . . . . . 22 V
Supply voltage, $V_{CC-}$ (see Note 1) . . . . . –22 V
Differential input voltage (see Note 2) . . . . . ±44 V
Input voltage range, $V_I$ (any input) . . . . . $V_{CC+}$ to $V_{CC-}$ – 0.3 V
Input current, $I_I$ (each input) . . . . . ±1 mA
Output current, $I_O$ . . . . . ±80 mA
Total current into $V_{CC+}$ . . . . . 80 mA
Total current out of $V_{CC-}$ . . . . . 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$ . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between $V_{CC+}$ and $V_{CC-}$.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input voltage is brought below $V_{CC-}$ – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 105°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 495 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 378 mW | 210 mW |

## recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC\pm}$ | | ±2 | ±22 | V |
| Common-mode input voltage, $V_{IC}$ | $V_{CC}$ = 5 V | 0 | 2.7 | V |
| | $V_{CC\pm}$ = ±15 V | –15 | 12.7 | |
| Operating free-air temperature, $T_A$ | | –55 | 125 | °C |

## electrical characteristics at specified free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$† | TLE2141M | | | TLE2141AM | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 2.5 V, $R_S$ = 50 Ω, $V_{IC}$ = 2.5 V | 25°C | | 225 | 1400 | | 200 | 1000 | μV |
| | | | Full range | | | 2100 | | | 1700 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | Full range | | 1.7 | | | 1.7 | | μV/°C |
| $I_{IO}$ | Input offset current | | 25°C | | 8 | 100 | | 8 | 100 | nA |
| | | | Full range | | | 250 | | | 250 | |
| $I_{IB}$ | Input bias current | | 25°C | | −0.8 | −2 | | −0.8 | −2 | μA |
| | | | Full range | | | −2.3 | | | −2.3 | |
| $V_{ICR}$ | Common-mode input voltage range | $R_S$ = 50 Ω | 25°C | 0 to 3 | −0.3 to 3.2 | | 0 to 3 | −0.3 to 3.2 | | V |
| | | | Full range | 0 to 2.7 | −0.3 to 2.9 | | 0 to 2.7 | −0.3 to 2.9 | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −150 μA | 25°C | 3.9 | 4.1 | | 3.9 | 4.1 | | V |
| | | $I_{OH}$ = −1.5 mA | | 3.8 | 4 | | 3.8 | 4 | | |
| | | $I_{OH}$ = −15 mA | | 3.2 | 3.7 | | 3.2 | 3.7 | | |
| | | $I_{OH}$ = −100 μA | Full range | 3.75 | | | 3.75 | | | |
| | | $I_{OH}$ = −1 mA | | 3.65 | | | 3.65 | | | |
| | | $I_{OH}$ = −10 mA | | 3.25 | | | 3.25 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 150 μA | 25°C | | 75 | 125 | | 75 | 125 | mV |
| | | $I_{OL}$ = 1.5 mA | | | 150 | 225 | | 150 | 225 | |
| | | $I_{OL}$ = 15 mA | | | 1.2 | 1.4 | | 1.2 | 1.4 | V |
| | | $I_{OL}$ = 100 μA | Full range | | | 200 | | | 200 | |
| | | $I_{OL}$ = 1 mA | | | | 250 | | | 250 | mV |
| | | $I_{OL}$ = 10 mA | | | | 1.25 | | | 1.25 | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{CC}$ = ±2.5 V, $R_L$ = 2 kΩ, $V_O$ = 1 V to −1.5 V | 25°C | 50 | 220 | | 50 | 220 | | V/mV |
| | | | Full range | 5 | | | 5 | | | |
| $r_i$ | Input resistance | | 25°C | | 70 | | | 70 | | MΩ |
| $c_i$ | Input capacitance | | 25°C | | 2.5 | | | 2.5 | | pF |
| $z_o$ | Open-loop output impedance | f = 1 MHz | 25°C | | 30 | | | 30 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min, $R_S$ = 50 Ω | 25°C | 85 | 118 | | 85 | 118 | | dB |
| | | | Full range | 80 | | | 80 | | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | $V_{CC\pm}$ = ±2.5 V to ±15 V, $R_S$ = 50 Ω | 25°C | 90 | 106 | | 90 | 106 | | dB |
| | | | Full range | 85 | | | 85 | | | |
| $I_{CC}$ | Supply current | $V_O$ = 2.5 V, No load, $V_{IC}$ = 2.5 V | 25°C | | 3.4 | 4.4 | | 3.4 | 4.4 | mA |
| | | | Full range | | | 4.6 | | | 4.6 | |

† Full range is −55°C to 125°C.

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TLE2141M | | | TLE2141AM | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR+ | Positive slew rate | $A_{VD}$ = –1, $C_L$ = 500 pF | $R_L$= 2 kΩ†, | | 45 | | | 45 | | V/μs |
| SR– | Negative slew rate | | | | 42 | | | 42 | | |
| | Settling time | $A_{VD}$ = –1, 2.5-V step | To 0.1% | | 0.16 | | | 0.16 | | μs |
| | | | To 0.01% | | 0.22 | | | 0.22 | | |
| $V_n$ | Equivalent input noise voltage | $R_S$ = 100 Ω, | f = 10 Hz | | 15 | | | 15 | | nV/√Hz |
| | | $R_S$ = 100 Ω, | f = 1 kHz | | 10.5 | | | 10.5 | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | | | 0.48 | | | 0.48 | | μV |
| | | f = 0.1 Hz to 10 Hz | | | 0.51 | | | 0.51 | | |
| $I_n$ | Equivalent input noise current | f = 10 Hz | | | 1.92 | | | 1.92 | | pA/√Hz |
| | | f = 1 kHz | | | 0.5 | | | 0.5 | | |
| THD + N | Total harmonic distortion plus noise | $V_O$ = 1 V to 3 V, $A_{VD}$ = 2, | $R_L$= 2 kΩ†, f = 10 kHz | | 0.0052% | | | 0.0052% | | |
| B1 | Unity-gain bandwidth | $R_L$= 2 kΩ†, | $C_L$ = 100 pF | | 5.9 | | | 5.9 | | MHz |
| | Gain-bandwidth product | $R_L$= 2 kΩ†, f = 100 kHz | $C_L$ = 100 pF, | | 5.8 | | | 5.8 | | MHz |
| $B_{OM}$ | Maximum output-swing bandwidth | $R_L$= 2 kΩ†, $A_{VD}$ = 1 | $V_{O(PP)}$ = 2 V, | | 6.6 | | | 6.6 | | MHz |
| $\phi_m$ | Phase margin at unity gain | $R_L$= 2 kΩ†, | $C_L$ = 100 pF | | 57° | | | 57° | | |

† $R_L$ terminates at 2.5 V.

## electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$† | TLE2141M | | | TLE2141AM | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = 0, | $R_S$ = 50 Ω | 25°C | | 200 | 900 | | 175 | 500 | μV |
| | | | | Full range | | | 1700 | | | 1200 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | | Full range | | 1.7 | | | 1.7 | | μV/°C |
| $I_{IO}$ | Input offset current | | | 25°C | | 7 | 100 | | 7 | 100 | nA |
| | | | | Full range | | | 250 | | | 250 | |
| $I_{IB}$ | Input bias current | | | 25°C | | −0.7 | −1.5 | | −0.7 | −1.5 | μA |
| | | | | Full range | | | −1.8 | | | −1.8 | |
| $V_{ICR}$ | Common-mode input voltage range | $R_S$ = 50 Ω | | 25°C | −15 to 13 | −15.3 to 13.2 | | −15 to 13 | −15.3 to 13.2 | | V |
| | | | | Full range | −15 to 12.7 | −15.3 to 12.9 | | −15 to 12.7 | −15.3 to 12.9 | | |
| $V_{OM+}$ | Maximum positive peak output voltage swing | $I_O$ = −150 μA | | 25°C | 13.8 | 14.1 | | 13.8 | 14.1 | | V |
| | | $I_O$ = −1.5 mA | | | 13.7 | 14 | | 13.7 | 14 | | |
| | | $I_O$ = −15 mA | | | 13.1 | 13.7 | | 13.1 | 13.7 | | |
| | | $I_O$ = −100 μA | | Full range | 13.7 | | | 13.7 | | | |
| | | $I_O$ = −1 mA | | | 13.6 | | | 13.6 | | | |
| | | $I_O$ = −10 mA | | | 13.1 | | | 13.1 | | | |
| $V_{OM-}$ | Maximum negative peak output voltage swing | $I_O$= 150 μA | | 25°C | −14.7 | −14.9 | | −14.7 | −14.9 | | V |
| | | $I_O$= 1.5 mA | | | −14.5 | −14.8 | | −14.5 | −14.8 | | |
| | | $I_O$ = 15 mA | | | −13.4 | −13.8 | | −13.4 | −13.8 | | |
| | | $I_O$ = 100 μA | | Full range | −14.6 | | | −14.6 | | | |
| | | $I_O$ = 1 mA | | | −14.5 | | | −14.5 | | | |
| | | $I_O$ = 10 mA | | | −13.4 | | | −13.4 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_O$ = ±10 V, | $R_L$ = 2 kΩ | 25°C | 100 | 450 | | 100 | 450 | | V/mV |
| | | | | Full range | 20 | | | 20 | | | |
| $r_i$ | Input resistance | | | 25°C | | 65 | | | 65 | | MΩ |
| $c_i$ | Input capacitance | | | 25°C | | 2.5 | | | 2.5 | | pF |
| $z_o$ | Open-loop output impedance | f = 1 MHz | | 25°C | | 30 | | | 30 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$ min, | $R_S$ = 50 Ω | 25°C | 85 | 108 | | 85 | 108 | | dB |
| | | | | Full range | 80 | | | 80 | | | |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | $V_{CC\pm}$ = ±2.5 V to ±15 V, | $R_S$ = 50 Ω | 25°C | 90 | 106 | | 90 | 106 | | dB |
| | | | | Full range | 85 | | | 85 | | | |
| $I_{OS}$ | Short-circuit output current | $V_O$ = 0 | $V_{ID}$ = 1 V | 25°C | −25 | −50 | | −25 | −50 | | mA |
| | | | $V_{ID}$ = −1 V | | 20 | 31 | | 20 | 31 | | |
| $I_{CC}$ | Supply current | $V_O$ = 0, $V_{IC}$ = 2.5 V | No load, | 25°C | | 3.5 | 4.5 | | 3.5 | 4.5 | mA |
| | | | | Full range | | | 4.7 | | | 4.7 | |

† Full range is −55°C to 125°C.

## operating characteristics, $V_{CC\pm}$ = ±15, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TLE2141M | | | TLE2141AM | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR+ | Positive slew rate | $A_{VD}$ = –1, $C_L$ = 500 pF | $R_L$ = 2 kΩ, | 30 | 45 | | 30 | 45 | | V/µs |
| SR– | Negative slew rate | | | 30 | 42 | | 30 | 42 | | |
| | Settling time | $A_{VD}$ = –1, 10-V step | To 0.1% | | 0.34 | | | 0.34 | | µs |
| | | | To 0.01% | | 0.4 | | | 0.4 | | |
| $V_n$ | Equivalent input noise voltage | $R_S$ = 100 Ω, | f = 10 Hz | | 15 | | | 15 | | nV/√Hz |
| | | $R_S$ = 100 Ω, | f = 1 kHz | | 10.5 | | | 10.5 | | |
| $V_{N(PP)}$ | Peak-to-peak equivalent input noise voltage | f = 0.1 Hz to 1 Hz | | | 0.48 | | | 0.48 | | µV |
| | | f = 0.1 Hz to 10 Hz | | | 0.51 | | | 0.51 | | |
| $I_n$ | Equivalent input noise current | f = 10 Hz | | | 1.89 | | | 1.89 | | pA/√Hz |
| | | f = 1 kHz | | | 0.47 | | | 0.47 | | |
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)}$ = 20 V, $A_{VD}$ = 10, | $R_L$ = 2 kΩ, f = 10 kHz | | 0.01% | | | 0.01% | | |
| $B_1$ | Unity-gain bandwidth | $R_L$ = 2 kΩ, | $C_L$ = 100 pF | | 6 | | | 6 | | MHz |
| | Gain-bandwidth product | $R_L$ = 2 kΩ, f = 100 kHz | $C_L$ = 100 pF, | | 5.9 | | | 5.9 | | MHz |
| $B_{OM}$ | Maximum output-swing bandwidth | $V_{O(PP)}$ = 20 V, $A_{VD}$ = 1, | $R_L$ = 2 kΩ, $C_L$ = 100 pF | | 668 | | | 668 | | kHz |
| $\phi_m$ | Phase margin at unity gain | $R_L$ = 2 kΩ, | $C_L$ = 100 pF | | 58° | | | 58° | | |

## electrical characteristics, $V_{CC\pm}$ = ±15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = 0, $R_S$ = 50 Ω, $V_O$ = 0 | | | 200 | 1000 | μV |
| $I_{IO}$ | Input offset current | | | | 7 | 100 | nA |
| $I_{IB}$ | Input bias current | | | | –0.7 | –1.5 | μA |
| $V_{ICR}$ | Common-mode input voltage range | $R_S$ = 50 Ω | | –15 to 13 | –15.3 to 13.2 | | V |
| $V_{OM+}$ | Maximum positive peak output voltage swing | $I_O$ = –150 μA | | 13.8 | 14.1 | | V |
| | | $I_O$ = –1.5 mA | | 13.7 | 14 | | |
| | | $I_O$ = –15 mA | | 13.3 | 13.7 | | |
| $V_{OM-}$ | Maximum negative peak output voltage swing | $I_O$= 150 μA | | –14.7 | –14.9 | | V |
| | | $I_O$= 1.5 mA | | –14.5 | –14.8 | | |
| | | $I_O$ = 15 mA | | –13.4 | –13.8 | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_O$ = ±10 V, $R_L$ = 2 kΩ | | 100 | 450 | | V/mV |
| $r_i$ | Input resistance | | | | 65 | | MΩ |
| $c_i$ | Input capacitance | | | | 2.5 | | pF |
| $z_o$ | Open-loop output impedance | f = 1 MHz | | | 30 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min, $R_S$ = 50 Ω | | 80 | 108 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | $V_{CC\pm}$ = ±2.5 V to ±15 V, $R_S$ = 50 Ω | | 85 | 106 | | dB |
| $I_{OS}$ | Short-circuit output current | $V_O$ = 0 | $V_{ID}$ = 1 V | –25 | –50 | | mA |
| | | | $V_{ID}$ = –1 V | 20 | 31 | | |
| $I_{CC}$ | Supply current | $V_O$ = 0, No load | | | 3.5 | 4.5 | mA |

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | | FIGURE |
|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | | Distribution | 1 |
| $I_{IO}$ | Input offset current | | vs Temperature | 2 |
| $I_{IB}$ | Input bias current | | vs Temperature<br>vs Common-mode input voltage | 3<br>4 |
| $V_{OM+}$ | Maximum positive peak output voltage | | vs Supply voltage<br>vs Temperature<br>vs Output current<br>vs Setting time | 5<br>6<br>7<br>9 |
| $V_{OM-}$ | Maximum negative peak output voltage | | vs Supply voltage<br>vs Temperature<br>vs Output curren<br>vs Setting time | 5<br>6<br>8<br>9 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage swing | | vs Frequency | 10 |
| $V_{OH}$ | High-level output voltage | | vs Output current | 11 |
| $V_{OL}$ | Low-level output voltage | | vs Output current | 12 |
| $A_{VD}$ | Differential voltage amplification | | vs Temperature<br>vs Frequency | 13<br>14 |
| $z_o$ | Closed loop output impedance | | vs Frequency | 15 |
| $I_{OS}$ | Short-circuit output current | | vs Supply current | 16 |
| CMRR | Common-mode rejection ratio | | vs Supply current<br>vs Temperature | 17<br>18 |
| $k_{SVR}$ | Supply-voltage rejection ratio | | vs Frequency<br>vs Temperature | 19<br>20 |
| $I_{CC}$ | Supply current | | vs Temperature<br>vs Supply voltage | 21<br>22 |
| $V_n$ | Equivalent input noise voltage | | vs Frequency | 23 |
| $V_{N(PP)}$ | Equivalent input noise voltage | | Over a 10-second period | 24 |
| $I_n$ | Noise current | | vs Frequency | 25 |
| THD + N | Total harmonic distortion plus noise | | vs Frequency | 26 |
| SR | Slew rate | | vs Temperature<br>vs Load capacitance | 27<br>28 |
| | Pulse response | Noninverting large signal | vs Time | 29 |
| | | Inverting large signal | vs Time | 30 |
| | | Small signal | vs Time | 31 |
| $B_1$ | Unity-gain-bandwidth | | vs Load capacitance | 32 |
| | Gain margin | | vs Load capacitance | 33 |
| $\phi_m$ | Phase margin | | vs Load capacitance | 34 |
| | Phase shift | | vs Frequency | 14 |

## TYPICAL CHARACTERISTICS

**TLE2141M
DISTRIBUTION OF
INPUT OFFSET VOLTAGE**

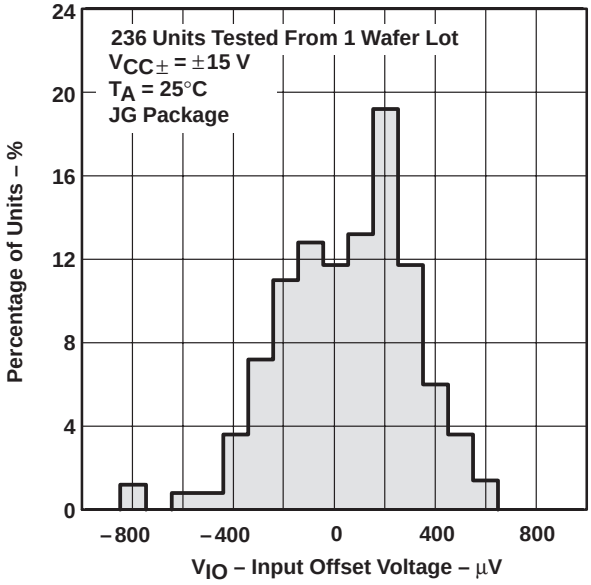



**Figure 1**

**INPUT OFFSET CUURENT
vs
FREE-AIR TEMPERATURE**

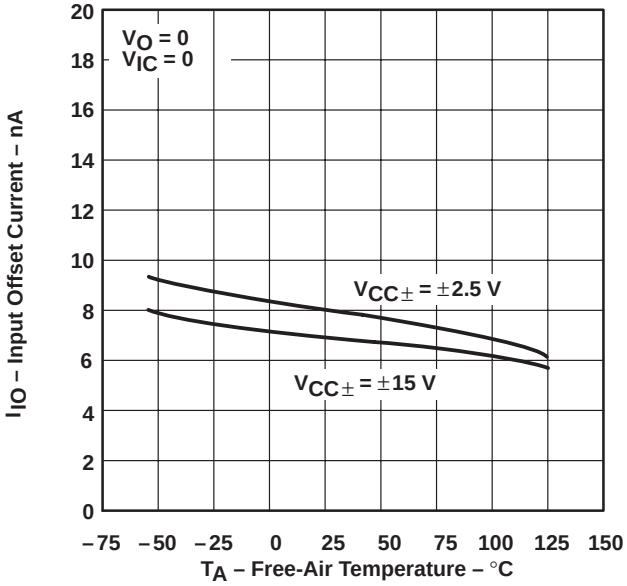



**Figure 2**

**INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE**

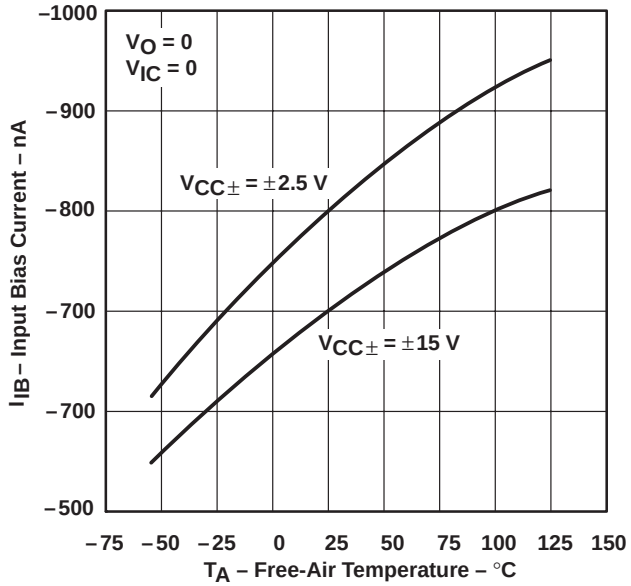



**Figure 3**

**INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE**

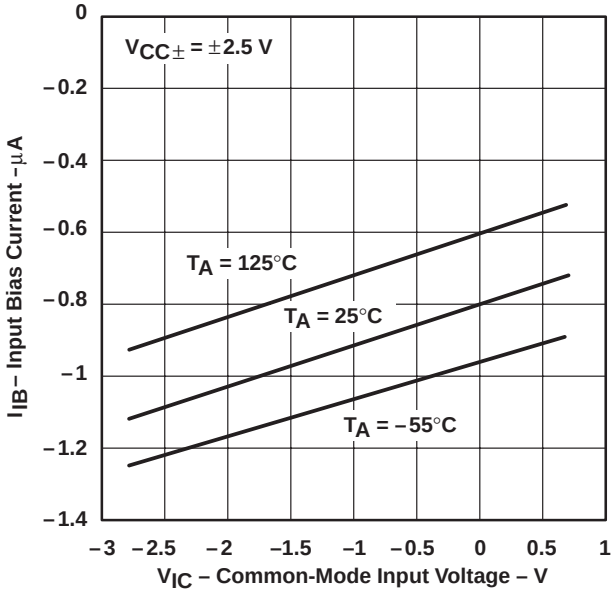



**Figure 4**

## TYPICAL CHARACTERISTICS

**MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE**

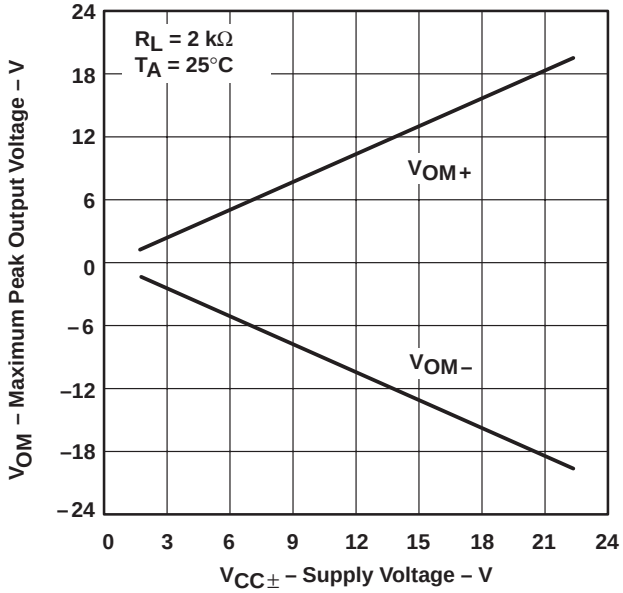



Figure 5

**MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

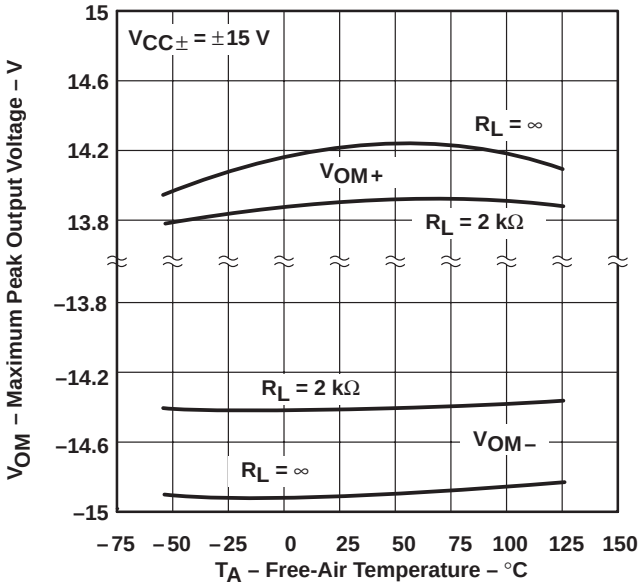



Figure 6

**MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT**

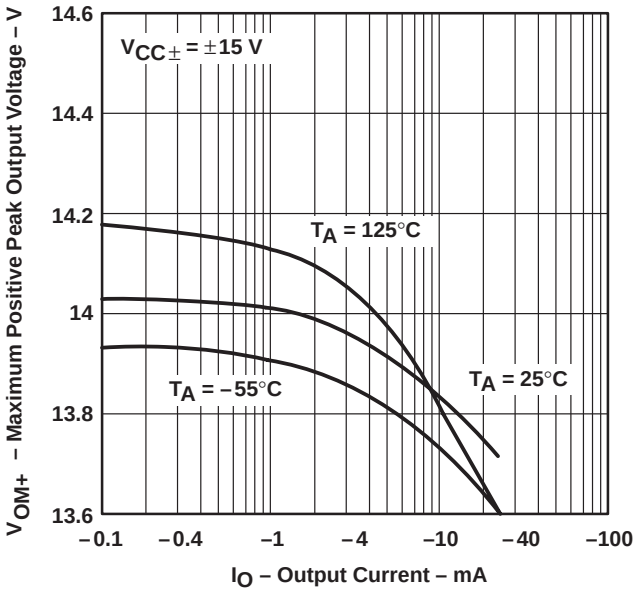



Figure 7

**MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT**

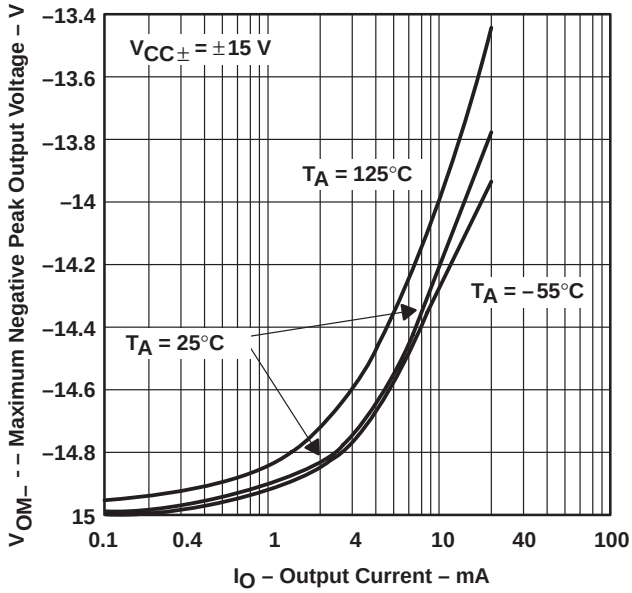



Figure 8

## TYPICAL CHARACTERISTICS

**MAXIMUM PEAK OUTPUT VOLTAGE vs SETTLING TIME**

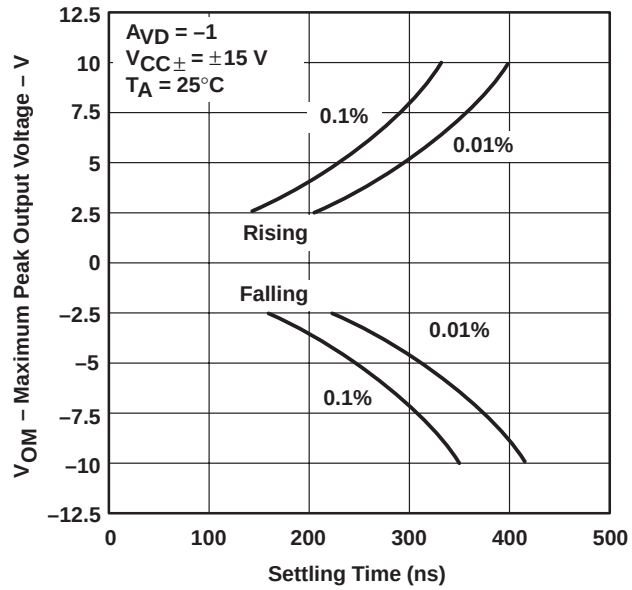



Figure 9

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

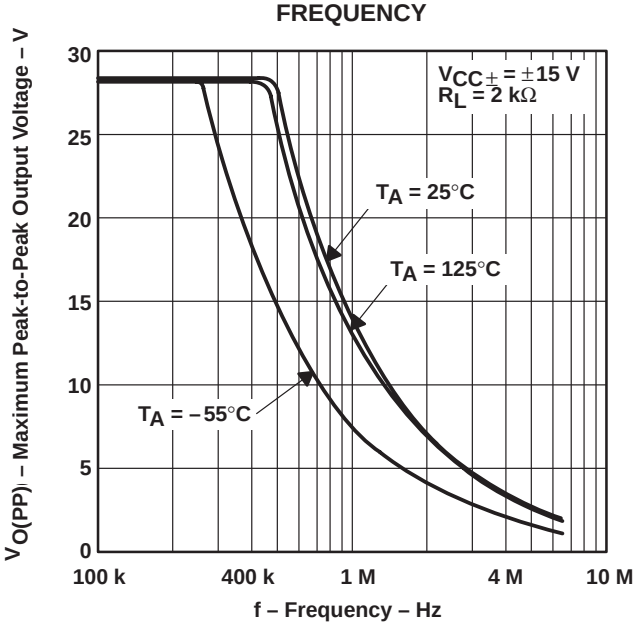



Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT**

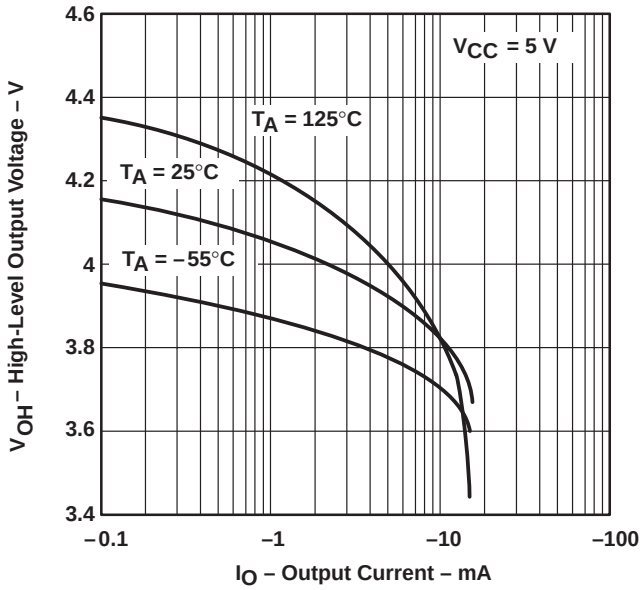



Figure 11

**LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT**

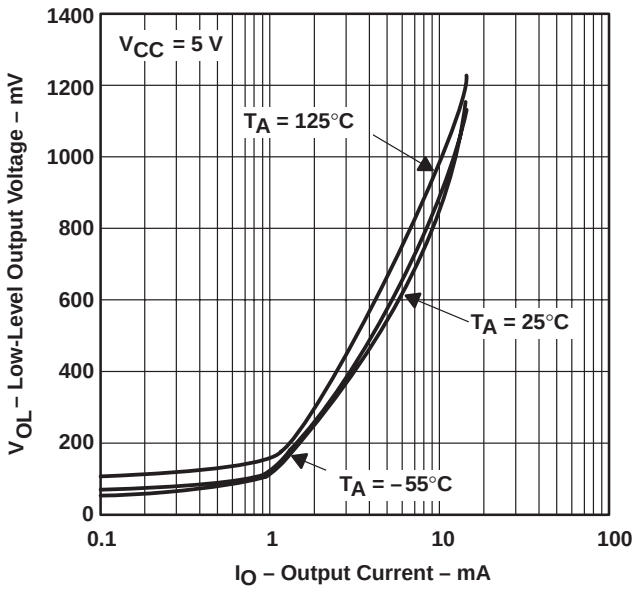



Figure 12

## TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE**

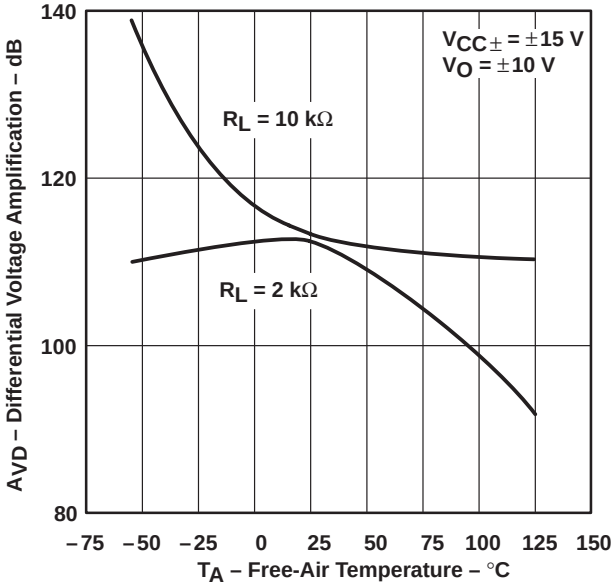



Figure 13

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY**

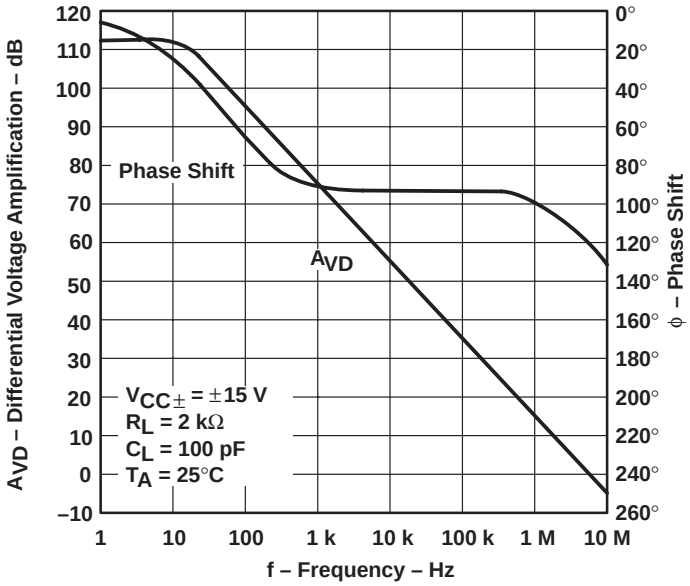



Figure 14

**CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

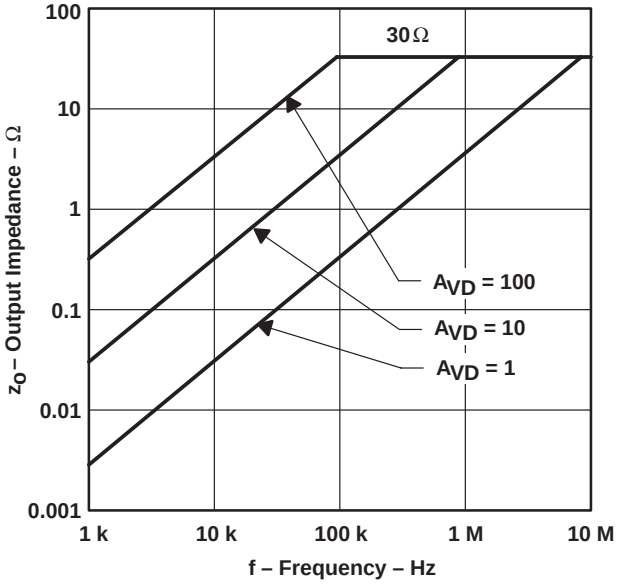



Figure 15

**SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE**

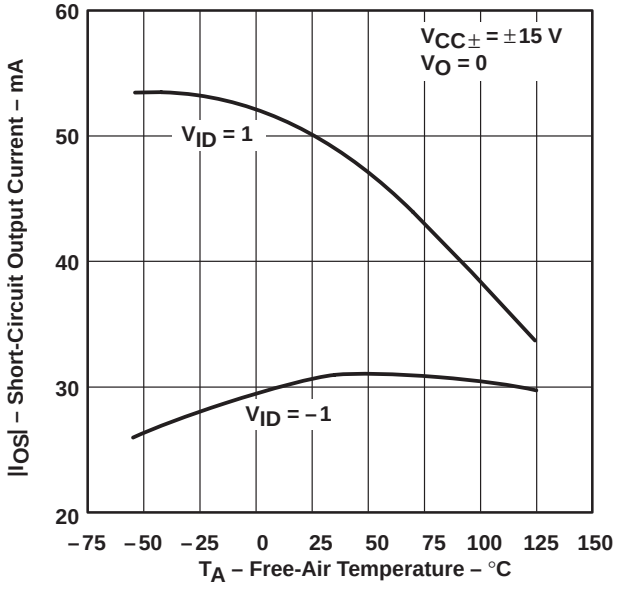



Figure 16

## TYPICAL CHARACTERISTICS

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

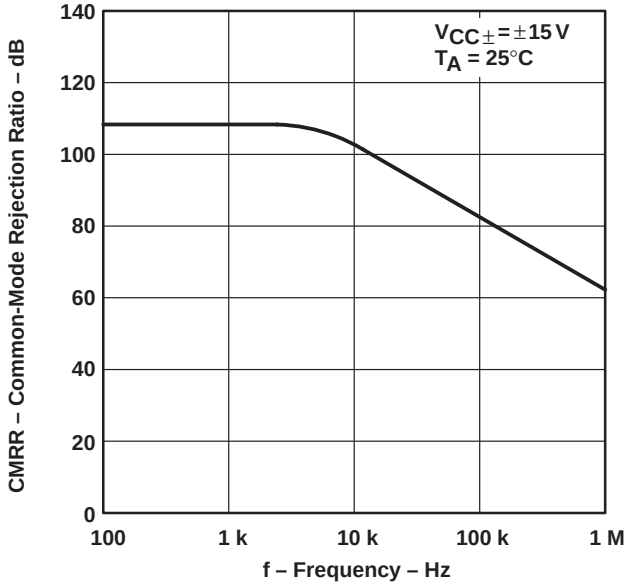



Figure 17

**COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE**

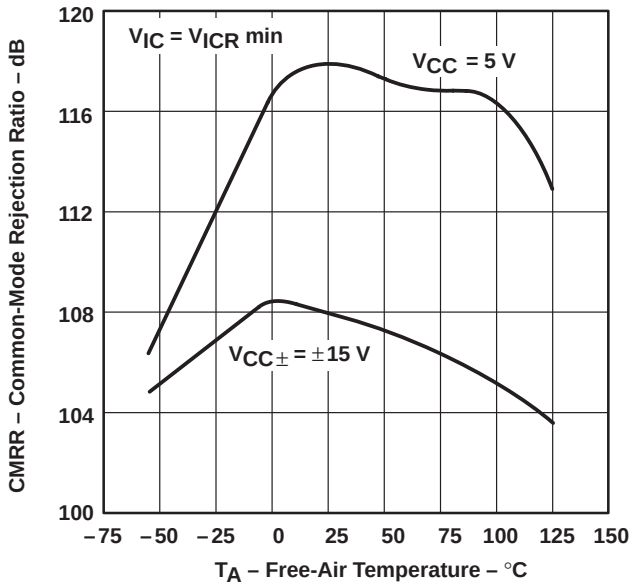



Figure 18

**SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY**

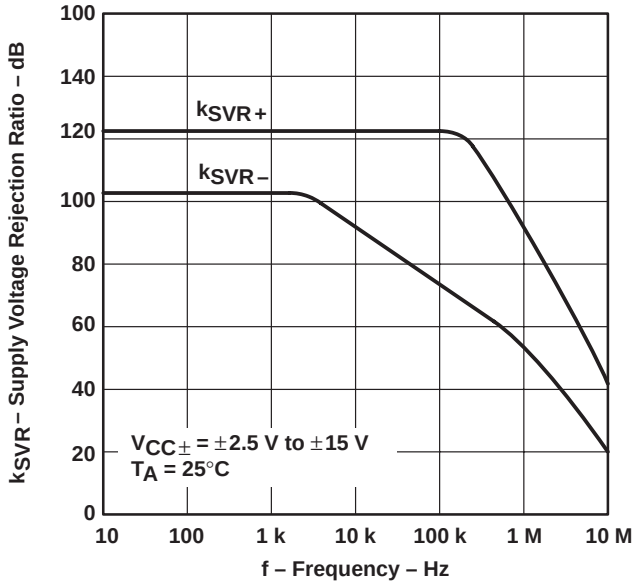



Figure 19

**SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE**

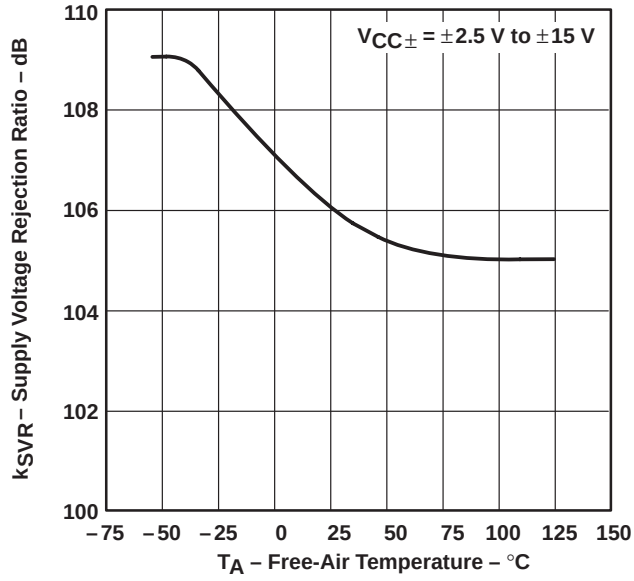



Figure 20

## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

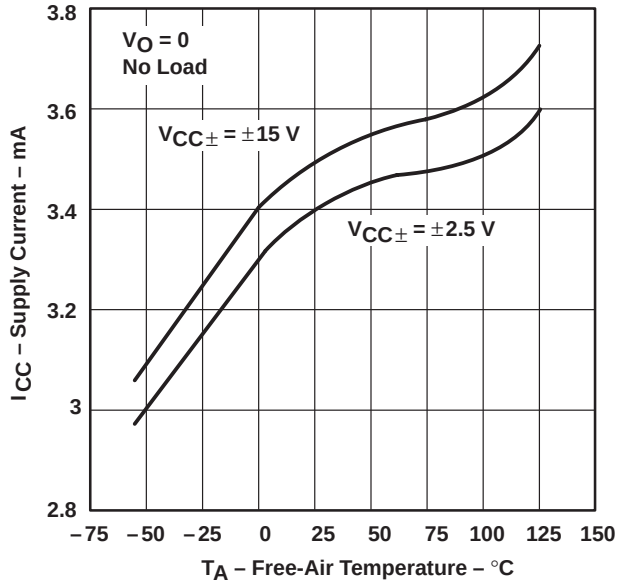



Figure 21

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

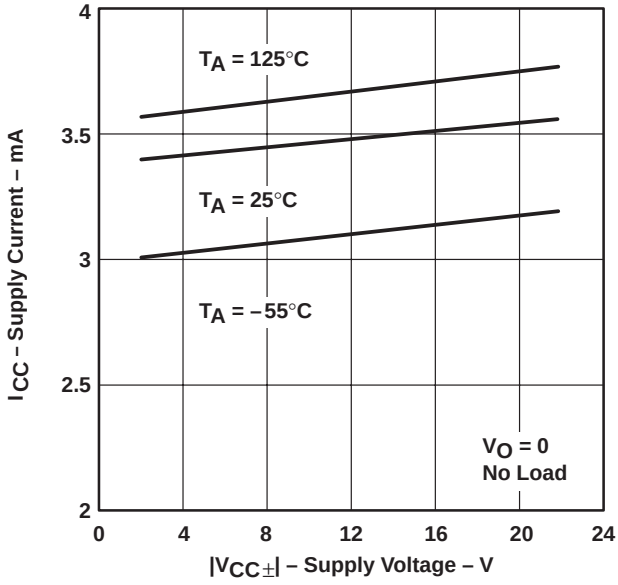



Figure 22

**EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY**

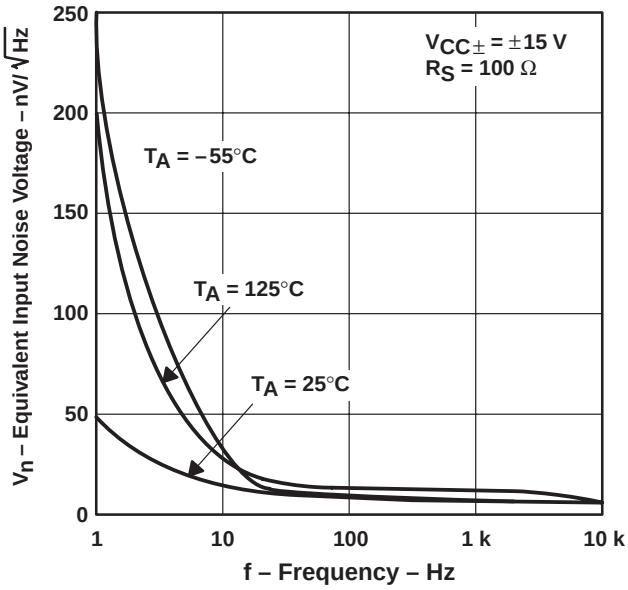



Figure 23

**EQUIVALENT INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD**

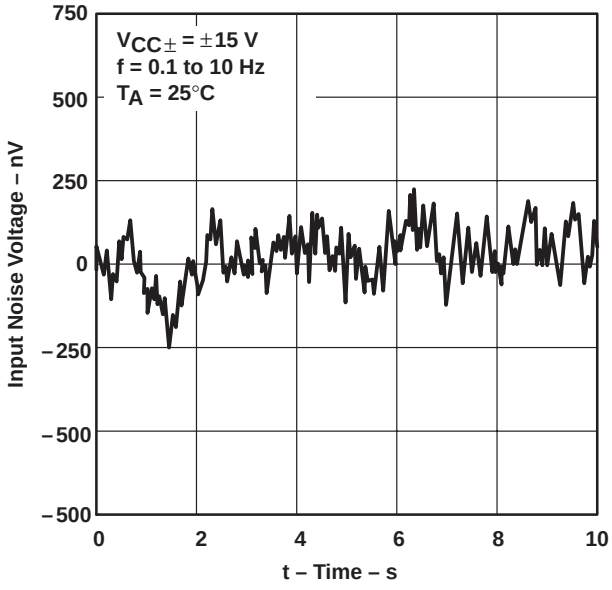



Figure 24

## TYPICAL CHARACTERISTICS

**NOISE CURRENT vs FREQUENCY**

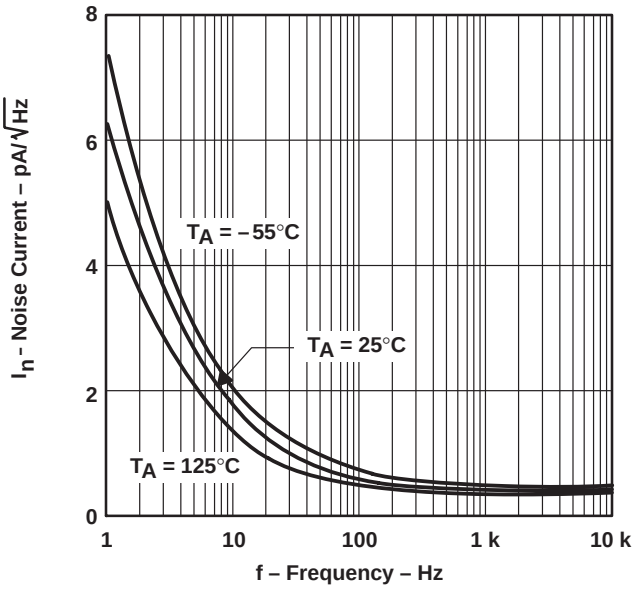



Figure 25

**TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY**

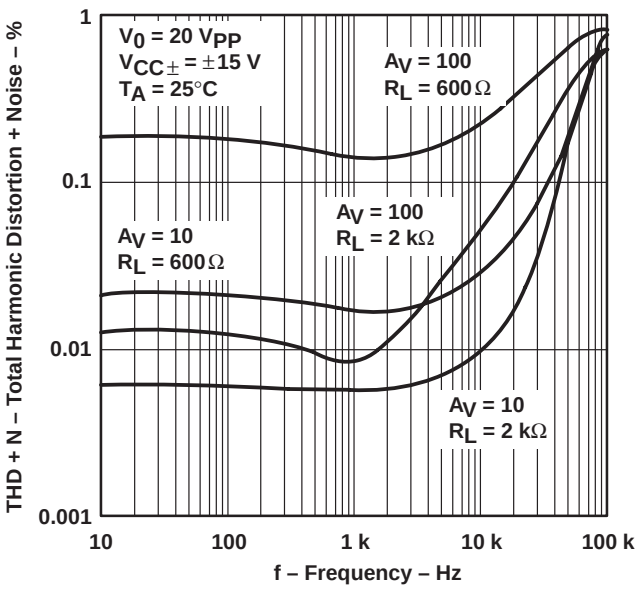



Figure 26

**SLEW RATE vs FREE-AIR TEMPERATURE**

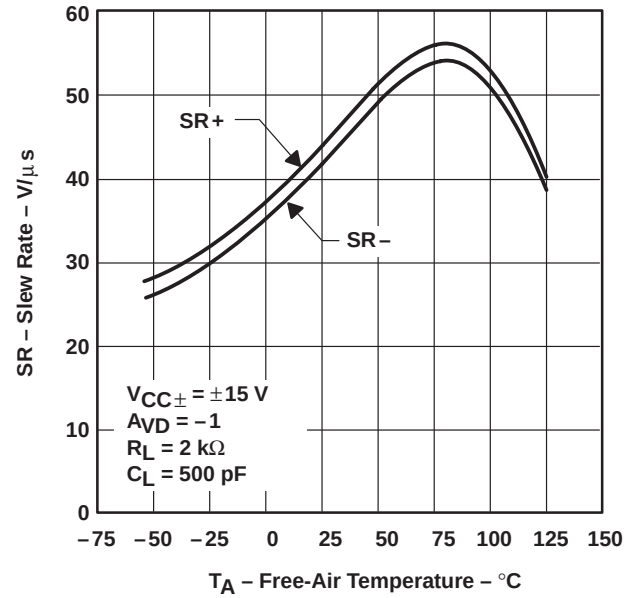



Figure 27

**SLEW RATE vs LOAD CAPACITANCE**

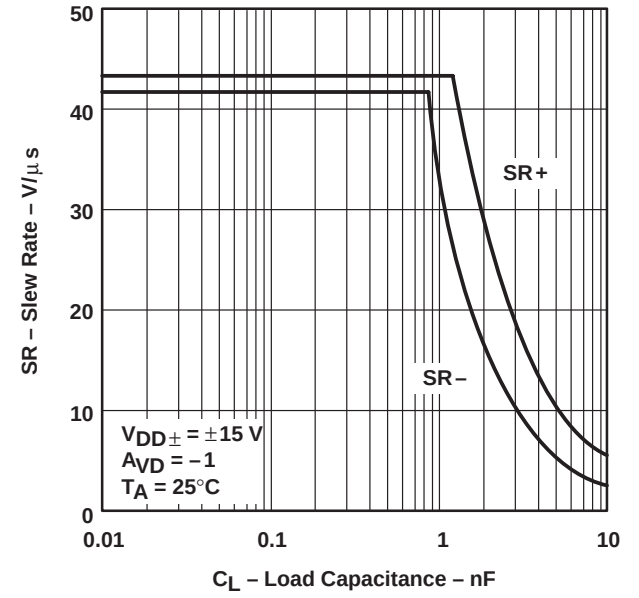



Figure 28

## TYPICAL CHARACTERISTICS

**NONINVERTING
LARGE-SIGNAL
PULSE RESPONSE**

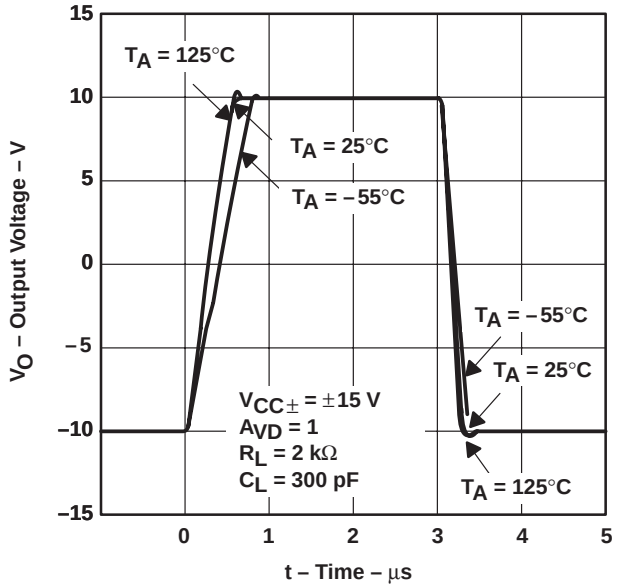



Figure 29

**INVERTING
LARGE-SIGNAL
PULSE RESPONSE**

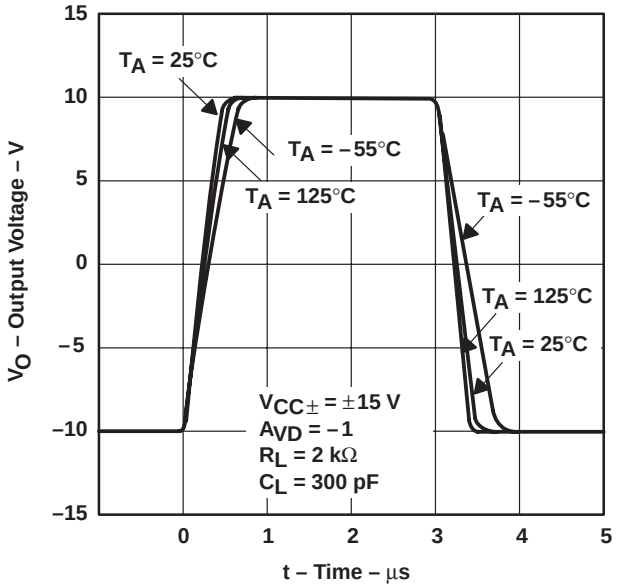



Figure 30

**SMALL-SIGNAL
PULSE RESPONSE**

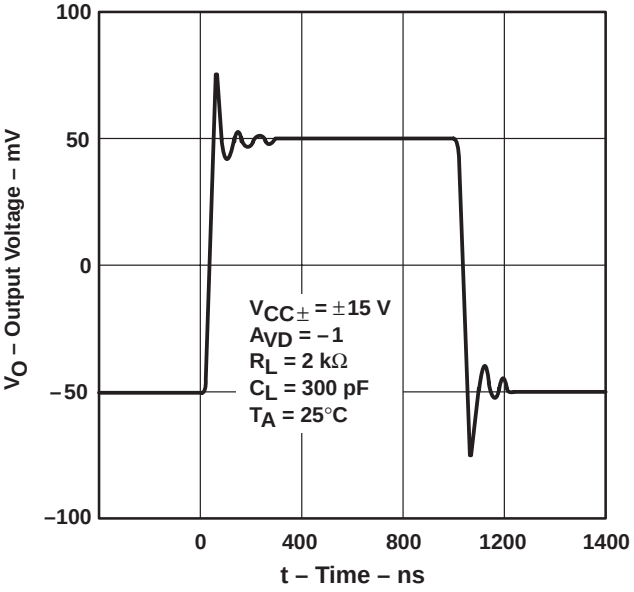



Figure 31

**UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE**

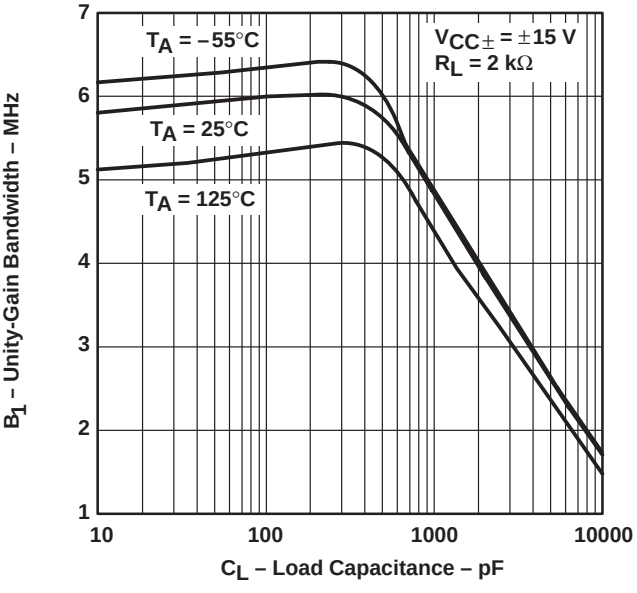



Figure 32

## TYPICAL CHARACTERISTICS

**GAIN MARGIN vs LOAD CAPCITANCE**

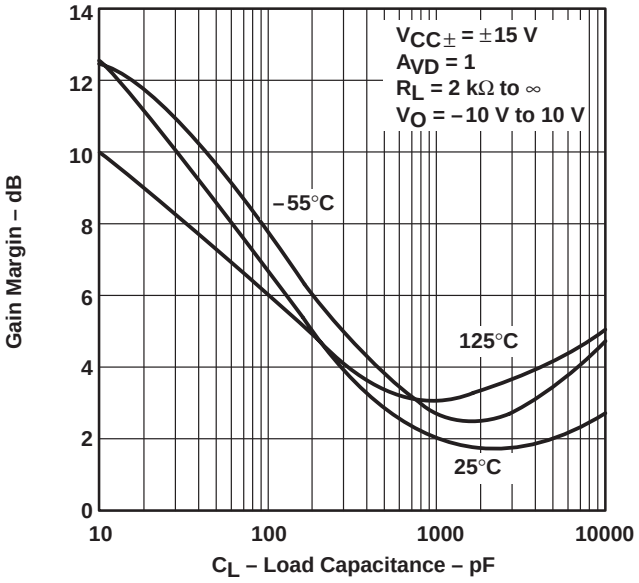



Figure 33

**PHASE MARGIN vs LOAD CAPACITANCE**

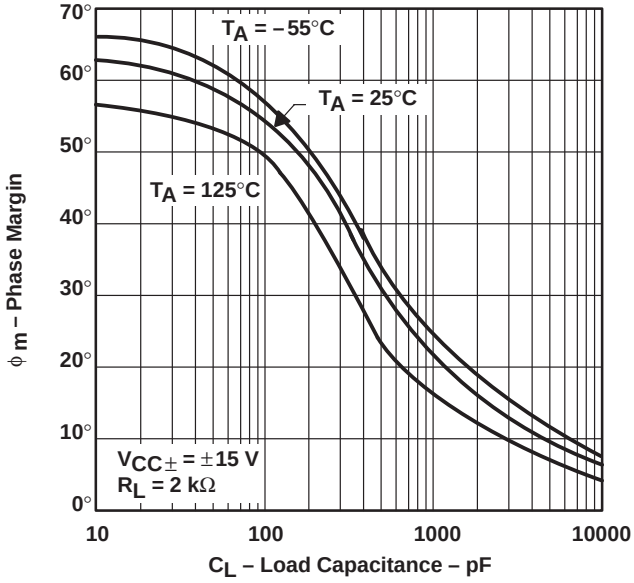



Figure 34

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9321601QPA | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 9321601QPA TLE2141M |
| 5962-9321602QPA | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 9321602QPA TLE2141AM |
| TLE2141AMJGB | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 9321602QPA TLE2141AM |
| TLE2141AMJGB.A | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 9321602QPA TLE2141AM |
| TLE2141MDG4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | 2141M |
| TLE2141MDG4.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | 2141M |
| TLE2141MDRG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | 2141M |
| TLE2141MDRG4.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | 2141M |
| TLE2141MJGB | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 9321601QPA TLE2141M |
| TLE2141MJGB.A | Active | Production | CDIP (JG) \| 8 | 50 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 9321601QPA TLE2141M |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

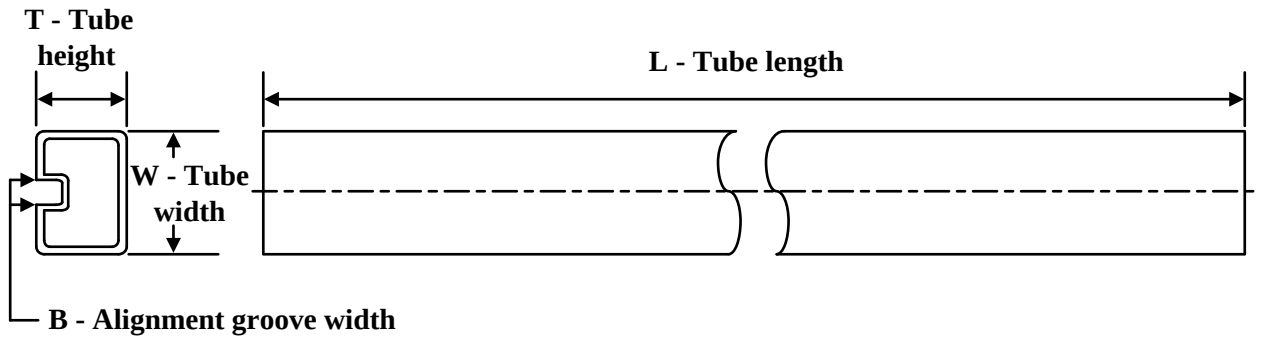
**OTHER QUALIFIED VERSIONS OF TLE2141AM, TLE2141M :**

- Catalog : TLE2141A, TLE2141
- Automotive : TLE2141-Q1
- Enhanced Product : TLE2141-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TLE2141MDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TLE2141MDG4.A | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |

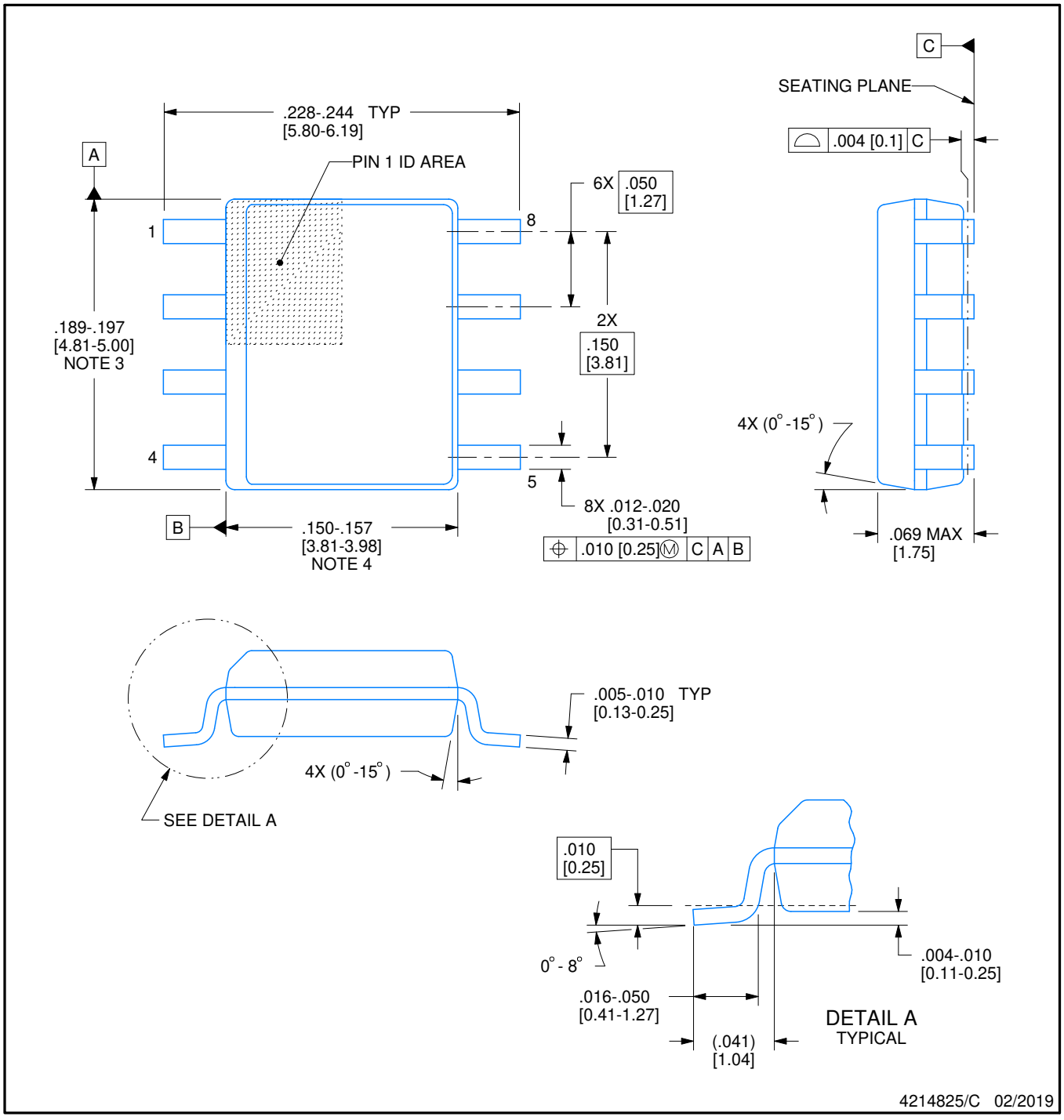


# PACKAGE OUTLINE

## D0008A

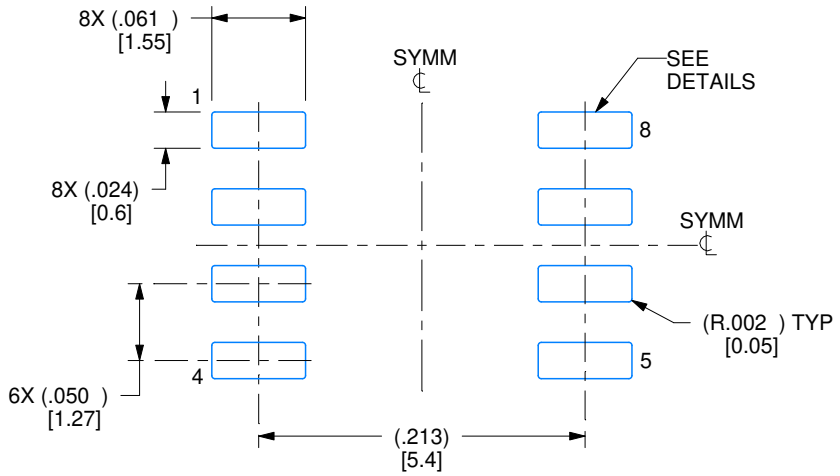
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

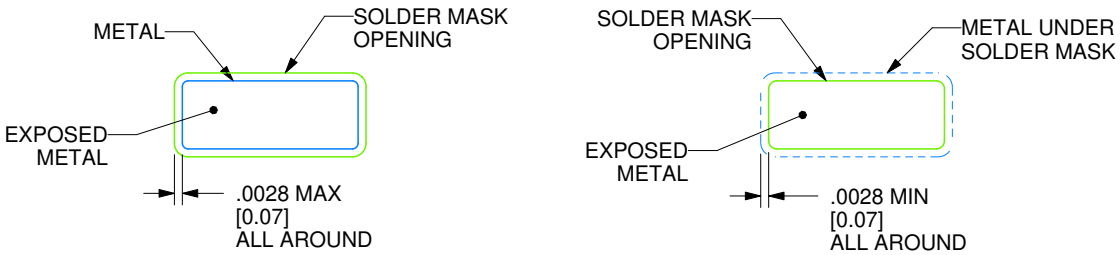



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

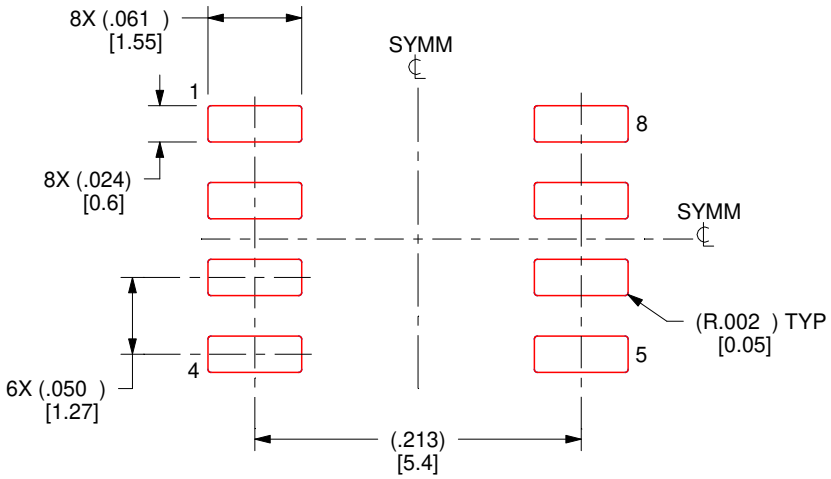
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

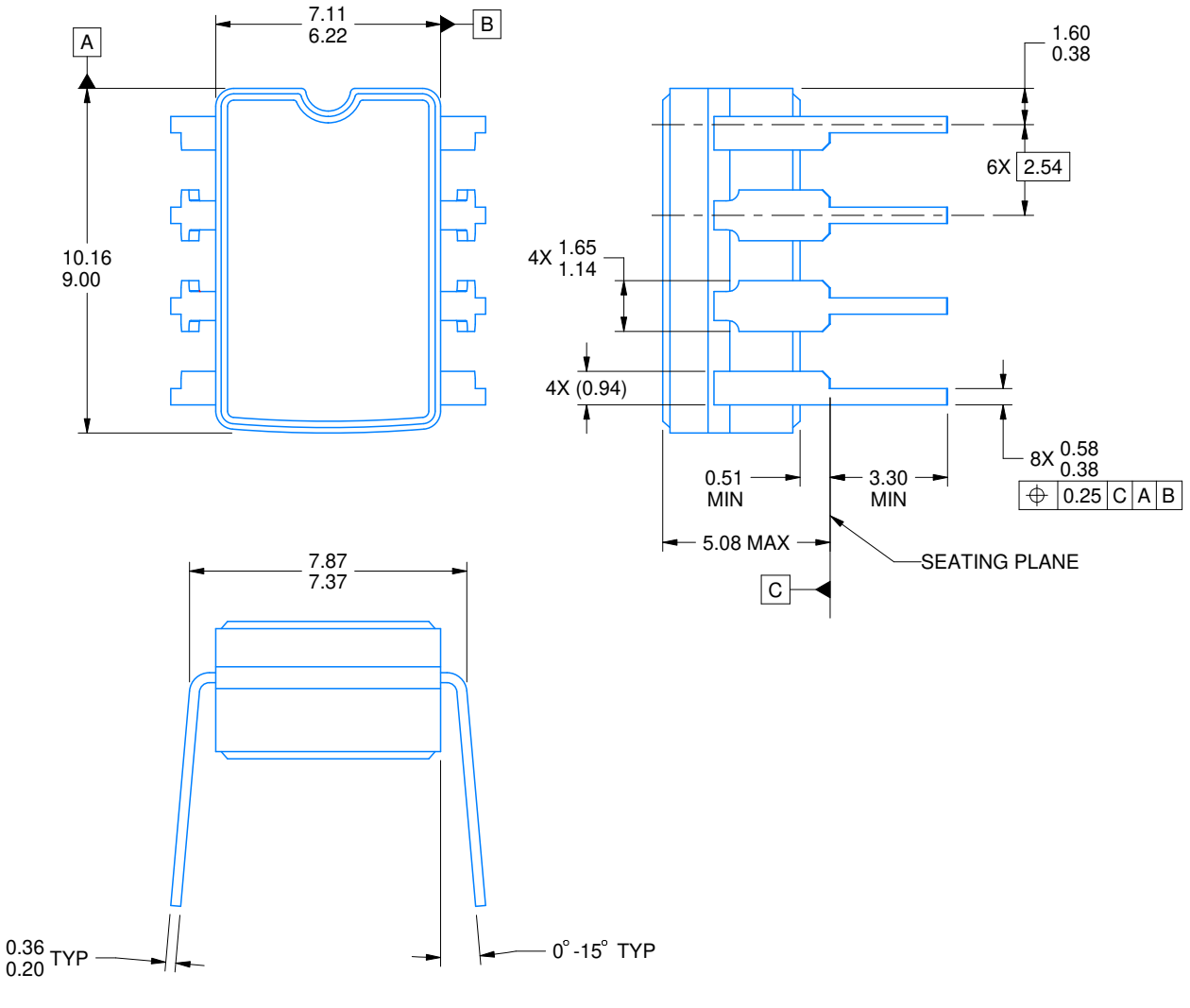
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## JG0008A

## CDIP - 5.08 mm max height

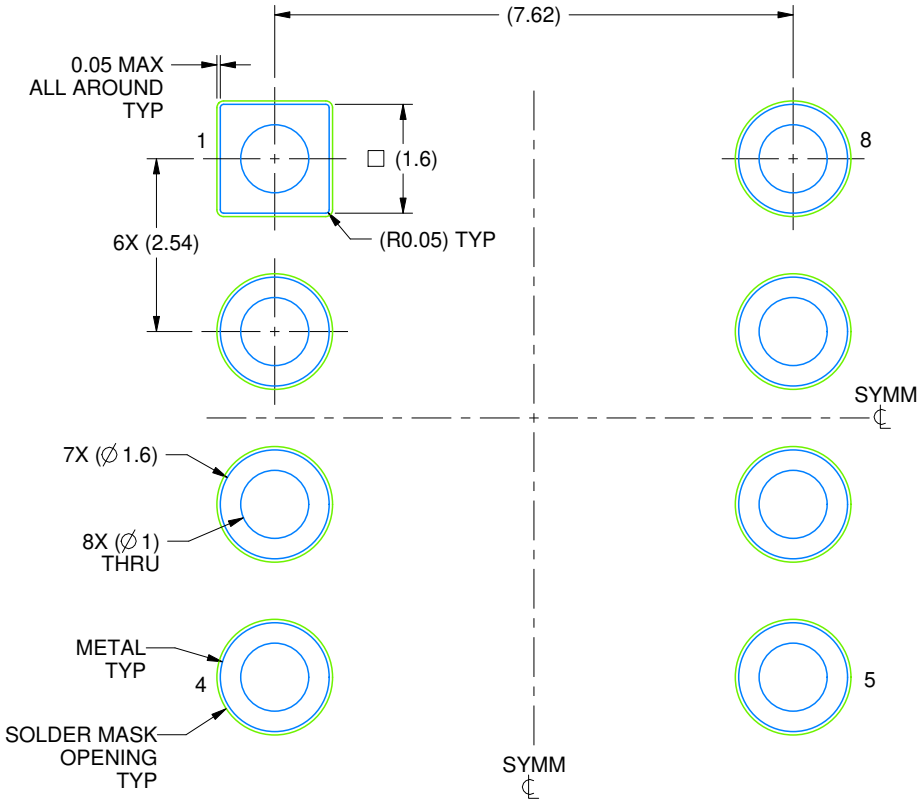
CERAMIC DUAL IN-LINE PACKAGE




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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8




LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

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