H-Bridge Driver IC

Features

- Compatible to very low ohmic normal level input N-Channel MOSFETs
- PWM – DIR - Interface
- PWM frequency up to 50kHz
- Operates down to 7.5V supply voltage
- Low EMC sensitivity and emission
- Adjustable dead time with shoot through protection
- Deactivation of dead time and shoot through protection possible
- Short circuit protection for each Mosfet
- Driver undervoltage shut down
- Reverse polarity protection for the driver IC
- Fast disable function / Inhibit for low quiescent current
- Input with TTL characteristics
- 2 bit diagnosis
- Thermal overload warning for driver IC
- Shoot through protection
- Integrated bootstrap diodes

Product Summary

Turn on current	$I_{Gxx(on)}$	850	mA
Turn off current	$I_{Gxx(off)}$	580	mA
Supply voltage range	V_{Vs}	7.5 … 60	V
Gate Voltage	V_{GS}	10	V
Temperature range	T_J	-40...+150	°C



P-DSO-20

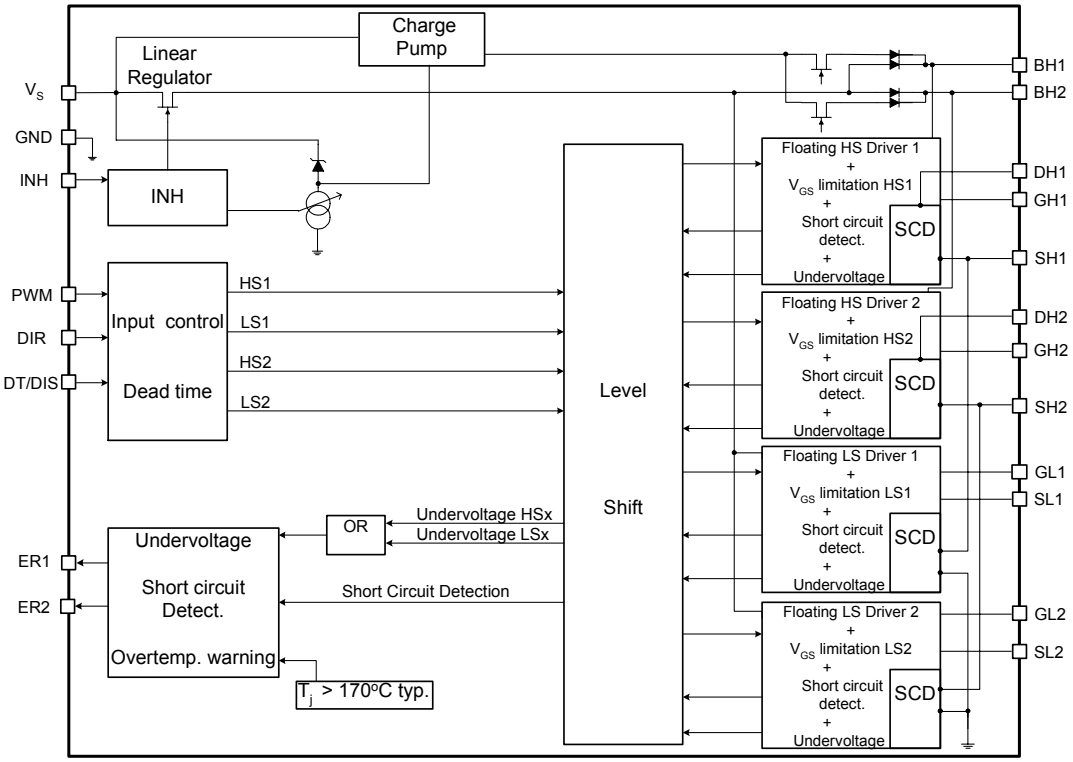
Application

- Dedicated for DC-brush high current motor bridges in PWM control mode for 12, 24 and 42V powernet applications.
- The input structure allows an easy control of a DC-brush motor

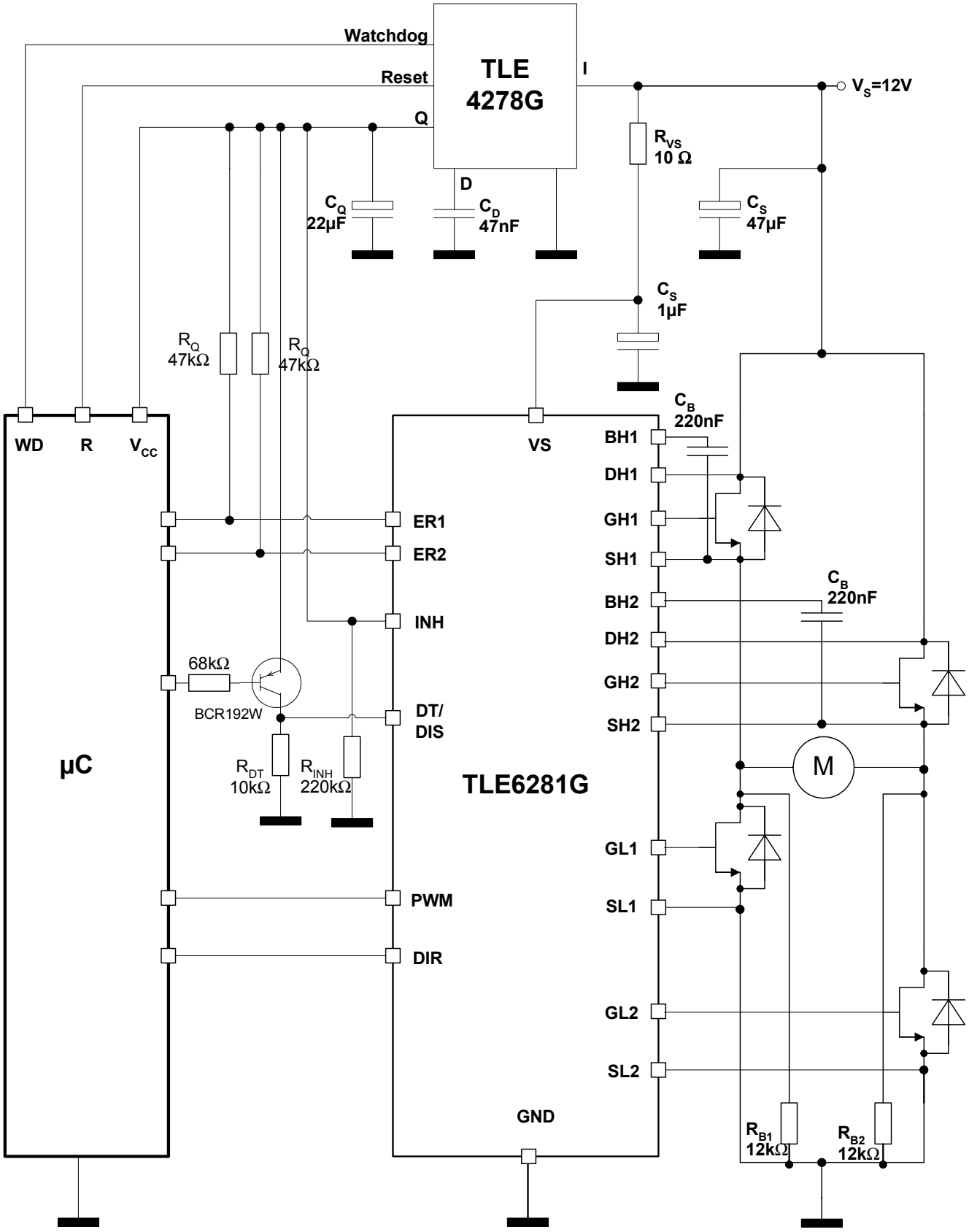
General Description

H-bridge driver IC for MOSFET power stages with multiple protection functions

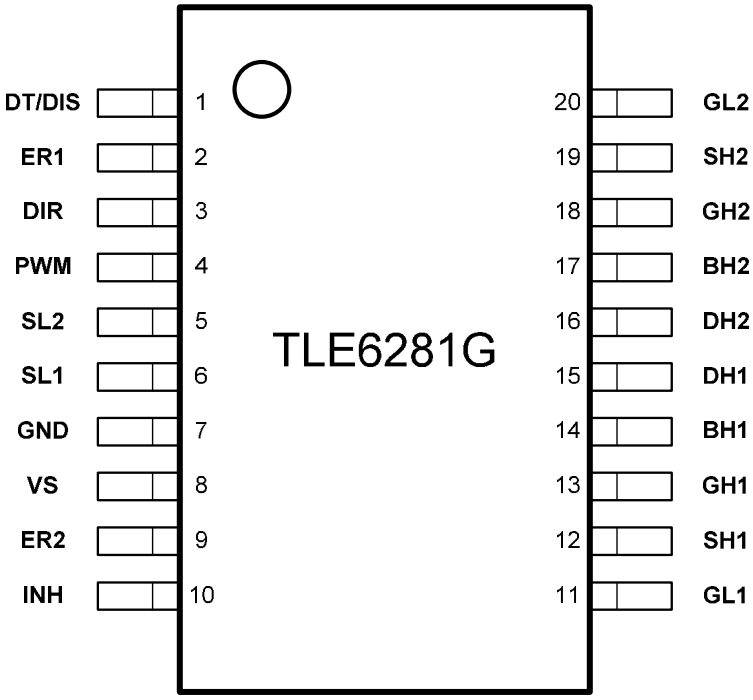
Block Diagram



Example Application Circuit



This example application circuit shows one possibility to use this Driver IC.



Pin	Symbol		Function
1	DT / DIS		a) Set adjustable dead time by external resistor b) Reset ERx register c) Disable output stages
2	ER1		Error flag for driver shut down
3	DIR		Control input for spinning direction of the motor
4	PWM		Control input for PWM frequency and duty cycle
5	SL2		Connection to source low side switch 2
6	SL1		Connection to source low side switch 1
7	GND		Logic Ground
8	VS		Voltage supply
9	ER2		Warning flag Temperature / distinguish if short circuit or undervoltage lock out occurred
10	INH		Sets complete device to sleep mode to achieve low quiescent currents
11	GL1		Output to gate low side switch 1
12	SH1		Connection to source high side switch 1
13	GH1		Output to gate high side switch 1
14	BH1		Bootstrap supply high side switch 1
15	DH1		Sense contact for short circuit detection high side 1
16	DH2		Sense contact for short circuit detection high side 2
17	BH2		Bootstrap supply high side switch 2
18	GH2		Output to gate high side switch 2
19	SH2		Connection to source high side switch 2
20	GL2		Output to gate low side switch 2

Maximum Ratings at T_j=-40…+150°C unless specified otherwise

Parameter	Symbol	Limits Values		Unit
		min	max	
Supply voltage [1]	V_S	-4	60	V
Operating temperature range	T_j	-40	150	°C
Storage temperature range	T_{stg}	-55	150	
Max. voltage range at PWM, DIR, DT/DIS		-1	6	V
Max. voltage range at ERx		-0.3	6	V
Max. voltage range at INH	V_{INH}	-0.6	60	V
Max. voltage range at BHx	V_{BHx}	-0.3	90	V
Max. voltage range at DHx[2]	V_{DHx}	-4	75	V
Max. voltage range at GHx[3]	V_{GHx}	-6.8	86	V
Max. voltage range at SHx[3]	V_{SHx}	-6.8	75	V
Max. voltage range at GLx	V_{GLx}	-2	12	V
Max. voltage range at SLx	V_{SLx}	-2	7	V
Max. voltage difference BHx – SHx	V_{BHx}-V_{SHx}	-0.3	17	V
Max. voltage difference Gxx – Sxx	V_{Gxx}-V_{Sxx}	-0.3	11	V
Power dissipation (DC) @ T_A=125°C / min.footprint	P_{tot}	--	0.33	W
Power dissipation (DC) @ T_A=85°C / min.footprint	P_{tot}	--	0.85	W
Electrostatic discharge voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 – 1993	V_{ESD}[4]	--	2	kV
Thermal resistance junction - ambient (minimal foot-print with thermal vias)	R_{thJA}	--	75	K/W
Thermal resistance junction - ambient (6 cm^2)	R_{thJA}	--	75	K/W

Functional range

Parameter and Conditions at T_j = -40…+150°C, unless otherwise specified	Symbol	Values		Unit
		min	max	
Supply voltage	V_S	7.5	60	V
Operating temperature range	T_j	-40	150	°C
Max. voltage range at PWM, DIR, DT/DIS		-0.3	5.5	V
Max. voltage range at ERx		-0.3	5.5	V
Max. voltage range at INH	V_{INH}	-0.6	60	V
Max. voltage range at BHx	V_{BHx}	-0.3	90	V
Max. voltage range at DHx[2]	V_{DHx}	-4	75	V
Max. voltage range at GHx[3]	V_{GHx}	-7	86	V
Max. voltage range at SHx[3]	V_{SHx}	-7	75	V

[1] With external resistor (≥10 Ω) and capacitor
[2] The min value -4V is reduced to –(V_{BHx} - V_{SHx}) in case of bootstrap voltages V_{BHx}-V_{SHx} <4V
[3] The min value -7V is reduced to –(V_{BHx} - V_{SHx} - 1V) in case of bootstrap voltages V_{BHx}-V_{SHx} <8V
[4] All test involving Gxx pins V_{ESD}=1 kV!

Max. voltage range at GLx	V_{GHx}	-2	12	V
Max. voltage range at SLx	V_{SLx}	-2	6	V
Max. voltage difference BHx – SHx	V_{BHx}-V_{SHx}	-0.3	12	V
Max. voltage difference Gxx – Sxx	V_{Gxx}-V_{Sxx}	-0.3	11	V
PWM frequency	F_{PWM}	0	50	kHz
Minimum on time external lowside switch – static condition @ 20 kHz; Q_{Gate} = 200nC	$t_{p(min)}$	--	2	µs

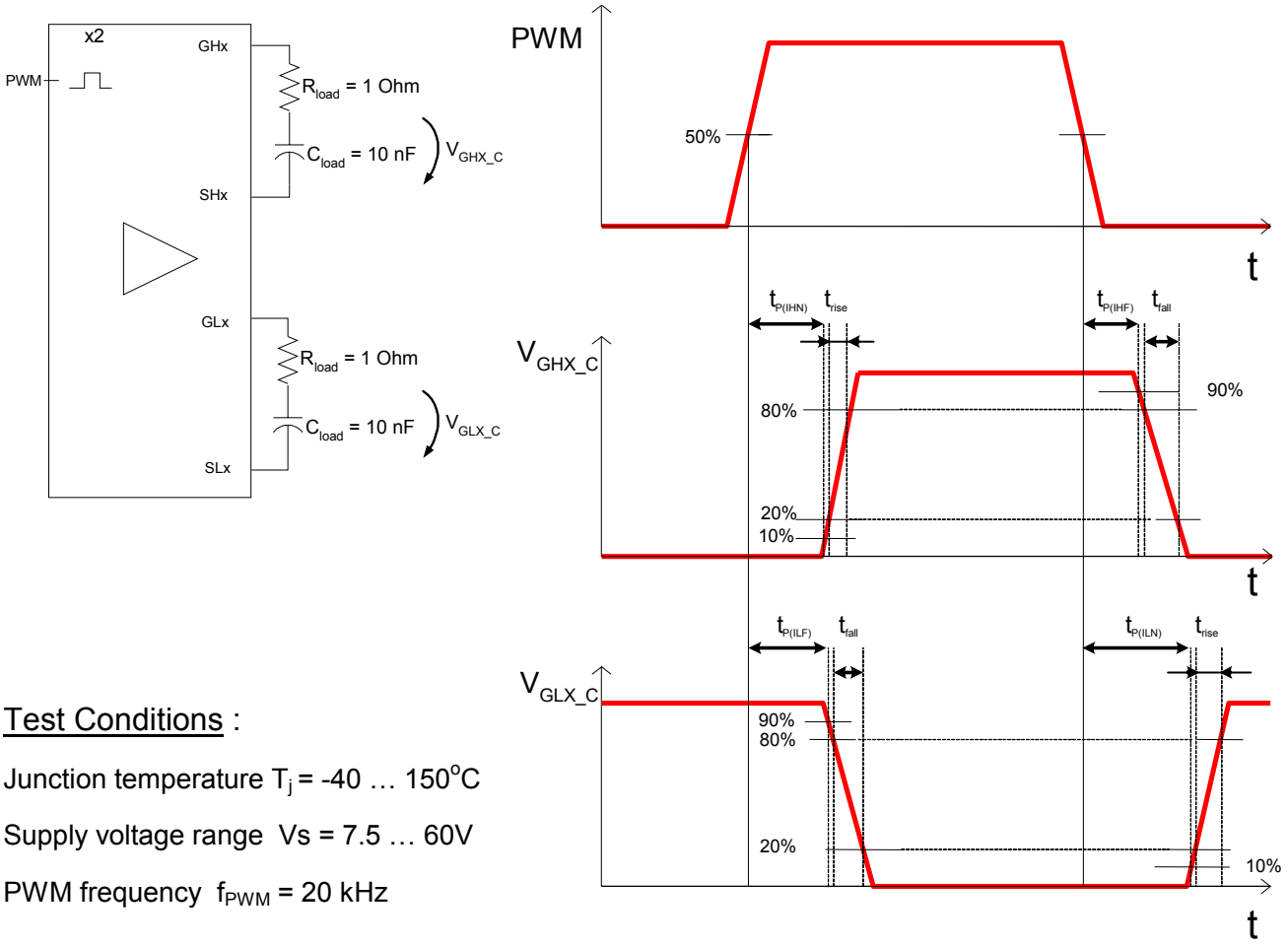
Electrical Characteristics

Parameter and Conditions at T_j = -40…150°C, unless otherwise specified and supply voltage range V_S = 7.5 … 60V; f_{PWM} = 20kHz	**Symbol**	**Values**			**Unit**
		min	typ	max	
Static Characteristics					
Low level output voltage (V_{GSxx}) @ I=10mA	ΔV_{LL}	--	60	150	mV
High level output voltage (V_{GSxx}) @ I=-10mA; Vs≥11.5V	ΔV_{HL}	8	10	11	V
High level output voltage (V_{GSxx}) @ I=-10mA; Vs<11.5V	ΔV_{HL}	--	Vs-1.5	--	V
Supply current at VS (device disabled) @ V_{bat}= V_S =14V R_{DT}=400kΩ	$I_{VS(dis)14V}$	--	4	8	mA
Supply current at VS (device disabled) @ V_{bat}= V_S =42V R_{DT}=400kΩ	$I_{VS(dis)42V}$	--	4	8	mA
Quiescent current at VS (device inhibited) @ V_{bat}= V_S =14V R_{DT}=400kΩ R_{Bx}=12kΩ	$I_{VS(inh)14V}$	--	0.6	1.5	mA
Quiescent current at VS (device inhibited) @ V_{bat}= V_S =42V R_{DT}=400kΩ R_{Bx}=12kΩ	$I_{VS(inh)42V}$	--	0.6	1.5	mA
Supply current at VS @ V_{bat}= V_S =14V, f_{PWM} = 20kHz (Outputs open)	$I_{VS(open)14V}$	--	7	15	mA
Supply current at VS @ V_{bat}= V_S =14V, f_{PWM} = 50kHz (Outputs open)	$I_{VS(open)14V}$	--	7	15	mA
Supply current at VS @ V_{bat}= V_S =42V, f_{PWM} = 20kHz (Outputs open)	$I_{VS(open)42V}$	--	7	15	mA
Low level input voltage	$V_{IN(LL)}$	--	--	1.0	V
High level input voltage	$V_{IN(HL)}$	2.0	--	--	V
Input hysteresis	ΔV_{IN}	100	170		mV
Inhibit trip level	V_{INH}	1.3	2	3	V

Dynamic characteristics (pls. see test circuit and timing diagram)

Turn on current @ $V_{Gxx} - V_{Sxx}$ = 0V; T_j=25°C @ $V_{Gxx} - V_{Sxx}$ = 4V; T_j=125°C @ C_{Load}=22nF ; R_{load}= 0Ω	$I_{Gxx(on)}$	-- --	850 700	-- --	mA
Turn off current @ $V_{Gxx} - V_{Sxx}$ = 10V; T_j=25°C @ $V_{Gxx} - V_{Sxx}$ = 4V; T_j=125°C @ C_{Load}= 22nF ; R_{load}=0Ω	$I_{Gxx(off)}$	-- --	580 300	-- --	mA
Dead time (adjustable) @ R_{DT} = 1 kΩ @ R_{DT} = 10 kΩ @ R_{DT} = 50 kΩ @ R_{DT} = 200 kΩ @ C_{Load}=10nF ; R_{load}=1Ω	t_{DT}	-- 0.05 0.40 --	0.01 0.20 1.0 3.1	-- 0.38 2.50 --	µs
Rise time @ C_{Load}=10nF; R_{load}=1Ω (20% to 80%)	t_{rise}	--	100	300	ns
Fall time @ C_{Load}=10nF; R_{load}=1Ω (80% to 20%)	t_{fall}	--	150	440	ns
Disable propagation time @ C_{Load}=10nF ; R_{load}=1Ω	$t_{P(DIS)}$	3.4	5	7	µs
Reset time of diagnosis @ C_{Load}=10nF ; R_{load}=1Ω	$t_{P(CL)}$	1	2	3.1	µs
Input propagation time (low side turns on, 0% to 10%)	$t_{P(ILN)}$	--	250	500	ns
Input propagation time (low side turns off, 100% to 90%)	$t_{P(ILF)}$	--	110	500	ns
Input propagation time (high side turns on, 0% to 10%)	$t_{P(IHN)}$	--	200	500	ns
Input propagation time (high side turns off, 100% to 90%)	$t_{P(IHF)}$	--	130	500	ns
Input propagation time difference (all channels turn on)	$t_{P(Diff)}$	20	50	70	ns
Input propagation time difference (all channels turn off)	$t_{P(Diff)}$	--	25	50	ns
Input propagation time difference (one channel; low on – high off)	$t_{P(Diff)}$	--	120	180	ns
Input propagation time difference (one channel; high on – low off)	$t_{P(Diff)}$	--	100	180	ns
Input propagation time difference (all channels; low on – high off)	$t_{P(Diff)}$	--	120	180	ns
Input propagation time difference (all channels; high on – low off)	$t_{P(Diff)}$	--	100	180	ns

Test Circuit and Timing Diagram



Test Conditions :

Junction temperature T_j = -40 … 150°C

Supply voltage range Vs = 7.5 … 60V

PWM frequency f_{PWM} = 20 kHz

Diagnosis and Protection Functions

Parameter and Conditions at T_j = -40…150°C, unless otherwise specified and supply voltage range V_S = 7.5 … 60V; f_{PWM} = 20kHz	Symbol	Values			Unit
		min	typ	max	
Overtemperature warning	$T_{J(OV)}$	150	170	190	°C
Hysteresis for overtemperature warning	$\Delta T_{J(OV)}$	--	20	--	°C
Short circuit protection filter time	$t_{SCP(off)}$	6	9	12	µs
Short circuit criteria (V_{DS} of Mosfets) For Low sides For High sides	$V_{DS(SCP)}$	 0.5 0.45	 0.75 0.75	 1.0 1.05	 V
Disable input level	V_{DIS}	3.3	3.7	4.0	V
Disable input hysteresis	ΔV_{DIS}	--	180	--	mV
Error level @ 1.6mA I_{ERR}	V_{ERR}	--	--	1.0	V
Under voltage lock out for highside output – bootstrap voltage	$V_{BHx\,(uvlo)}$	--	3.7	4.6	V
Under voltage lock out for lowside output – supply voltage	$V_{Vs\,(uvlo)}$	--	4.8	5.9	V

Remarks:

Default status of input pins:

To assure a defined status of the logic input pins in case of disconnection, these pins are internally secured by pull up / pull down current sources with approx. 20µA. The high voltage proof input INH should be secured by an external pull down resistor close to the device. The following table shows the default status of the logic input pins.

Input pin	Default status
PWM and DIR	Low (= break in high side)
DT/DIS (active high)	High

Definition:
In this datasheet a duty cycle of 98% means that the GLx pin is 2% of the PWM period in high condition.
Remark: Please consider the influence of the dead time and the propagation time differences for the input duty cycle

Functional description

Description of Dead Time Pin / Disable Pin / Reset

This pin allows to adjust the internal generated dead time. The dead time protects the external high side and lowside Mosfets in the same halfbridge against a lowohmic connection between battery and GND and the resulting cross current through these Mosfets. The adjustable dead time allows to minimize the power dissipation caused by the current flowing through the body diode during switching the halfbridge.
In addition this pin allows to reset the diagnosis registers without shut down of any output stage as well as the possibility to shut down all outputs simultaneously.

Condition of DT/DIS pin	Function
0 - 3.5V	Adjust dead time between 10ns and 3.1µs
> 4V	a) Reset of diagnosis register if DT/DIS voltage is higher than 4V for a time between 3.1µs and 3.6µs
	b) Shut down of output stages if DT/DIS voltage is higher than 4V for a time above 7µs (Active pull down of gate voltage)

Description of Inhibit functionality

In automotive applications which are permanently connected to the battery line, it is very important to reduce the current consumption of the single devices. Therefore the TLE6281G offers an inhibit mode to put the device to sleep and assure low quiescent currents. To deactivate the inhibit mode the INH pin has to be set to high. This can be done by connecting this pin to voltages between 3.3 and 60V without external protection. An inhibit mode means a complete reinitialisation of the device.

Description of Diagnosis

The two ERx pins are open collector outputs and have to be pulled up with external pull up resistors to 5V. In normal conditions both ERx signals are high. In case of shutdown of any

output stage the ER1 is pulled down. This shut down can be caused by undervoltage or short circuit. In this condition ER2 indicates the reason for the shut down.

Condition of ER1 pin	Condition of ER2 pin	Function
5V	5V	no errors
5V	0V	overtemperature warning of driver IC
0V	5V	Shut down of any output stage caused by short circuit
0V	0V	Shut down of any output stage caused by undervoltage

Recommended Start-up procedure

The following procedure is recommended whenever the Driver IC is powered up:

- Disable the Driver IC via DT/DIS pin
- Wait until the bootstrap capacitors C_{Bx} are charged (the waiting time depends on application conditions, e.g. C_{Bx} and R_{Bx})
- Enable the Driver IC via DT/DIS pin
- Start the operation by applying the desired pulse patterns. Do not apply any pulse patterns to the PWM or DIR pin, before the C_{Bx} capacitors are charged up.

Shut down of the driver

A shut down can be caused by undervoltage or short circuit. A short circuit will shut down only the affected Mosfet until a reset of the error register by a disable of the driver occurs. A shut down due to short circuit will occur only when the Short Circuit criteria $V_{DS(SCP)}$ is met for a duration equal to or longer than the Short Circuit filter time $t_{SCP(off)}$. Yet, the exposure to or above $V_{DS(SCP)}$ is not counted or accumulated. Hence, repetitive Short Circuit conditions shorter than $t_{scp(off)}$ will not result in a shut down of the affected MOSFET.
An undervoltage shut down shuts only the affected output down. The affected output will auto restart after the undervoltage situation is over.

Operation at Vs<12V

If Vs<11.5V the gate voltage will not reach 10V. It will reach approx Vs-1.5V, dependent on duty cyle, bootstrap capacitor, total gate charge of the external Mosfet and switching frequency.

Operation at different voltages for Vs, DH1 and DH2

If DH1 and DH2 are used with a voltage higher than Vs, a duty cycle of 100% can not be guaranteed. In this case the driver is acting like a normal driver IC based on the bootstrap principle. This means that after a maximum “On” time of the highside switch of more than 1ms a refresh pulse to charge the bootstrap capacitor of about 1µs is needed to avoid undervoltage lock out of this output stage.

Operation at extreme duty cycle:

The integrated charge pump allows an operation at 100% duty cycle. The charge pump is strong enough to replace leakage currents during “on”-phase of the highside switch. The gate charge for fast switching of the highside switches is supplied by the bootstrap capaci-

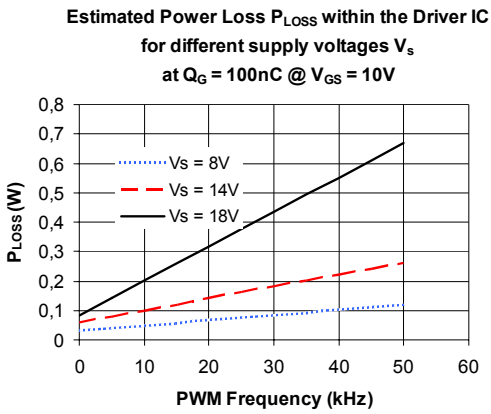
tors. This means, that the bootstrap capacitor needs a minimum charging time of about 1µs, if the highside switch is operated in PWM mode (e.g. with 20kHz a maximum duty cycle of 96% can be reached). The exact value for the upper limit is given by the RC time formed by the impedance of the internal bootstrap diode and the capacitor formed by the external Mosfet ($C_{Mosfet}=Q_{Gate} / V_{GS}$). The size of the bootstrap capacitor has to be adapted to the external MOSFET the driver IC has to drive. Usually the bootstrap capacitor is about 10-20 times bigger than C_{Mosfet}. External components at the Vs Pin have to be considered, too.
The charge pump is active when the highside switch is “ON” and the voltage level at the SHx is higher than 4V. Only under these conditions the bootstrap capacitor is charged by the charge pump.

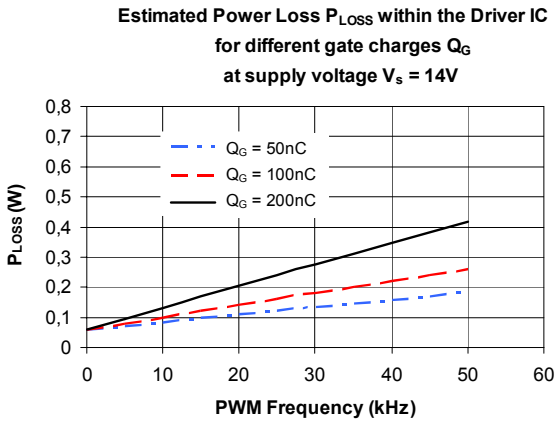
Estimation of power loss within the Driver IC

The power loss within the Driver IC is strongly dependent on the use of the driver and the external components. Nevertheless a rough estimation of the worst case power loss is possible.
Worst case calculation is:

$P_{Loss} = (Q_{gate}*n*const* f_{PWM} + I_{VS(open)})* V_{Vs} - P_{RGate}$
With:
P_{Loss} = Power loss within the Driver IC
f_{PWM} = Switching freqency
Q_{gate} = Total gate charge of used MOSFETs at 10V V_{GS}
n = Number of switched MOSFETs
const = Constant considering some leakage current in the driver (about 1.2)
$I_{VS(open)}$ = Current consumption of driver without connected Mosfets during switching
V_{VS} = Voltage at Vs
P_{RGate} = Power dissipation in the external gate resistors

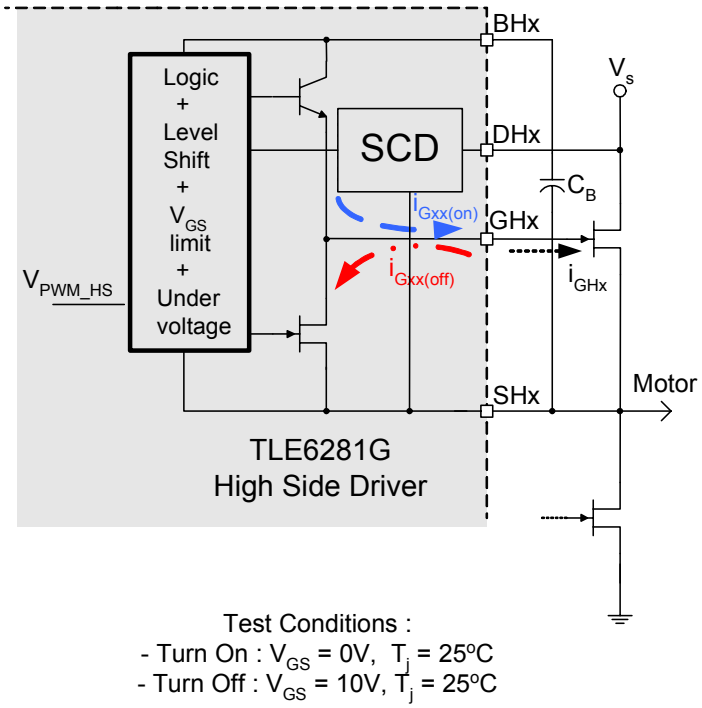
This value can be reduced dramatically by usage of external gate resistors.





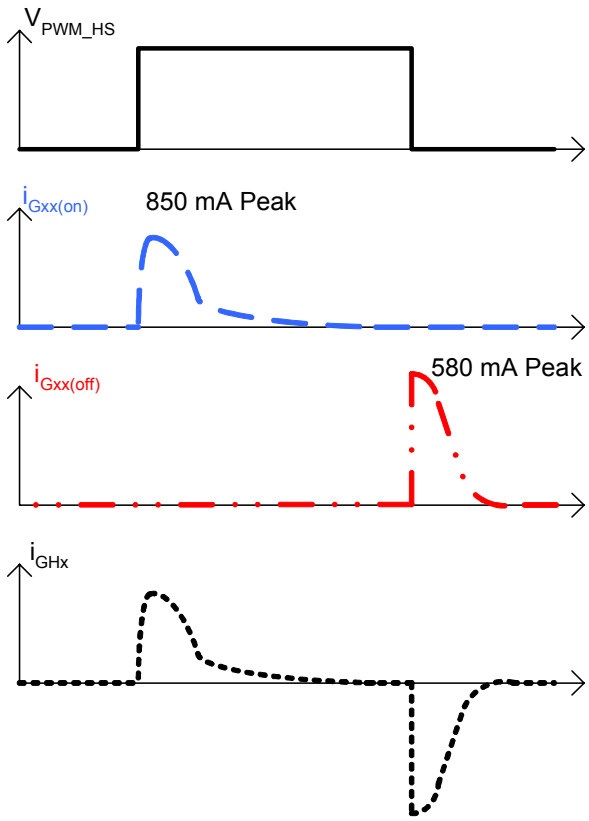
Conditions :
Junction temperature $T_j = 25^oC$
Number of switched MOSFET n = 2
Power dissipation in the external gate resistors $P_{RGate} = 0,2*P_{Loss}$

Gate Drive characteristics



Test Conditions :
- Turn On : V_{GS} = 0V, T_j = 25ºC
- Turn Off : V_{GS} = 10V, T_j = 25ºC

This figure represents the simplified internal circuit of one high side gate drive. The drive circuit for the low sides looks similar.



This figure illustrates typical voltage and current waveforms of the high side gate drive; the associated waveforms of the low side drives look similar.

Truth Table

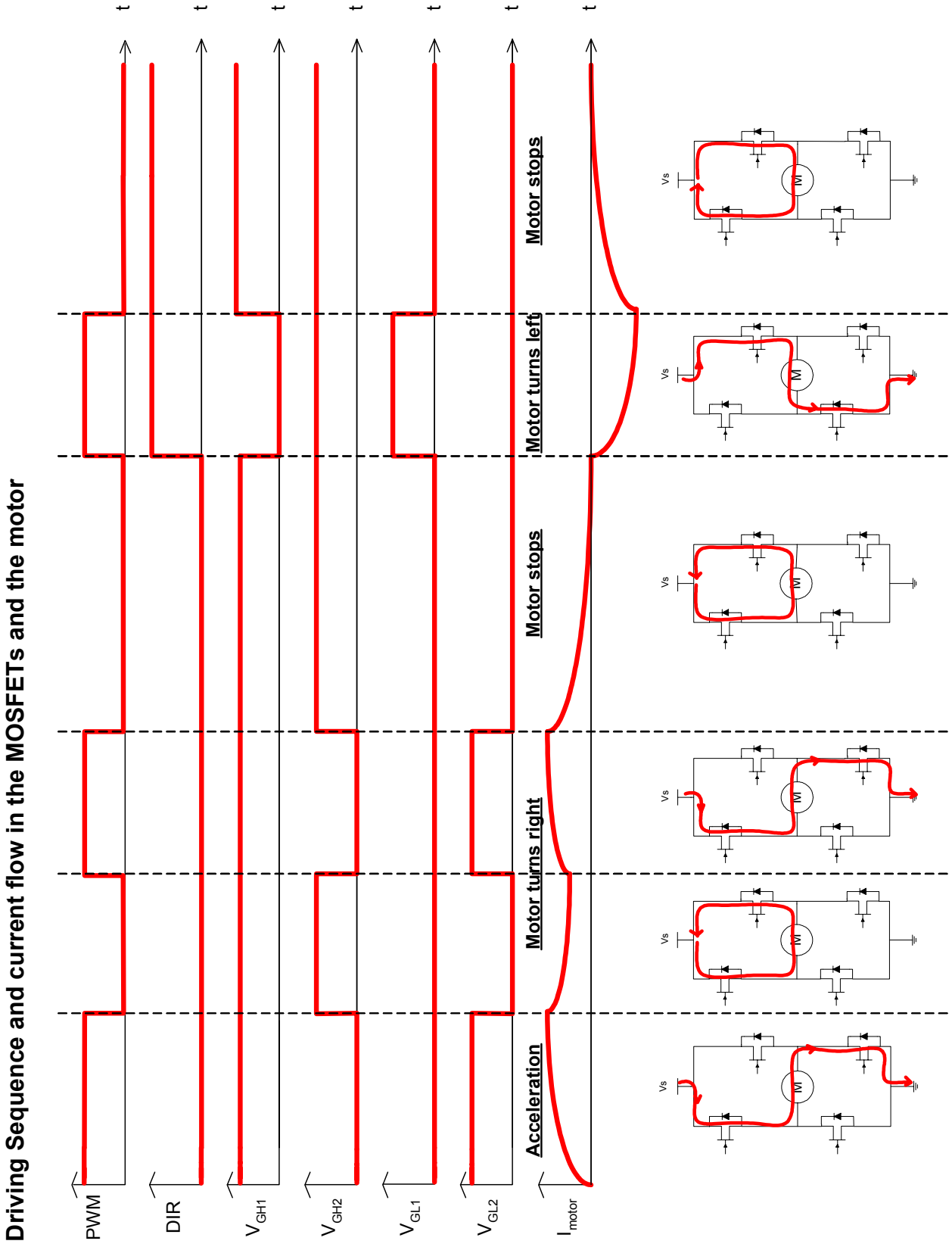
Input			Conditions			Output driver IC						Output Bridge	
DIR	PWM	DT / DIS	UV	OT	SC	GH 1	GL 1	GH 2	GL 2	ER 1	ER 2	Out1	Out2
0	1	<3.5V	0	0	0	1	0	0	1	5V	5V	1	0
0	0	<3.5V	0	0	0	1	0	1	0	5V	5V	1	1
1	1	<3.5V	0	0	0	0	1	1	0	5V	5V	0	1
1	0	<3.5V	0	0	0	1	0	1	0	5V	5V	1	1
0	1	<3.5V	1	0	0	B	0	0	B	C	D	1 [A]	0 [A]
0	0	<3.5V	1	0	0	B	0	B	0	C	D	1 [A]	1 [A]
1	1	<3.5V	1	0	0	0	B	B	0	C	D	0 [A]	1 [A]
1	0	<3.5V	1	0	0	B	0	B	0	C	D	1 [A]	1 [A]
0	1	<3.5V	0	1	0	1	0	0	1	5V	0V	1	0
0	0	<3.5V	0	1	0	1	0	1	0	5V	0V	1	1
1	1	<3.5V	0	1	0	0	1	1	0	5V	0V	0	1
1	0	<3.5V	0	1	0	1	0	1	0	5V	0V	1	1
0	1	<3.5V	0	0	1	E	0	0	E	F	5V	1 [A]	0 [A]
0	0	<3.5V	0	0	1	E	0	E	0	F	5V	1 [A]	1 [A]
1	1	<3.5V	0	0	1	0	E	E	0	F	5V	0 [A]	1 [A]
1	0	<3.5V	0	0	1	E	0	E	0	F	5V	1 [A]	1 [A]
X	X	X	X	X	X	0	0	0	0	5V	5V	T	T
X	X	>4V	X	X	X	0	0	0	0	5V	5V	T	T

A) Tristate when affected by undervoltage shut down or short circuit
B) 0 when affected; 1 when not affected; self recovery
C) 0V when output does not correspond to input patterns; 5V when output corresponds to input patterns
D) Is an output affected by undervoltage ER2 is 0V
E) 0 when affected– the outputs of the affected halfbridge are shut down and stay latched until reset; 1 when not affected
F) 0V when output does not correspond to input patterns – the outputs of the affected half-bridge are shut down and stay latched until reset; 5V when output corresponds to input patterns.

T) Tristate
X) Condition has no influence

Remark: To generate fast decay control mode, set PWM to 1 and send pwm-pattern to DIR input.

Driving Sequence and current flow in the MOSFETs and the motor

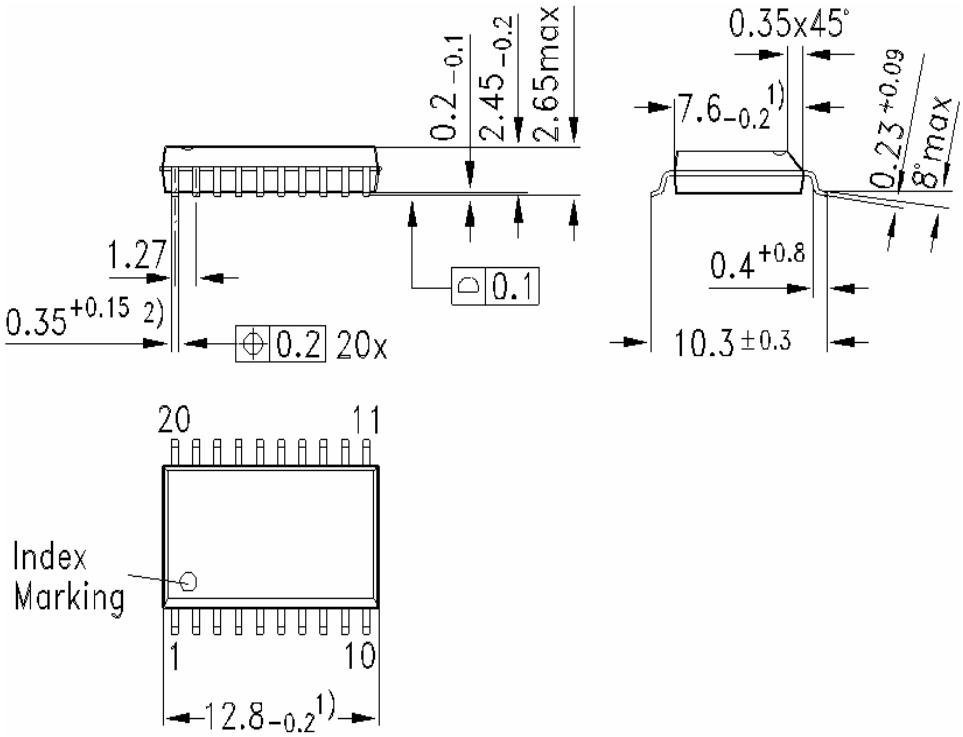


Package and Ordering Code

(all dimensions in mm)[5]

Package

P-DSO 20



[5] More information about packages can be found at our internet page **http://www.infineon.com/packages**

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