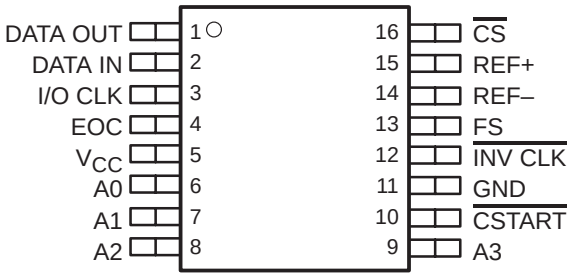
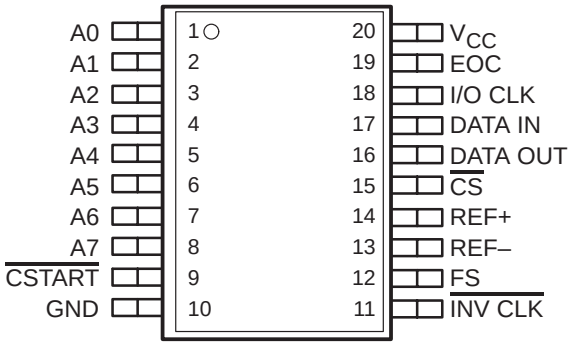
- **Conversion Time ≤ 10 μs**
- **10-Bit-Resolution ADC**
- **Programmable Power-Down Mode . . . 1 μA**
- **Wide Range Single-Supply Operation of 2.7 V dc to 5.5 V dc**
- **Analog Input Range of 0 V to $V_{CC}$**
- **Built-in Analog Multiplexer with 8 Analog Input Channels**
- **TMS320 DSP and Microprocessor SPI and QSPI Compatible Serial Interfaces**
- **End-of-Conversion (EOC) Flag**
- **Inherent Sample-and-Hold Function**
- **Built-In Self-Test Modes**
- **Programmable Power and Conversion Rate**
- **Asynchronous Start of Conversion for Extended Sampling**
- **Hardware I/O Clock Phase Adjust Input**

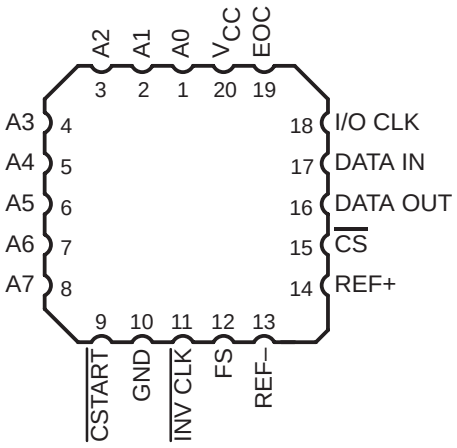
**D OR PW PACKAGE**
**(TOP VIEW)**




**DB OR J PACKAGE**
**(TOP VIEW)**




**FK PACKAGE**
**(TOP VIEW)**




## description

The TLV1544 and TLV1548 are CMOS 10-bit switched-capacitor successive-approximation (SAR) analog-to-digital (A/D) converters. Each device has a chip select ($\overline{CS}$), input-output clock (I/O CLK), data input (DATA IN) and serial data output (DATA OUT) that provide a direct 4-wire synchronous serial peripheral interface (SPI™, QSPI™) port of a host microprocessor. When interfacing with a TMS320 DSP, an additional frame sync signal (FS) indicates the start of a serial data frame. The devices allow high-speed data transfers from the host. The $\overline{INV\ CLK}$ input provides further timing flexibility for the serial interface.

In addition to a high-speed converter and versatile control capability, the device has an on-chip 11-channel multiplexer that can select any one of eight analog inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic except for the extended sampling cycle, where the sampling cycle is started by the falling edge of asynchronous $\overline{CSTART}$. At the end of the A/D conversion, the end-of-conversion (EOC) output goes high to indicate that the conversion is complete. The TLV1544 and TLV1548 are designed to operate with a wide range of supply voltages with very low power consumption. The power saving feature is further enhanced with a software-programmed power-down mode and conversion rate. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

SPI and QSPI are registered trademarks of Motorola, Inc.

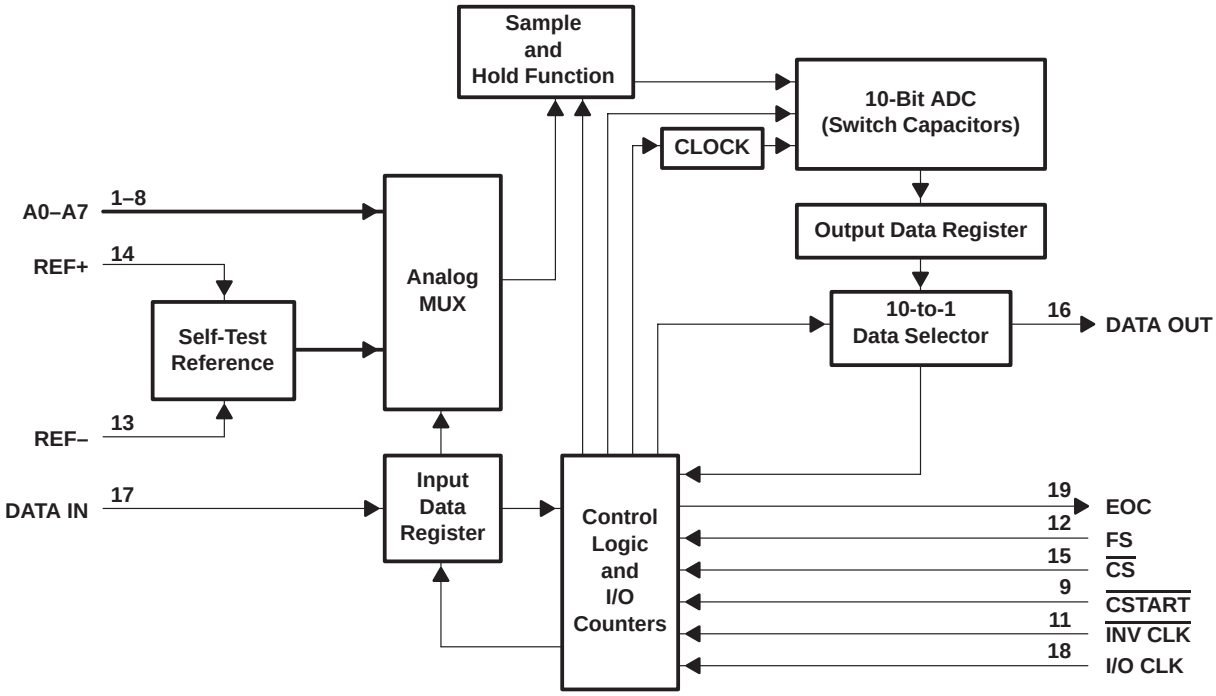
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description (continued)

The TLV1544 has four analog input channels while the TLV1548 has eight analog input channels. The TLV1544C and TLV1548C are characterized for operation from 0°C to 70°C. The TLV1544I and TLV1548I are characterized for operation over the full industrial temperature range of –40°C to 85°C. The TLV1548M is characterized for operation over the full military temperature range of –55°C to 125°C.

## functional block diagram




Terminals shown are for the DB package.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE | | | | |
|---|---|---|---|---|---|
| | SMALL OUTLINE | | | | |
| | (DB) | (D) | (PW) | (J) | (FK) |
| 0°C to 70°C | TLV1548CDB | TLV1544CD | TLV1544CPW | | |
| –40°C to 85°C | TLV1548IDB | TLV1544ID | TLV1544IPW | | |
| –55°C to 125°C | | | | TLV1548MJ | TLV1548MFK |

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR† ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| DB | 785 mW | 8.7 mW/°C | 393 mW | 261 mW | — |
| D | 799 mW | 8.9 mW/°C | 399 mW | 266 mW | — |
| PW | 604 mW | 6.7 mW/°C | 302 mW | 201 mW | — |
| J | 1894 mW | 15.1 mW/°C | 1212 mW | 985 mW | 379 mW |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |

† This is the inverse of the traditional junction-to-ambient thermal resistance ($R\Theta_{JA}$). $R\Theta_{JA}$ values are derived from Texas Instruments characterization data. Thermal resistance is not production tested and values are given for informational purposes only.

## Terminal Functions

| TERMINAL NAME | TERMINAL NO.† | TERMINAL NO.‡ | I/O | DESCRIPTION |
|---|---|---|---|---|
| A0–A3<br>A4–A7 | 6–9<br>– | 1–4<br>5–8 | I | Analog inputs. The analog inputs are internally multiplexed. (For a source impedance greater than 1 kΩ, the asynchronous start should be used to increase the sampling time.) |
| $\overline{CS}$ | 16 | 15 | I | Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA IN, DATA OUT, and I/O CLK within the maximum setup time. A low-to-high transition disables DATA IN, DATA OUT, and I/O CLK within the setup time. |
| $\overline{CSTART}$ | 10 | 9 | I | Sampling/conversion start control. $\overline{CSTART}$ controls the start of the sampling of an analog input from a selected multiplex channel. A high-to-low transition starts the sampling of the analog input signal. A low-to-high transition puts the sample-and-hold function in hold mode and starts the conversion. $\overline{CSTART}$ is independent from I/O CLK and works when $\overline{CS}$ is high. The low $\overline{CSTART}$ duration controls the duration of the sampling cycle for the switched capacitor array. $\overline{CSTART}$ is tied to $V_{CC}$ if not used. |
| DATA IN | 2 | 17 | I | Serial data input. The 4-bit serial data selects the desired analog input and test voltage to be converted next in a normal cycle. These bits can also set the conversion rate and enable the power-down mode.<br>When operating in the microprocessor mode, the input data is presented MSB first and is shifted in on the first four rising ($\overline{INV\ CLK}$ = $V_{CC}$) or falling ($\overline{INV\ CLK}$ = GND) edges of I/O CLK (after $\overline{CS}\downarrow$).<br>When operating in the DSP mode, the input data is presented MSB first and is shifted in on the first four falling ($\overline{INV\ CLK}$ = $V_{CC}$) or rising ($\overline{INV\ CLK}$ = GND) edges of I/O CLK (after FS↓).<br>After the four input data bits have been read into the input data register, DATA IN is ignored for the remainder of the current conversion period. |
| DATA OUT | 1 | 16 | O | Three-state serial output of the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low or after FS↓ (in DSP mode). With a valid $\overline{CS}$ signal, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB or LSB value of the previous conversion result. DATA OUT changes on the falling (microprocessor mode) or rising (DSP mode) edge of I/O CLK. |
| EOC | 4 | 19 | O | End of conversion. EOC goes from a high to a low logic level on the tenth rising (microprocessor mode) or tenth falling (DSP mode) edge of I/O CLK and remains low until the conversion is complete and data is ready for transfer. EOC can also indicate that the converter is busy. |
| FS | 13 | 12 | I | DSP frame synchronization input. FS indicates the start of a serial data frame into or out of the device. FS is tied to $V_{CC}$ when interfacing the device with a microprocessor. |
| GND | 11 | 10 | | Ground return for internal circuitry. All voltage measurements are with respect to GND, unless otherwise noted. |
| $\overline{INV\ CLK}$ | 12 | 11 | I | Inverted clock input. $\overline{INV\ CLK}$ is tied to GND when an inverted I/O CLK is used as the source of the input clock. This affects both microprocessor and DSP interfaces. $\overline{INV\ CLK}$ is tied to $V_{CC}$ if I/O CLK is not inverted. $\overline{INV\ CLK}$ can also invoke a built-in test mode. |

† Terminal numbers are for the D package.
‡ Terminal numbers are for the DB, J, and FK packages.

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL NO.† | TERMINAL NO.‡ | I/O | DESCRIPTION |
|---|---|---|---|---|
| I/O CLK | 3 | 18 | I | Input/output clock. I/O CLK receives the serial I/O clock input in the two modes and performs the following four functions in each mode:<br>**Microprocessor mode**<br>● When $\overline{\text{INVCLK}}$ = $V_{CC}$, I/O CLK clocks the four input data bits into the input data register on the first four rising edges of I/O CLK after $\overline{\text{CS}}\downarrow$ with the multiplexer address available after the fourth rising edge. When $\overline{\text{INV CLK}}$ = GND, input data bits are clocked in on the first four falling edges instead.<br>● On the fourth falling edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth rising edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{\text{CSTART}}$ determines when to end the sampling cycle.<br>● Output data bits change on the first ten falling I/O clock edges regardless of the condition of $\overline{\text{INV CLK}}$.<br>● I/O CLK transfers control of the conversion to the internal state machine on the tenth rising edge of I/O CLK regardless of the condition of $\overline{\text{INV CLK}}$.<br>**Digital signal processor (DSP) mode**<br>● When $\overline{\text{INV CLK}}$ = $V_{CC}$, I/O CLK clocks the four input data bits into the input data register on the first four falling edges of I/O CLK after FS↓ with the multiplexer address available after the fourth falling edges. When $\overline{\text{INV CLK}}$ = GND, input data bits are clocked in on the first four rising edges instead.<br>● On the fourth rising edge of I/O CLK, the analog input voltage on the selected multiplex input begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLK except in the extended sampling cycle where the duration of $\overline{\text{CSTART}}$ determines when to end the sampling cycle.<br>● Output data MSB shows after FS↓ and the rest of the output data bits change on the first ten rising I/O CLK edges regarless of the condition of $\overline{\text{INV CLK}}$.<br>● I/O CLK transfers control of the conversion to the internal state machine on the tenth falling edge of I/O CLK regardless of the condition of $\overline{\text{INV CLK}}$. |
| REF+ | 15 | 14 | I | Upper reference voltage (nominally $V_{CC}$ ). The maximum input voltage range is determined by the difference between the voltages applied to REF+ and REF–. |
| REF– | 14 | 13 | I | Lower reference voltage (nominally ground) |
| $V_{CC}$ | 5 | 20 | I | Positive supply voltage |

† Terminal numbers are for the D package.
‡ Terminal numbers are for the DB, J, and FK packages.

### detailed description

Initially, with $\overline{\text{CS}}$ high (inactive), DATA IN and I/O CLK are disabled and DATA OUT is in the high-impedance state. When the serial interface takes $\overline{\text{CS}}$ low (active), the conversion sequence begins with the enabling of I/O CLK and DATA IN and the removal of DATA OUT from the high-impedance state. The host then provides the 4-bit channel address to DATA IN and the I/O clock sequence to I/O CLK. During this transfer, the host serial interface also receives the previous conversion result from DATA OUT. I/O CLK receives an input sequence from the host that is from 10 to 16 clocks long. The first four valid I/O CLK cycles load the input data register with the 4-bit input data on DATA IN that selects the desired analog channel. The next six clock cycles provide the control timing for sampling the analog input. Sampling of the analog input is held after the first valid I/O CLK sequence of ten clocks. The tenth clock edge also takes EOC low and begins the conversion. The exact locations of the I/O clock edges depend on the mode of operation.

### serial interface

The TLV1548 is compatible with generic microprocessor serial interfaces such as SPI and QSPI, and a TMS320 DSP serial interface. The internal latched flag If_mode is generated by sampling the state of FS at the falling edge of $\overline{\text{CS}}$. If_mode is set to one (for microprocessor) when FS is high at the falling edge of $\overline{\text{CS}}$, and If_mode is cleared to zero (for DSP) when FS is low at the falling edge of $\overline{\text{CS}}$. This flag controls the multiplexing of I/O CLK and the state machine reset function. FS is pulled high when interfacing with a microprocessor.

### I/O CLK

The I/O CLK can go up to 10 MHz for most of the voltage range when fast I/O is possible. The maximum I/O CLK is limited to 2.8 MHz for a supply voltage range from 2.7 V. Table 1 lists the maximum I/O CLK frequencies for all different supply voltage ranges. This also depends on input source impedance. For example, I/O CLK speed faster than 2.39 MHz is achievable if the input source impedance is less than 1 kΩ.

**Table 1. Maximum I/O CLK Frequency**

| $V_{CC}$ | MAXIMUM INPUT RESISTANCE (Max) | SOURCE IMPEDANCE | I/O CLK |
|---|---|---|---|
| 2.7 V | 5 K | 1 kΩ | 2.39 MHz |
| | | 100 Ω | 2.81 MHz |
| 4.5 V | 1 K | 1 kΩ | 7.18 MHz |
| | | 100 Ω | 10 MHz |

### microprocessor serial interface

Input data bits from DATA IN are clocked in on the first four rising edges of the I/O CLK sequence if $\overline{\text{INV CLK}}$ is held high when the device is in microprocessor interface mode. Input data bits are clocked in on the first four falling edges of the I/O CLK sequence if $\overline{\text{INV CLK}}$ is held low. The MSB of the previous conversion appears on DATA OUT on the falling edge of $\overline{\text{CS}}$. The remaining nine bits are shifted out on the next nine edges (depending on the state of $\overline{\text{INV CLK}}$) of I/O CLK. Ten bits of data are transmitted to the host through DATA OUT.

A minimum of 9.5 clock pulses is required for the conversion to begin. On the tenth clock rising edge, the EOC output goes low and returns to the high logic level when the conversion is complete; then the result can be read by the host. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLK transfer is more than ten clocks long.

$\overline{\text{CS}}$ is inactive (high) between serial I/O CLK transfers. Each transfer takes at least ten I/O CLK cycles. The falling edge of $\overline{\text{CS}}$ begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of $\overline{\text{CS}}$ ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of $\overline{\text{CS}}$ disables I/O CLK and DATA IN within a setup time. A conversion does not begin until the tenth I/O CLK rising edge.

A high-to-low transition on $\overline{\text{CS}}$ within the specified time during an ongoing cycle aborts the cycle, and the device returns to the initial state (the output data register holds the previous conversion result). $\overline{\text{CS}}$ should not be taken low close to completion of conversion because the output data can be corrupted.

### DSP interface

The TLV1544/1548 can also interface with a DSP, from the TMS320 family for example, through a serial port. The analog-to-digital converter (ADC) serves as a slave device where the DSP supplies FS and the serial I/O CLK. Transmit and receive operations are concurrent. The falling edge of FS must occur no later than seven I/O CLK periods after the falling edge of $\overline{CS}$.

DSP I/O cycles differ from microprocessor I/O cycles in the following ways:

- When interfaced with a DSP, the output data MSB is available after FS↓. The remaining output data changes on the rising edge of I/O CLK. The input data is sampled on the first four falling edges of I/O CLK after FS↓ and when $\overline{\text{INV CLK}}$ is high, or the first four rising edges of I/O CLK after FS↓ and when $\overline{\text{INV CLK}}$ is low. This operation is inverted when interfaced with a microprocessor.
- A new DSP I/O cycle is started on the rising edge of I/O CLK after the rising edge of FS. The internal state machine is reset on each falling edge of I/O CLK when FS is high. This operation is opposite when interfaced with a microprocessor.
- The TLV1544/1548 supports a 16-clock cycle when interfaced with a DSP. The output data is padded with six trailing zeros when it is operated in DSP mode.

**Table 2. TLV1544/TLV1548 Serial Interface Modes**

| I/O | INTERFACE MODE | |
|---|---|---|
| | MICROPROCESSOR ACTION | DSP ACTION |
| $\overline{CS}$↓ | Initializes counter | Samples state of FS |
| $\overline{CS}$↑ | Resets state machine and disable I/O | Disables I/O |
| FS | Connects to $V_{CC}$ | Connects to DSP FSX output<br>Initializes the state machine at each CLK↓ after FS↑<br>Starts a new cycle at each CLK↑ following the initialization (initializes the counter) |
| I/O CLK | Starts sampling of the analog input started at fourth I/O CLK↑<br>Conversion started at tenth I/O CLK↑ | Starts sampling of the analog input at fourth I/O CLK↓<br>Starts sampling of the analog input at tenth I/O CLK↓ |
| DATA IN | Samples input data on I/O CLK↑ ($\overline{\text{INV CLK}}$ high)<br>Samples input data on I/O CLK↓ (INV CLK low) | Samples input data at I/O CLK↓ ($\overline{\text{INV CLK}}$ high)<br>Samples input data at I/O CLK↑ (INV CLK low) |
| DATA OUT | Makes MSB available on $\overline{CS}$↓<br>Changes remaining data on I/O CLK↓ | Makes MSB available FS↓<br>Changes remaining data at each following I/O CLK↑ after FS↓ |

### input data bits

DATA IN is internally connected to a 4-bit serial input data register. The input data selects a different mode or selects different analog input channels. The host provides the data word with the MSB first. Each data bit clocks in on the edge (rising or falling depending on the status of $\overline{\text{INV CLK}}$ and FS) of the I/O CLK sequence. The input clock can be inverted by grounding $\overline{\text{INV CLK}}$ (see Table 3 for the list of software programmed operations set by the input data).

**Table 3. TLV1544/1548 Software-Programmed Operation Modes**

| FUNCTION SELECT | INPUT DATA BYTE A3 – A0 | | COMMENT |
|---|---|---|---|
| | BINARY | HEX | |
| Analog channel A0 for TLV1548 selected | 0000b | 0h | Channel 0 for TLV1544 |
| Analog channel A1 for TLV1548 selected | 0001b | 1h | |
| Analog channel A2 for TLV1548 selected | 0010b | 2h | Channel 1 for TLV1544 |
| Analog channel A3 for TLV1548 selected | 0011b | 3h | |
| Analog channel A4 for TLV1548 selected | 0100b | 4h | Channel 2 for TLV1544 |
| Analog channel A5 for TLV1548 selected | 0101b | 5h | |
| Analog channel A6 for TLV1548 selected | 0110b | 6h | Channel 3 for TLV1544 |
| Analog channel A7 for TLV1548 selected | 0111b | 7h | |
| Software power down set | 1000b | 8h | No conversion result (cleared by any access) |
| Fast conversion rate (10 μs) set | 1001b | 9h | No conversion result (cleared by setting to fast) |
| Slow conversion rate (40 μs) set | 1010b | Ah | No conversion result (cleared by setting to slow) |
| Self-test voltage ($V_{ref+} - V_{ref-}$)/2 selected | 1011b | Bh | Output result = 200h |
| Self-test voltage $V_{ref-}$ selected | 1100b | Ch | Output result = 000h |
| Self-test voltage $V_{ref+}$ selected | 1101b | Dh | Output result = 3FFh |
| Reserved | 1110b | Eh | No conversion result |
| Reserved | 1111b | Fh | No conversion result |

### analog inputs and internal test voltages

The eight analog inputs and the three internal test inputs are selected by the 11-channel multiplexer according to the input data bit as shown in Table 3. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

The device can be operated in two distinct sampling modes: normal sampling mode (fixed sampling time) and extended sampling mode (flexible sampling time). When $\overline{\text{CSTART}}$ is held high, the device is operated in normal sampling mode. When operated in normal sampling mode, sampling of the analog input starts on the rising edge of the fourth I/O CLK pulse in the microprocessor interface mode (and on the fourth falling edge of I/O CLK in the DSP interface mode). Sampling continues for 6 I/O CLK periods. The sample is held on the falling edge of the tenth I/O CLK pulse in the microprocessor interface mode. The sample is held on the falling edge of the tenth I/O CLK pulse in the DSP interface mode.The three test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs.

**converter**

The CMOS threshold detector in the successive-approximation conversion system determines the value of each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the $S_C$ switch and all $S_T$ switches simultaneously. This action charges all of the capacitors to the input voltage.

In the next phase of the conversion process, all $S_T$ and $S_C$ switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF –) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF –. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half $V_{CC}$), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF –. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF + through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

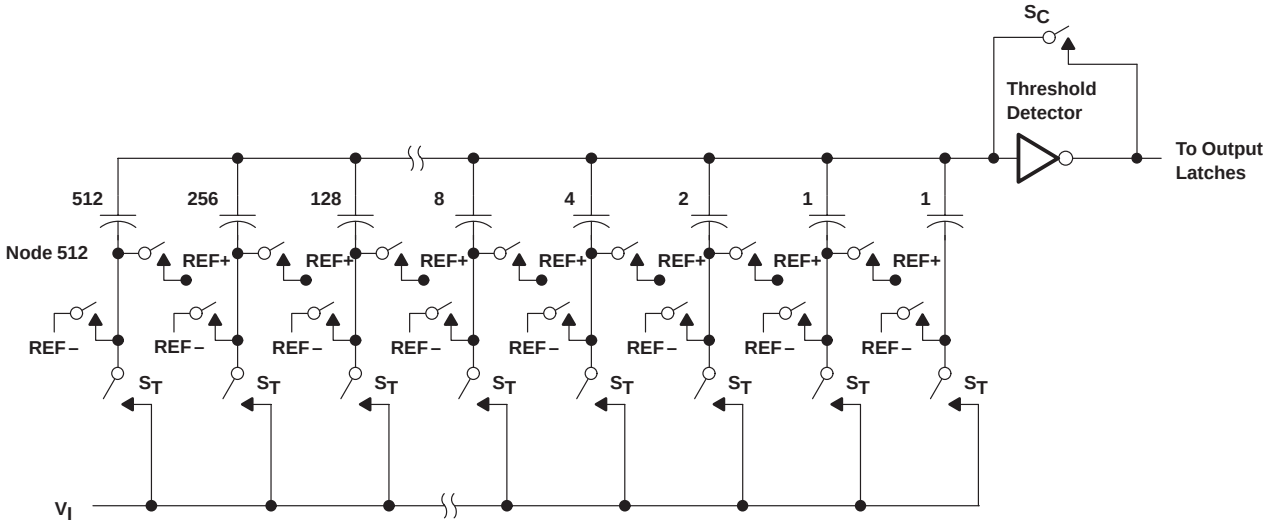



**Figure 1. Simplified Model of the Successive-Approximation System**

### extended sampling, asynchronous start of sampling: $\overline{\text{CSTART}}$ operation

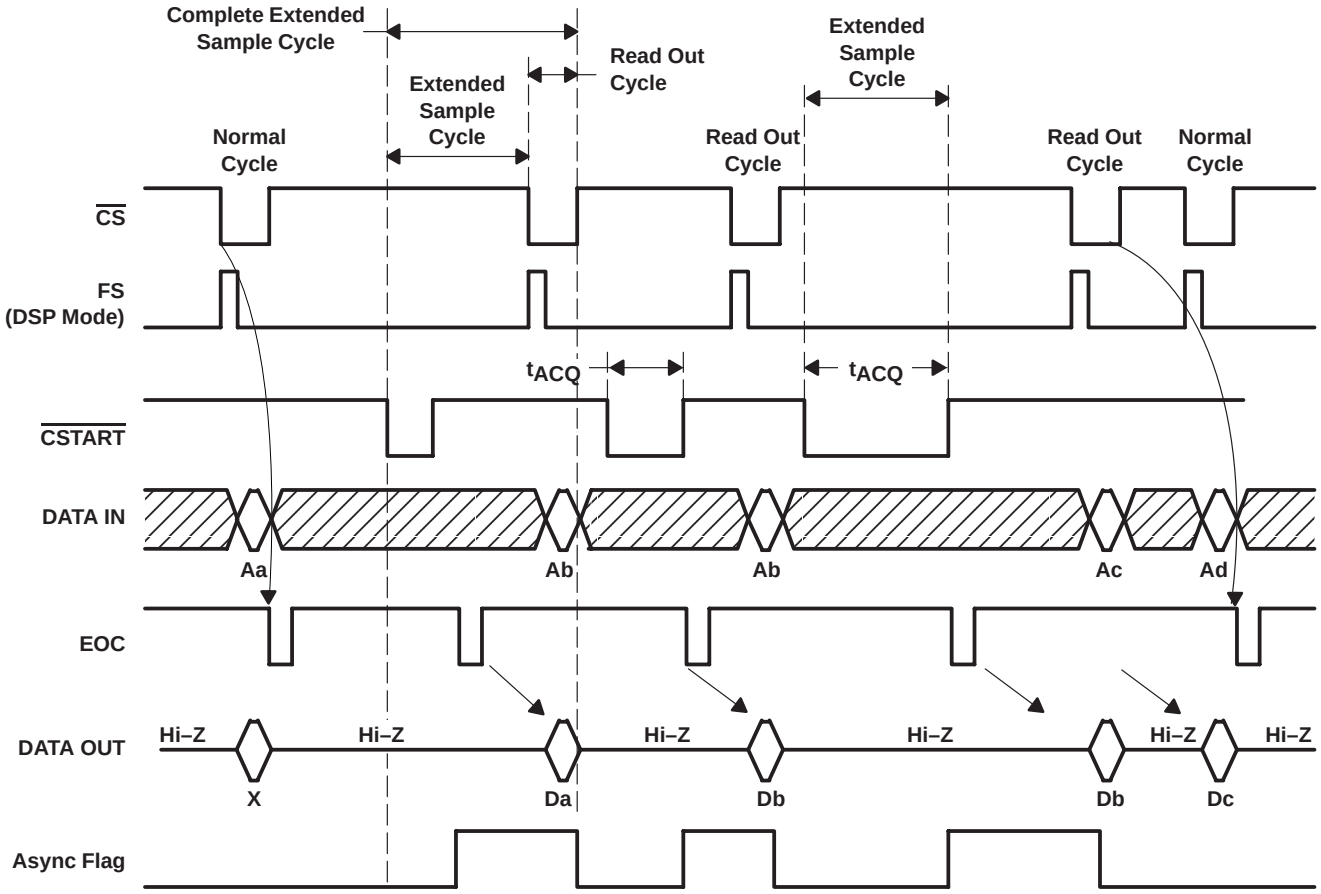
The extended sampling mode of operation programs the acquisition time ($t_{ACQ}$) of the sample-and-hold circuit. This allows the analog inputs of the device to be directly interfaced to a wide range of input source impedances. The extended sampling mode consumes higher power depending on the duration of the sampling period chosen.

$\overline{\text{CSTART}}$ controls the sampling period and starts the conversion. The falling edge of $\overline{\text{CSTART}}$ initiates the sampling period of a preset channel. The low time of $\overline{\text{CSTART}}$ controls the acquisition time of the input sample-and-hold circuit. The sample is held on the rising edge of $\overline{\text{CSTART}}$. Asserting $\overline{\text{CSTART}}$ causes the converter to perform a new sample of the signal on the preset valid MUX channel (one of the eight) and discard the current conversion result ready for output. Sampling continues as long as $\overline{\text{CSTART}}$ is active (negative). The rising edge of $\overline{\text{CSTART}}$ ends the sampling cycle. The conversion cycle starts two internal system clocks after the rising edge of $\overline{\text{CSTART}}$.

Once the conversion is complete, the processor can initiate a normal I/O cycle to read the conversion result and set the MUX address for the next conversion. Since the internal flag AsyncFlag is set high, this flag setting indicates the cycle is an output cycle, so no conversion is performed during the cycle. The internal state machine tests the AsyncFlag on the falling edge of $\overline{\text{CS}}$. AsyncFlag is set high at the rising edge of $\overline{\text{CSTART}}$, and it is reset low at the rising edge of each $\overline{\text{CS}}$. A conversion cycle follows a sampling cycle only if AsyncFlag is tested as low at the falling edge of $\overline{\text{CS}}$. As shown in Figure 2, an asynchronous I/O cycle can be removed by two consecutive normal I/O cycles.

**Table 4. TLV1544/1548 Hardware Configuration for Different Operating Modes**

| OPERATING MODES | $\overline{\text{CS}}$ | $\overline{\text{CSTART}}$ | AsyncFlag at $\overline{\text{CS}}\downarrow$ | ACTION |
|---|---|---|---|---|
| Normal sampling | Low | High | Low | Fixed 6 I/O CLK sampling, synchronous conversion follows |
| Normal I/O (read out only) | Low | High | High | No sampling, no conversion |
| Extended sampling | High | Low | N/A | Flexible sampling period controlled by $\overline{\text{CSTART}}$, asynchronous conversion follows |




NOTES: A. Aa = Address for input channel a.
B. Da = Conversion result from channel a.

**Figure 2. Extended Sampling Operation**

## reference voltage inputs

There are two reference inputs used with the TLV1544/TLV1548, REF+ and REF–. These voltage values establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REF+, REF–, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and is at zero when the input signal is equal to or lower than REF–.

## programmable conversion rate

The TLV1544/TLV1548 offers two conversion rates to maximize battery life when high-speed operation is not necessary. The conversion rate is programmable. Once the conversion rate has been selected, it takes effect immediately in the same cycle and stays at the same rate until the other rate is chosen. The conversion rate should be set at power up. Activation and deactivation of the power-down state (digital logic active) has no effect on the preset conversion rate.

**Table 5. Conversion Rate and Power Consumption Selection**

| CONVERSION RATE | CONVERSION TIME, $t_{conv}$ | AVAILABLE $V_{CC}$ RANGE | INPUT DATA | TYPICAL SUPPLY CURRENT, $I_{CC}$ | | |
|---|---|---|---|---|---|---|
| | | | | OPERATING | | POWER DOWN |
| Fast conversion speed | 7 μs typ | 5.5 V to 3.3 V | 9h | 0.6 mA typ | 1.5 mA max | 1 μA typ |
| Slow conversion speed | 15 μs typ | 5.5 V to 2.7 V | Ah | 0.4 mA typ | 1 mA max | 1 μA typ |

## programmable power-down state

The device is put into the power-down state by writing 8h to DATA IN. The power-up state is restored during the next active access by pulling $\overline{CS}$ low. The conversion rate selected before the device is put into the power-down state is not affected by the power-down mode. Power-down can be used to achieve even lower power consumption. This is because the sustaining power (when not converting) is only 1.3 mA maximum and standby power is only 1 μA maximum. (By averaging out the power consumption can be much lower than the 1 mA peak when the conversion throughput is lower.)

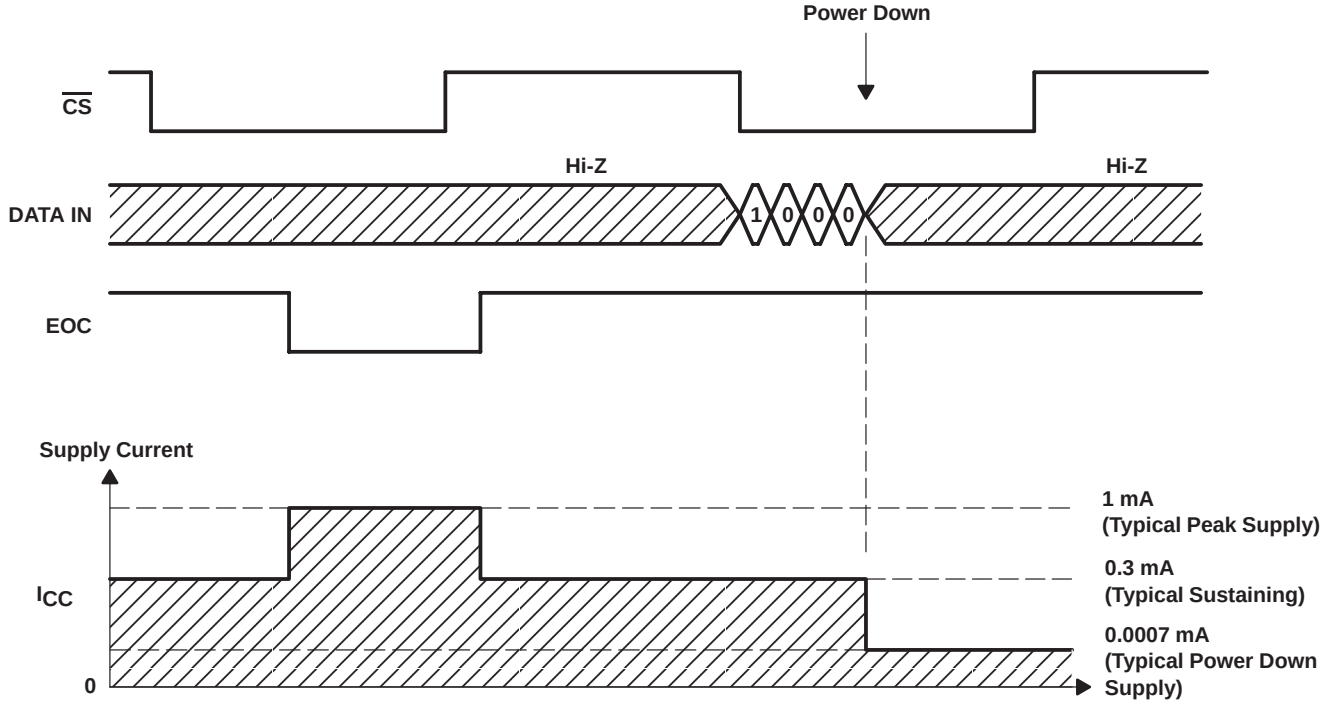



**Figure 3. Typical Supply Current During Conversion/Power Down**

## power up and initialization

After power up, if operating in DSP mode, $\overline{CS}$ and FS must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeroes. The content of the output data register is random, and the first conversion result should be ignored. For initialization during operation, $\overline{CS}$ is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state can be invalid and should be disregarded.

When power is first applied to the device, the conversion rate must be programmed, and the internal Async Flag must be taken low once. The rising edge of $\overline{CS}$ of the same cycle then takes Async Flag low.

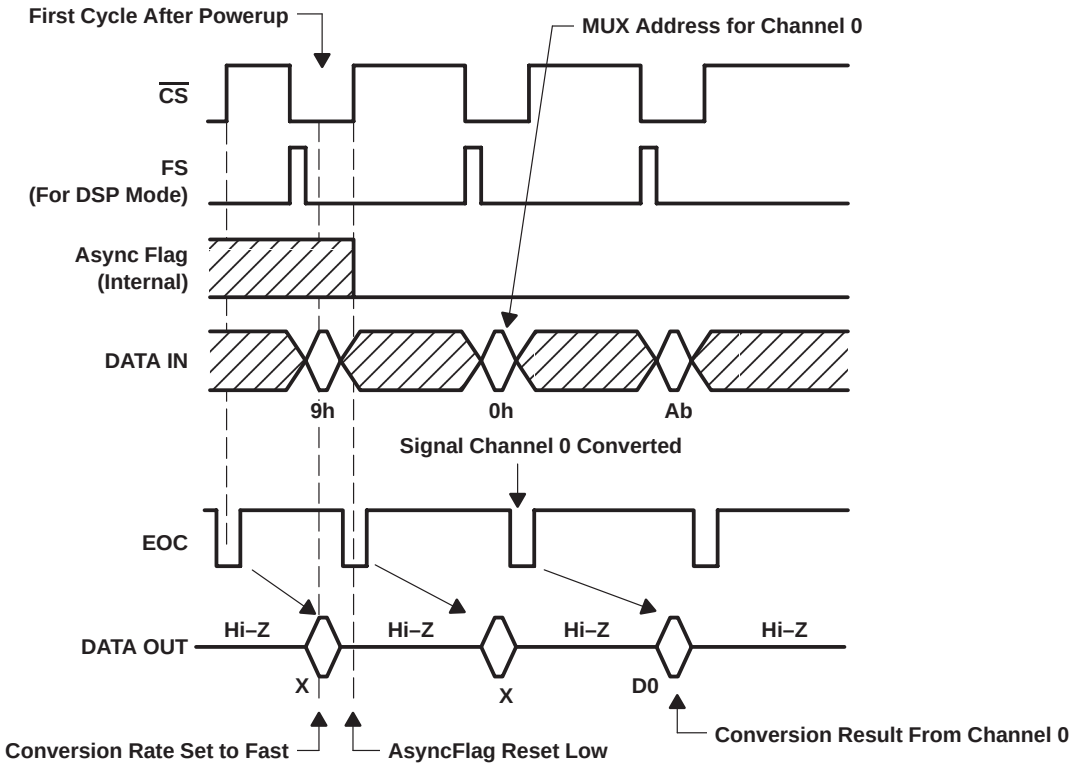



**Figure 4. Power Up Initialization**

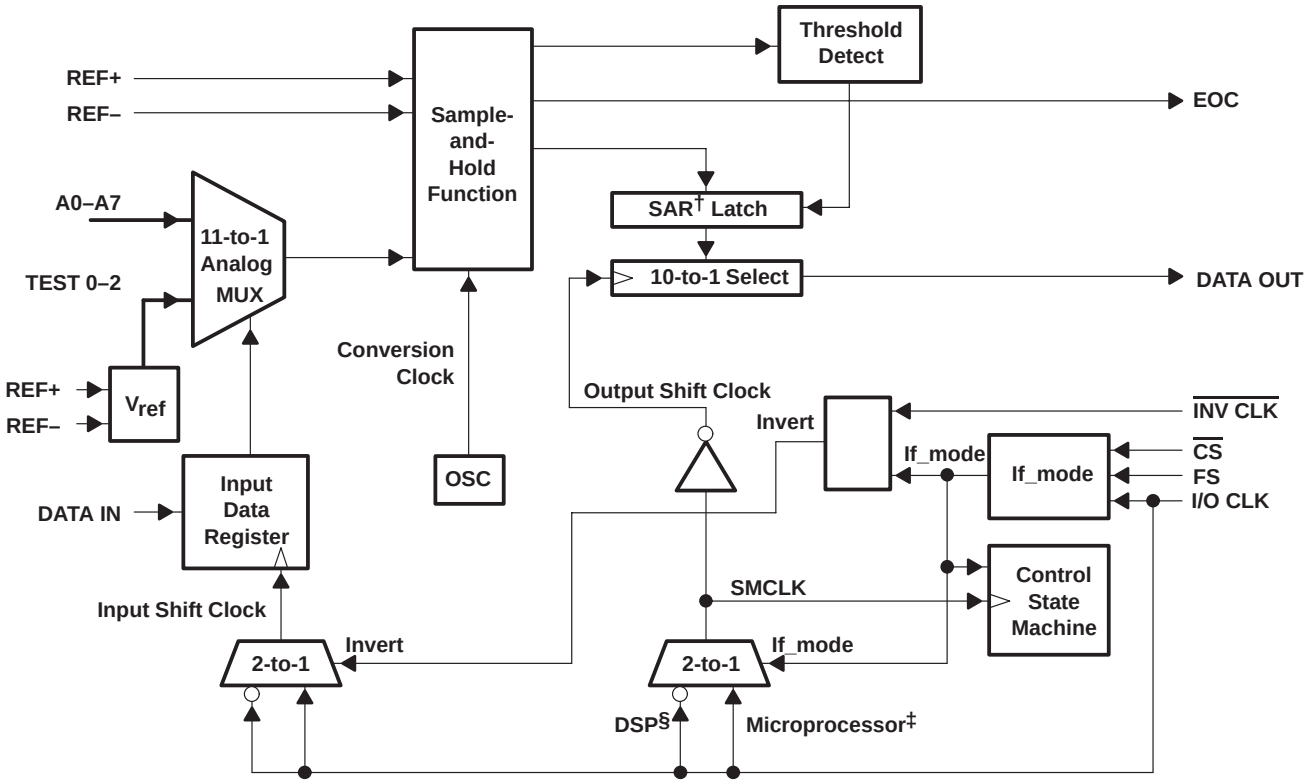
## input clock inversion – $\overline{\text{INV CLK}}$

The input data register uses I/O CLK as the source of the sampling clock. This clock can be inverted to provide more setup time. $\overline{\text{INV CLK}}$ can invert the clock. When $\overline{\text{INV CLK}}$ is grounded, the input clock for the input data register is inverted. This allows an additional one-half I/O CLK period for the input data setup time. This is useful for some serial interfaces. When the input sampling clock is inverted, the output data changes at the same time that the input data is sampled.

**Table 6. Function of $\overline{\text{INV CLK}}$**

| CONDITION CLOCK | | I/O CLK ACTIVE EDGE | |
|---|---|---|---|
| $\overline{\text{INV CLK}}$ | FS at $\overline{\text{CS}}\downarrow$ | OUTPUT DATA CHANGES ON | INPUT DATA SAMPLED ON |
| High | High (MP† mode) | ↓ | ↑ |
| High | Low (DSP‡ mode) | ↑ | ↓ |
| Low | High (MP† mode) | ↓ | ↓ |
| Low | Low (DSP‡ mode) | ↑ | ↑ |

† MP = microprocessor mode
‡ DSP = digital signal processor mode




† Successive approximation register
‡ If_mode = 1, microprocessor interface mode
§ If_mode = 0, DSP interface mode

**Figure 5. Clock Scheme**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.5 V to 6.5 V
Input voltage range, $V_I$ (any input) . . . . . –0.3 V to $V_{CC}$ + 0.3 V
Output voltage range, $V_O$ . . . . . –0.3 V to $V_{CC}$ + 0.3 V
Positive reference voltage, $V_{ref+}$ . . . . . $V_{CC}$ + 0.1 V
Negative reference voltage, $V_{ref–}$ . . . . . –0.1 V
Peak input current, $I_I$ (any input) . . . . . ±20 mA
Peak total input current (all inputs) . . . . . –30 mA
Operating free-air temperature range, $T_A$: TLV1544C, TLV1548C . . . . . 0°C to 70°C
TLV1544I, TLV1548I . . . . . –40°C to 85°C
TLV1548M . . . . . –55°C to 125°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND with REF– and GND wired together (unless otherwise noted).

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 2.7 | | 5.5 | V |
| Positive reference voltage, $V_{ref+}$ (see Note 2) | | | $V_{CC}$ | | V |
| Negative reference voltage, $V_{ref-}$ (see Note 2) | | | 0 | | V |
| Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2) | | 2.5 | $V_{CC}$ | $V_{CC}$ +0.2 | V |
| Analog input voltage, $V_{I\ (analog)}$ (see Note 2) | | 0 | | $V_{CC}$ | V |
| High-level control input voltage, $V_{IH}$ | | 2.1 | | | V |
| Low-level control input voltage, $V_{IL}$ | | | | 0.6 | V |
| Setup time, input data bits valid before I/O CLK↑↓, $t_{su(A)}$ (see Figure 9) | | 100 | | | ns |
| Hold time, input data bits valid after I/O CLK↑↓, $t_{h(A)}$ (see Figure 9) | | 5 | 30 | | ns |
| Setup time, $\overline{CS}$↓ to I/O CLK↑, $t_{su(CS)}$ | See Figure 10 | 5 | 30 | | ns |
| Hold time, I/O CLK↓ to $\overline{CS}$↑, $t_{h(CS)}$ | See Figure 10 | 65 | | | ns |
| Pulse duration, FS high, $t_{wH(FS)}$ | See Figure 12 | 1 | | | I/O CLK periods |
| Pulse duration, $\overline{CSTART}$, $t_{w(CSTART)}$ | Source impedance ≤ 1 kΩ, $V_{CC}$ = 5.5 V, See Figure 14 | 0.84 | | | µs |
| Setup time, $\overline{CS}$↑ to $\overline{CSTART}$↓, $t_{su(CSTART)}$ | See Figure 14 | 10 | | | ns |
| Clock frequency at I/O CLK, $f_{CLK}$ | $V_{CC}$ = 5.5 V | 0.1 | 6 | 10 | MHz |
| | $V_{CC}$ = 2.7 V | 0.1 | 2 | 2.81 | |
| Pulse duration, I/O CLK high, $t_{wH(I/O)}$ | $V_{CC}$ = 5.5 V | 50 | | | ns |
| | $V_{CC}$ = 2.7 V | 100 | | | |
| Pulse duration, I/O CLK low, $t_{wL(I/O)}$ | $V_{CC}$ = 5.5 V | 50 | | | ns |
| | $V_{CC}$ = 2.7 V | 100 | | | |
| Transition time, I/O CLK, $t_{t(I/O)}$ (see Figure 11 and Note 4) | | | | 1 | µs |
| Transition time, DATA IN, $t_{t(DATA\ IN)}$ (see Figure 9) | | | | 10 | µs |
| Transition time, $\overline{CS}$, $t_{t(CS)}$ (see Figure 10) | | | | 10 | µs |
| Transition time, FS, $t_{t(FS)}$ (see Figure 13) | | | | 10 | µs |
| Transition time, $\overline{CSTART}$, $t_{t(CSTART)}$ (see Figure 14) | | | | 10 | µs |
| Operating free-air temperature, $T_A$ | TLV1544C, TLV1548C | 0 | | 70 | °C |
| | TLV1544I, TLV1548I | –40 | | 85 | |
| | TLV1548M | –55 | | 125 | |
| Junction temperature, $T_J$ | TLV1544C, TLV1548C | | | 115 | °C |
| | TLV1544I, TLV1548I | | | 115 | |
| | TLV1548M | | | 150 | |

NOTES: 2. Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF– convert as all zeros (000000000000). The device is functional with reference ($V_{ref+} - V_{ref-}$) down to 1 V; however, the electrical specifications are no longer applicable.

3. To minimize errors caused by noise at $\overline{CS}$↓, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an input dat until the minimum $\overline{CS}$ setup time has elapsed.

4. This is the time required for the I/O CLK signal to fall from $V_{IH}$max to $V_{IL}$min or to rise from $V_{IL}$max to $V_{IH}$min. In the vicinity of normal room temperature, the devices function with an input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 2.7 V to 5.5 V, I/O CLK frequency = 2.2 MHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 5.5 V, | $I_{OH}$ = –0.2 mA | 2.4 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –20 µA | $V_{CC}$–0.1 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 5.5 V, | $I_{OL}$ = 0.8 mA | | | 0.4 | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OL}$ = 20 µA | | | 0.1 | |
| $I_{OZ}$ | High-impedance output current | $V_O = V_{CC}$, | $\overline{CS} = V_{CC}$ | | 1 | 2.5 | µA |
| | | $V_O$ = 0, | $\overline{CS} = V_{CC}$ | | –1 | –2.5 | |
| $I_{IH}$ | High-level input current | $V_I = V_{CC}$ | | | 0.005 | 2.5 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0 | | | –0.005 | 2.5 | µA |
| $I_{CC}$ | Operating supply current | Conversion speed = fast, For all digital inputs, $0 \le V_I \le 0.3$ V or $V_I \ge V_{CC} – 0.3$ V | $V_{CC}$ = 3.3 V to 5.5 V | | 0.6 | 1.5 | mA |
| | | Conversion speed = slow, For all digital inputs, $0 \le V_I \le 0.3$ V or $V_I \ge V_{CC} – 0.3$ V | $V_{CC}$ = 3.3 V to 5.5 V | | 0.4 | 1 | |
| | | | $V_{CC}$ = 2.7 V to 3.3 V | | 0.35 | 0.75 | |
| $I_{CC(ES)}$ | Extended sampling mode operating current | $V_{CC}$ = 3.3 V to 5.5 V | | | 1.5 | | mA |
| | | $V_{CC}$ = 2.7 V to 3.3 V | | | 1 | | mA |
| $I_{CC(ST)}$ | Sustaining supply current | Conversion speed = slow, For all digital inputs, $0 \le V_I \le 0.3$ V or $V_I \ge V_{CC} – 0.3$ V | $V_{CC}$ = 2.7 V to 3.3 V | | 0.3 | | mA |
| $I_{CC(PD)}$ | Power-down supply current | For all digital inputs, $0 \le V_I \le 0.3$ V or $V_I \ge V_{CC} – 0.3$ V | | | 1 | 25 | µA |
| $I_{lkg}$ | Selected channel leakage current | Selected channel at $V_{CC}$, unselected channel at 0 V | | | | 1 | µA |
| | | Selected channel at 0 V, unselected channel at $V_{CC}$ | | | | –1 | µA |
| | Maximum static analog reference current into REF+ | $V_{ref+} = V_{CC}$ = 5.5 V, | $V_{ref–}$ = GND | | | 1 | µA |
| $C_i$ ‡ | Input capacitance, analog inputs | | | | 20 | 55 | pF |
| | Input capacitance, control inputs | | | | 20 | 15 | |
| $Z_i$ ‡ | Input multiplexer on resistance | $V_{CC}$ = 4.5 V | | | | 1 | kΩ |
| | | $V_{CC}$ = 2.7 V | | | | 5 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not production tested.

## operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 2.7 V to 5.5 V, I/O CLK frequency = 2.2 MHz (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_L$ | Linearity error (see Note 6) | | | | ±0.5 | ±1 | LSB |
| $E_D$ | Differential linearity error | | See Note 2 | | ±0.5 | ±1 | LSB |
| $E_O$ | Offset error (see Note 7) | | See Note 2 | | | ±1.5 | LSB |
| $E_G$ | Gain error (see Note 7) | | See Note 2 | | | ±1 | LSB |
| $E_T$ | Total unadjusted error (see Note 8) | | | | | ±1.75 | LSB |
| | Self-test output code (see Table 3 and Note 9) | | DATA IN = 1011 | | 512 | | |
| | | | DATA IN - 1100 | | 0 | | |
| | | | DATA IN = 1101 | | 1023 | | |
| $t_{conv}$ | Conversion time | Fast conversion speed | See Figures 15 through 17 | | 7 | 10 | µs |
| | | Slow conversion speed | | | 15 | 25 | µs |
| $t_c$ | Total cycle time (access, sample, conversion and EOC↑ to $\overline{CS}$↓ delay) | Fast conversion speed | See Figures 15 through 18 and Notes 10, 11, 12 | | | 10.1 + 10 I/O CLK | µs |
| | | Slow conversion speed | See Figures 15 through 18 and Notes 10 and 12 | | | 40.1 + 10 I/O CLK | |
| $t_{acq}$ | Channel acquisition time (sample) | | See Figures 15 through 18 and Note 10 | | | 6 | I/O CLK periods |
| $t_v$ | Valid time, DATA OUT remains valid after I/O CLK↓ | | See Figure 11 | 50 | | | ns |
| $t_{d1(FS)}$ | Delay time, I/O CLK high to FS high | | See Figure 13 | 5 | 30 | 50 | ns |
| $t_{d2(FS)}$ | Delay time, I/O CLK high to FS low | | See Figure 13 | 10 | 30 | 60 | ns |
| $t_{d(EOC↑ – CS↓)}$ | Delay time, EOC↑ to CS low | | See Figure 14 and Note 5 | 100 | | | ns |
| $t_{d(CS↓ – FS↑)}$ | Delay time, CS↓ to FS↑ | | See Figures 17 and 18 | 1 | | 7 | I/O CLK periods |
| $t_{d(I/O\ -CS)}$ | Delay time, 10th I/O CLK low to CS low to abort conversion (see Note 13) | | See Figure 10 | | | 1.1 | µs |

† All typical values are at $T_A$ = 25°C.

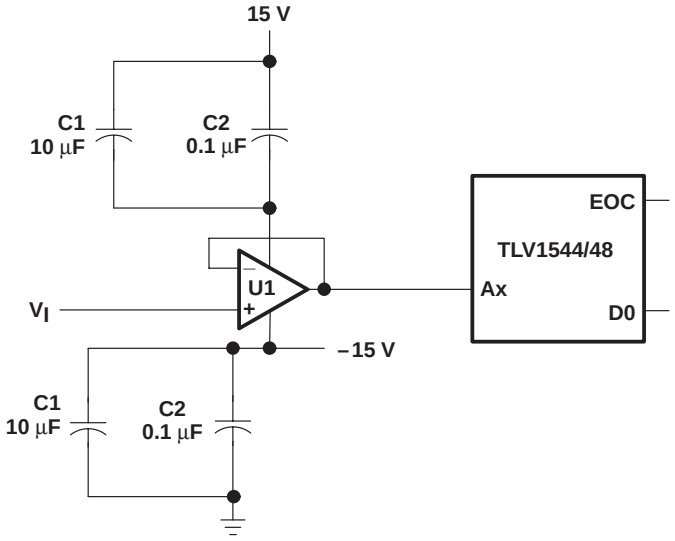
NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000). The device is functional with reference down to 1 V ($V_{ref+} – V_{ref} – 1$); however, the electrical specifications are no longer applicable.
5. For all operating modes.
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero error is the difference between 0000000000 and the converted output for zero input voltage. Full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input data and the output codes are expressed in positive logic.
10. I/O CLK period = 1/(I/O CLK frequency) (see Figure 8).
11. For 3.3 V to 5.5 V only
12. For microprocessor mode
13. Any transitions of $\overline{CS}$ are recognized as valid only when the level is maintained for a setup time after the transition.

**operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 2.7 V to 5.5 V, I/O CLK frequency = 2.2 MHz (unless otherwise noted) (continued)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(I/O-DATA)}$ | Delay time, I/O CLK low to DATA OUT valid | See Figure 11 | | | 50 | ns |
| $t_{d(I/O-EOC)}$ | Delay time, 10th I/O CLK↓ to EOC low | See Figure 12 | | 70 | 240 | ns |
| $t_{PZH}$, $t_{PZL}$ | Enable time, $\overline{CS}$ low to DATA OUT valid (MSB driven) | See Figure 8 | | 0.7 | 1.3 | µs |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time, $\overline{CS}$ high to DATA OUT invalid (high impedance) | See Figure 8 | | 70 | 150 | ns |
| $t_{f(EOC)}$ | Fall time, EOC | See Figure 12 | | 15 | 50 | ns |
| $t_{r(bus)}$ | Rise time, output data bus at 2.2 MHz I/O CLK | See Figure 11 | | 50 | 250 | ns |
| $t_{f(bus)}$ | Fall time, output data bus at 2.2 MHz I/O CLK | See Figure 11 | | 50 | 250 | ns |

† All typical values are at $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION




| LOCATION | DESCRIPTION | PART NUMBER |
|---|---|---|
| U1 | OP27 | — |
| C1 | 10-µF 35-V tantalum capacitor | — |
| C2 | 0.1-µF ceramic NPO SMD capacitor | AVX 12105C104KA105 or equivalent |

**Figure 6. Analog Input Buffer to Analog Inputs**

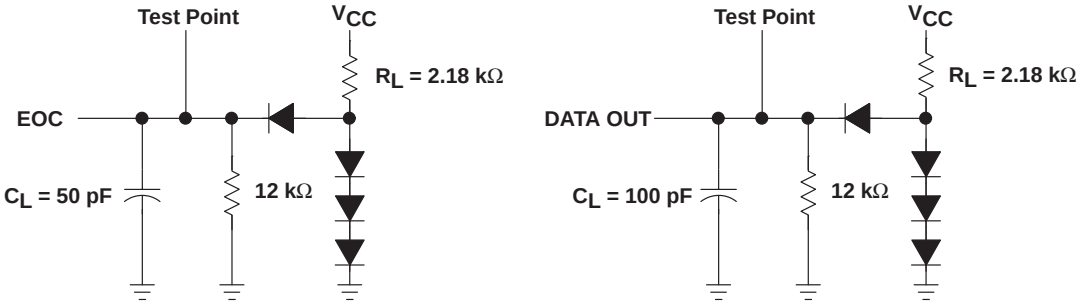



**Figure 7. Load Circuits**

## PARAMETER MEASUREMENT INFORMATION

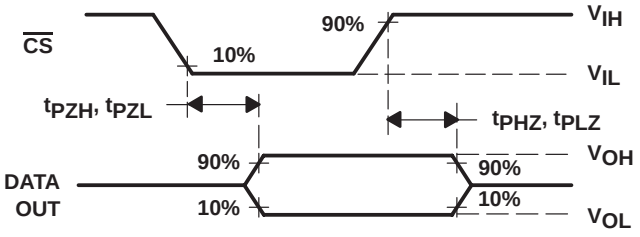



Figure 8. DATA OUT to Hi-Z Voltage Waveforms

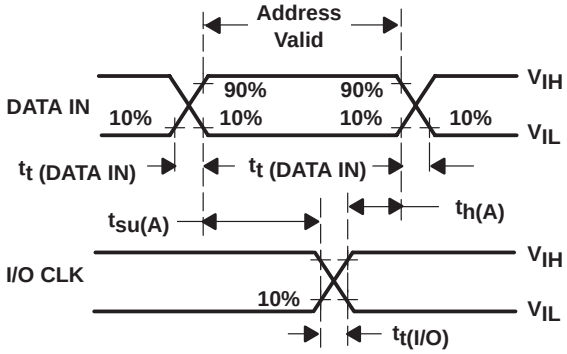



Figure 9. DATA IN Setup Voltage Waveforms

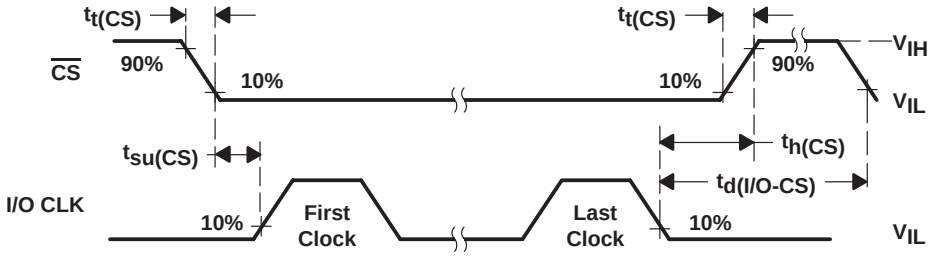



Figure 10. $\overline{CS}$ and I/O CLK Voltage Waveforms

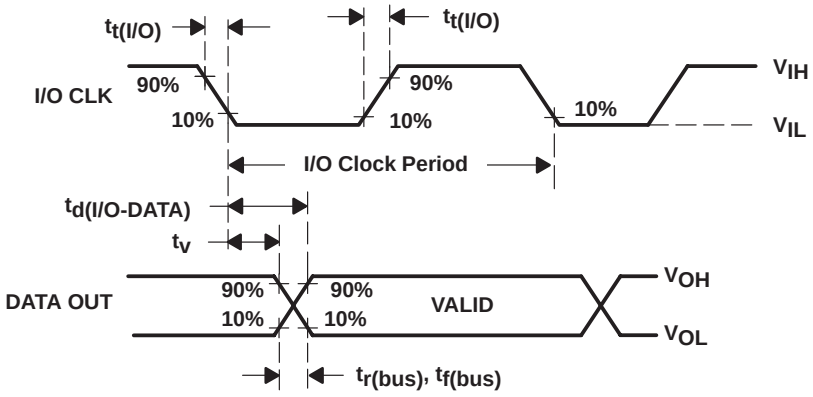



Figure 11. DATA OUT and I/O CLK Voltage Waveforms

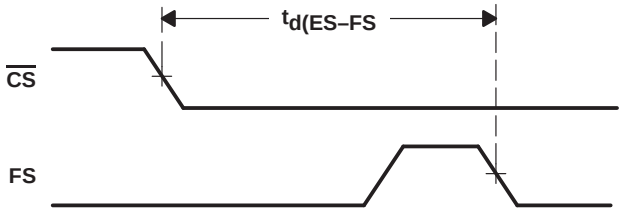



Figure 12. CS Low to FS Low

## PARAMETER MEASUREMENT INFORMATION

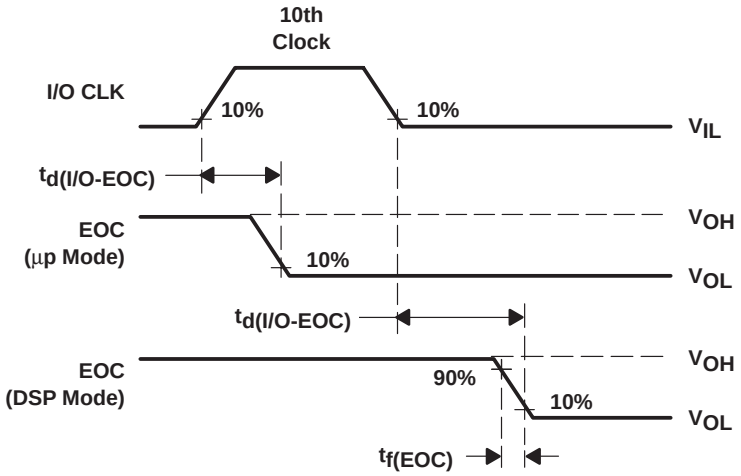



**Figure 13. I/O CLK and EOC Voltage Waveforms**

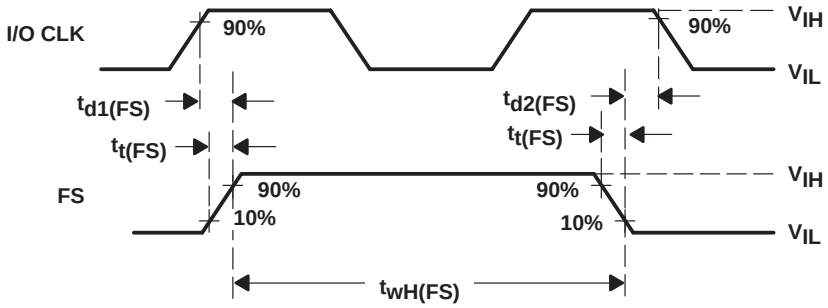



**Figure 14. FS and I/O CLK Voltage Waveforms**

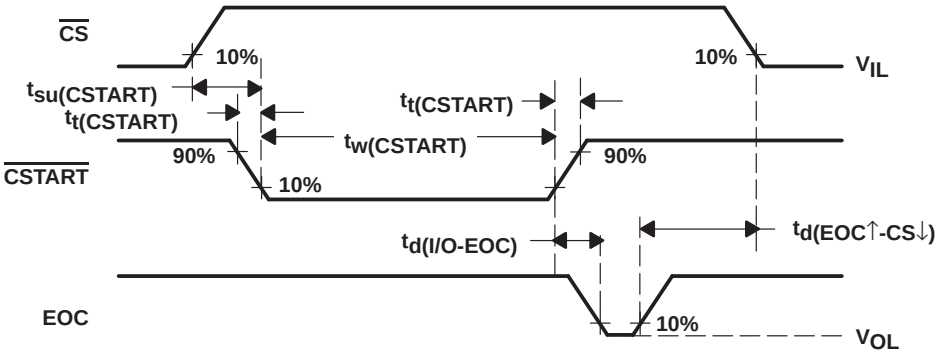
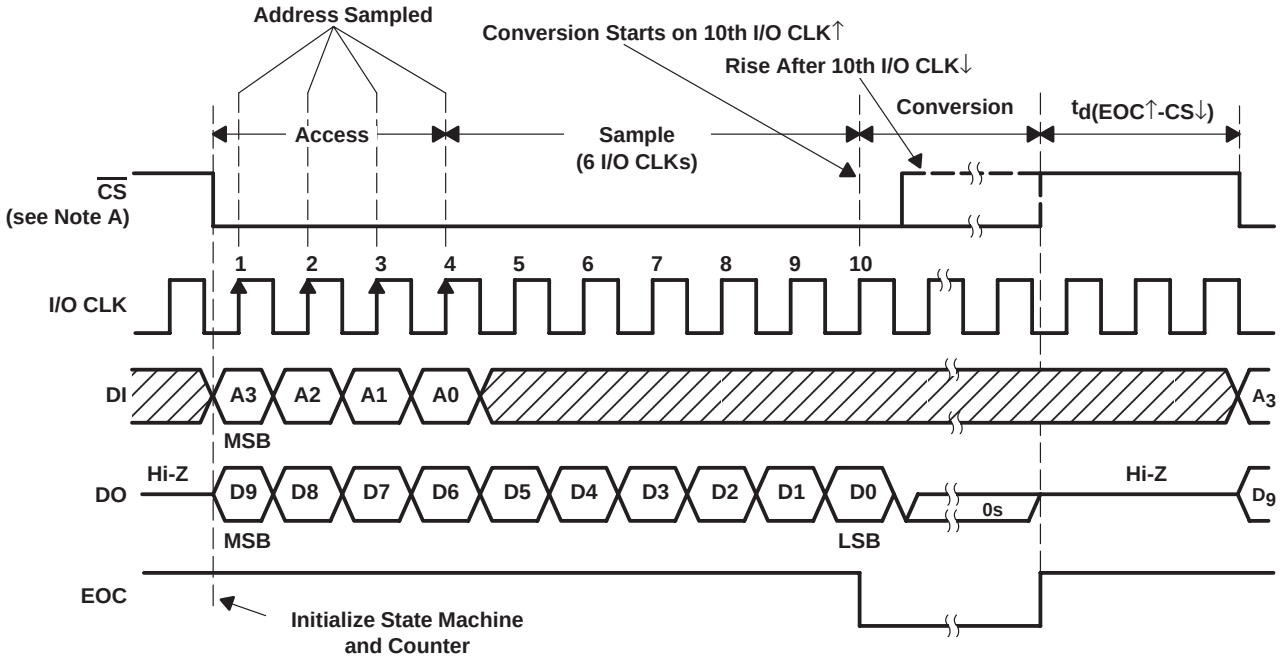


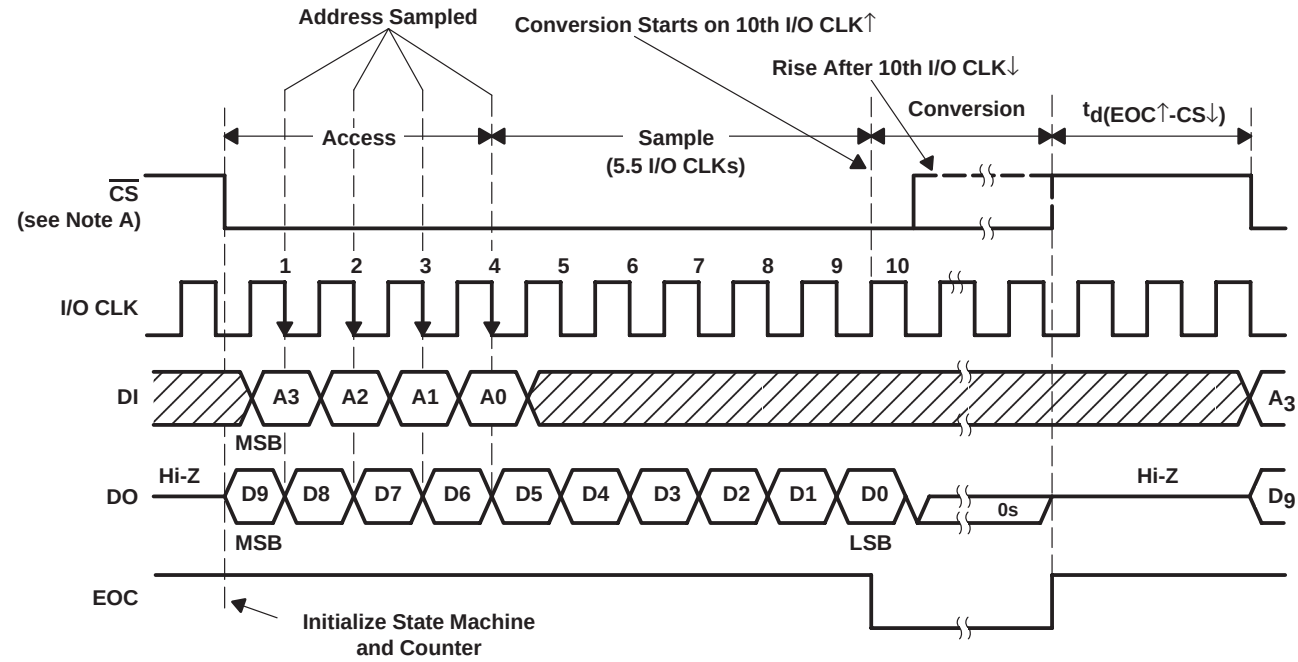

**Figure 15. $\overline{CSTART}$ and $\overline{CS}$ Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

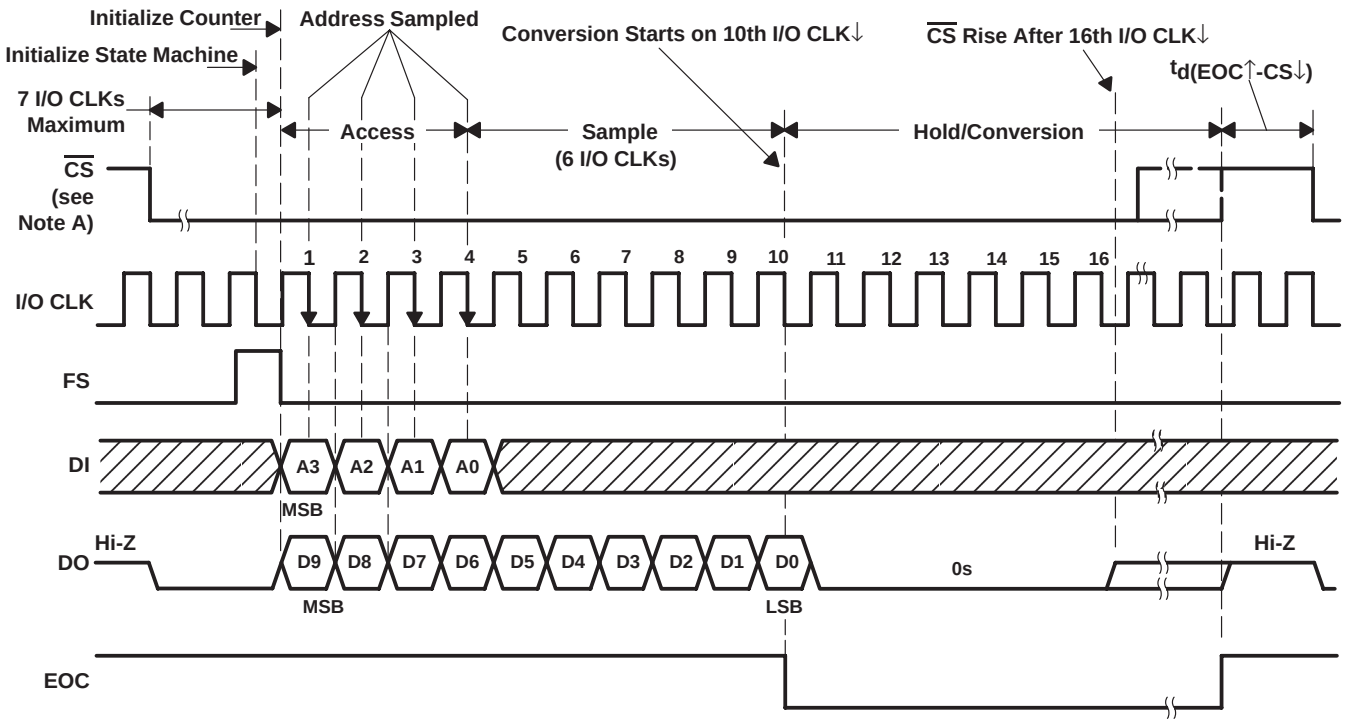
**Figure 16. Microprocessor Interface Timing (Normal Sample Mode, $\overline{INV\ CLK}$ = High)**




NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time has elapsed.

**Figure 17. Microprocessor Interface Timing (Normal Sample Mode, $\overline{INV\ CLK}$ = Low)**

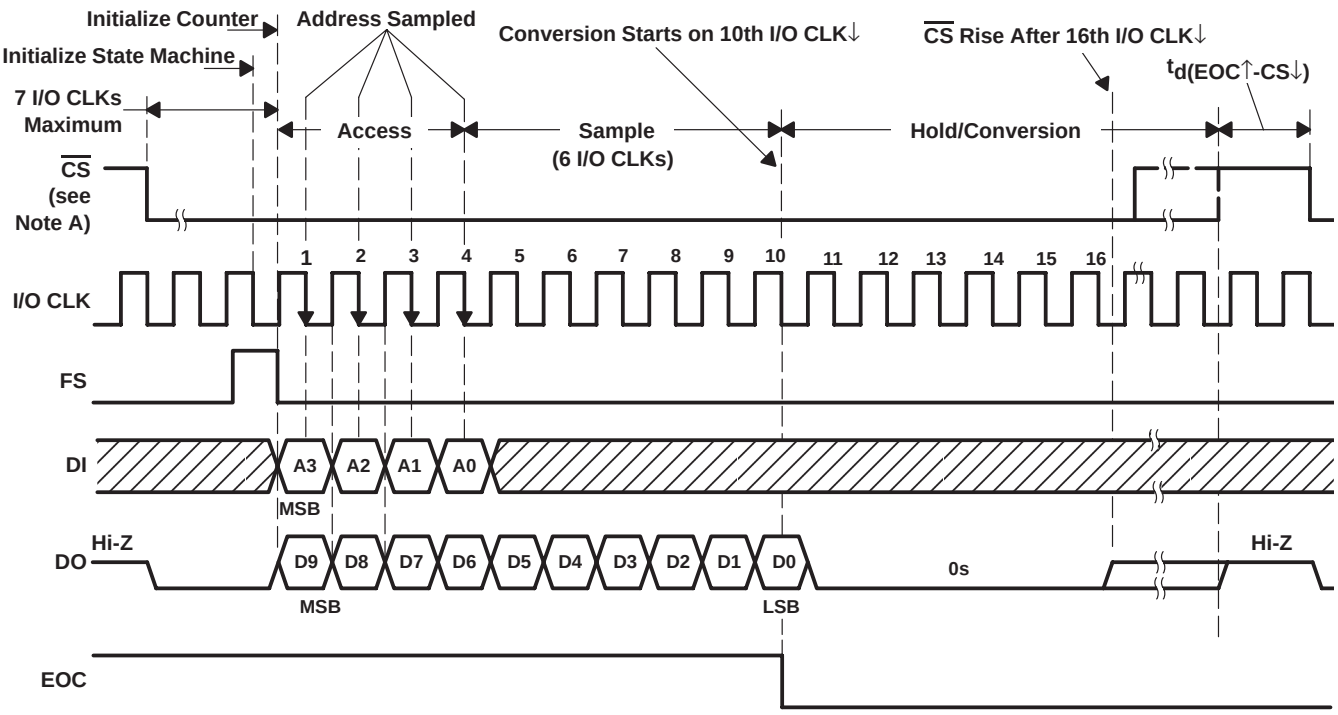
## PARAMETER MEASUREMENT INFORMATION




NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

**Figure 18. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{INV\ CLK}$ = High)**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{CS}$ setup time elapses.

**Figure 19. DSP Interface Timing (16-Clock Transfer, Normal Sample Mode, $\overline{INV\ CLK}$ = Low)**

## TYPICAL CHARACTERISTICS

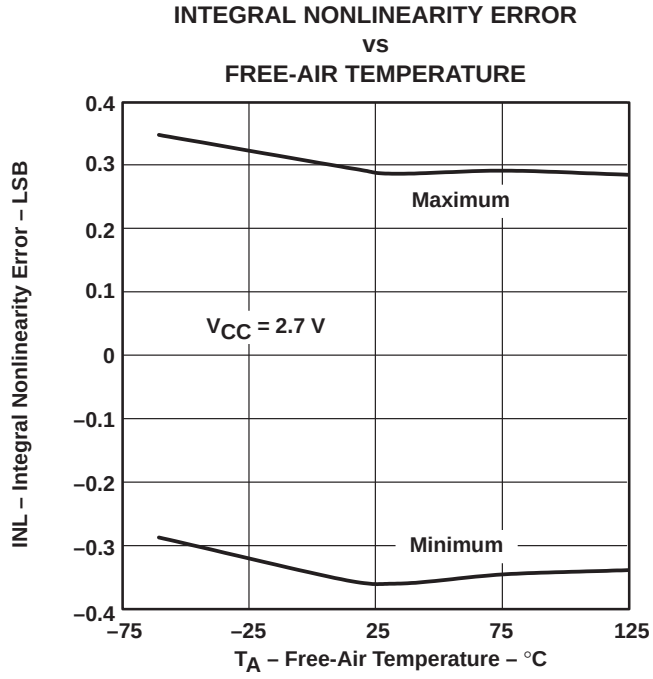



Figure 20

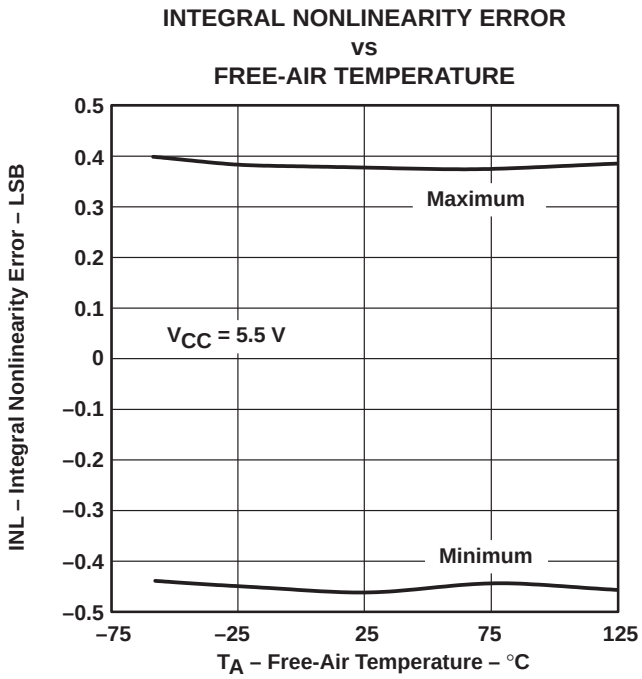



Figure 21

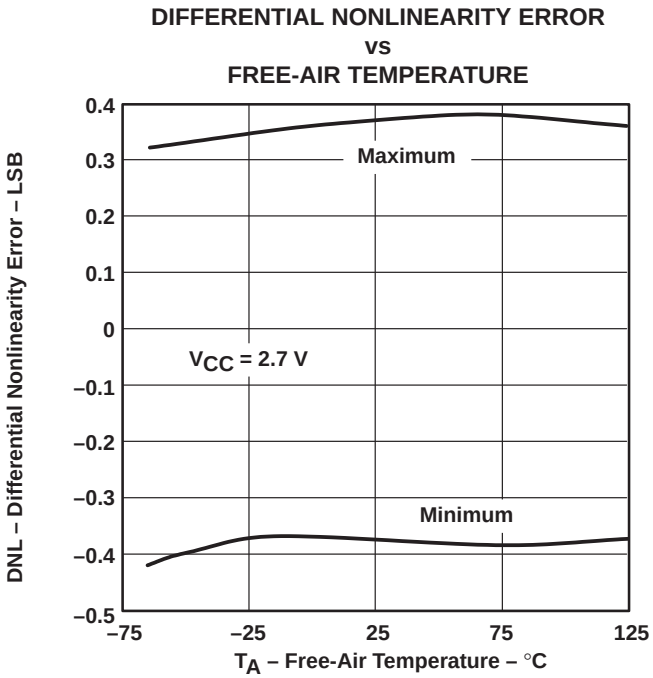



Figure 22

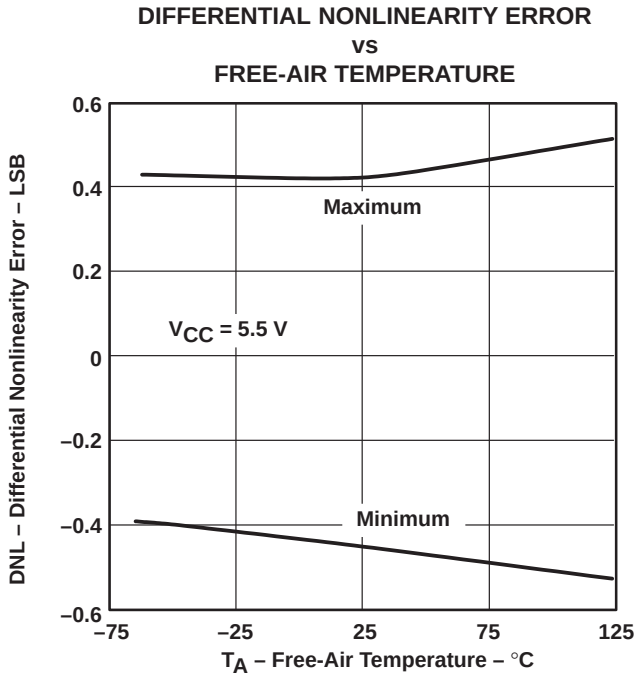



Figure 23

## TYPICAL CHARACTERISTICS

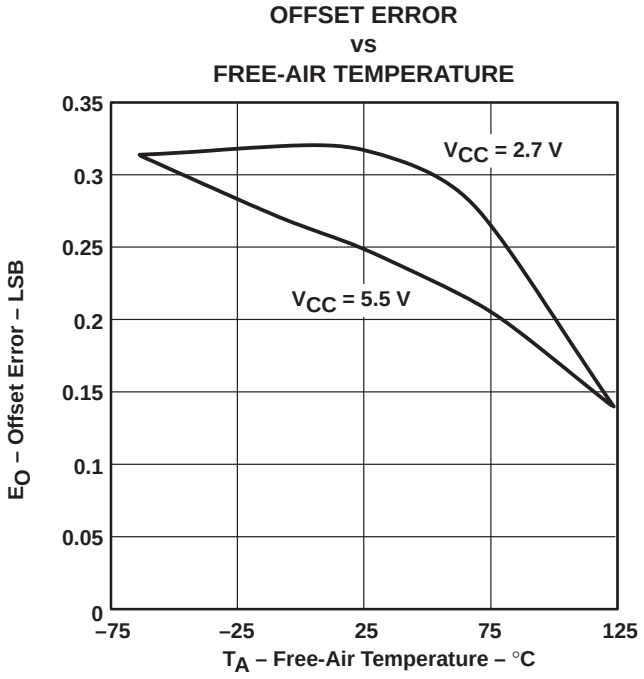



Figure 24

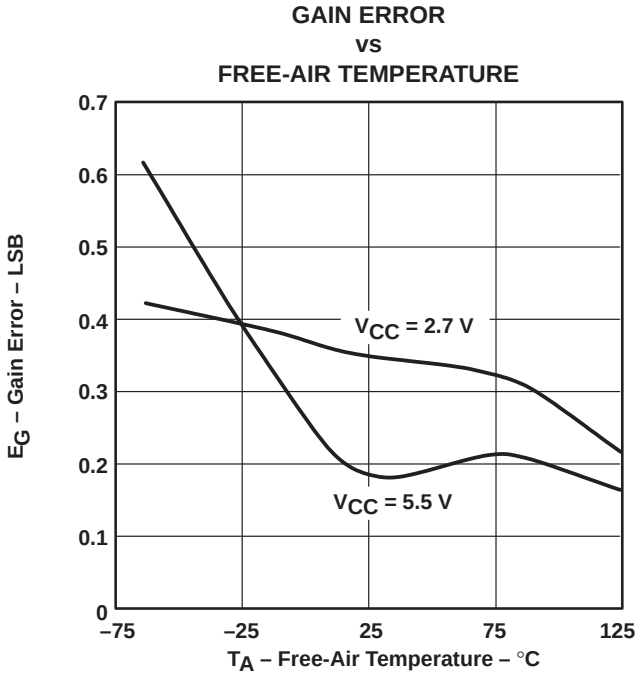



Figure 25

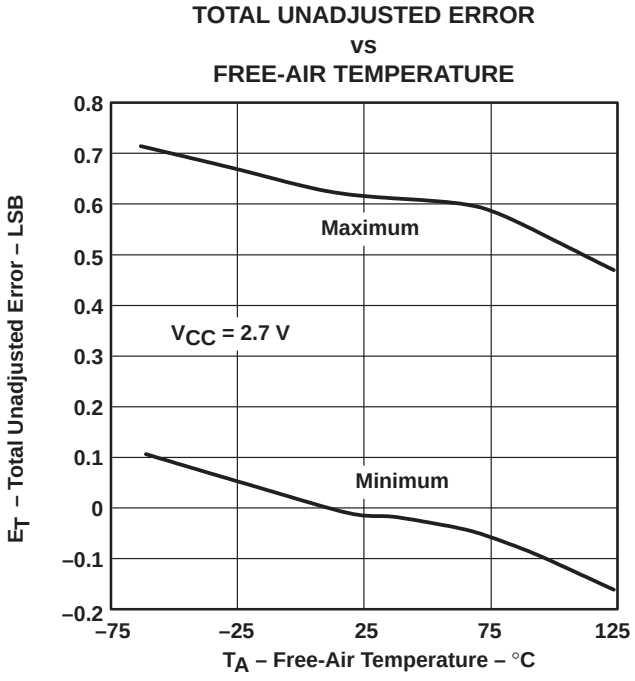



Figure 26

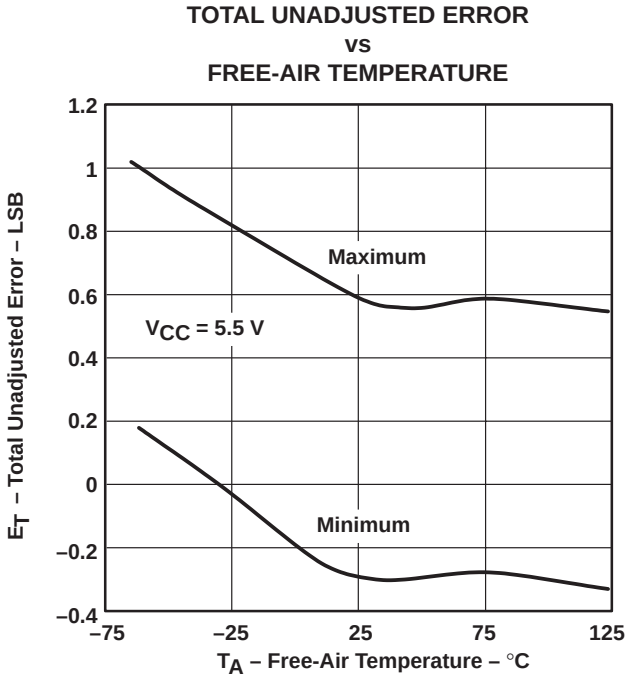



Figure 27

## TYPICAL CHARACTERISTICS

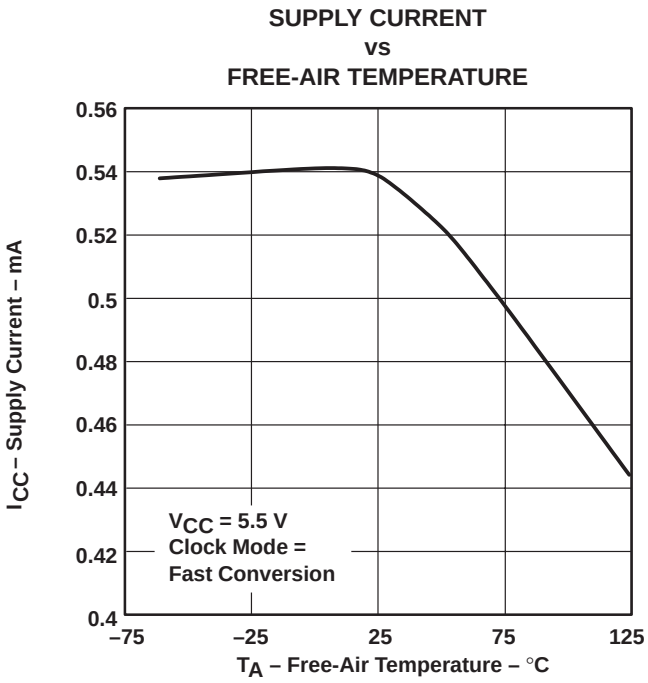



**Figure 28**

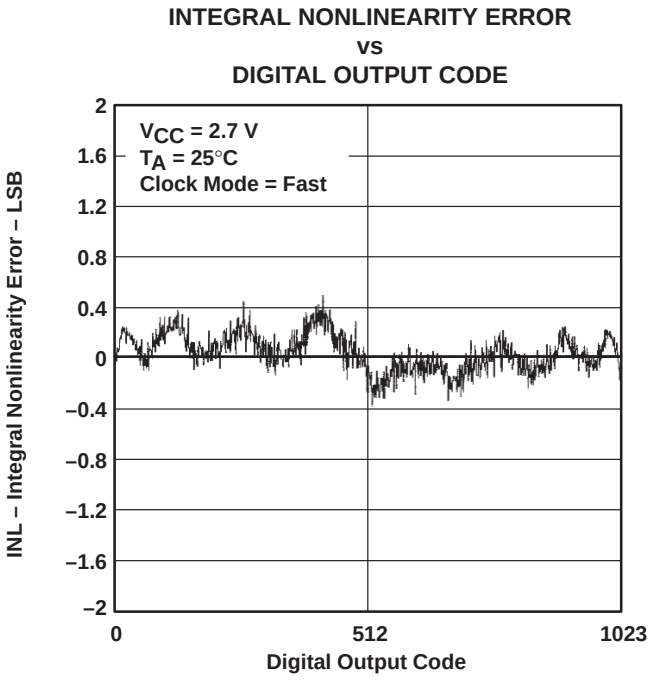



**Figure 29**

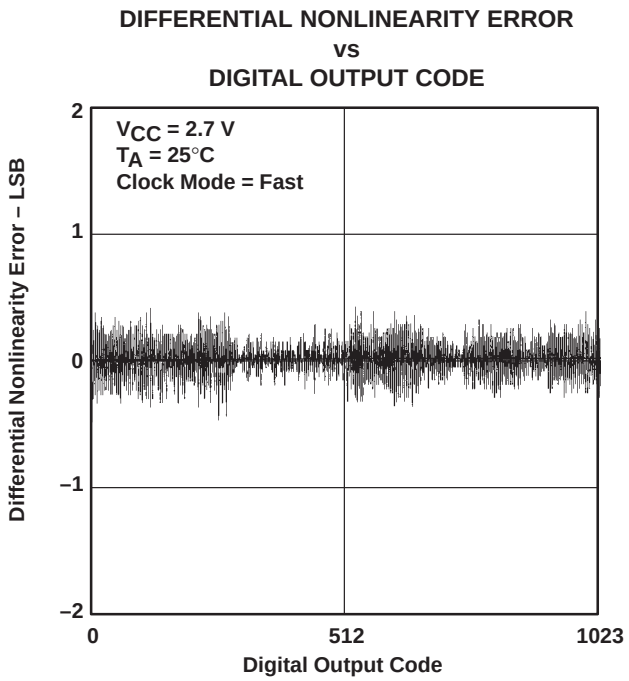



**Figure 30**

## TYPICAL CHARACTERISTICS

**INTEGRAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE**

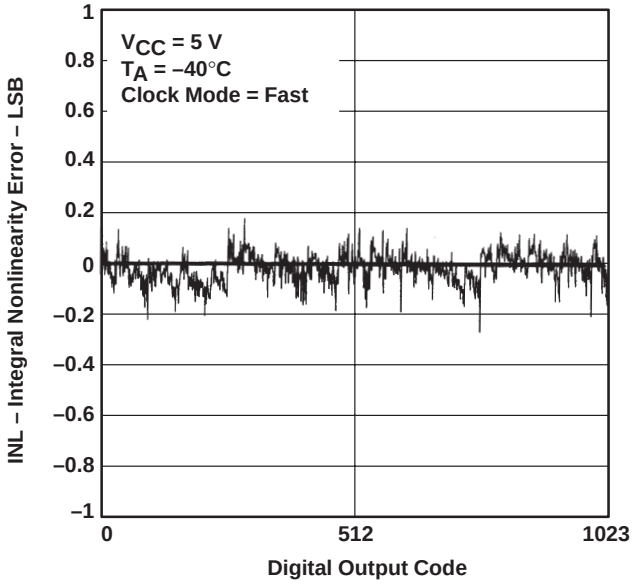



Figure 31

**DIFFERENTIAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE**

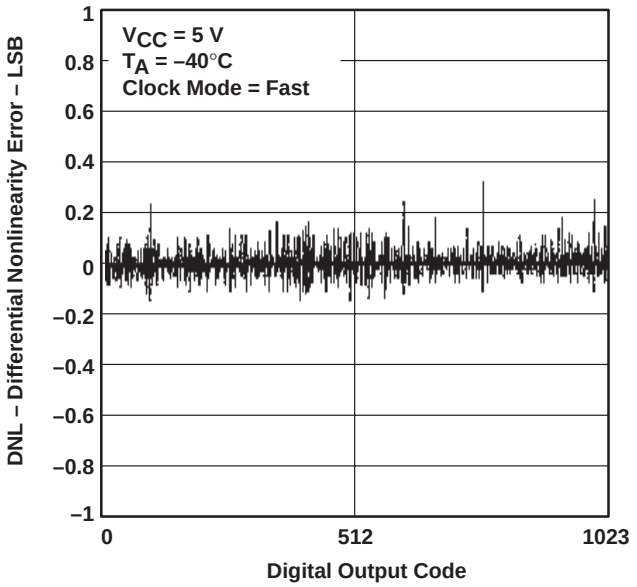



Figure 32

**INTEGRAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE**

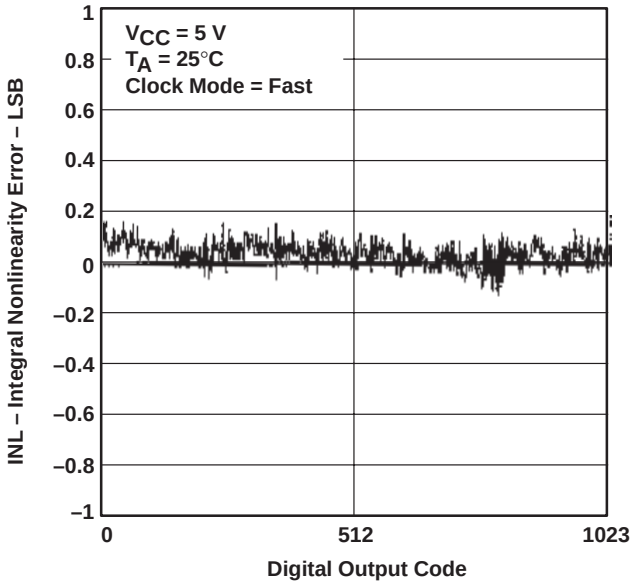



Figure 33

**DIFFERENTIAL NONLINEARITY ERROR vs DIGITAL OUTPUT CODE**

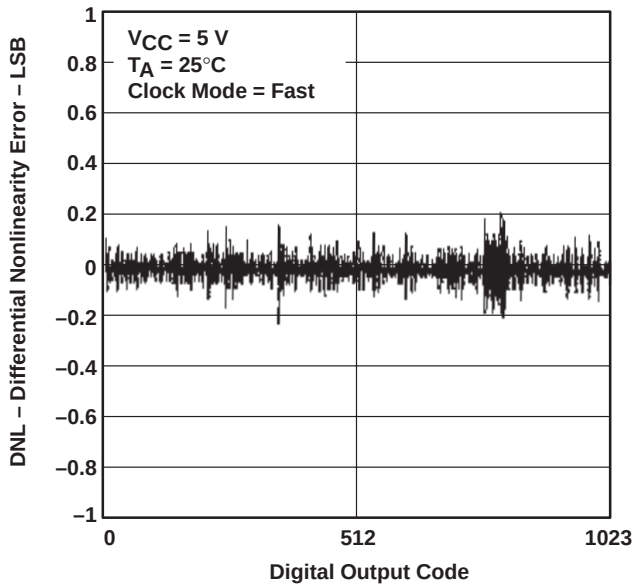



Figure 34

## TYPICAL CHARACTERISTICS

**INTEGRAL NONLINEARITY ERROR**
**vs**
**DIGITAL OUTPUT CODE**

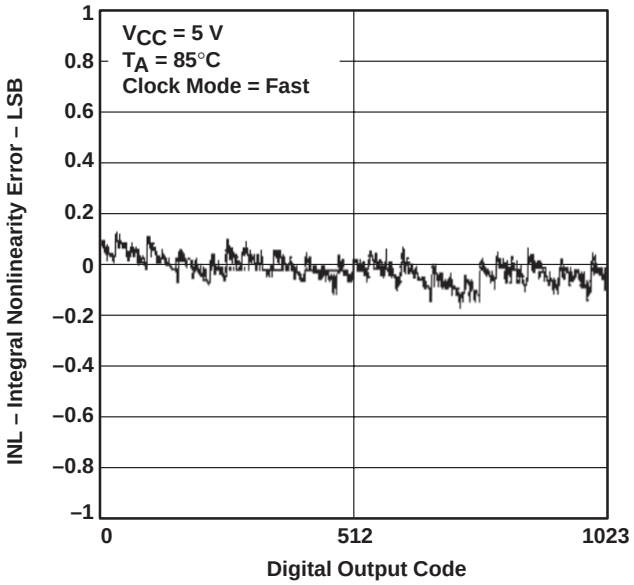



**Figure 35**

**DIFFERENTIAL NONLINEARITY ERROR**
**vs**
**DIGITAL OUTPUT CODE**

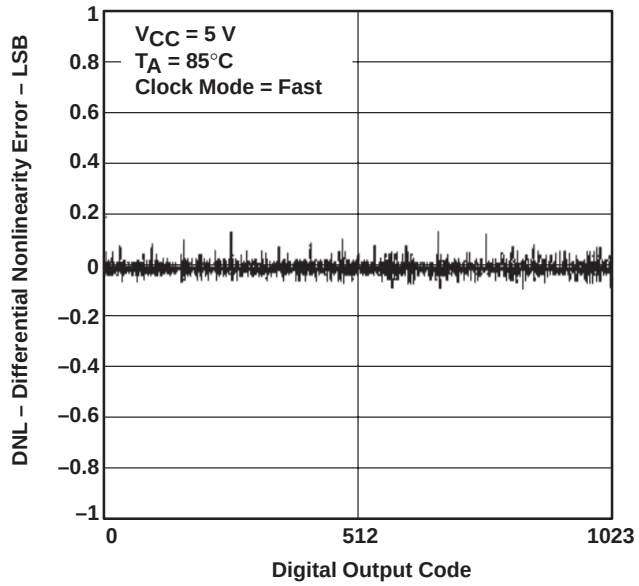
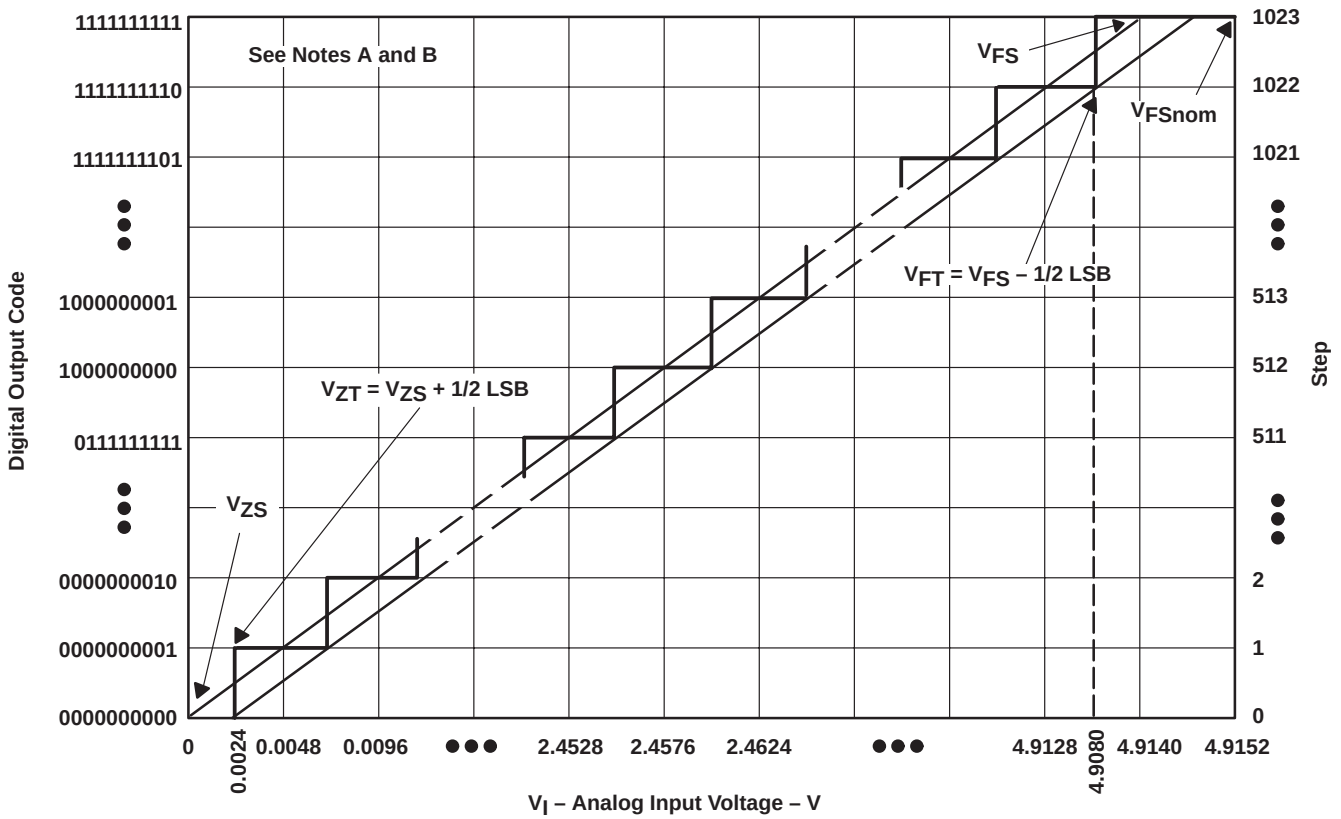



**Figure 36**

## APPLICATION INFORMATION

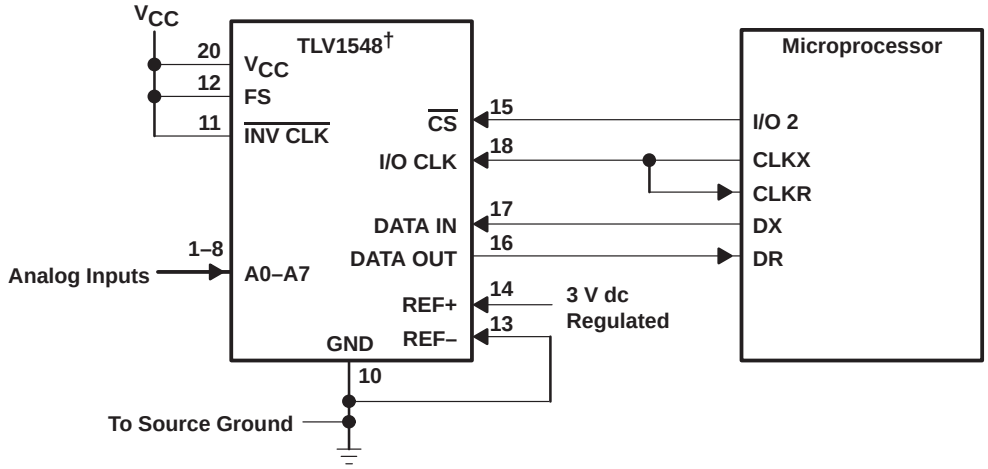



NOTES: A. This curve is based on the assumption that $V_{ref+}$ and $V_{ref-}$ have been adjusted so that the voltage at the transition from digital 0 to 1 ($V_{ZT}$) is 0.0024 V, and the transition to full scale ($V_{FT}$) is 4.908 V. 1 LSB = 4.8 mV.

B. The full-scale value ($V_{FS}$) is the step whose nominal midstep value has the highest absolute value. The zero-scale value ($V_{ZS}$) is the step whose nominal midstep value equals zero.

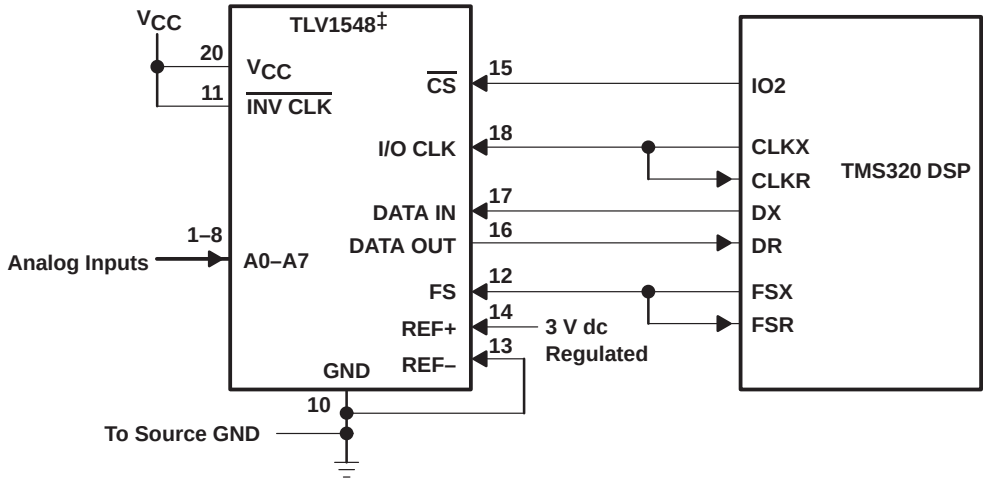
**Figure 37. Ideal Conversion Characteristics**

## APPLICATION INFORMATION




† DB package is shown for TLV1548

**Figure 38. Typical Interface to a Microprocessor**




‡ DB package is shown for TLV1548

**Figure 39. Typical Interface to a TMS320 DSP**

## APPLICATIONS INFORMATION

### simplified analog input analysis

Using the equivalent circuit in Figure 33, the time required to charge the analog input capacitance from 0 to $V_S$ within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by:

$$V_C = V_S\left(1-e^{-t_c/R_tC_i}\right) \quad (1)$$

where

$R_t = R_S + r_i$

$t_c$ = Cycle time

The input impedance $Z_i$ is 1 kΩ at 5 V, and is higher (~ 5 kΩ) at 2.7 V. The final voltage to 1/2 LSB is given by:

$$V_C\ (1/2\ LSB) = V_S - (V_S/2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for cycle time $t_c$ gives:

$$V_S - \left(V_S/2048\right) = V_S\left(1-e^{-t_c/R_tC_i}\right) \quad (3)$$

and time to change to 1/2 LSB (minimum sampling time) is:

$$t_{ch}\ (1/2\ LSB) = R_t \times C_i \times \ln(2048)$$

where

$\ln(2048) = 7.625$

Therefore, with the values given, the time for the analog input signal to settle is:

$$t_{ch}\ (1/2\ LSB) = (R_s + 1\ k\Omega) \times 55\ pF \times \ln(2048) \quad (4)$$

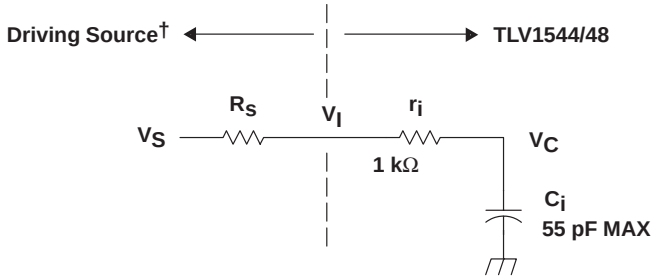
This time must be less than the converter sample time shown in the timing diagrams. Which is 6x I/O CLK.

$$t_{ch}\ (1/2\ LSB) \le 6x\ 1/f_{I/O} \quad (5)$$

Therefore the maximum I/O CLK frequency is:

$$max(f_{I/O}) = 6/t_{ch}\ (1/2\ LSB) = 6/(\ln(2048) \times R_t \times C_i) \quad (6)$$

## APPLICATIONS INFORMATION




$V_I$ = Input Voltage at AIN
$V_S$ = External Driving Source Voltage
$R_S$ = Source Resistance
$r_i$ = Input Resistance (MUX on Resistance)
$C_i$ = Input Capacitance
$V_C$ = Capacitance Charging Voltage

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- $R_S$ must be real at the input frequency.

**Figure 40. Equivalent Input Circuit Including the Driving Source**

### maximum conversion throughput

For a supply voltage at 5 V, if the source impedance is less than 1 kΩ, this equates to a minimum sampling time $t_{ch}$(0.5 LSB) of 0.84 μs. Since the sampling time requires six I/O clocks, the fastest I/O clockfrequency is $6/t_{ch}$ = 7.18 MHz. The minimal total cycle time is given as:

$$t_c = t_{address} + t_{sample} + t_{conv} + t_{d(EOC\uparrow - CS\downarrow)}$$
$$= 0.56\ \mu s + 0.84\ \mu s + 10\ \mu s + 0.1\ \mu s$$
$$= 11.5\ \mu s$$

A maximum throughput of 87 KSPS. The throughput can be even higher with a smaller source impedance.

When source impedance is 100Ω, the minimum sampling time is 0.46 μs. The maximum I/O clock frequency possible is almost 13 MHz. Then 10 MHz clock (maximum I/O CLK for TLV1544/1548) can be used. The minimal total cycle time is:

$$t_c = t_{address} + t_{sample} + t_{conv} + t_{d(EOC\uparrow - CS\downarrow)}$$
$$= 4 \times 1/f + 0.46\ \mu s + 10\ \mu s + 0.1\ \mu s$$
$$= 0.4\ \mu s + 0.46\ \mu s + 10\ \mu s + 0.1\ \mu s$$
$$= 10.96\ \mu s$$

The maximum throughput is 1/10.96 μs = 91 KSPS for this case.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9853801Q2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9853801Q2A TLV1548 MFKB |
| 5962-9853801QRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9853801QRA TLV1548MJB |
| TLV1544CD | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV1544C |
| TLV1544CD.A | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV1544C |
| TLV1544CDR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TLV1544C |
| TLV1544CDR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV1544C |
| TLV1544CPW | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TV1544 |
| TLV1544CPW.A | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV1544 |
| TLV1544CPWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TV1544 |
| TLV1544CPWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV1544 |
| TLV1544ID | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TLV1544I |
| TLV1544ID.A | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV1544I |
| TLV1544IDR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TLV1544I |
| TLV1544IDR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV1544I |
| TLV1544IPW | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TY1544 |
| TLV1544IPW.A | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TY1544 |
| TLV1544IPWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TY1544 |
| TLV1544IPWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TY1544 |
| TLV1548CDB | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV1548 |
| TLV1548CDB.A | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV1548 |
| TLV1548CDBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TV1548 |
| TLV1548CDBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV1548 |
| TLV1548IDB | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TY1548 |
| TLV1548IDB.A | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TY1548 |
| TLV1548IDBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TY1548 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV1548IDBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TY1548 |
| TLV1548MFKB | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9853801Q2A TLV1548 MFKB |
| TLV1548MFKB.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9853801Q2A TLV1548 MFKB |
| TLV1548MJB | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9853801QRA TLV1548MJB |
| TLV1548MJB.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9853801QRA TLV1548MJB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV1548, TLV1548M :**

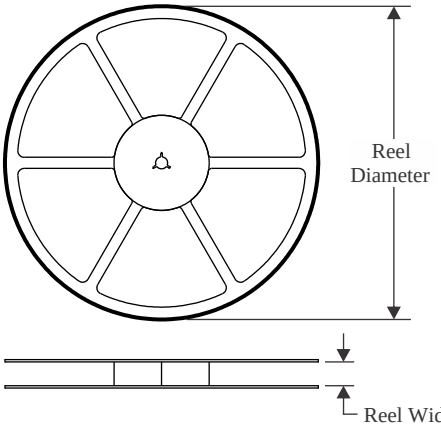
- Catalog : TLV1548
- Automotive : TLV1548-Q1, TLV1548-Q1
- Enhanced Product : TLV1548-EP, TLV1548-EP
- Military : TLV1548M

NOTE: Qualified Version Definitions:

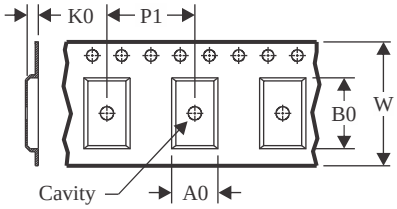
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

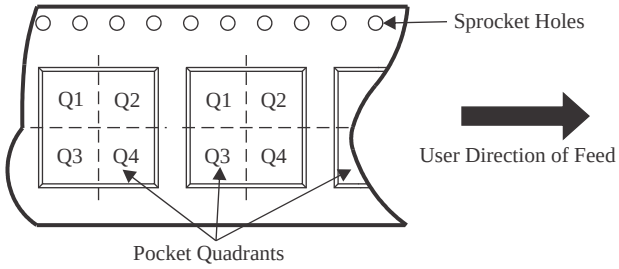



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

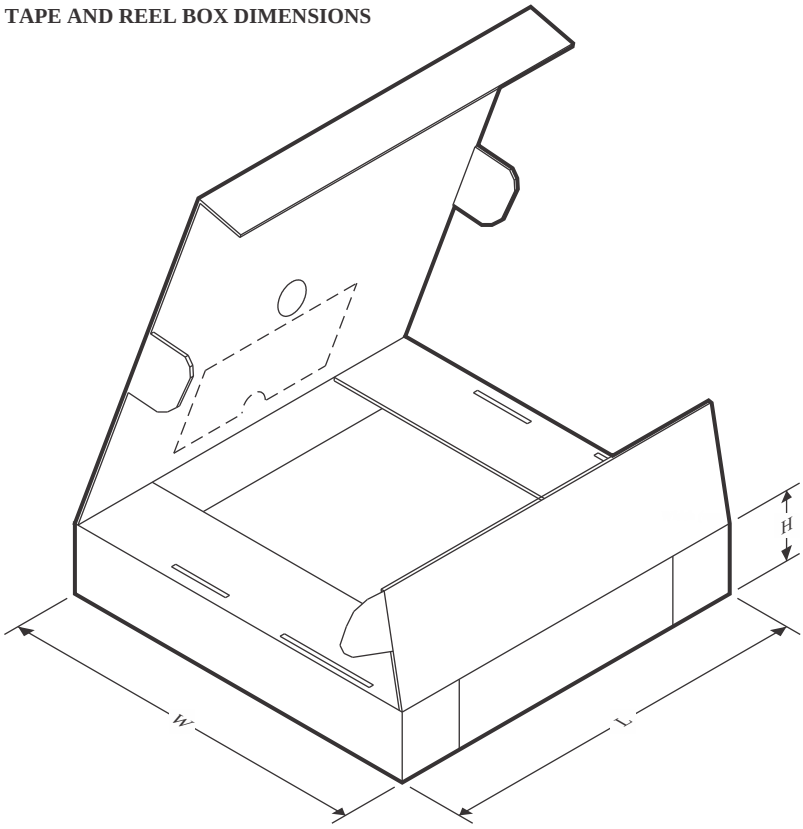
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV1544CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV1544CPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV1544IDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV1544IPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV1548CDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TLV1548IDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |

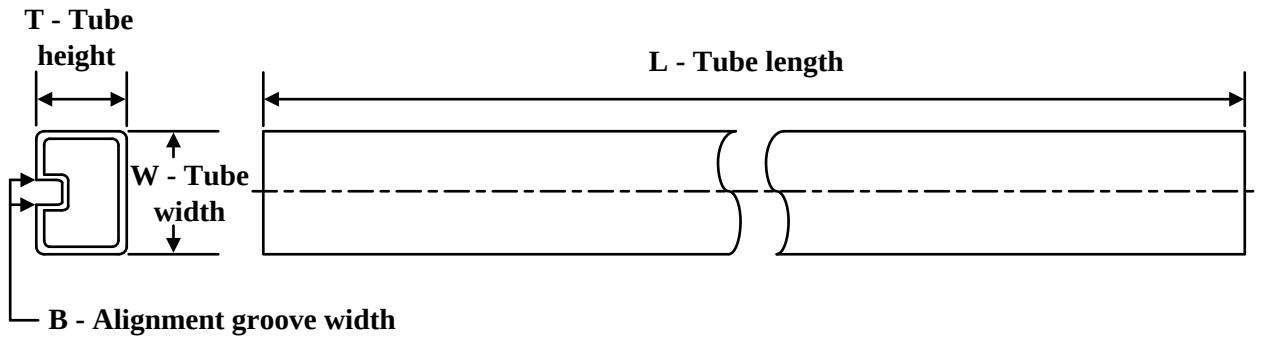
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV1544CDR | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| TLV1544CPWR | TSSOP | PW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| TLV1544IDR | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| TLV1544IPWR | TSSOP | PW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| TLV1548CDBR | SSOP | DB | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TLV1548IDBR | SSOP | DB | 20 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9853801Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TLV1544CD | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| TLV1544CD.A | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| TLV1544CPW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TLV1544CPW.A | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TLV1544ID | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| TLV1544ID.A | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| TLV1544IPW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TLV1544IPW.A | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TLV1548CDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV1548CDB.A | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV1548IDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV1548IDB.A | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV1548MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TLV1548MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

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