

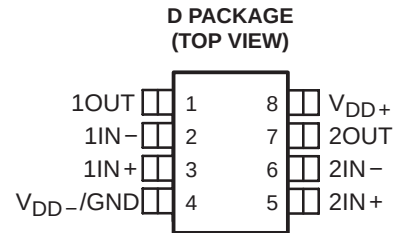
TLV2422-Q1, TLV2422A-Q1

Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT

WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS

SGLS175A – AUGUST 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Output Swing Includes Both Supply Rails
- Extended Common-Mode Input Voltage Range . . . 0 V to 4.5 V (Min) With 5-V Single Supply
- No Phase Inversion
- Low Noise . . . 18 nV/√Hz Typ at f = 1 kHz
- Low Input Offset Voltage
950 μV Max at T_A = 25°C (TLV2422A)
- Low Input Bias Current . . . 1 pA Typ
- Micropower Operation . . . 50 μA Per Channel
- 600-Ω Output Drive



description

The TLV2422 and TLV2422A are dual low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range for this device has been extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, the devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. The TLV2422 only requires 50 μA of supply current per channel, making it ideal for battery-powered applications. The TLV2422 also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecom applications.

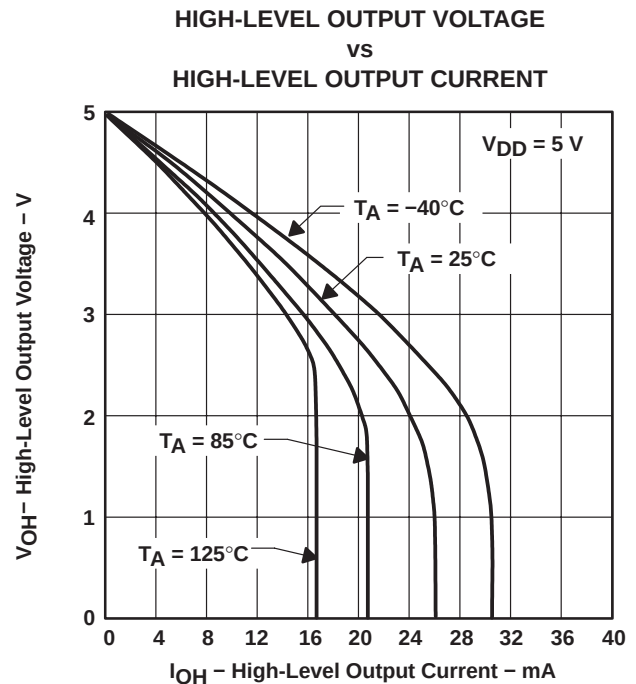


Figure 1

Other members in the TLV2422 family are the high-power, TLV2442, and low-power, TLV2432, versions.

The TLV2422, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV2422A is available with a maximum input offset voltage of 950 μV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.



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ORDERING INFORMATION†

T _A	V _{IO} max AT 25°C	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	950 µV	SOIC (D)	Tape and reel	TLV2422AQDRQ1	2422AQ
	2.5 mV	SOIC (D)	Tape and reel	TLV2422QDRQ1	2422Q1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

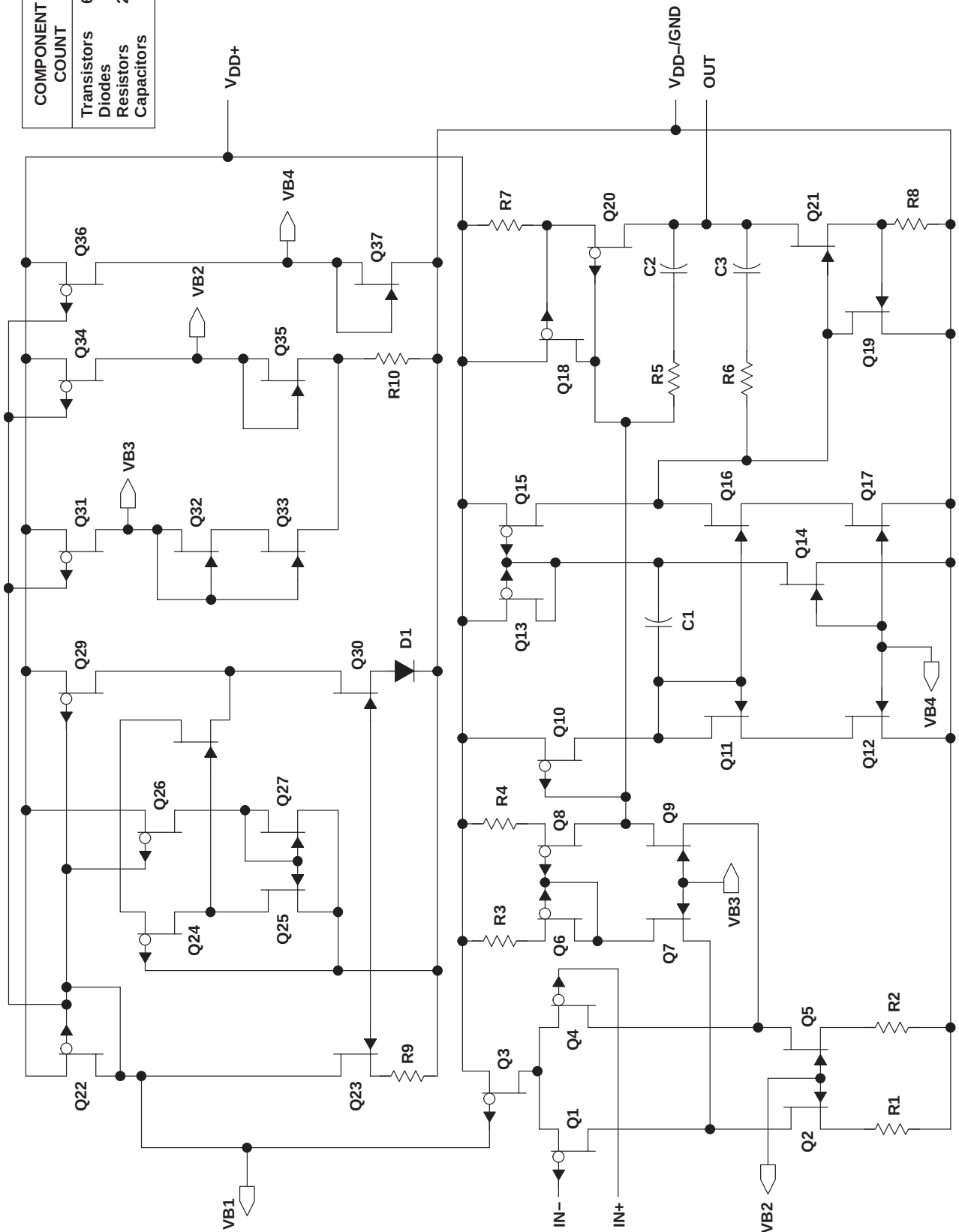


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equivalent schematic (each amplifier)

COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage, V_I (any input, see Note 1): C and I suffix	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : Q suffix	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 0.8$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 0.8$	V
Operating free-air temperature, T_A	-40	125	°C

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2422-Q1			TLV2422A-Q1			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
V _{IO}	Input offset voltage	V _{IC} = 0, V _O = 0, V _{DD} ± = ±1.5 V, R _S = 50 Ω		25°C		300	2000		300	950	μV	
				Full range			2500			1800		
α _{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C	
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo	
I _{IO}	Input offset current			25°C		0.5	60		0.5	60	pA	
				Full range			150			150		
I _{IB}	Input bias current			25°C		1	60		1	60	pA	
				Full range			300			300		
V _{ICR}	Common-mode input voltage range			V _{IO} ≤ 5 mV, R _S = 50 Ω		25°C	0 to 2.5	−0.25 to 2.75		0 to 2.5	−0.25 to 2.75	V
						Full range	0 to 2.2			0 to 2.2		
V _{OH}	High-level output voltage	I _{OH} = −100 μA		25°C	2.97			2.97		V		
				25°C	2.75			2.75				
				Full range	2.5			2.5				
V _{OL}	Low-level output voltage	V _{IC} = 0, I _{OL} = 100 μA		25°C	0.05			0.05		V		
				25°C	0.2			0.2				
				Full range	0.5			0.5				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 1.5 V, V _O = 1 V to 2 V	R _L = 10 kΩ [‡]	25°C	6	10		6	10	V/mV		
				Full range	2			2				
				25°C	700			700				
r _{i(d)}	Differential input resistance			25°C	10 ¹²			10 ¹²		Ω		
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²			10 ¹²		Ω		
c _{i(c)}	Common-mode input capacitance	f = 10 kHz		25°C	8			8		pF		
z _o	Closed-loop output impedance	f = 100 kHz, A _V = 10		25°C	130			130		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, V _O = 1.5 V, R _S = 50 Ω		25°C	70	83		70	83	dB		
				Full range	70			70				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 2.7 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB		
				Full range	80			80				
I _{DD}	Supply current	V _O = 1.5 V, No load		25°C	100 150			100 150		μA		
				Full range	175			175				

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLV2422-Q1, TLV2422A-Q1			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.1\text{ V to }1.9\text{ V},$ $C_L = 100\text{ pF}^\ddagger$	$R_L = 10\text{ k}\Omega^\ddagger,$	25°C	0.01	0.02		V/ μs
				Full range	0.008			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		100		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		2.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 1\text{ kHz},$ $R_L = 10\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.25%		
			$A_V = 10$			1.8%		
	Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}^\ddagger$	$R_L = 10\text{ k}\Omega^\ddagger,$	25°C		46		kHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 1\text{ V},$ $R_L = 10\text{ k}\Omega^\ddagger,$	$A_V = 1,$ $C_L = 100\text{ pF}^\ddagger$	25°C		8.3		kHz
t_s	Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V, $R_L = 10\text{ k}\Omega^\ddagger,$ $C_L = 100\text{ pF}^\ddagger$	$T_o = 0.1\%$	25°C		8.6		μs
			$T_o = 0.01\%$			16		
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega^\ddagger,$	$C_L = 100\text{ pF}^\ddagger$	25°C		62°		
	Gain margin			25°C		11		dB

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 1.5 V



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2422-Q1			TLV2422A-Q1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = 0, V _O = 0, V _{DD} ± = ±2.5 V, R _S = 50 Ω		25°C		300	2000		300	950	μV
				Full range			2500			1800	
α _{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I _{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			150			150	
I _{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			300			300	
V _{ICR}	Common-mode input voltage range	V _{IO} ≤ 5 mV, R _S = 50 Ω		25°C	0 to 4.5	−0.25 to 4.75		0 to 4.5	−0.25 to 4.75	V	
				Full range	0 to 4.2			0 to 4.2			
V _{OH}	High-level output voltage	I _{OH} = −100 μA I _{OH} = −1 mA		25°C	4.97			4.97		V	
				25°C	4.75			4.75			
				Full range	4.5			4.5			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 100 μA		25°C	0.04			0.04		V	
		V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	0.15			0.15			
				Full range	0.5			0.5			
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V	R _L = 10 kΩ‡	25°C	8	12		8	12	V/mV	
				Full range	3			3			
			R _L = 1 MΩ‡	25°C	1000			1000			
r _{i(d)}	Differential input resistance			25°C	10 ¹²			10 ¹²		Ω	
r _{i(c)}	Common-mode input resistance			25°C	10 ¹²			10 ¹²		Ω	
c _{i(c)}	Common-mode input capacitance	f = 10 kHz		25°C	8			8		pF	
z _o	Closed-loop output impedance	f = 100 kHz, A _V = 10		25°C	130			130		Ω	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min, V _O = 2.5 V, R _S = 50 Ω		25°C	70	90		70	90	dB	
				Full range	70			70			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 4.4 V to 8 V, V _{IC} = V _{DD} /2, No load		25°C	80	95		80	95	dB	
				Full range	80			80			
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	100	150		100	150	μA	
				Full range		175			175		

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLV2422-Q1, TLV2422A-Q1			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 1.5 V to 3.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	0.01	0.02	V/μs	
				Full range	0.008			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	100		nV/√Hz	
		f = 1 kHz		25°C	18			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	1.9		μV	
		f = 0.1 Hz to 10 Hz		25°C	2.8			
I _n	Equivalent input noise current			25°C	0.6		fA√Hz	
THD + N	Total harmonic distortion plus noise	V _O = 1.5 V to 3.5 V, f = 1 kHz, R _L = 10 kΩ [‡]	A _V = 1	25°C	0.24%			
			A _V = 10		1.7%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF [‡]	R _L =10 kΩ [‡] ,	25°C	52		kHz	
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 2 V, R _L = 10 kΩ [‡] ,	A _V = 1, C _L = 100 pF [‡]	25°C	5.3		kHz	
t _s	Settling time	A _V = −1, Step = 1.5 V to 3.5 V, R _L = 10 kΩ [‡] , C _L = 100 pF [‡]	To 0.1%	25°C	8.5		μs	
			To 0.01%		15.5			
φ _m	Phase margin at unity gain	R _L = 10 kΩ [‡] , C _L = 100 pF [‡]		25°C	66°			
	Gain margin			25°C	11		dB	

† Full range is -40°C to 125°C for Q level part.

‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	2,3 4,5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6,7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_{OH}	High-level output voltage	vs High-level output current	9,11
V_{OL}	Low-level output voltage	vs Low-level output current	10,12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	14 15
V_{ID}	Differential input voltage	vs Output voltage	16,17
	Differential gain	vs Load resistance	18
A_{VD}	Large-signal differential voltage amplification Differential voltage amplification	vs Frequency vs Free-air temperature	19,20 21,22
z_o	Output impedance	vs Frequency	23,24
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	25 26
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	27,28 29
I_{DD}	Supply current	vs Supply voltage	30
SR	Slew rate	vs Load capacitance vs Free-air temperature	31 32
V_O	Inverting large-signal pulse response		33,34
V_O	Voltage-follower large-signal pulse response		35,36
V_O	Inverting small-signal pulse response		37,38
V_O	Voltage-follower small-signal pulse response		39,40
V_n	Equivalent input noise voltage	vs Frequency	41, 42
	Noise voltage (referred to input)	Over a 10-second period	43
THD + N	Total harmonic distortion plus noise	vs Frequency	44,45
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	46 47
ϕ_m	Phase margin	vs Frequency vs Load capacitance	19,20 48
	Gain margin	vs Load capacitance	49
B_1	Unity-gain bandwidth	vs Load capacitance	50

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2422
INPUT OFFSET VOLTAGE**

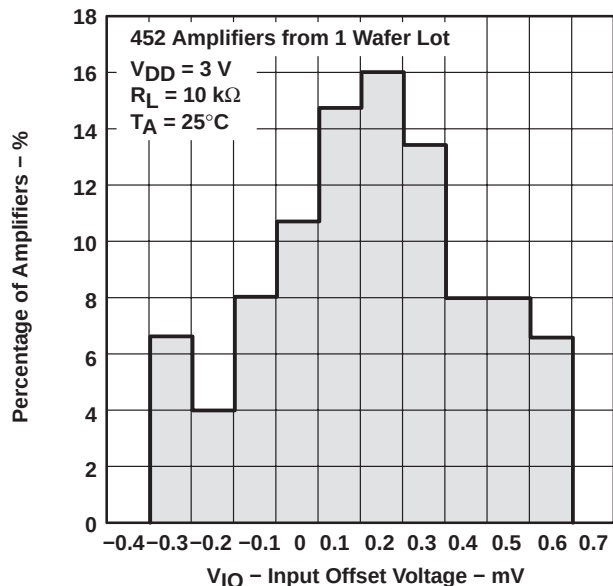


Figure 2

**DISTRIBUTION OF TLV2422
INPUT OFFSET VOLTAGE**

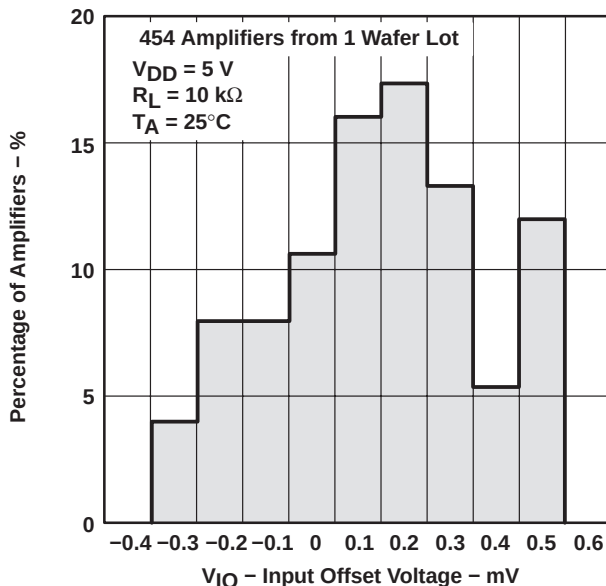


Figure 3

**INPUT OFFSET VOLTAGE
VS
COMMON-MODE INPUT VOLTAGE**

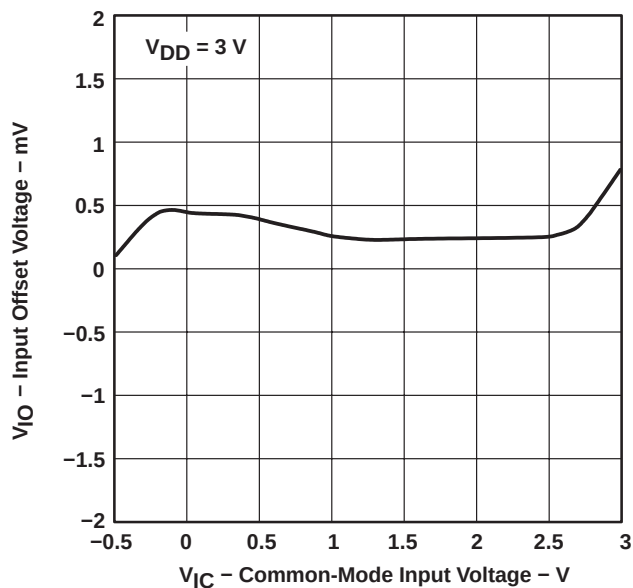


Figure 4

**INPUT OFFSET VOLTAGE
VS
COMMON-MODE INPUT VOLTAGE**

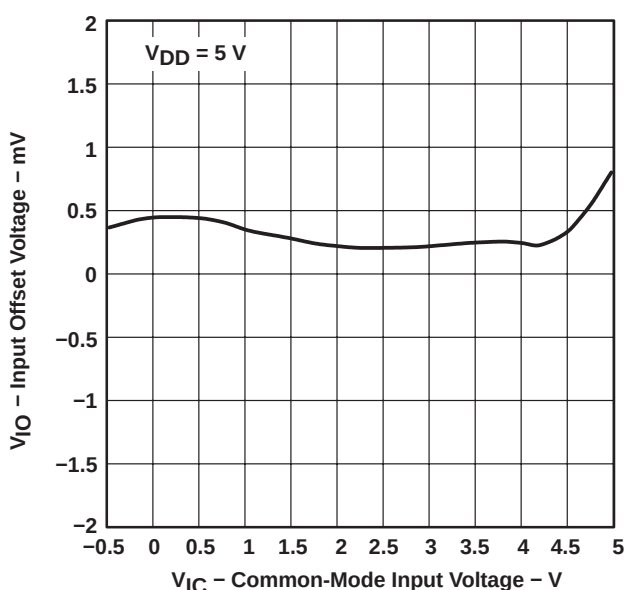


Figure 5

TYPICAL CHARACTERISTICS

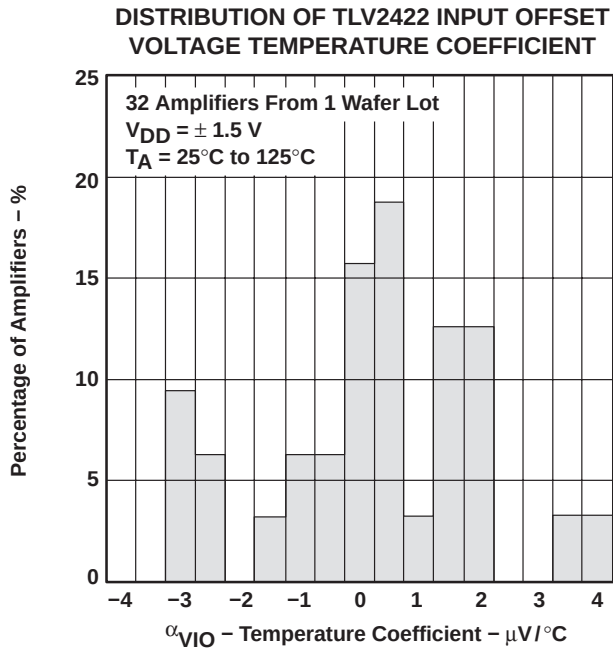


Figure 6

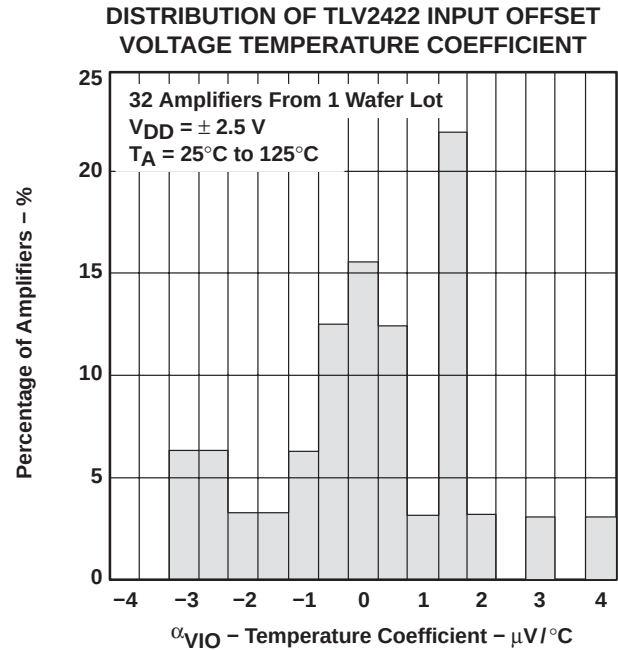


Figure 7

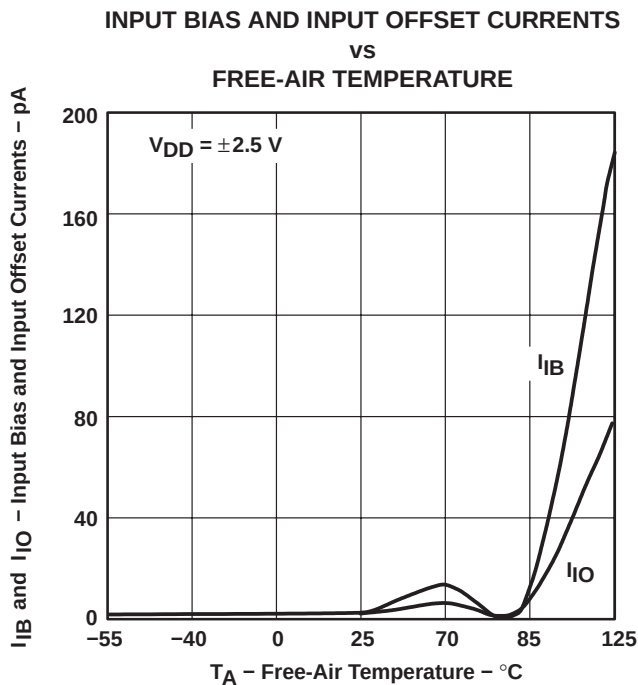


Figure 8

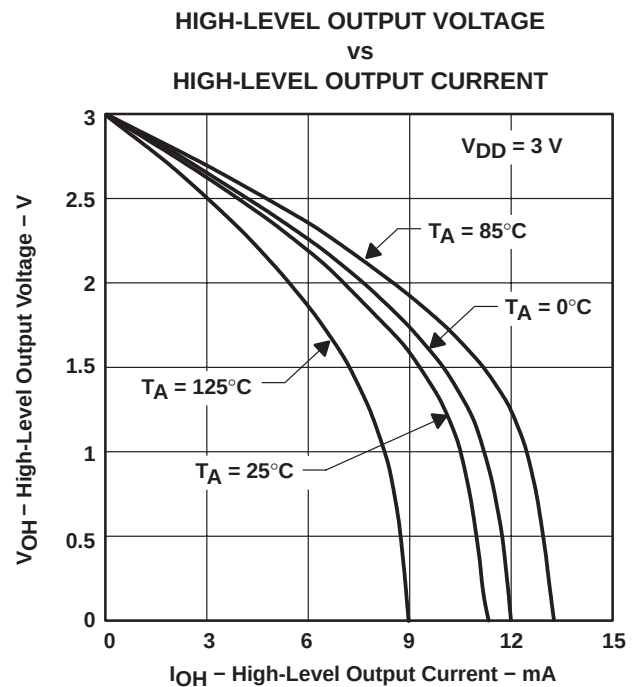


Figure 9

TYPICAL CHARACTERISTICS

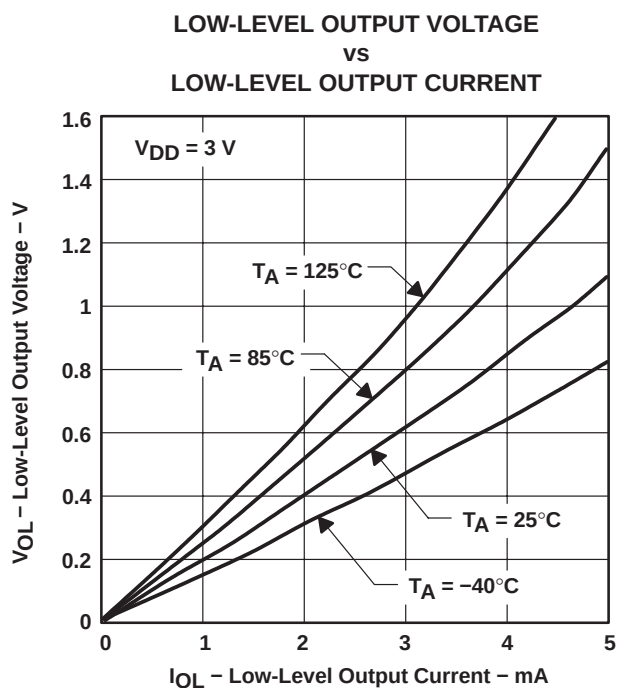


Figure 10

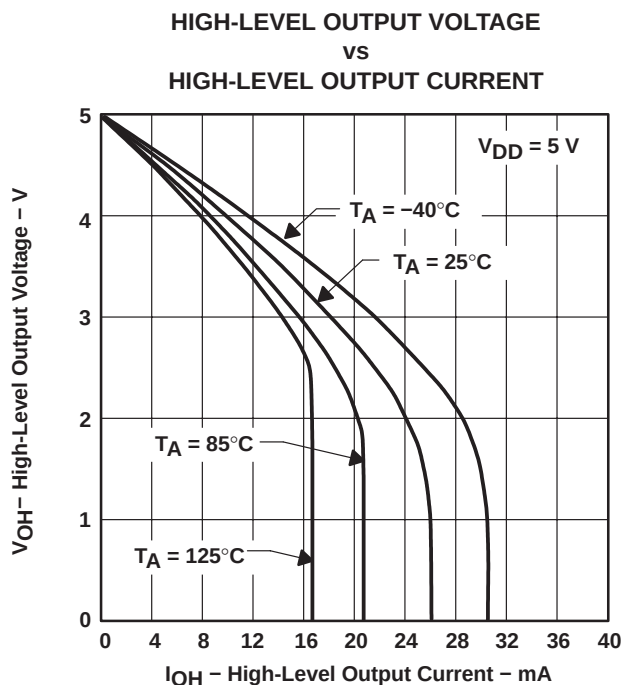


Figure 11

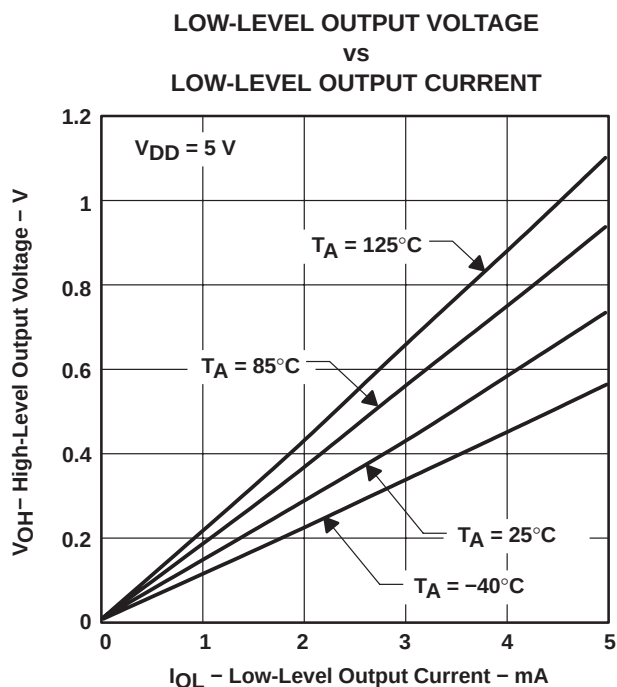


Figure 12

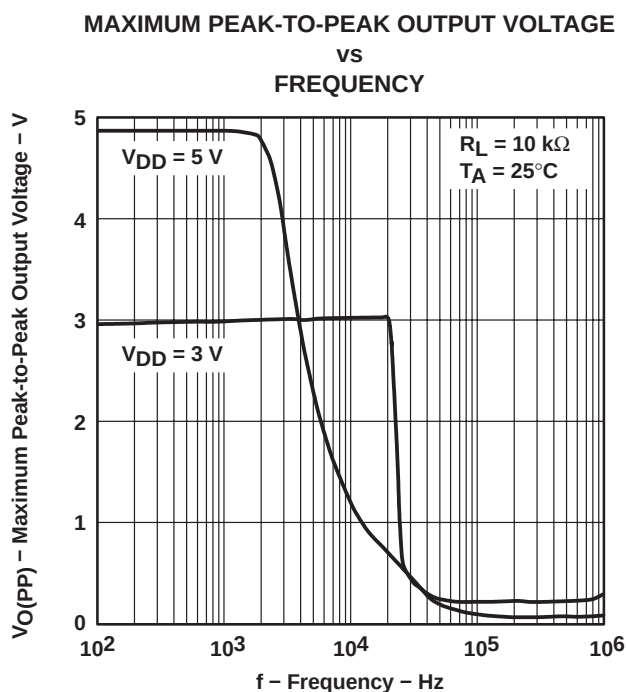
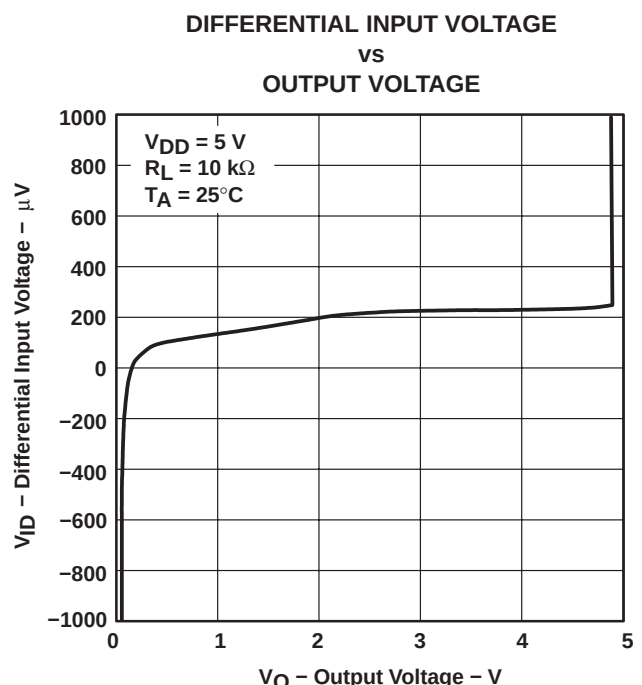
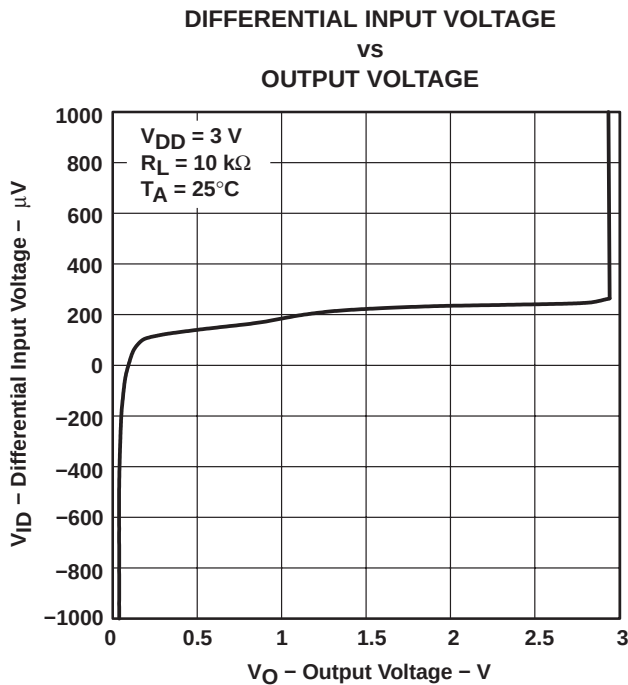
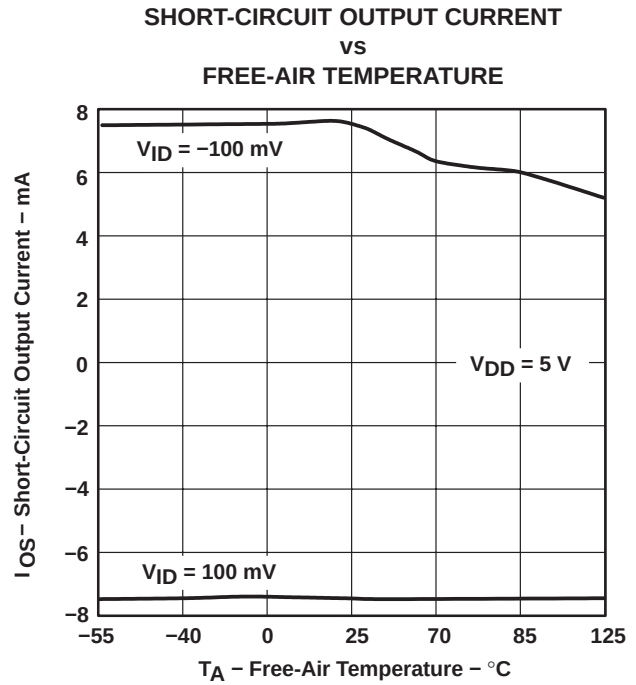
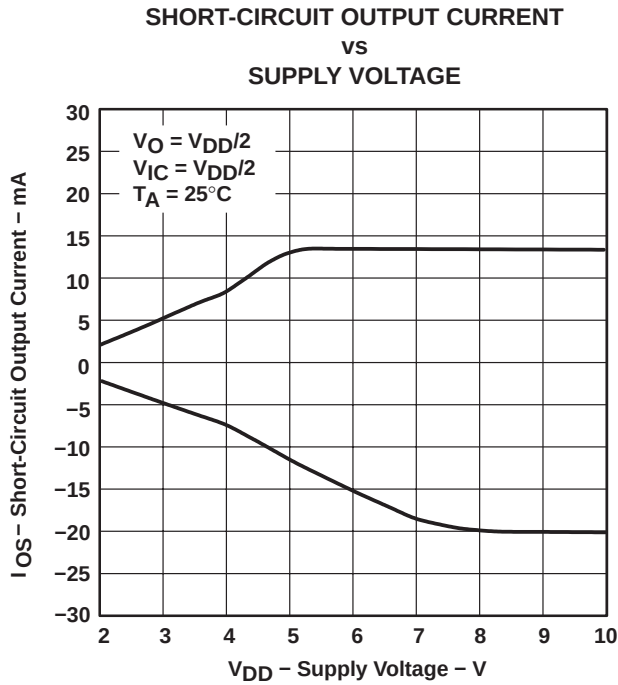


Figure 13

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

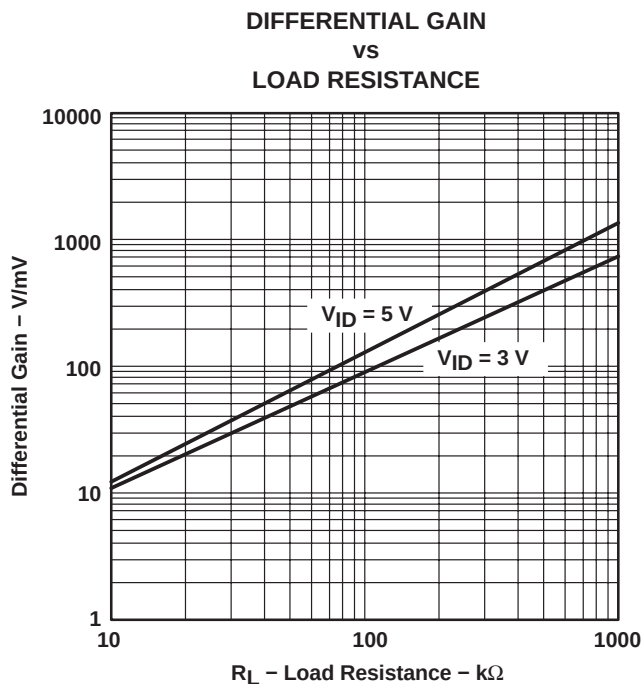


Figure 18

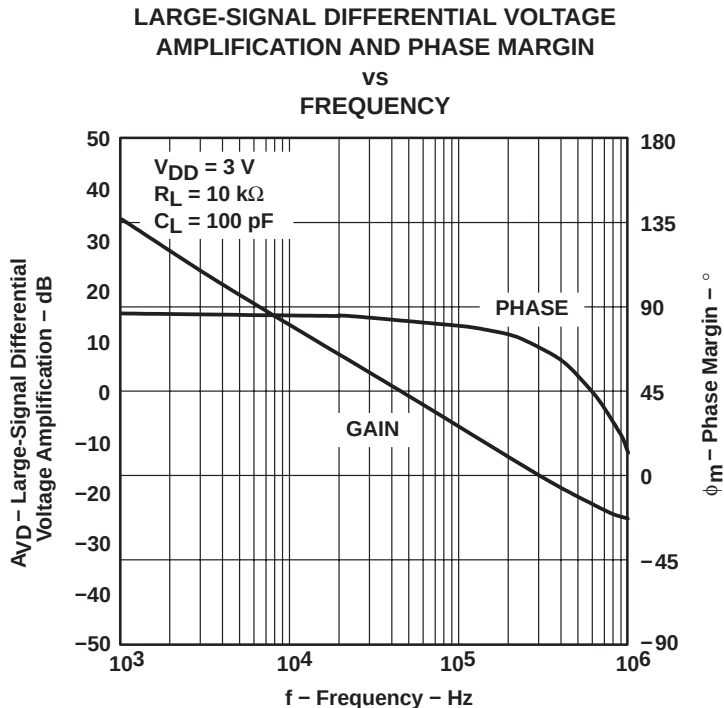


Figure 19

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

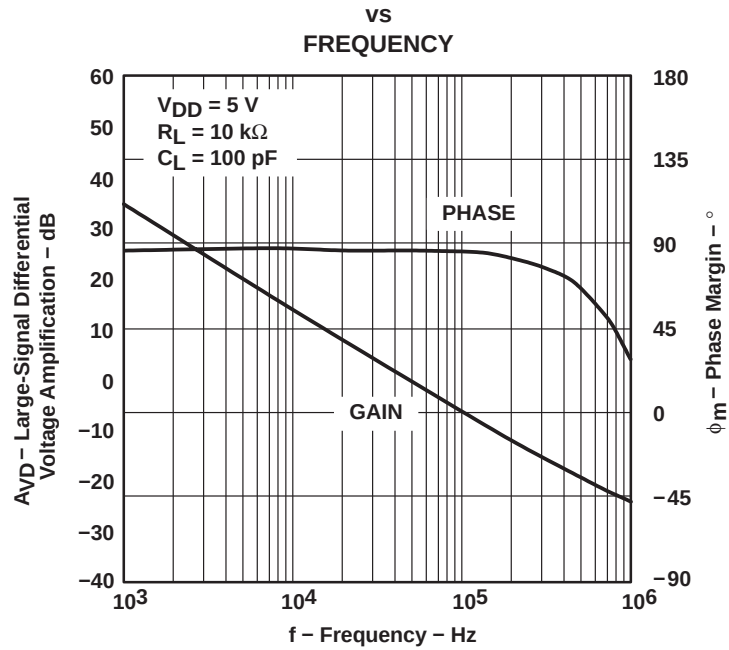


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

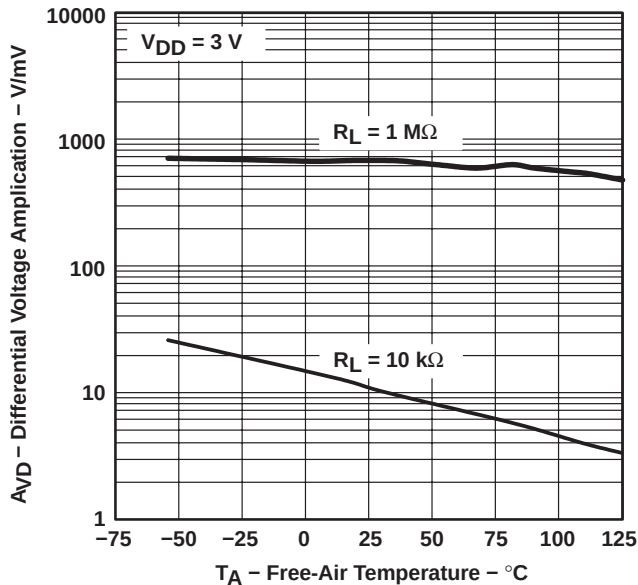


Figure 21

DIFFERENTIAL VOLTAGE AMPLIFICATION VS FREE-AIR TEMPERATURE

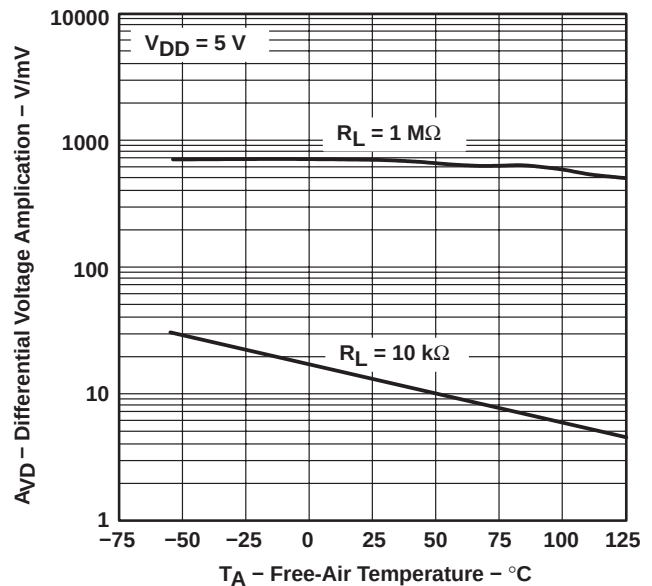


Figure 22

TYPICAL CHARACTERISTICS

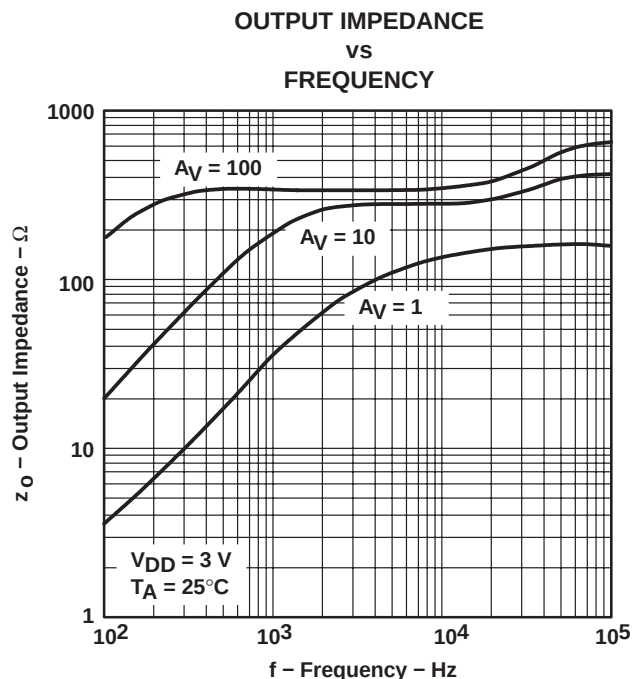


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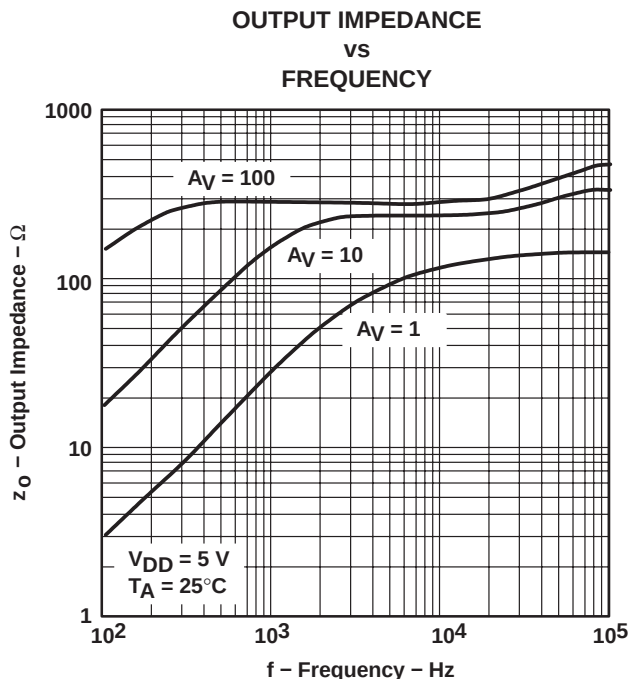


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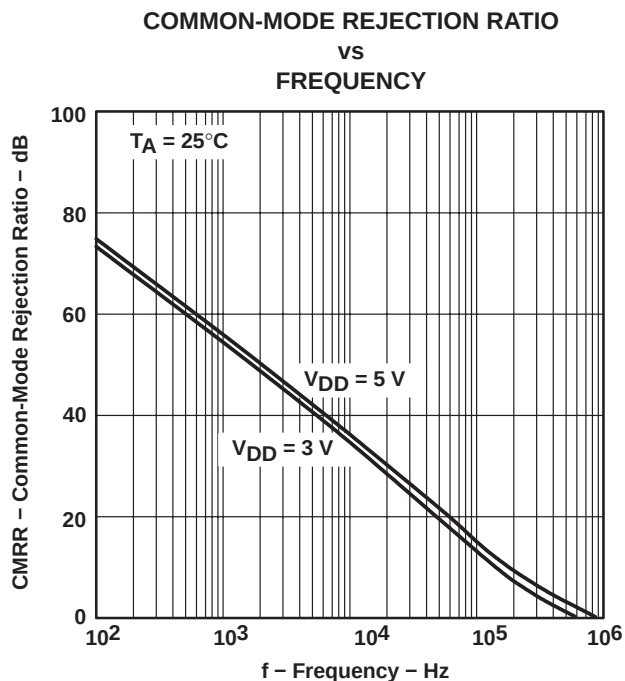


Figure 25

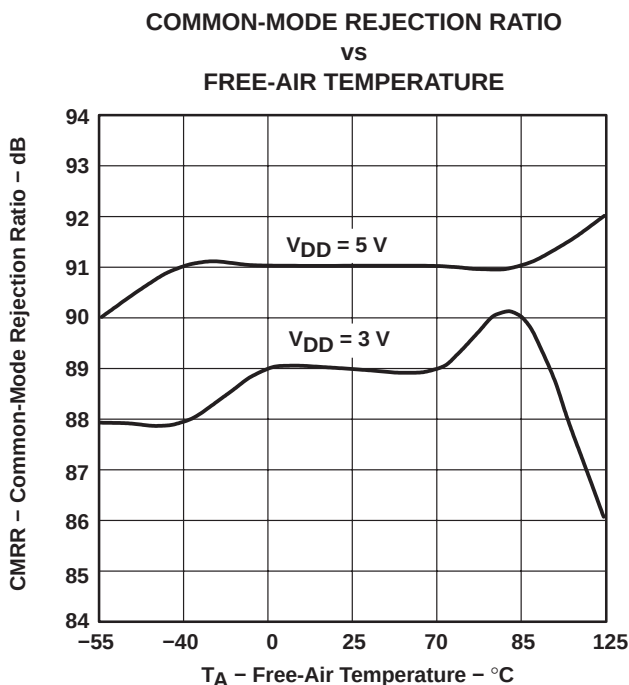


Figure 26

TYPICAL CHARACTERISTICS

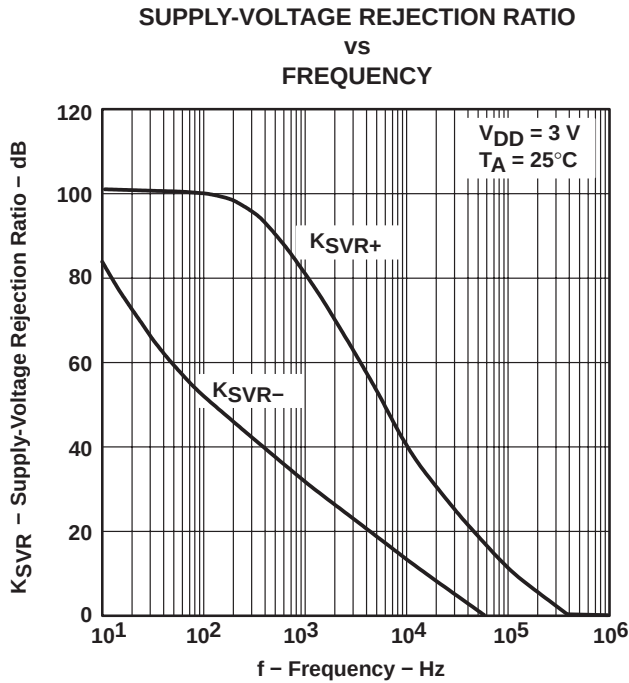


Figure 27

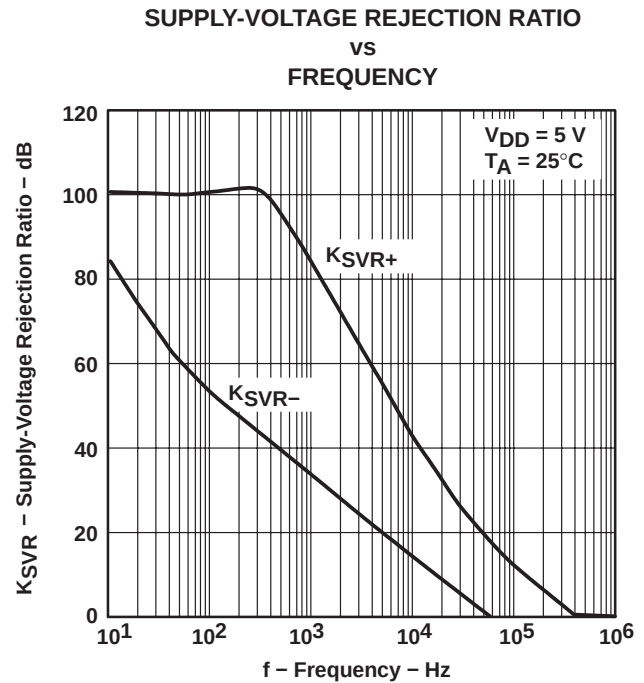


Figure 28

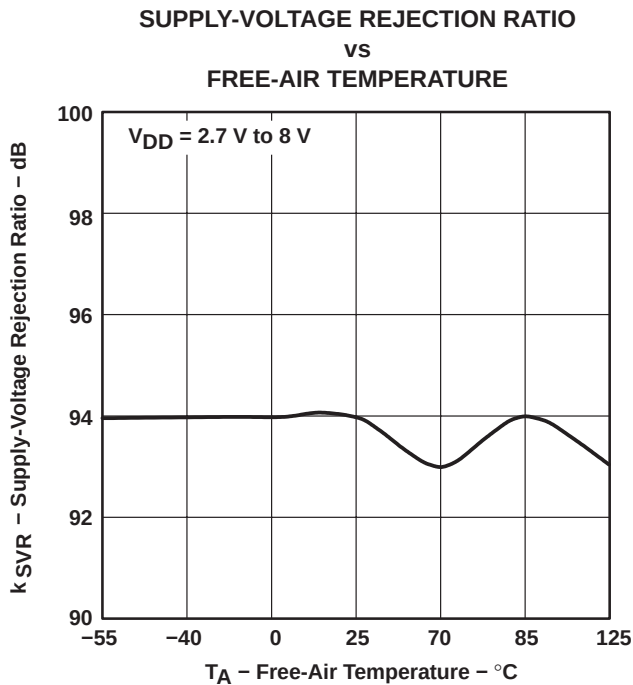


Figure 29

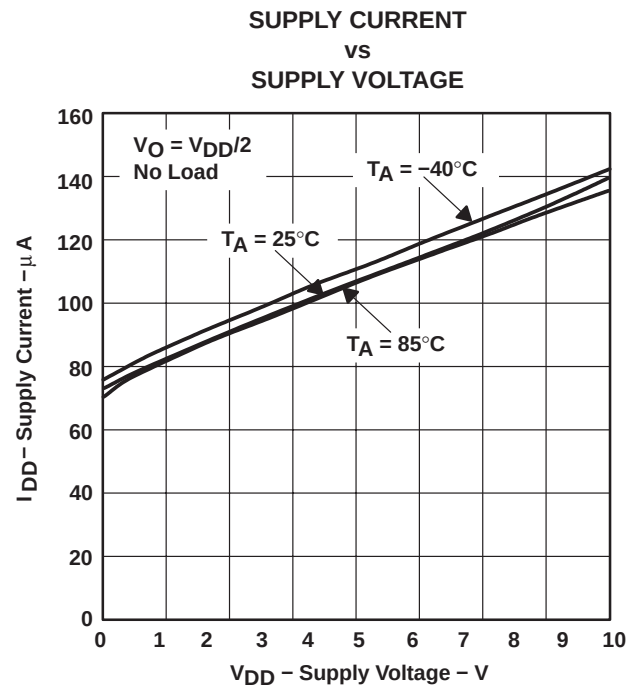


Figure 30

TYPICAL CHARACTERISTICS

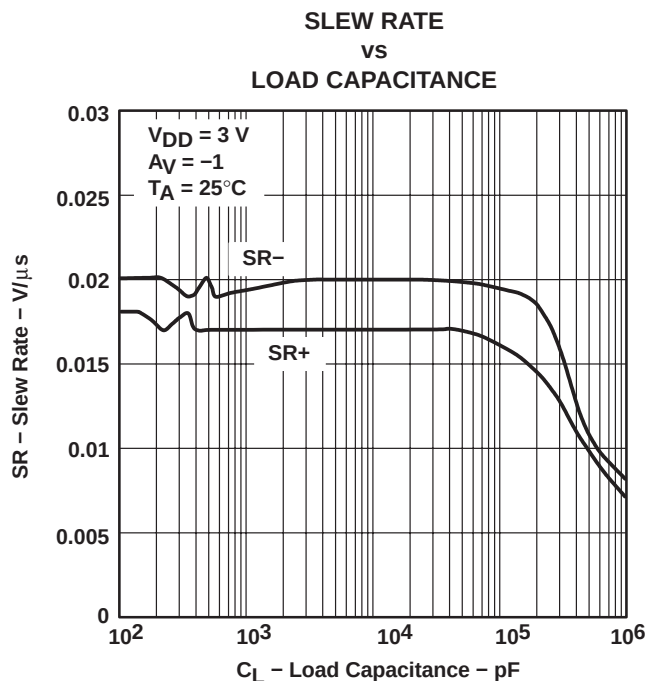


Figure 31

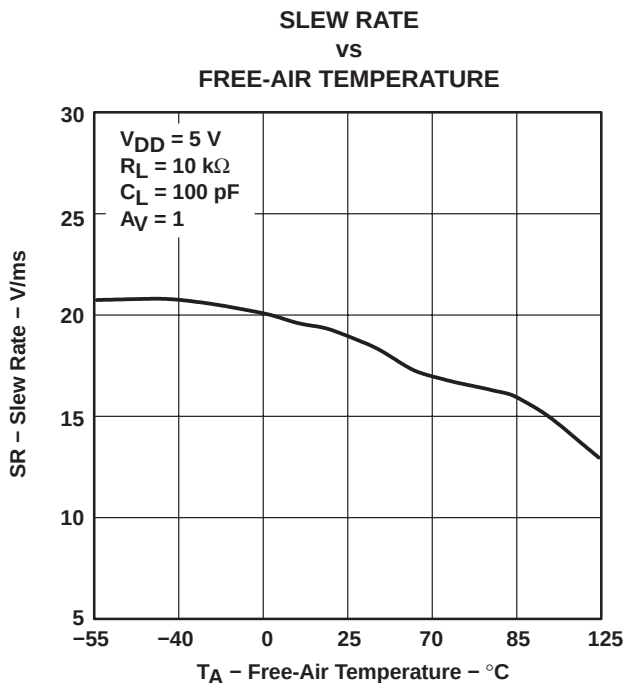


Figure 32

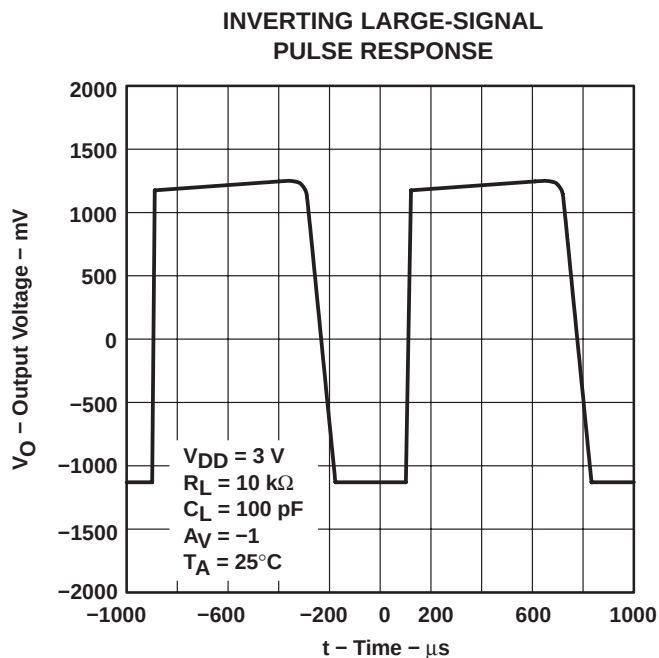


Figure 33

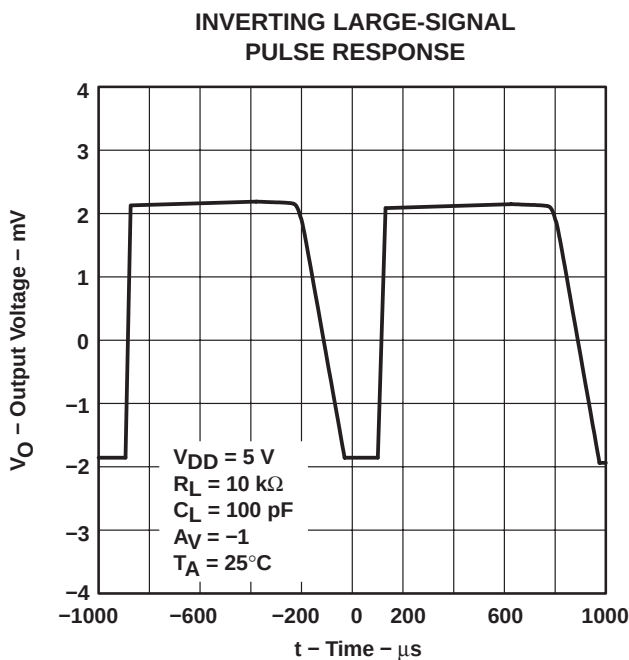


Figure 34

TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE**

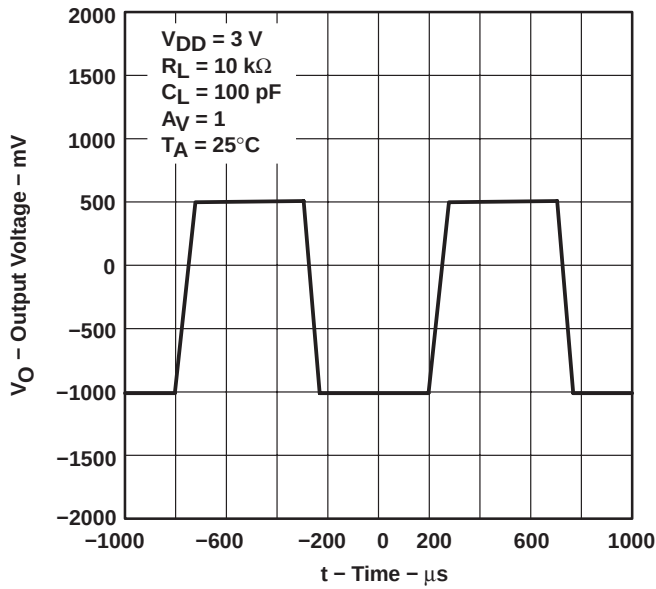


Figure 35

**VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE**

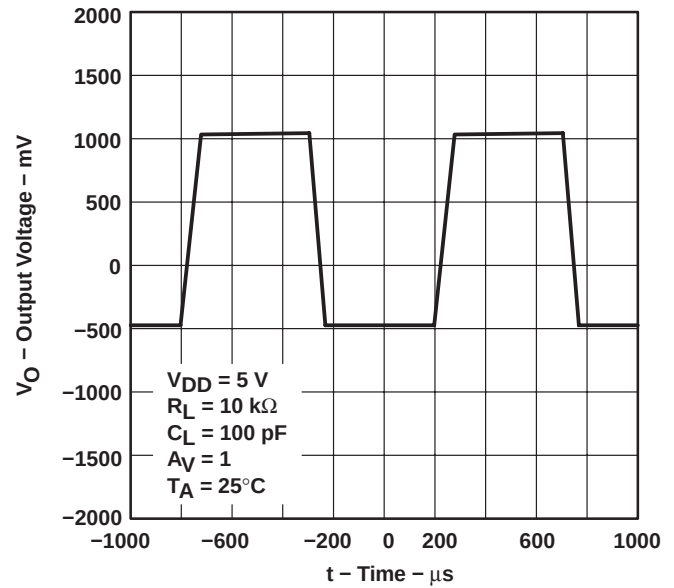


Figure 36

**INVERTING SMALL-SIGNAL
PULSE RESPONSE**

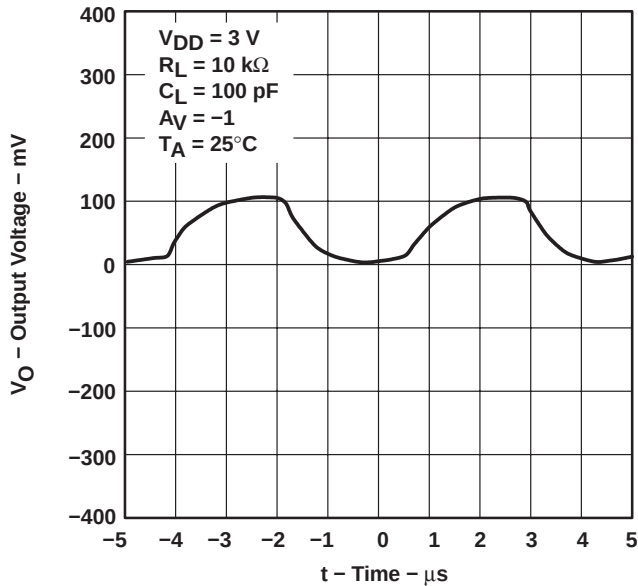


Figure 37

**INVERTING SMALL-SIGNAL
PULSE RESPONSE**

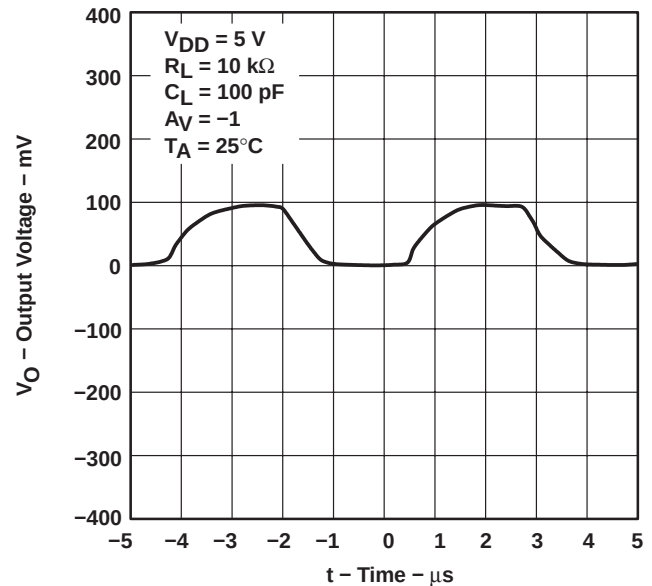


Figure 38

TLV2422-Q1, TLV2422A-Q1

Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT

WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS

SGLS175 – AUGUST 2003

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

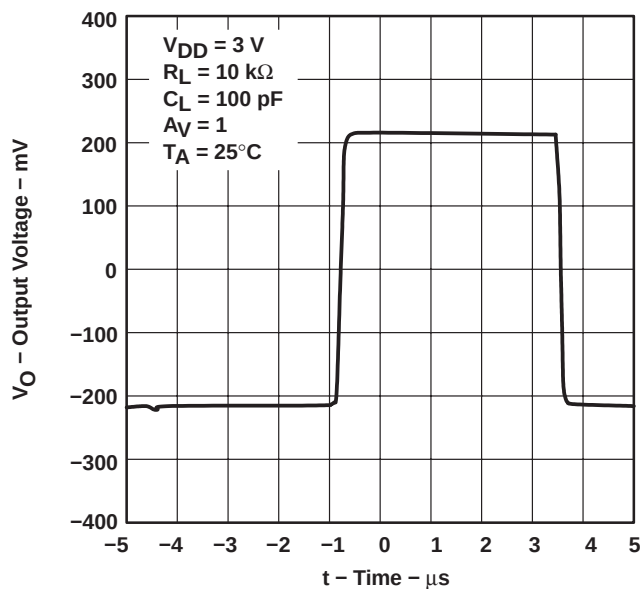


Figure 39

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

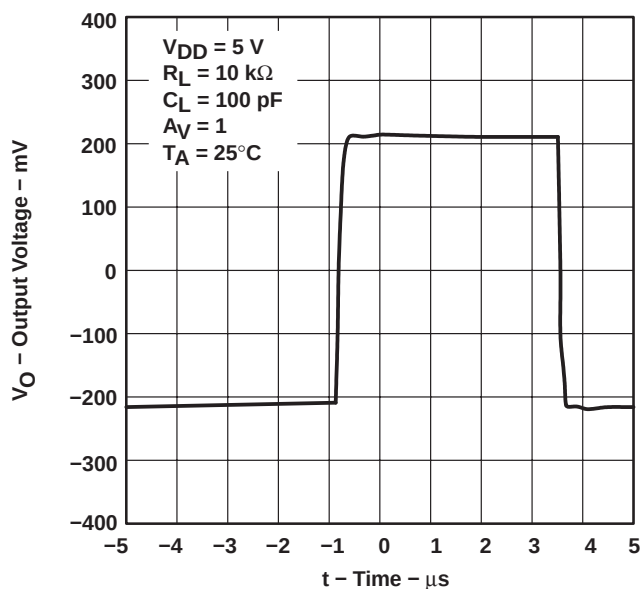


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY

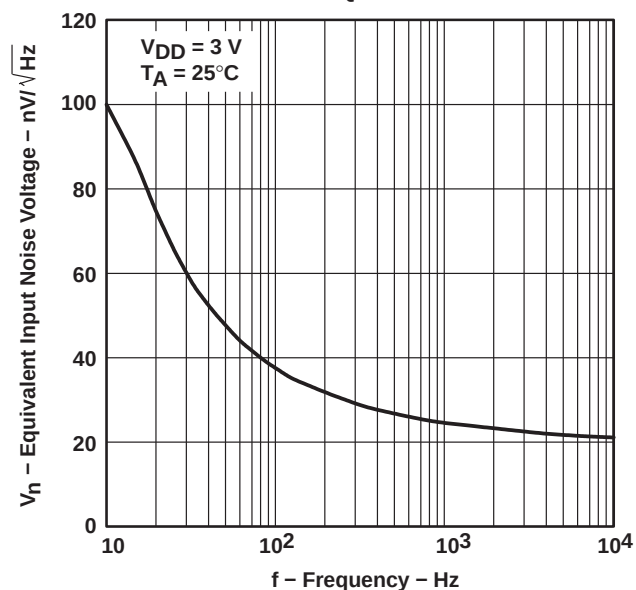


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY

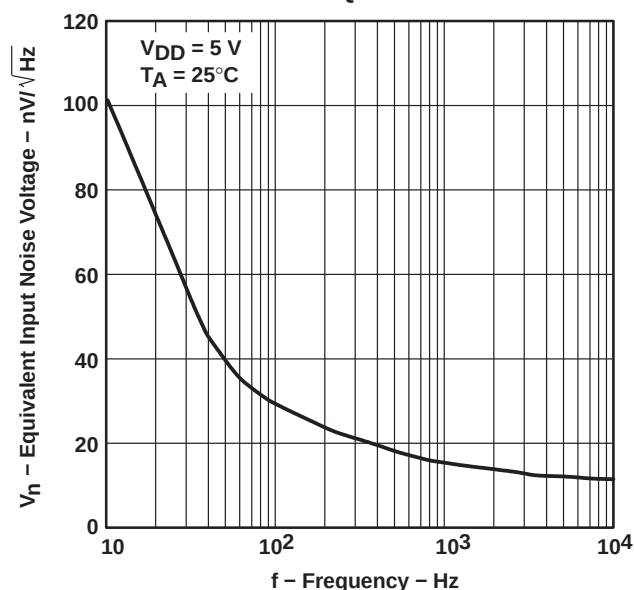


Figure 42

TYPICAL CHARACTERISTICS

NOISE VOLTAGE OVER A 10-SECOND PERIOD

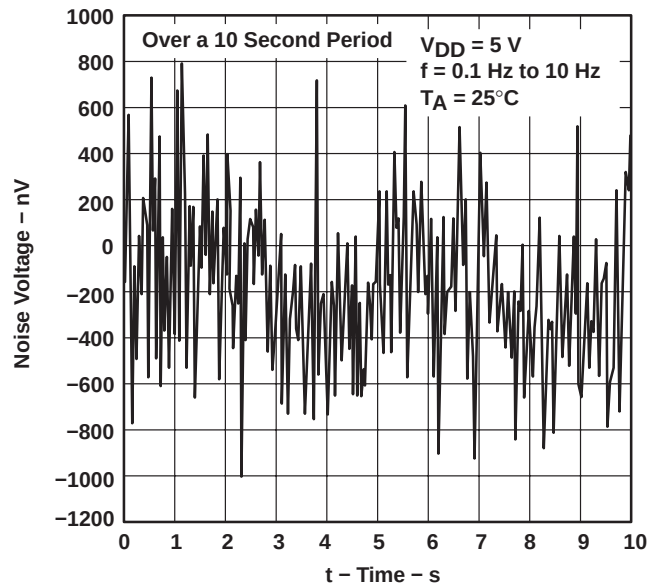


Figure 43

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

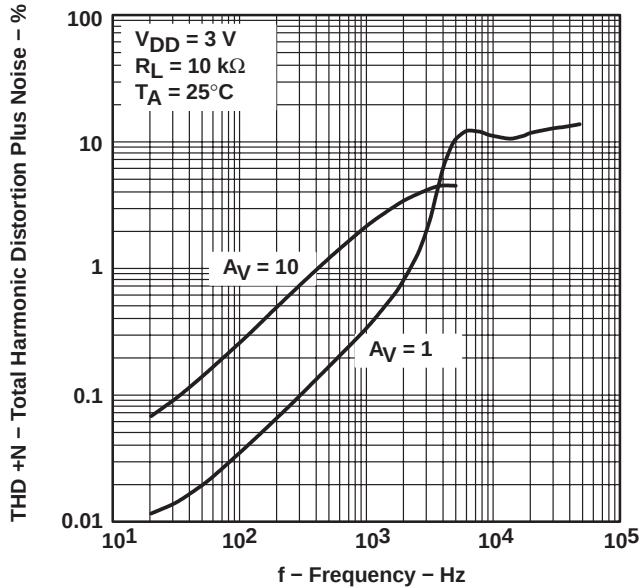


Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

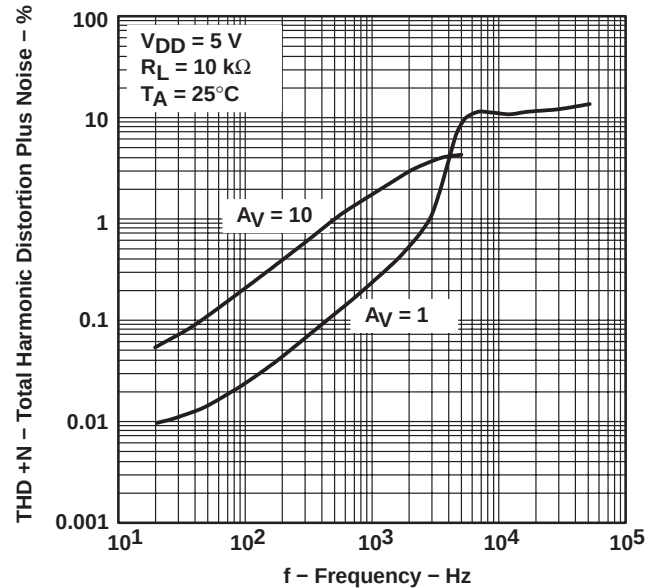


Figure 45

TLV2422-Q1, TLV2422A-Q1

Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT

WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS

SGLS175 – AUGUST 2003

TYPICAL CHARACTERISTICS

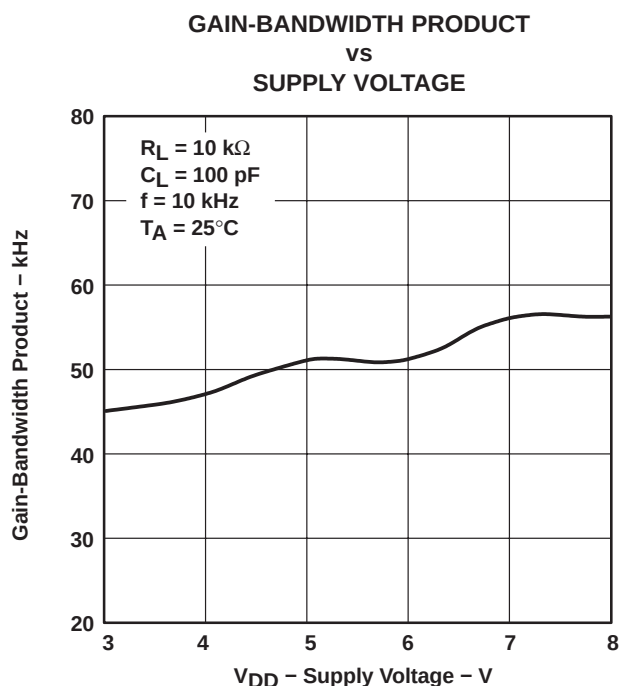


Figure 46

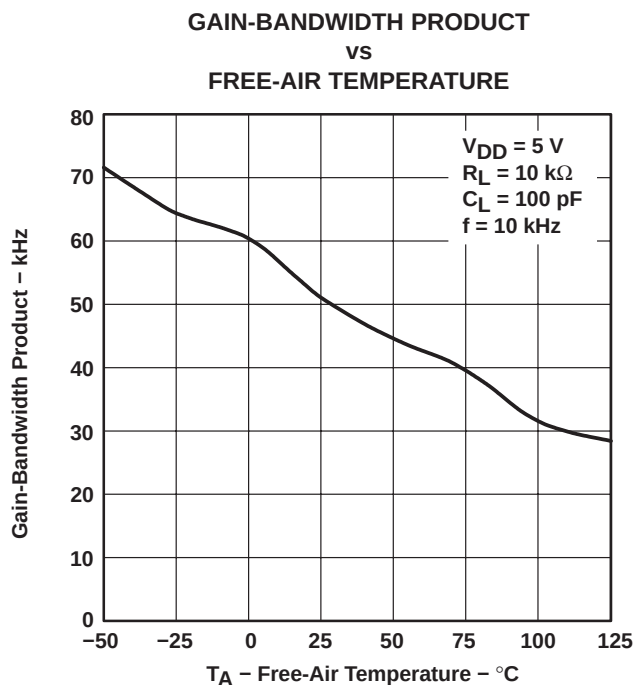


Figure 47

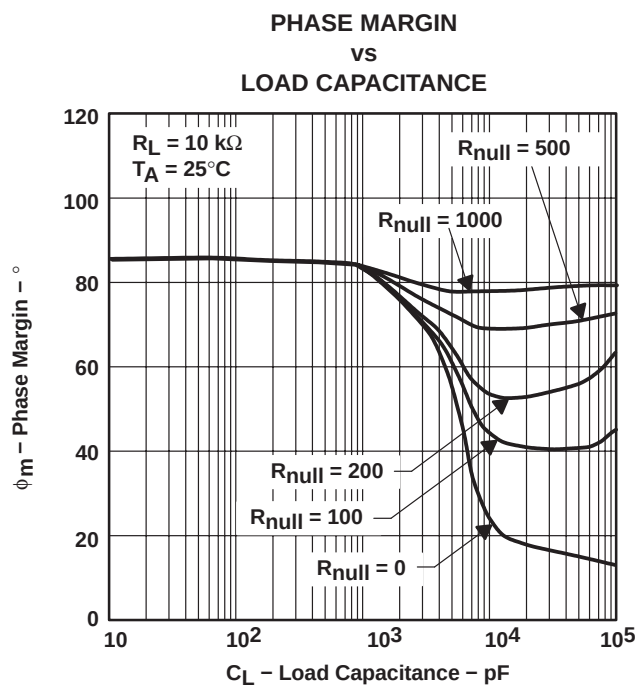


Figure 48

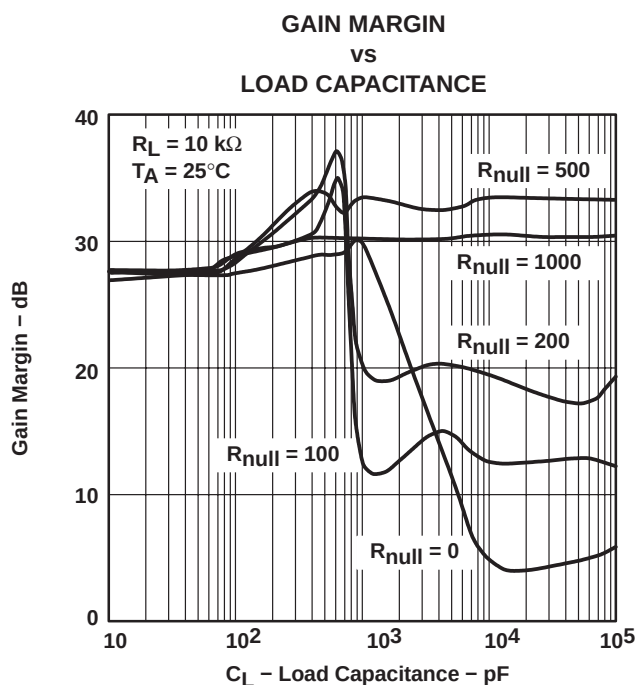


Figure 49

TYPICAL CHARACTERISTICS

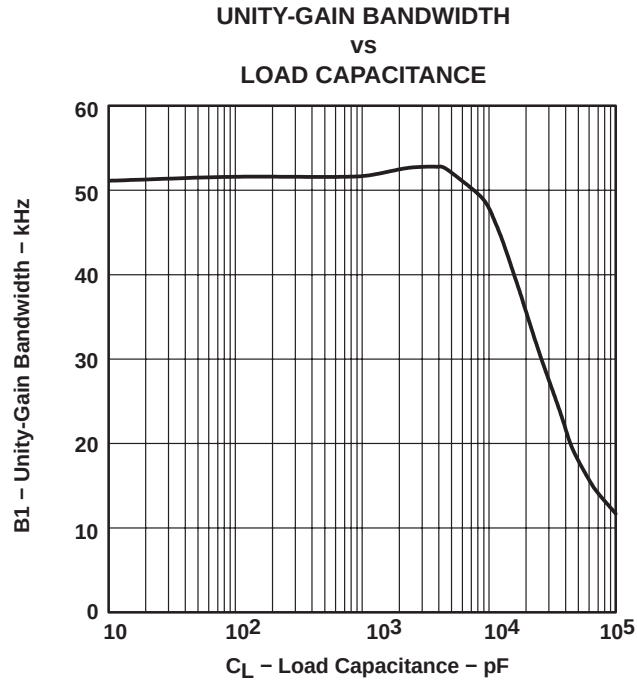


Figure 50

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2422QDRG4Q1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2422Q1
TLV2422QDRG4Q1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2422Q1

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV2422-Q1 :

- Catalog : [TLV2422](#)

- Military : [TLV2422M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

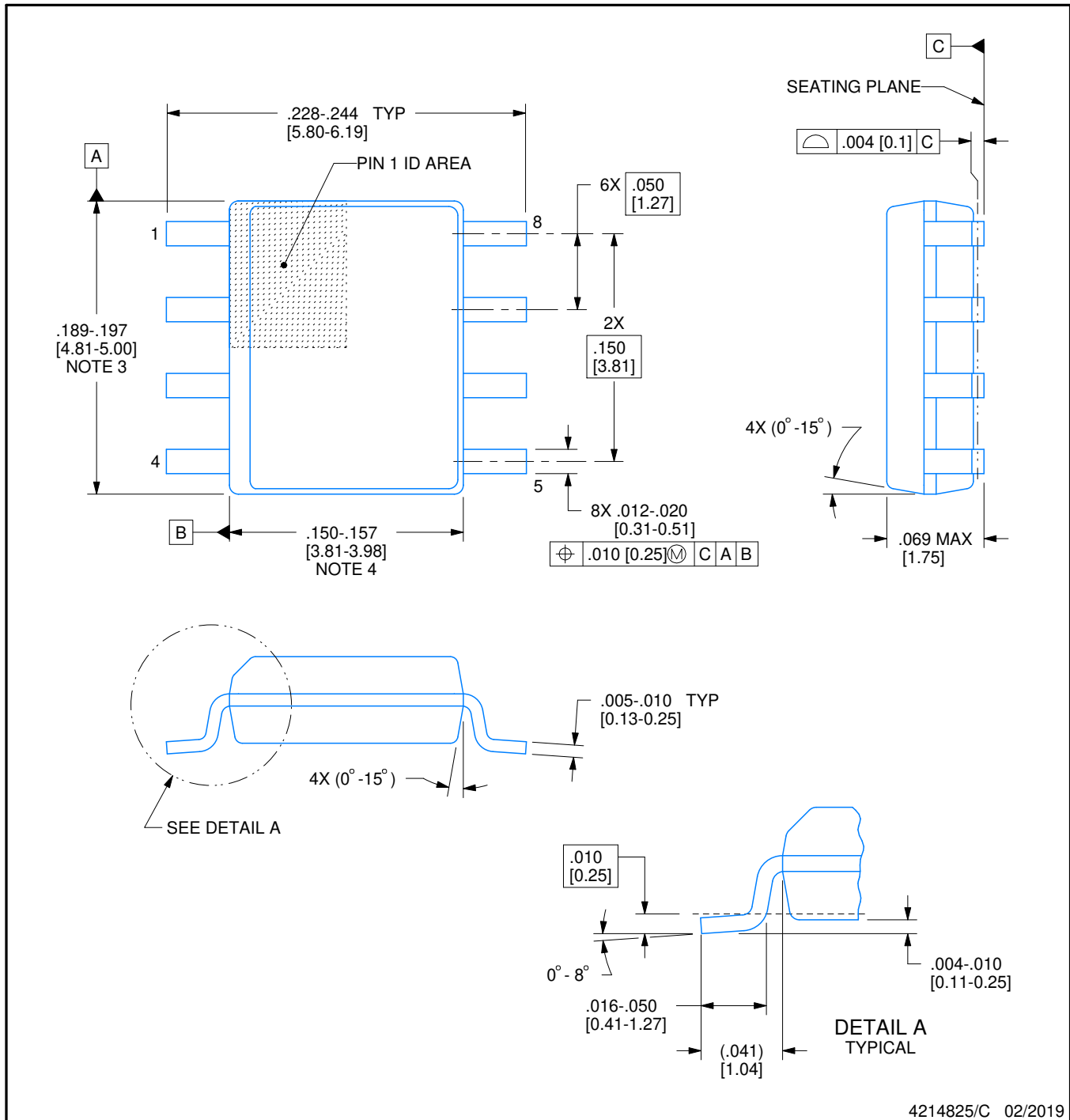


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

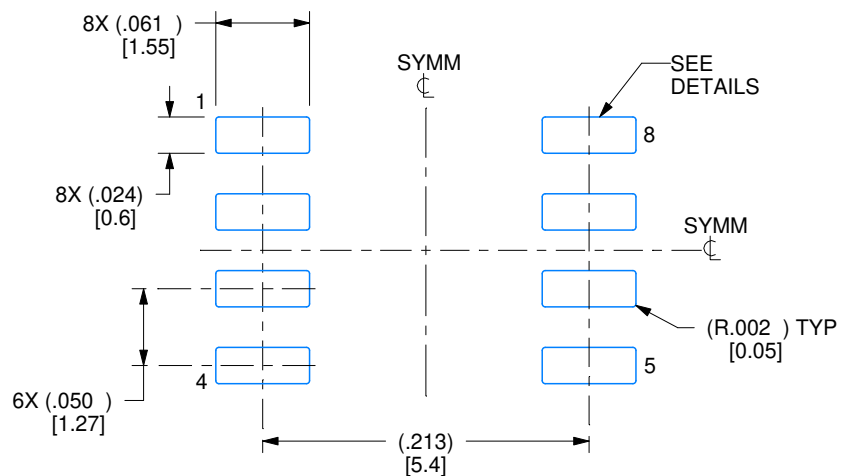
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

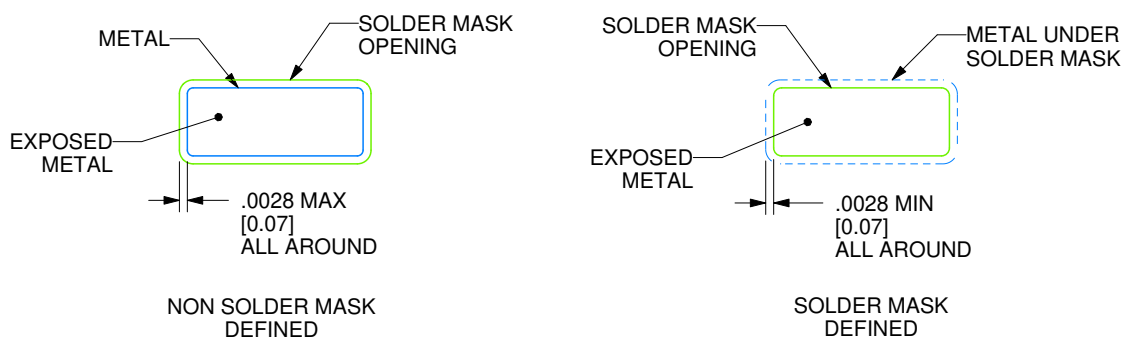
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

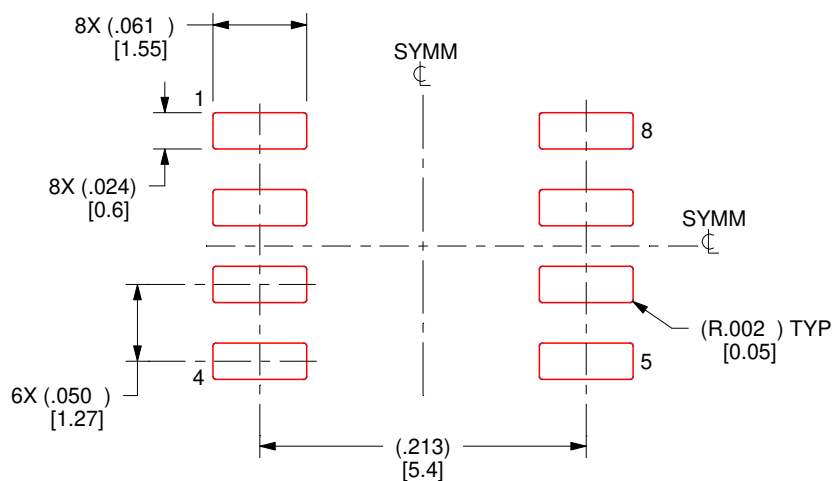
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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