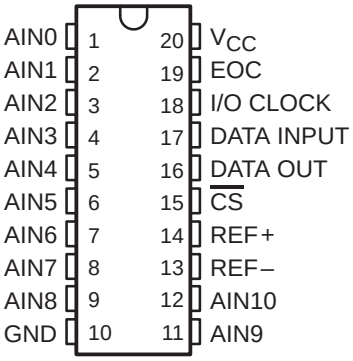
- **12-Bit-Resolution A/D Converter**
- **10-μs Conversion Time Over Operating Temperature Range**
- **11 Analog Input Channels**
- **3 Built-In Self-Test Modes**
- **Inherent Sample and Hold Function**
- **Linearity Error . . . ±1 LSB Max**
- **On-Chip System Clock**
- **End-of-Conversion (EOC) Output**
- **Unipolar or Bipolar Output Operation (Signed Binary With Respect to Half of the Applied Referenced Voltage)**
- **Programmable MSB or LSB First**
- **Programmable Power Down**
- **Programmable Output Data Length**
- **CMOS Technology**

**DB, DW, OR N PACKAGE**
**(TOP VIEW)**




## description

The TLV2543C and TLV2543I are 12-bit, switched-capacitor, successive-approximation, analog-to-digital converters (ADCs). Each device has three control inputs [chip select ($\overline{CS}$), the input-output clock (I/O CLOCK), and the address input (DATA INPUT)] and is designed for communication with the serial port of a host processor or peripheral through a serial 3-state output. The device allows high-speed data transfers from the host.

In addition to the high-speed converter and versatile control capability, the device has an on-chip 14-channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC) output goes high to indicate that conversion is complete. The converter incorporated in the device features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range.

The TLV2543 is available in the DW, DB, and N packages. The TLV2543C is characterized for operation from 0°C to 70°C, and the TLV2543I is characterized for operation from –40°C to 85°C.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE | | |
|---|---|---|---|
| | SMALL OUTLINE | | PLASTIC DIP |
| | DW† | DB† | N |
| 0°C to 70°C | TLV2543CDW | TLV2543CDB | TLV2543CN |
| –40°C to 85°C | TLV2543IDW | TLV2543IDB | TLV2543IN |

† Available in tape and reel and ordered as the TLV2543CDWR, TLV2543CDBLE, TLV2543IDBR, or TLV2543IDWR.

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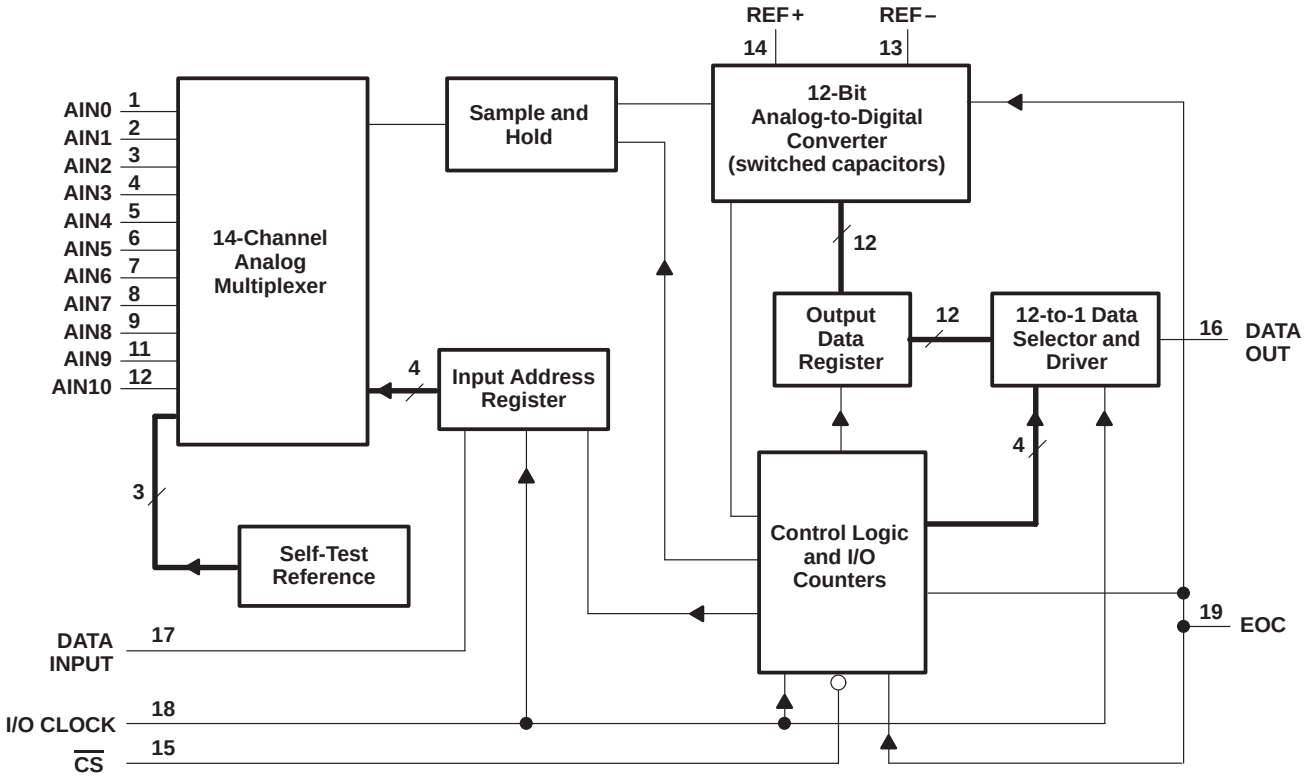
## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AIN0 – AIN10 | 1–9, 11, 12 | I | Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50 Ω for 4.1-MHz I/O CLOCK operation and capable of slewing the analog input voltage into a capacitance of 60 pF. |
| $\overline{CS}$ | 15 | I | Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low-to-high transition disables DATA INPUT and I/O CLOCK within a setup time. |
| DATA INPUT | 17 | I | Serial-data input. A 4-bit serial address selects the desired analog input or test voltage to be converted. The serial data is presented with the MSB first and is shifted in on the first four rising edges of I/O CLOCK. After the four address bits are read into the address register, I/O CLOCK clocks the remaining bits in order. |
| DATA OUT | 16 | O | Serial data output. This is the 3-state serial output for the A/D conversion result. DATA OUT is in the high-impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB/LSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order. |
| EOC | 19 | O | End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and data are ready for transfer. |
| GND | 10 | | Ground. This is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND. |
| I/O CLOCK | 18 | I | Input/output clock. I/O CLOCK receives the serial input and performs the following four functions:<br>1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge.<br>2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK.<br>3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK.<br>4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK. |
| REF+ | 14 | I | Reference+. The upper reference voltage value (nominally $V_{CC}$) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal. |
| REF– | 13 | I | Reference–. The lower reference voltage value (nominally ground) is applied to REF–. |
| $V_{CC}$ | 20 | | Positive supply voltage. |

## detailed description

Initially, with chip select ($\overline{CS}$) high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$, going low, begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clocks long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

### converter operation

The operation of the converter is organized as a succession of two distinct cycles: 1) the I/O cycle, and 2) the actual conversion cycle. The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods depending on the selected output data length.

1. I/O cycle

   During the I/O cycle, two operations take place simultaneously.

   a. An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12- or 16-clock I/O transfers.

   b. The data output with a length of 8, 12, or 16 bits is provided serially on DATA OUT. When $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. When $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of $\overline{CS}$. This data is the result of the previous conversion period, and after the first output data bit each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

2. Conversion cycle

   The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to the I/O CLOCK. During the conversion period, the device performs a successive-approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

### power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is initially high, and the input data register is set to all zeros. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

## operational terminology

| | |
|---|---|
| Previous (N – 1) conversion cycle | The conversion cycle prior to the current I/O cycle. |
| Current (N) I/O cycle | The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks the digital result from the previous conversion cycle from DATA OUT. The last falling edge of the clock in the I/O CLOCK sequence signifies the end of the current I/O cycle. |
| Current (N) conversion cycle | Immediately after the current I/O cycle, the current conversion cycle starts. When the current conversion cycle is complete, the current conversion result is loaded into the output register. |
| Current (N) conversion result | The result of the current conversion cycle that is serially shifted out during the next I/O cycle. |
| Next (N + 1) I/O cycle | The I/O cycle after the current conversion cycle. |

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion begins immediately after the twelfth falling edge of the current I/O cycle.

### data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence (see Table 1 for the data register format).

**data input (continued)**

**Table 1. Input-Register Format**

| FUNCTION SELECT | INPUT DATA BYTE | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | ADDRESS BITS | | | | L1 | L0 | LSBF | BIP |
| | D7 (MSB) | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) |
| Select input channel | | | | | | | | |
| AIN0 | 0 | 0 | 0 | 0 | | | | |
| AIN1 | 0 | 0 | 0 | 1 | | | | |
| AIN2 | 0 | 0 | 1 | 0 | | | | |
| AIN3 | 0 | 0 | 1 | 1 | | | | |
| AIN4 | 0 | 1 | 0 | 0 | | | | |
| AIN5 | 0 | 1 | 0 | 1 | | | | |
| AIN6 | 0 | 1 | 1 | 0 | | | | |
| AIN7 | 0 | 1 | 1 | 1 | | | | |
| AIN8 | 1 | 0 | 0 | 0 | | | | |
| AIN9 | 1 | 0 | 0 | 1 | | | | |
| AIN10 | 1 | 0 | 1 | 0 | | | | |
| Select test voltage | | | | | | | | |
| $(V_{ref+} - V_{ref-})/2$ | 1 | 0 | 1 | 1 | | | | |
| $V_{ref-}$ | 1 | 1 | 0 | 0 | | | | |
| $V_{ref+}$ | 1 | 1 | 0 | 1 | | | | |
| Software power down | 1 | 1 | 1 | 0 | | | | |
| Output data length | | | | | | | | |
| 8 bits | | | | | 0 | 1 | | |
| 12 bits | | | | | X | 0 | | |
| 16 bits | | | | | 1 | 1 | | |
| Output data format | | | | | | | | |
| MSB first | | | | | | | 0 | |
| LSB first | | | | | | | 1 | |
| Unipolar (binary) | | | | | | | | 0 |
| Bipolar (BIP, 2s complement) | | | | | | | | 1 |

**data input address bits**

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference-test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to $V_{ref+} - V_{ref-}$.

**data output length**

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, which is valid for the current I/O cycle, allows device start-up without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even when this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16-bit serial-data stream during the next I/O cycle with the four LSBs always set to 0 (pad bits). The current I/O cycle must be exactly 16 bits long to maintain synchronization even when this means corrupting the output data from the previous conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

**data output length (continued)**

With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, which allows fast communication with 8-bit serial interfaces. In the 8-bit mode, the result of the current conversion is output as an 8-bit serial-data stream during the next I/O cycle. The current I/O cycle must be exactly 8 bits long to maintain synchronization, even when this means corrupting the output data from the previous conversion. The four LSBs of the conversion result are truncated and discarded. The current conversion is immediately started after the eighth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first, since at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out.

In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only when it is shifted out in LSB first format.

**sampling period**

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed, time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty.

After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating that the conversion is complete) to maximize the sampling accuracy and minimize the influence of external digital noise.

**data register, LSB first**

D1 in the input data register (LSB first) controls the direction of the output binary data transfer. When D1 is set to 0, the conversion result shifts out MSB first. When set to 1, the data shifts out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

**data register, bipolar format**

D0 in the input data register controls the binary data format used to represent the conversion result. When D0 is set to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to $V_{ref-}$ is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to $V_{ref+}$ is a code of all ones (111 . . . 1), and the conversion result of $(V_{ref+} + V_{ref-})/2$ is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar data (signed binary). Nominally, conversion of an input voltage equal to $V_{ref-}$ is a code of a 1 followed by zeros (100 . . . 0), conversion of an input voltage equal to $V_{ref+}$ is a code of a 0 followed by all ones (011 . . . 1), and the conversion of $(V_{ref+} + V_{ref-})/2$ is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other's complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

### EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion completes and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when $\overline{CS}$ is low. When $\overline{CS}$ is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of $\overline{CS}$.

### data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When $\overline{CS}$ is held low continuously, the first data bit of the just completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a logic zero until EOC goes high again.

When $\overline{CS}$ is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{CS}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

### chip-select input ($\overline{CS}$)

The chip-select input ($\overline{CS}$) enables and disables the device. During normal operation, $\overline{CS}$ should be low. Although the use of $\overline{CS}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{CS}$ is brought high, the serial-data output is immediately brought to the high-impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, the I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{CS}$ is subsequently brought low again, the device is reset. $\overline{CS}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{CS}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{CS}$ can be used to interrupt any ongoing data transfer or any ongoing conversion. When $\overline{CS}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and then shifted out during the next I/O cycle.

### power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results, provided that all digital inputs are held above $V_{CC}$ – 0.3 V or below 0.3 V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid (other than 1110) input address clocks in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

### analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables 2, 3, and 4. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, sampled, and converted in the same manner as the external analog inputs. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

**Table 2. Analog-Channel-Select Address**

| ANALOG INPUT SELECTED | VALUE SHIFTED INTO DATA INPUT | |
|---|---|---|
| | BINARY | HEX |
| AIN0 | 0000 | 0 |
| AIN1 | 0001 | 1 |
| AIN2 | 0010 | 2 |
| AIN3 | 0011 | 3 |
| AIN4 | 0100 | 4 |
| AIN5 | 0101 | 5 |
| AIN6 | 0110 | 6 |
| AIN7 | 0111 | 7 |
| AIN8 | 1000 | 8 |
| AIN9 | 1001 | 9 |
| AIN10 | 1010 | A |

**Table 3. Test-Mode-Select Address**

| INTERNAL SELF-TEST VOLTAGE SELECTED† | VALUE SHIFTED INTO DATA INPUT | | UNIPOLAR OUTPUT RESULT (HEX)‡ |
|---|---|---|---|
| | BINARY | HEX | |
| $\frac{V_{ref+} - V_{ref-}}{2}$ | 1011 | B | 200 |
| $V_{ref-}$ | 1100 | C | 000 |
| $V_{ref+}$ | 1101 | D | 3FF |

† $V_{ref+}$ is the voltage applied to REF+, and $V_{ref-}$ is the voltage applied to REF–.
‡ The output results shown are the ideal values and may vary with the reference stability and with internal offsets.

**analog input, test, and power-down mode (continued)**

**Table 4. Power-Down-Select Address**

| INPUT COMMAND | VALUE SHIFTED INTO DATA INPUT | | RESULT |
|---|---|---|---|
| | BINARY | HEX | |
| Power down | 1110 | E | $I_{CC} \leq 25\ \mu A$ |

**converter and analog input**

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the $S_C$ switch and all $S_T$ switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all $S_T$ and $S_C$ switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. When the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half $V_{CC}$), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF–. When the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

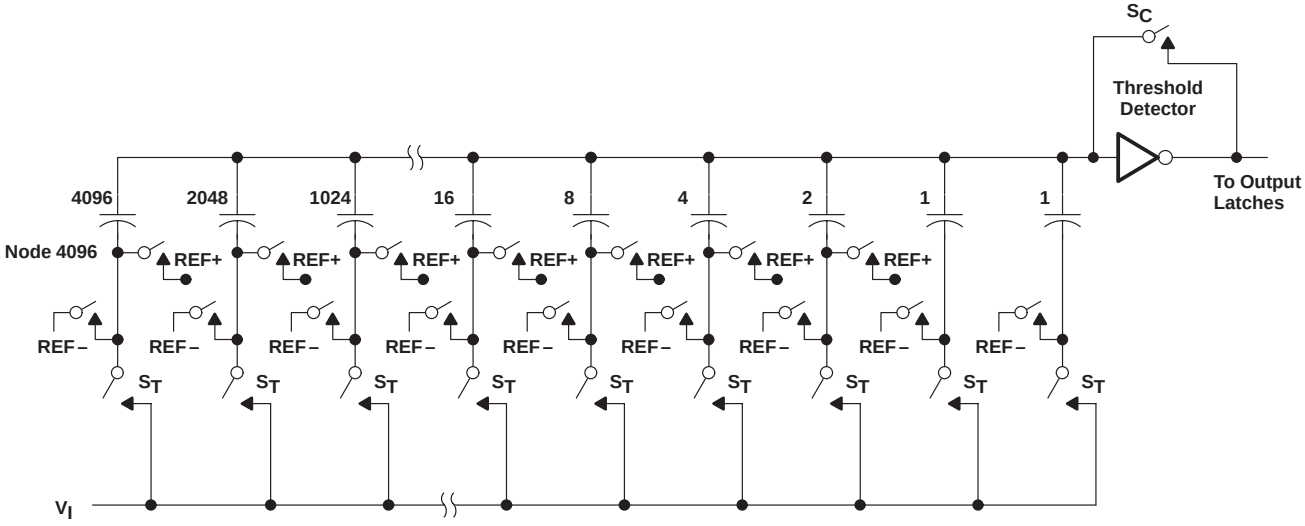



**Figure 1. Simplified Model of the Successive-Approximation System**

### reference voltage inputs

There are two reference voltage inputs on the device, REF+ and REF–. The voltage values on these terminals establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF– terminal voltage.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ (see Note 1) | –0.5 V to 6.5 V |
| Input voltage range, $V_I$ (any input) | –0.3 V to $V_{CC}$ + 0.3 V |
| Output voltage range, $V_O$ | –0.3 V to $V_{CC}$ + 0.3 V |
| Positive reference voltage, $V_{ref+}$ | $V_{CC}$ + 0.1 V |
| Negative reference voltage, $V_{ref-}$ | –0.1 V |
| Peak input current, $I_I$ (any input) | ±20 mA |
| Peak total input current (all inputs) | ±30 mA |
| Operating free-air temperature range, $T_A$: TLV2543C | 0°C to 70°C |
| TLV2543I | –40°C to 85°C |
| Storage temperature range, $T_{stg}$ | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminal with REF– and GND wired together (unless otherwise noted).

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | 3.3 | 3.6 | V |
| Positive reference voltage, $V_{ref+}$ (see Note 2) | | | $V_{CC}$ | | V |
| Negative reference voltage, $V_{ref-}$ (see Note 2) | | | 0 | | V |
| Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2) | | 2.5 | $V_{CC}$ | $V_{CC}+0.1$ | V |
| Analog input voltage (see Note 2) | | 0 | | $V_{CC}$ | V |
| High-level control input voltage, $V_{IH}$ | $V_{CC}$ = 3 V to 3.6 V | 2.1 | | | V |
| Low-level control input voltage, $V_{IL}$ | $V_{CC}$ = 3 V to 3.6 V | | | 0.6 | V |
| Clock frequency at I/O CLOCK | | 0 | 3 | 4.1 | MHz |
| Setup time, address bits at DATA INPUT before I/O CLOCK↑, $t_{su(A)}$ (see Figure 5) | | 100 | | | ns |
| Hold time, address bits at DATA INPUT after I/O CLOCK↑, $t_{h(A)}$ (see Figure 5) | | 0 | | | ns |
| Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$ (see Figure 6) | | 0 | | | ns |
| Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 3 and Figure 6) | | 1.425 | | | µs |
| Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$ | | 190 | | | ns |
| Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$ | | 190 | | | ns |
| Transition time, I/O CLOCK, $t_{t(I/O)}$ (see Note 4 and Figure 7) | | | | 1 | µs |
| Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$ | | | | 10 | µs |
| Operating free-air temperature, $T_A$ | TLV2543C | 0 | | 70 | °C |
| | TLV2543I | –40 | | 85 | |

NOTES: 2. Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF– convert as all zeros (000000000000).

3. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for a setup time after $\overline{CS}$↓ before responding to control input signals. No attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time elapses.

4. This is the time required for the clock input signal to fall from $V_{IH}$min to $V_{IL}$max or to rise from $V_{IL}$max to $V_{IH}$min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+} = 3$ V to 3.6 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = 3 V, | $I_{OH}$ = –0.2 mA | 2.4 | | | V |
| | | | $V_{CC}$ = 3 V to 3.6 V, | $I_{OH}$ = –20 μA | | $V_{CC}$–0.1 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 3 V, | $I_{OL}$ = 0.8 mA | | | 0.4 | V |
| | | | $V_{CC}$ = 3 V to 3.6 V, | $I_{OL}$ = 20 μA | | 0.1 | | |
| $I_{OZ}$ | Off-state (high-impedance-state) output current | | $V_O = V_{CC}$, | $\overline{CS}$ at $V_{CC}$ | | 1 | 2.5 | μA |
| | | | $V_O$ = 0, | $\overline{CS}$ at $V_{CC}$ | | 1 | –2.5 | |
| $I_{IH}$ | High-level input current | | $V_I = V_{CC}$ | | | 1 | 2.5 | μA |
| $I_{IL}$ | Low-level input current | | $V_I$ = 0 | | | 1 | –2.5 | μA |
| $I_{CC}$ | Operating supply current | | $\overline{CS}$ at 0 V | | | 1 | 2.5 | mA |
| $I_{CC(PD)}$ | Power-down current | | For all digital inputs, $0 \le V_I \le 0.3$ V or $V_I \ge V_{CC} - 0.3$ V | | | 4 | 25 | μA |
| $I_{lkg}$ | Selected channel leakage current | | Selected channel at $V_{CC}$, Unselected channel at 0 V | | | | 1 | μA |
| | | | Selected channel at 0 V, | Unselected channel at $V_{CC}$ | | | –1 | |
| | Maximum static analog reference current into REF+ | | $V_{ref+} = V_{CC}$, | $V_{ref-}$ = GND | | 1 | 2.5 | μA |
| $C_i$ | Input capacitance | Analog inputs | | | | 30 | 60 | pF |
| | | Control inputs | | | | 5 | 15 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

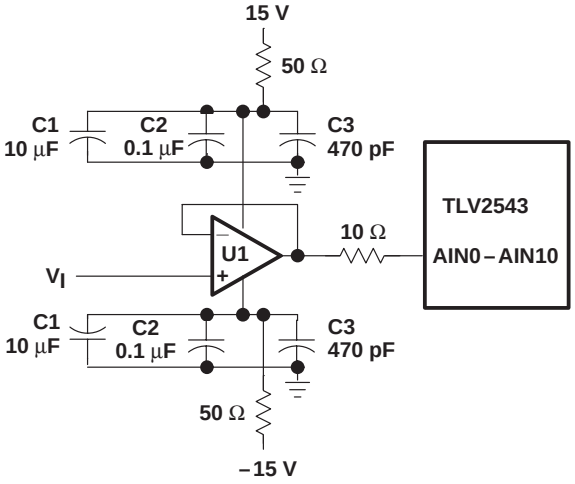
## operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{ref+}$ = 3 V to 3.6 V, I/O CLOCK frequency = 4.1 MHz, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $E_L$ | Linearity error (see Note 6) | See Figure 2 | | | ±1 | LSB |
| $E_D$ | Differential linearity error | See Figure 2 | | | ±1 | LSB |
| $E_O$ | Offset error (see Note 7) | See Note 2 and Figure 2 | | | ±1.5 | LSB |
| $E_G$ | Gain error (see Note 7) | See Note 2 and Figure 2 | | | ±1 | LSB |
| $E_T$ | Total unadjusted error (see Note 8) | | | | ±1.75 | LSB |
| | Self-test output code (see Table 3 and Note 9) | DATA INPUT = 1011 | 2038 | 2048 | 2058 | |
| | | DATA INPUT = 1100 | | 0 | 10 | |
| | | DATA INPUT = 1101 | 4075 | 4095 | | |
| $t_{(conv)}$ | Conversion time | See Figures 10–15 | | 8 | 10 | µs |
| $t_c$ | Total cycle time (access, sample, and conversion) | See Figures 10–15 and Note 10 | | | 10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$ | µs |
| $t_{acq}$ | Channel acquisition time (sample) | See Figures 10–15 and Note 10 | 4 | | 12 | I/O CLOCK periods |
| $t_v$ | Valid time, DATA OUT remains valid after I/O CLOCK↓ | See Figure 7 | 10 | | | ns |
| $t_{d(I/O-DATA)}$ | Delay time, I/O CLOCK↓ to DATA OUT valid | See Figure 7 | | | 250 | ns |
| $t_{d(I/O-EOC)}$ | Delay time, last I/O CLOCK↓ to EOC↓ | See Figure 8 | | 1.5 | 2.2 | µs |
| $t_{d(EOC-DATA)}$ | Delay time, EOC↑ to DATA OUT (MSB/LSB) | See Figure 9 | | | 200 | ns |
| $t_{PZH}$, $t_{PZL}$ | Enable time, $\overline{CS}$↓ to DATA OUT (MSB/LSB driven) | See Figure 4 | | 0.7 | 1.3 | µs |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time, $\overline{CS}$↑ to DATA OUT (high impedance) | See Figure 4 | | 70 | 150 | ns |
| $t_{r(EOC)}$ | Rise time, EOC | See Figure 9 | | 15 | 50 | ns |
| $t_{f(EOC)}$ | Fall time, EOC | See Figure 8 | | 15 | 50 | ns |
| $t_{r(bus)}$ | Rise time, data bus | See Figure 7 | | 15 | 50 | ns |
| $t_{f(bus)}$ | Fall time, data bus | See Figure 7 | | 15 | 50 | ns |
| $t_{d(I/O-CS)}$ | Delay time, last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion (see Note 11) | | | | 5 | µs |

† All typical values are at $T_A$ = 25°C.

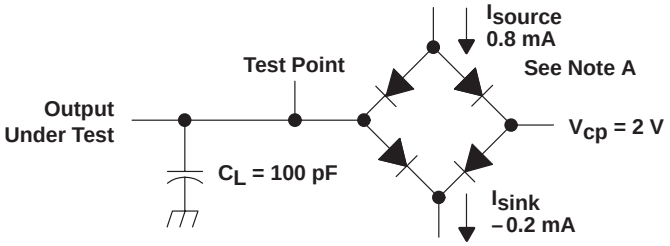
NOTES: 2. Analog input voltages greater than that applied to REF+ convert as all ones (111111111111), while input voltages less than that applied to REF– convert as all zeros (000000000000).
6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep value at the offset point.
8. Total unadjusted error comprises linearity, zero-scale, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.
10. I/O CLOCK period = 1/(I/O CLOCK frequency) (see Figure 7).
11. Any transitions of $\overline{CS}$ are recognized as valid only when the level is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 µs of the tenth I/O CLOCK falling edge to ensure that a conversion is aborted. Between 5 µs and 10 µs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

## PARAMETER MEASUREMENT INFORMATION




| LOCATION | DESCRIPTION | PART NUMBER |
|---|---|---|
| U1 | OP27 | — |
| C1 | 10-μF 35-V tantalum capacitor | — |
| C2 | 0.1-μF ceramic NPO SMD capacitor | AVX 12105C104KA105 or equivalent |
| C3 | 470-pF porcelain high-Q SMD capacitor | Johanson 201S420471JG4L or equivalent |

**Figure 2. Analog Input Buffer to Analog Inputs AIN0 – AIN10**




NOTE A: Equivalent load circuit of the Teradyne A580 tester for timing parameter measurement.

**Figure 3. Timing Load Circuits**

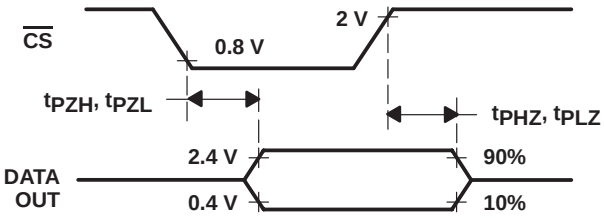



**Figure 4. DATA OUT to Hi-Z Voltage Waveforms**

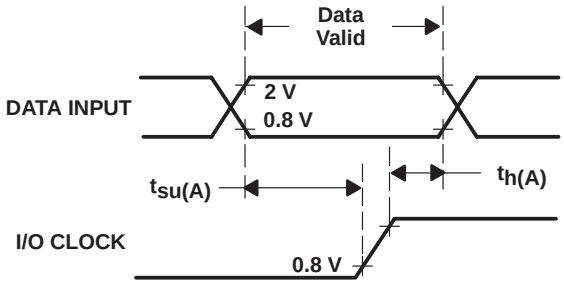



**Figure 5. DATA INPUT and I/O CLOCK Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION

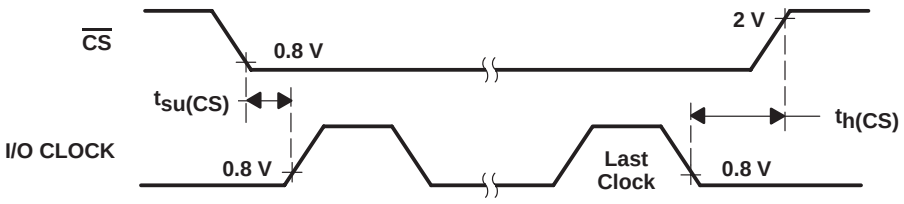



**Figure 6. $\overline{CS}$ and I/O CLOCK Voltage Waveforms†**

† To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

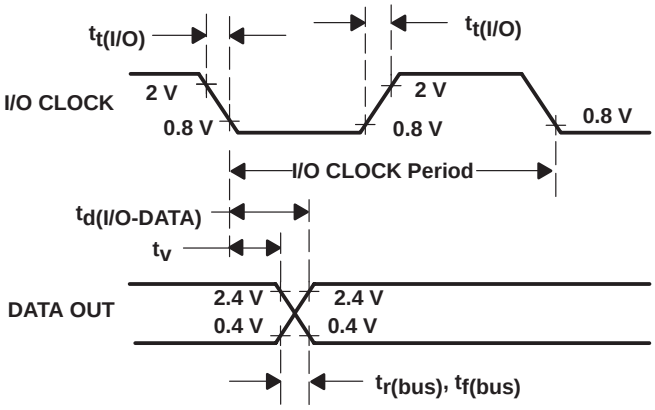



**Figure 7. I/O CLOCK and DATA OUT Voltage Waveforms**

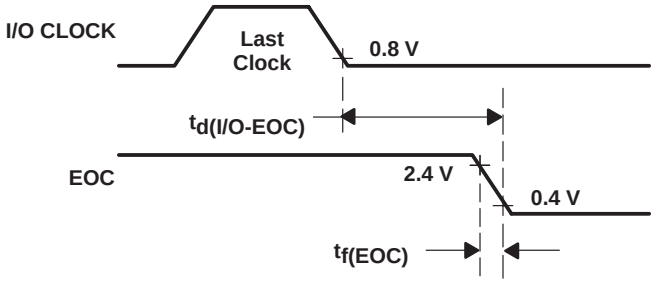



**Figure 8. I/O CLOCK and EOC Voltage Waveforms**

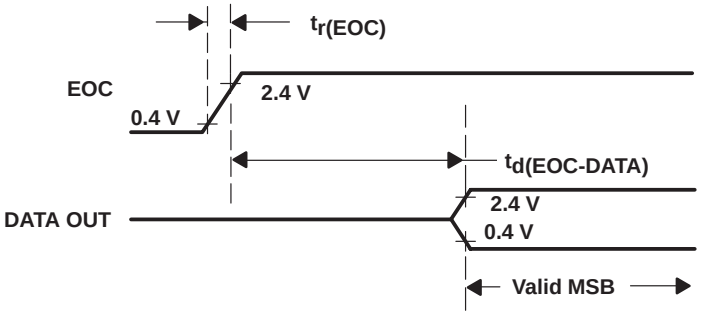



**Figure 9. EOC and DATA OUT Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION

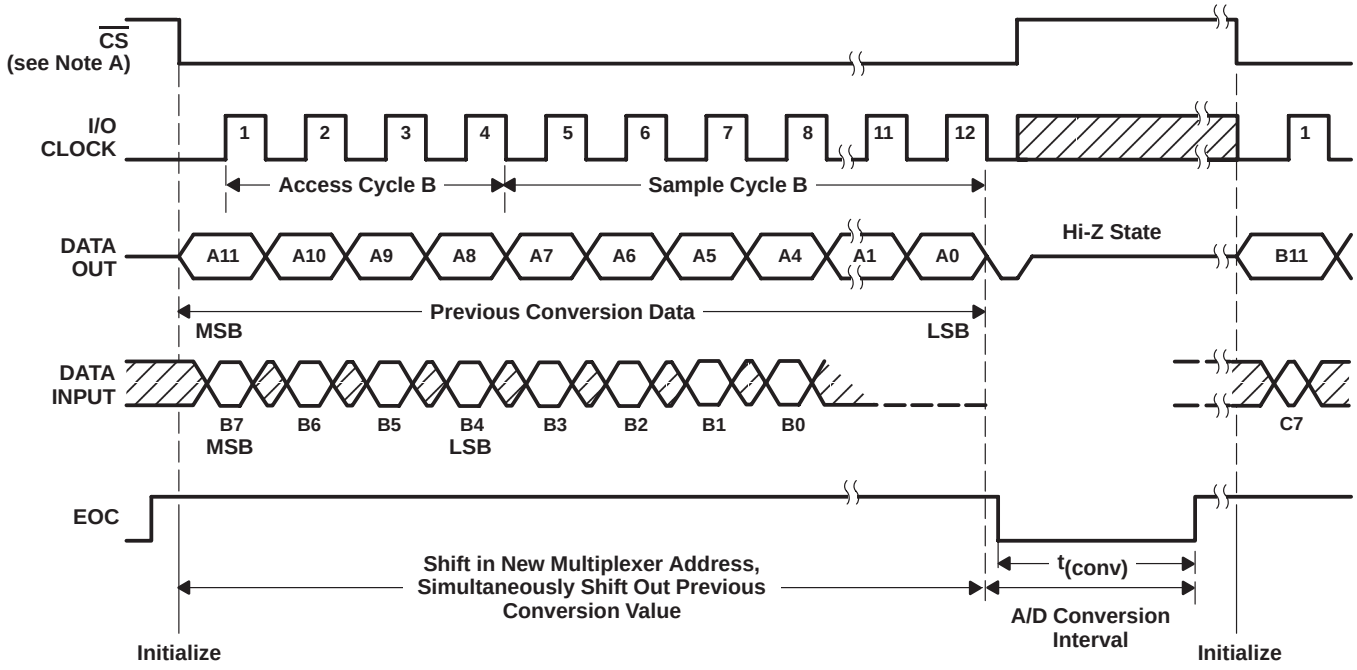



**Figure 10. Timing for 12-Clock Transfer Using $\overline{CS}$ With MSB First**

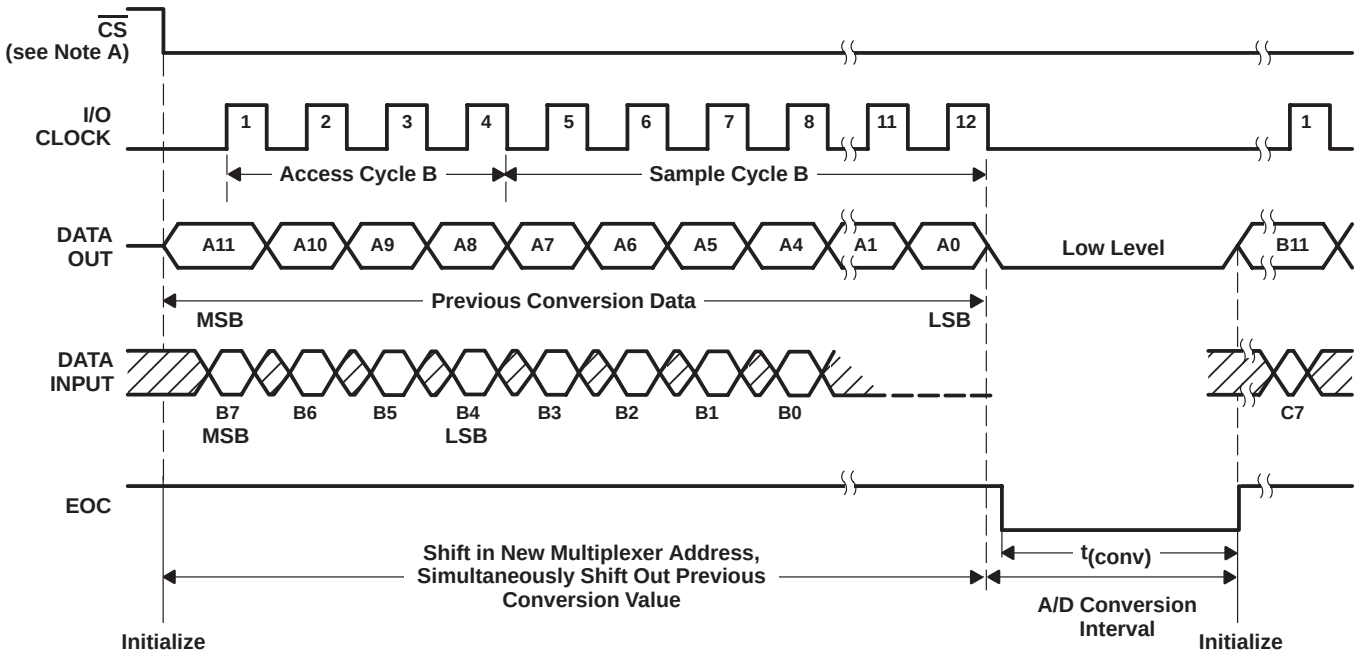



**Figure 11. Timing for 12-Clock Transfer Not Using $\overline{CS}$ With MSB First**

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

## PARAMETER MEASUREMENT INFORMATION

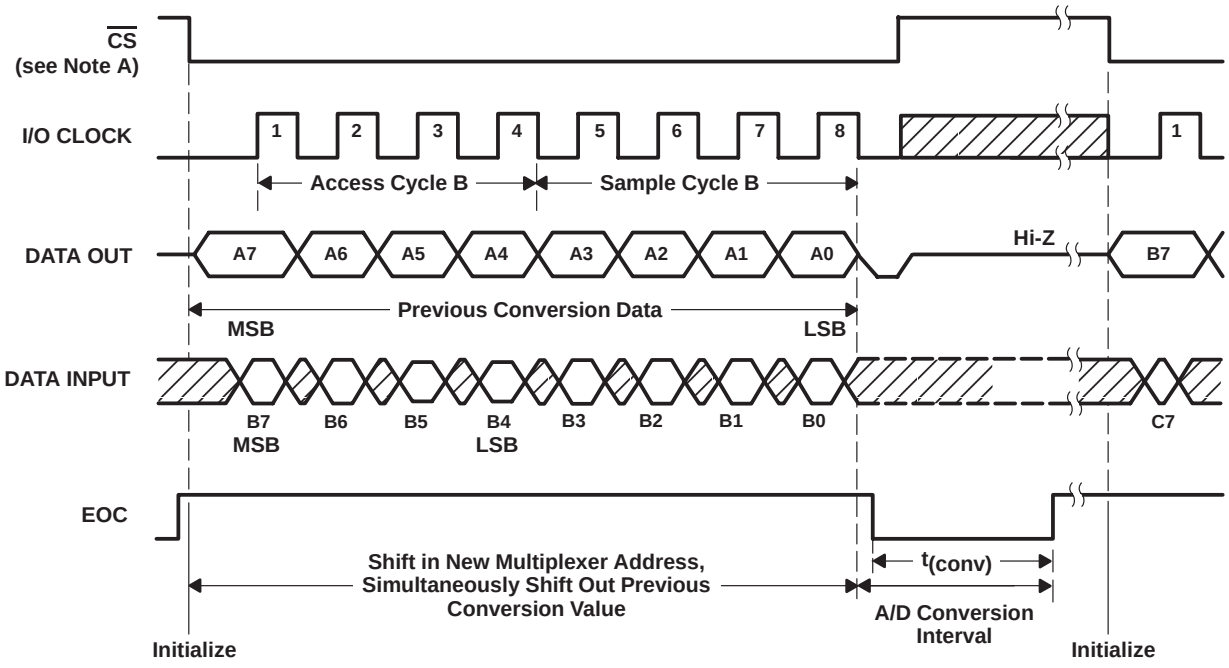



**Figure 12. Timing for 8-Clock Transfer Using $\overline{CS}$ With MSB First**

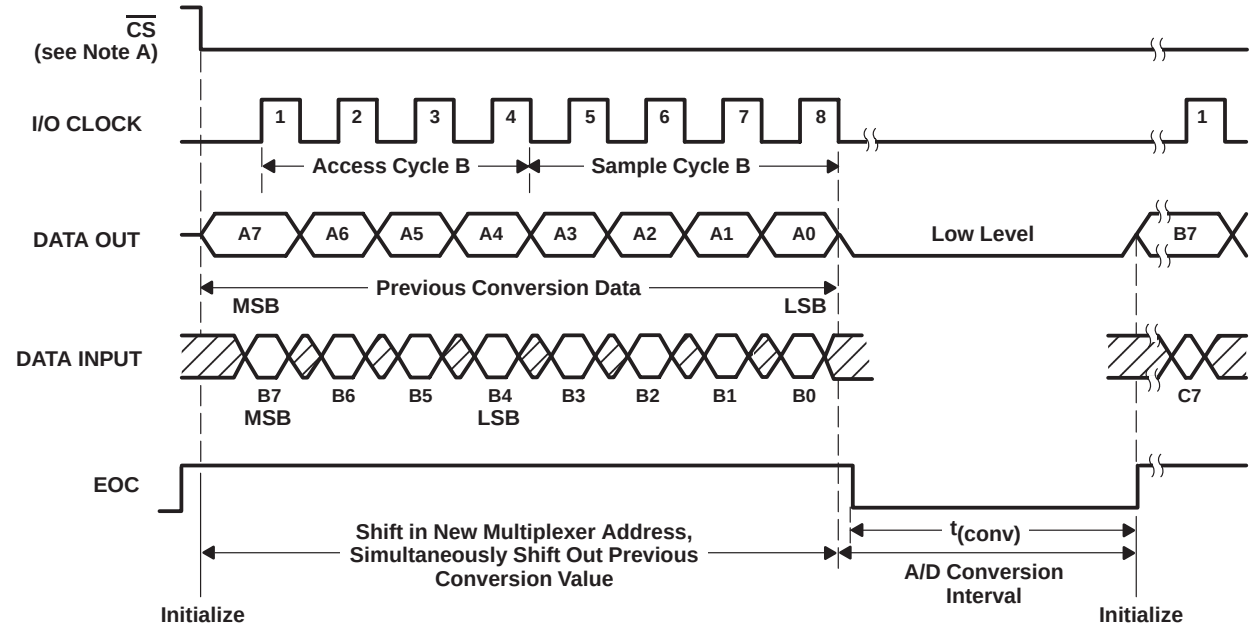



**Figure 13. Timing for 8-Clock Transfer Not Using $\overline{CS}$ With MSB First**

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

## PARAMETER MEASUREMENT INFORMATION

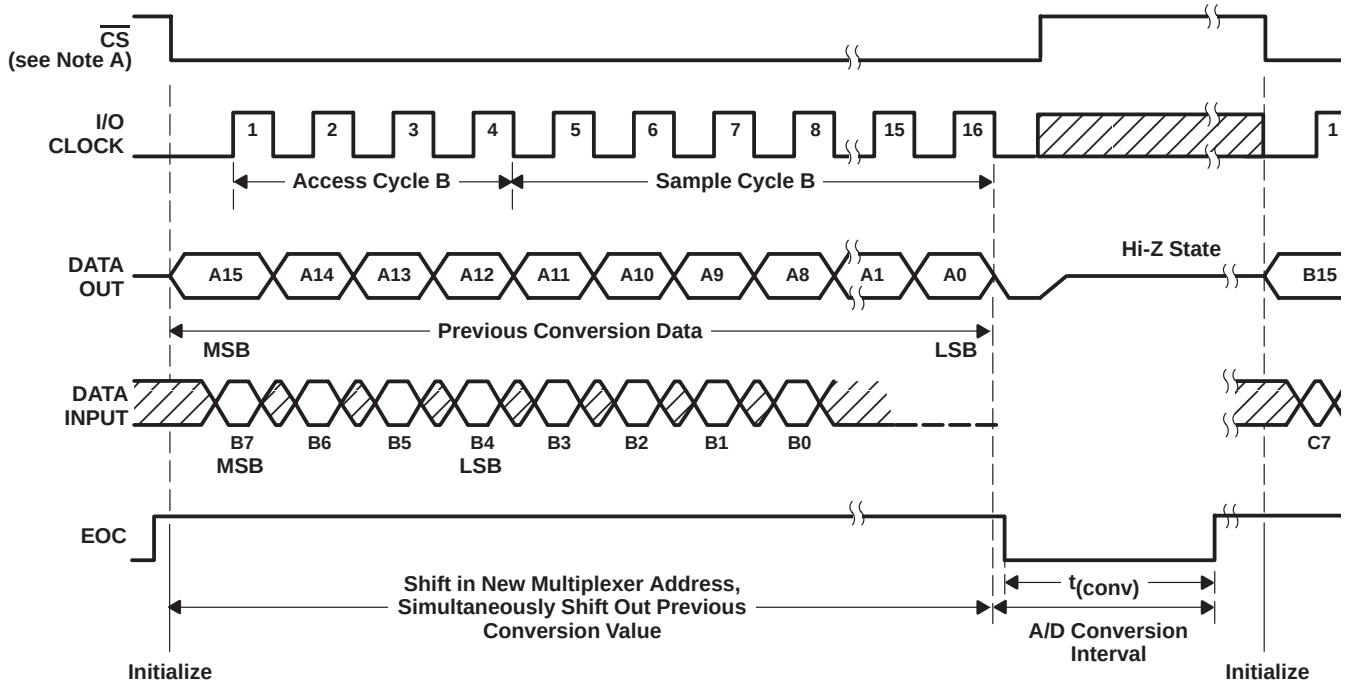



**Figure 14. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First**

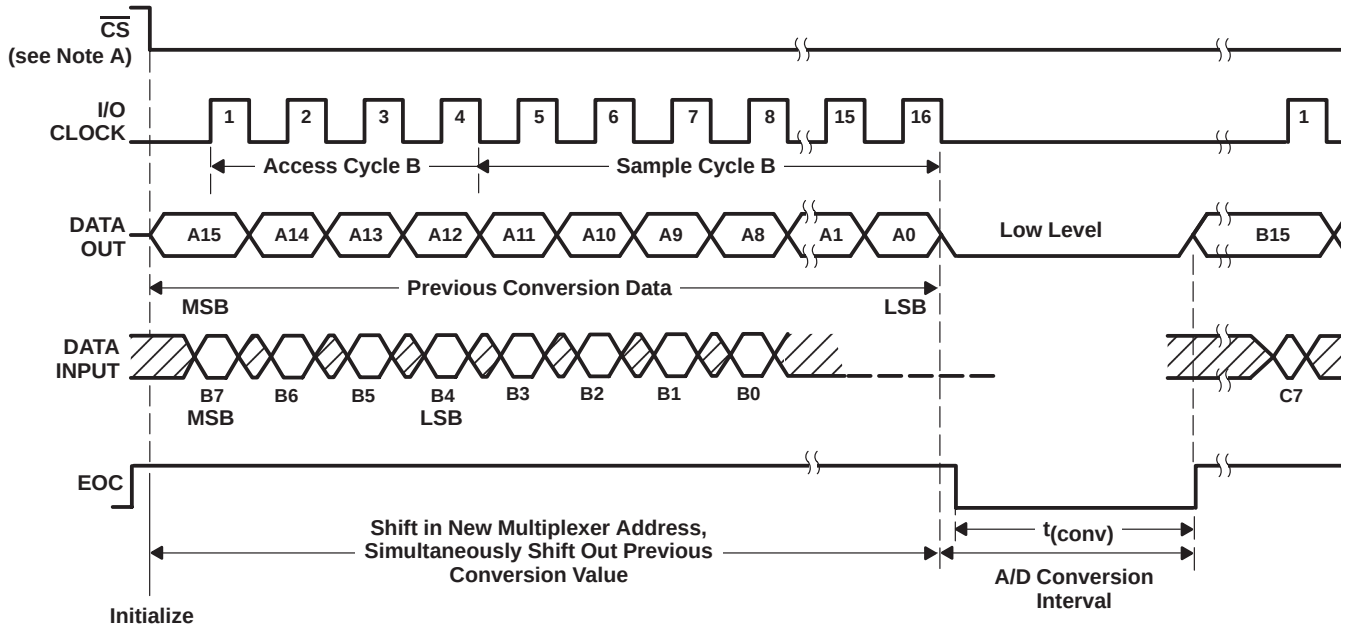
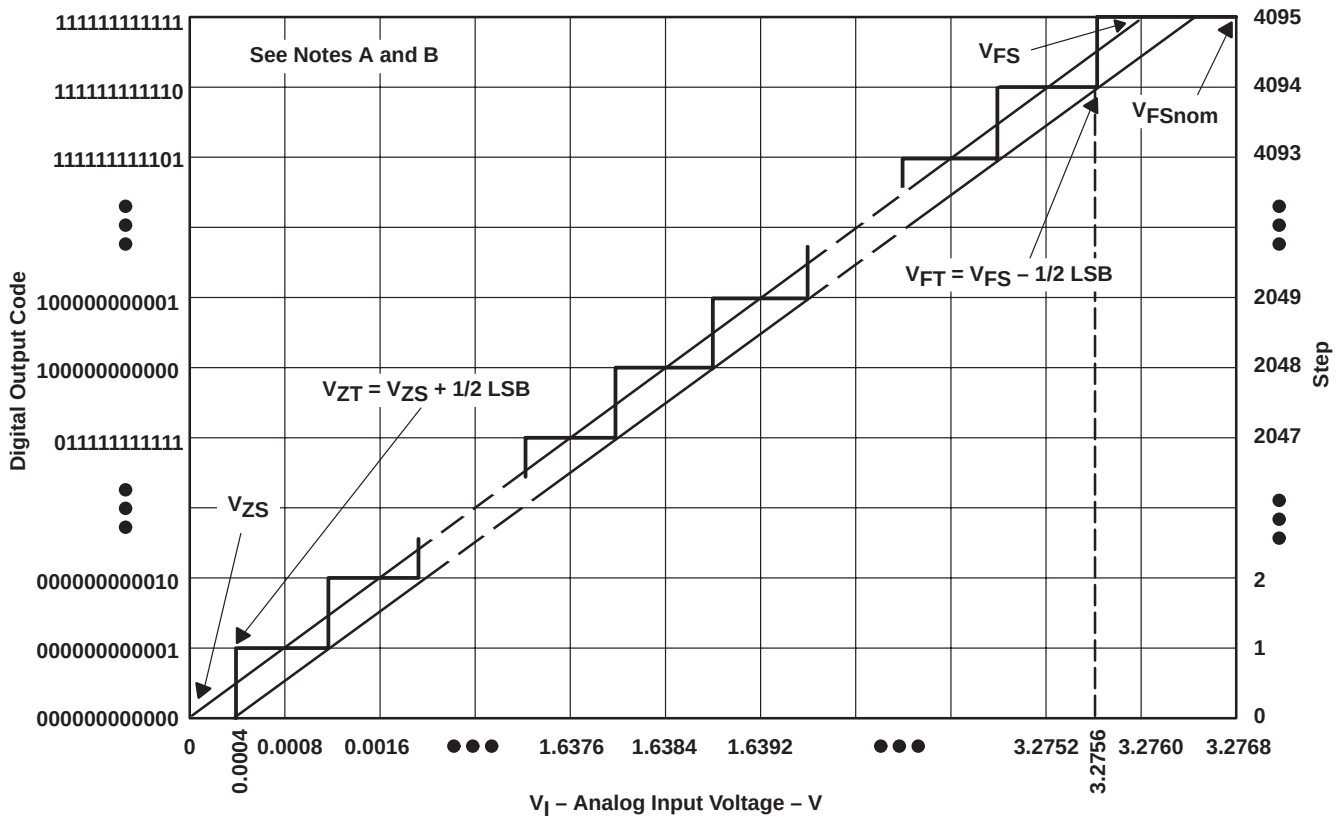



**Figure 15. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First**

NOTE A: To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time after $\overline{CS}\downarrow$ before responding to control input signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

## APPLICATION INFORMATION




NOTES: A. This curve is based on the assumption that $V_{ref+}$ and $V_{ref-}$ have been adjusted so that the voltage at the transition from digital 0 to 1 ($V_{ZT}$) is 0.0004 V and the transition to full scale ($V_{FT}$) is 3.2756 V. 1 LSB = 0.8 mV.

B. The full-scale value ($V_{FS}$) is the step whose nominal midstep value has the highest absolute value. The zero-scale value ($V_{ZS}$) is the step whose nominal midstep value equals zero.

**Figure 16. Ideal Conversion Characteristics**

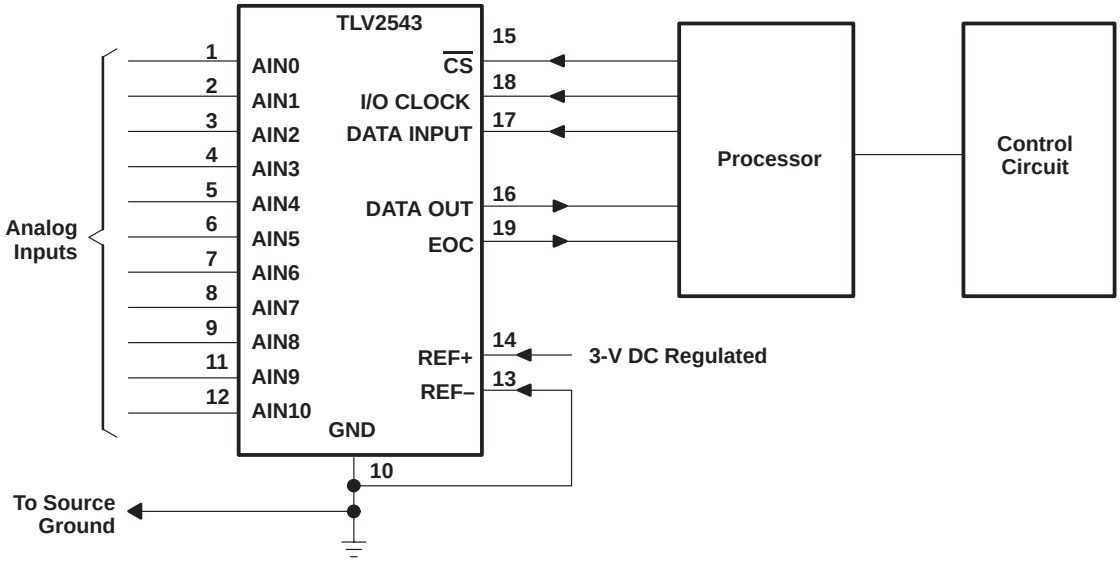



**Figure 17. Serial Interface**

## APPLICATIONS INFORMATION

### simplified analog input analysis

Using the equivalent circuit in Figure 18, the time required to charge the analog input capacitance from 0 to $V_S$ within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1–e^{-t_c/R_tC_i}\right) \quad (1)$$

Where:

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C\ (1/2\ LSB) = V_S – (V_S/8192) \quad (2)$$

Equating equation 1 to equation 2 and solving for time $t_c$ gives

$$V_S – \left(V_S/58192\right) = V_S\left(1–e^{-t_c/R_tC_i}\right) \quad (3)$$

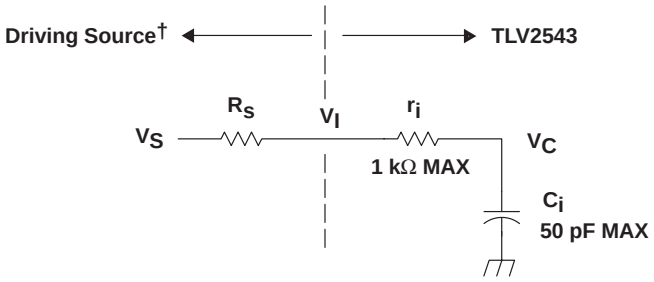
and

$$t_c\ (1/2\ LSB) = R_t \times C_i \times \ln(8192) \quad (4)$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c\ (1/2\ LSB) = (R_S + 1\ k\Omega) \times 60\ pF \times \ln(8192) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.




**$V_I$ = Input Voltage at AIN**
**$V_S$ = External Driving Source Voltage**
**$R_S$ = Source Resistance**
**$r_i$ = Input Resistance**
**$C_i$ = Input Capacitance**

† Driving source requirements:

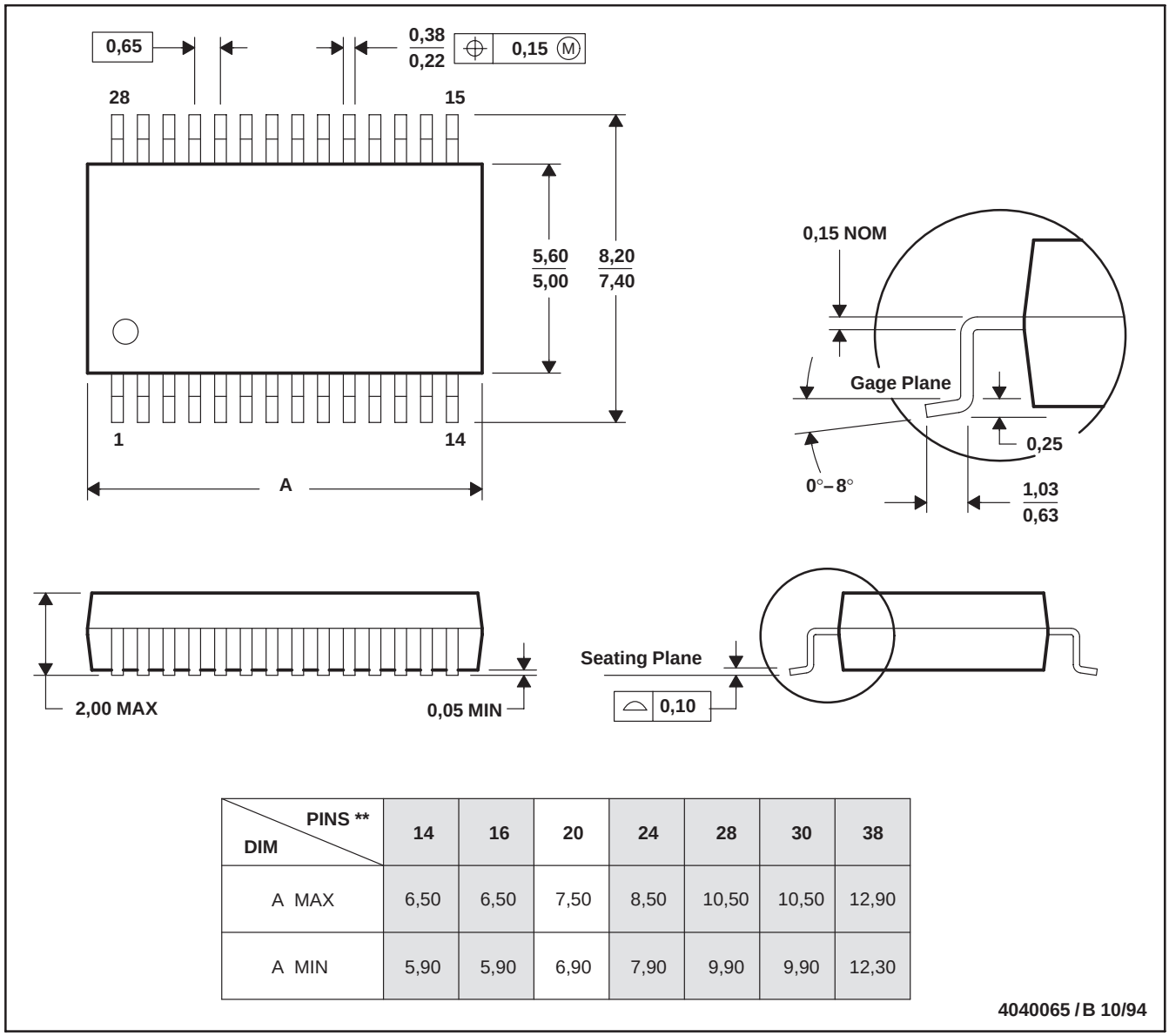
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- $R_S$ must be real at the input frequency.

**Figure 18. Equivalent Input Circuit Including the Driving Source**

## MECHANICAL DATA

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**28 PIN SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

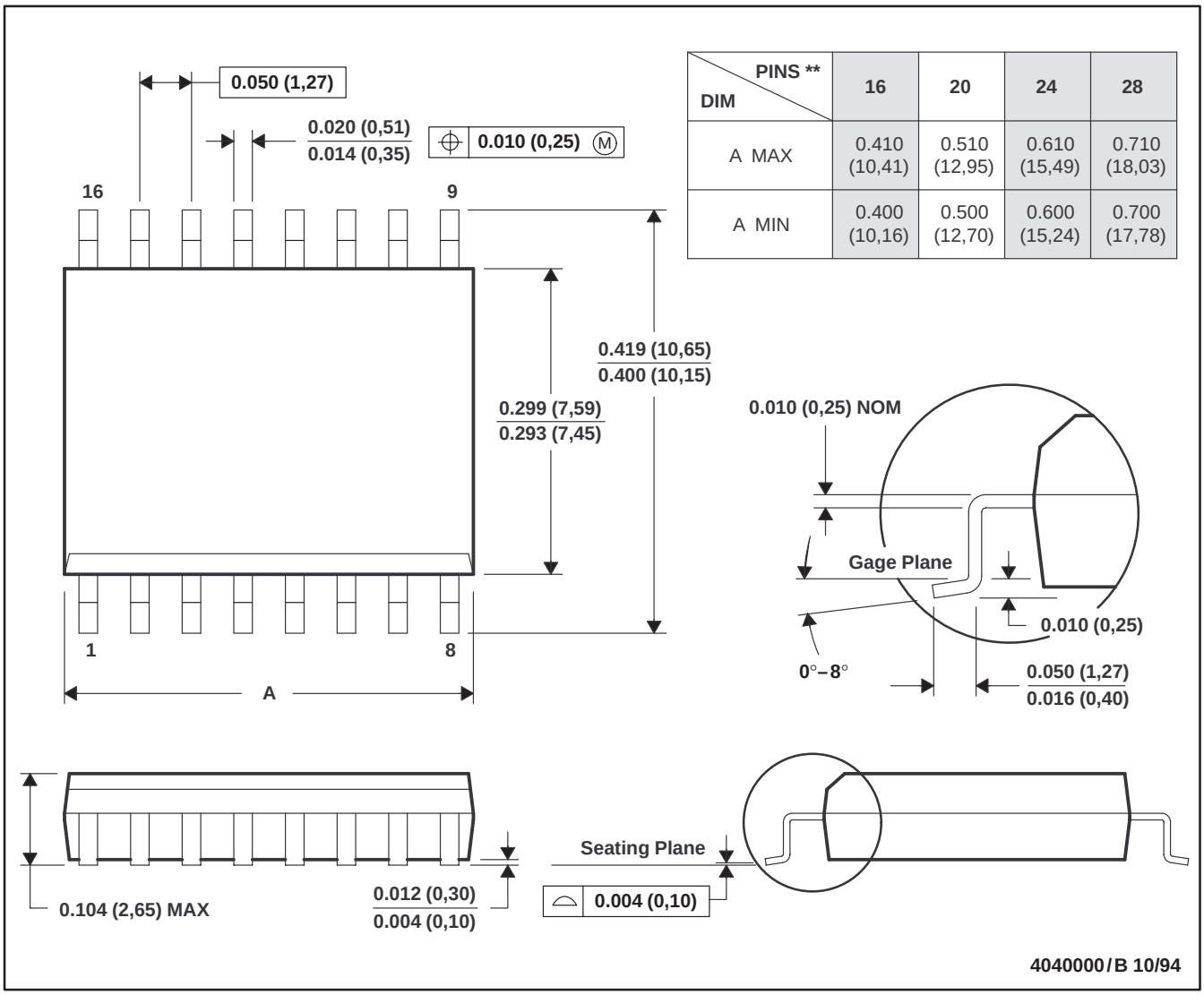
**4040065 / B 10/94**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

## MECHANICAL DATA

**DW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**16 PIN SHOWN**



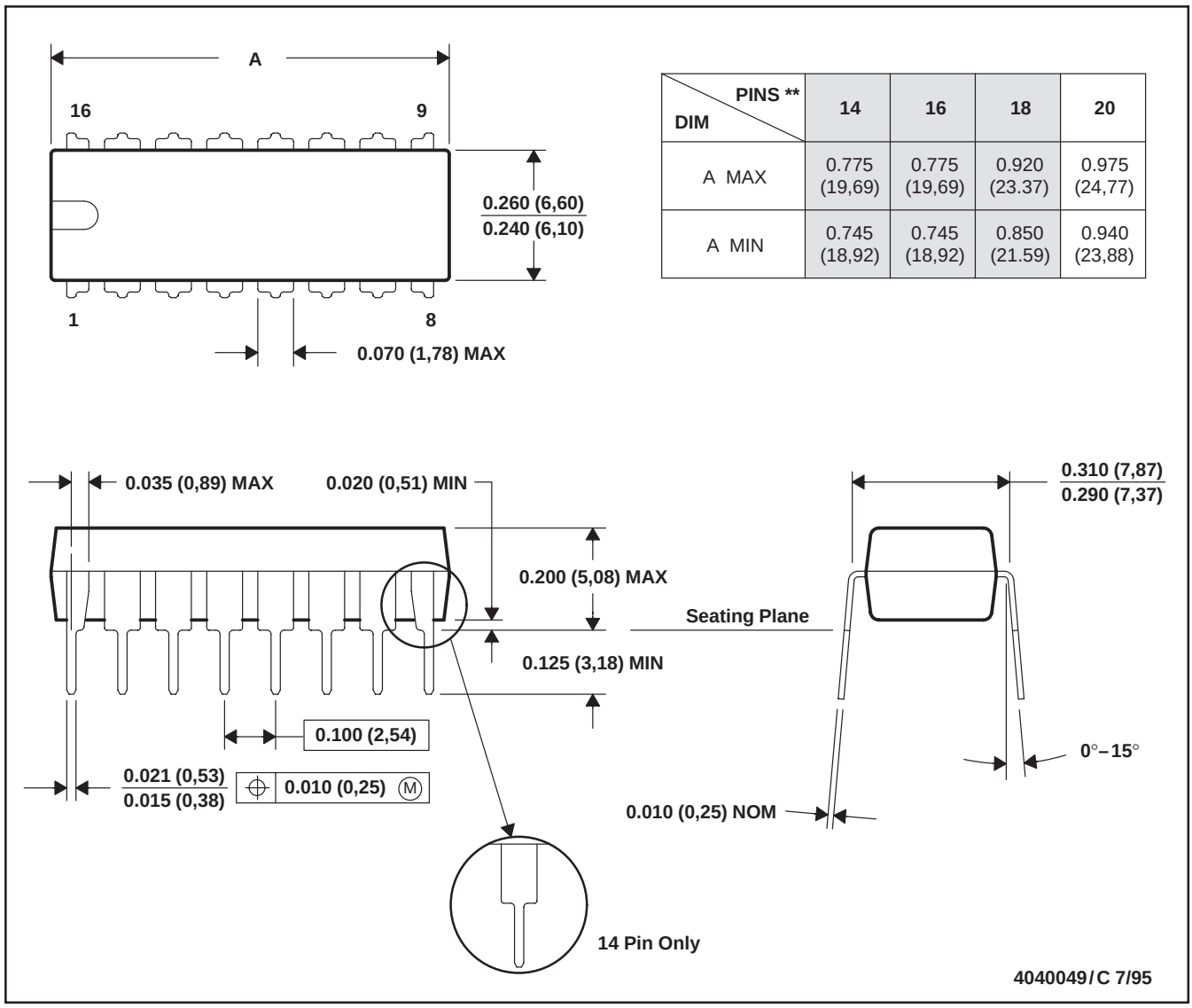

| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

## MECHANICAL DATA

**N (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**16 PIN SHOWN**




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23.37) | 0.975 (24,77) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21.59) | 0.940 (23,88) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2543CDB | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV2543 |
| TLV2543CDB.A | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV2543 |
| TLV2543CDBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TV2543 |
| TLV2543CDBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TV2543 |
| TLV2543CDW | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TLV2543C |
| TLV2543CDW.A | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV2543C |
| TLV2543CN | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | - | TLV2543CN |
| TLV2543CN.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TLV2543CN |
| TLV2543IDB | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TY2543 |
| TLV2543IDB.A | Active | Production | SSOP (DB) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TY2543 |
| TLV2543IDBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TY2543 |
| TLV2543IDBR.A | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TY2543 |
| TLV2543IDW | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | - | TLV2543I |
| TLV2543IDW.A | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV2543I |
| TLV2543IDWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | TLV2543I |
| TLV2543IDWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLV2543I |
| TLV2543IN | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | - | TLV2543IN |
| TLV2543IN.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | TLV2543IN |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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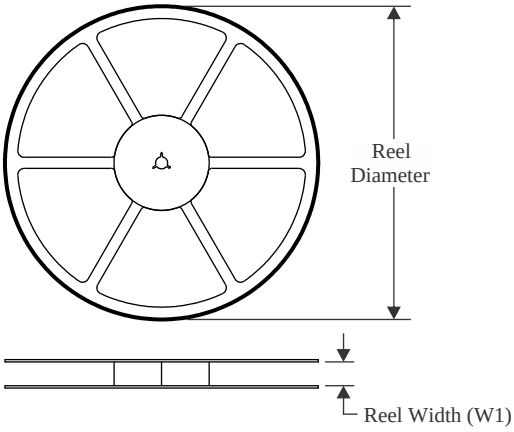
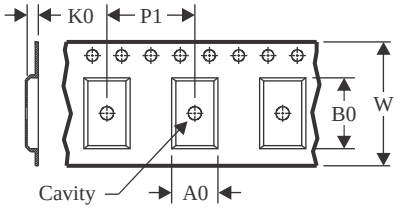
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

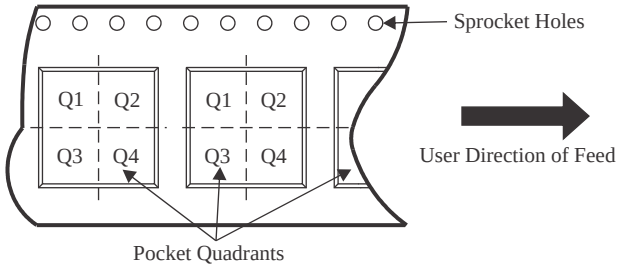



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

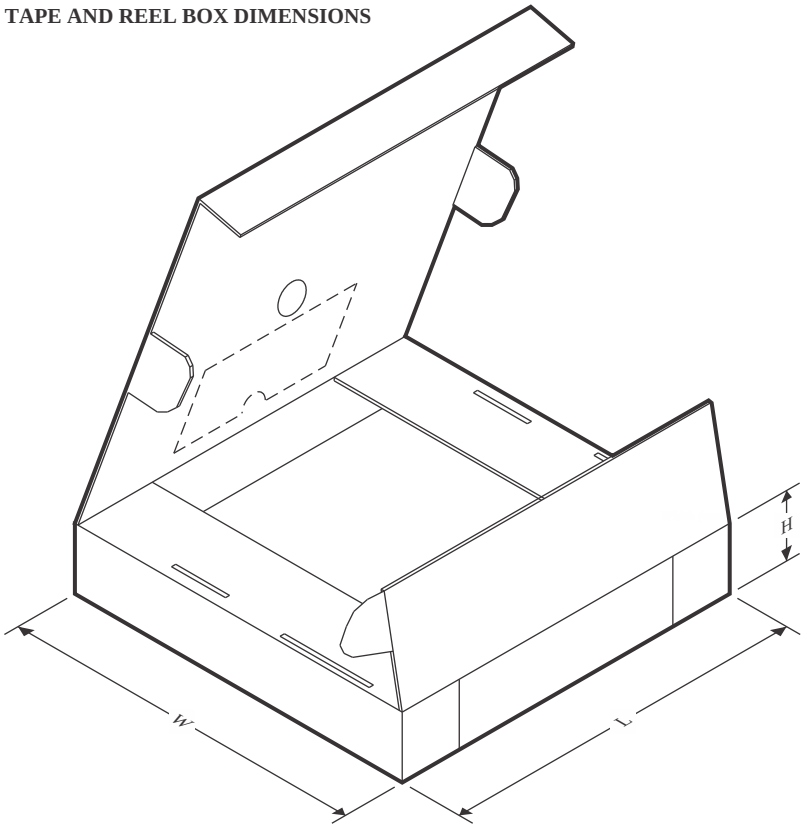
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2543CDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TLV2543IDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TLV2543IDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

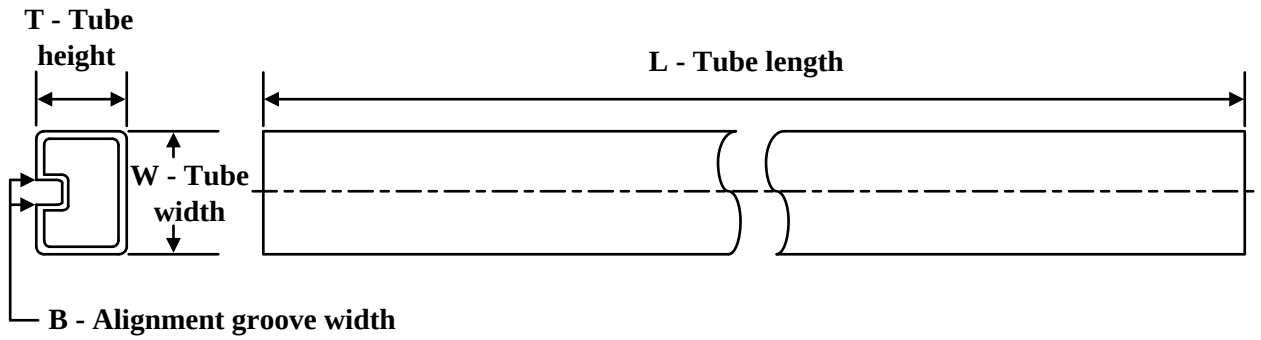
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2543CDBR | SSOP | DB | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TLV2543IDBR | SSOP | DB | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| TLV2543IDWR | SOIC | DW | 20 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TLV2543CDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543CDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543CDB.A | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543CDB.A | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543CDBR | DB | SSOP | 20 | 2000 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543CDBR.A | DB | SSOP | 20 | 2000 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543CDW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| TLV2543CDW.A | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| TLV2543CN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| TLV2543CN.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| TLV2543IDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543IDB | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543IDB.A | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543IDB.A | DB | SSOP | 20 | 70 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543IDBR | DB | SSOP | 20 | 2000 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543IDBR.A | DB | SSOP | 20 | 2000 | 530 | 10.5 | 4000 | 4.1 |
| TLV2543IDW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| TLV2543IDW.A | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| TLV2543IN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| TLV2543IN.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

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