# TLV349x 1.8-V, Nanopower, Push-Pull Output Comparator

## 1 Features

- Very Low Supply Current: 0.8 µA (Typical)
- Input Common-Mode Range: 200-mV Beyond Supply Rails
- Supply Voltage: 1.8 V to 5.5 V
- High Speed: 6 µs
- Push-Pull CMOS Output Stage
- Small Packages:
  - 5-Pin SOT-23 (Single)
  - 8-Pin SOT-23 (Dual)

## 2 Applications

- Portable Medical Equipment
- Wireless Security Systems
- Remote Control Systems
- Handheld Instruments
- Ultra-Low Power Systems

## 3 Description

The TLV349x family of push-pull output comparators features a fast 6-µs response time and < 1.2-µA (maximum) nanopower capability, allowing operation from 1.8 V to 5.5 V. Input common-mode range beyond supply rails make the TLV349x an ideal choice for low-voltage applications.

Micro-sized packages provide options for portable and space-restricted applications. The single (TLV3491) is available in 5-pin SOT-23 and 8-pin SOIC packages. The dual (TLV3492) comes in 8-pin SOT-23 and SOIC packages. The quad (TLV3494) is available in both 14-pin TSSOP and SOIC packages.

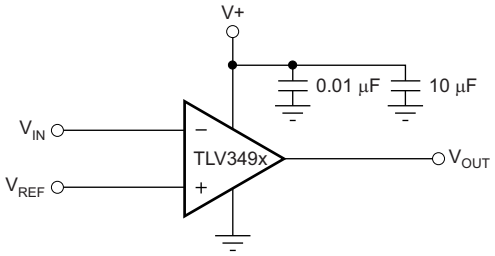
The TLV349x is excellent for power-sensitive, low-voltage (two-cell) applications.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV3491 | SOT-23 (5) | 2.90 mm × 1.60 mm |
| | SOIC (8) | 4.90 mm × 3.91 mm |
| TLV3492 | SOT-23 (8) | 2.90 mm × 1.63 mm |
| | SOIC (8) | 4.90 mm × 3.91 mm |
| TLV3494 | SOIC (14) | 8.65 mm × 3.91 mm |
| | TSSOP (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**TLV349x Basic Connections**




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## 4 Revision History

**Changes from Revision D (April 2005) to Revision E** **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed *Related Products* To: *Device Comparison* ... 3
- Deleted *Package/Ordering Information* table; see *Package Option Addendum* at the end of the data sheet ... 3
- Deleted Lead temperature from *Absolute Maximum Ratings* ... 5
- Changed Thermal Resistance, $R_{\theta JA}$, in *Thermal Information: TLV3491* From: 200°C/W To: 237.8°C/W (SOT-23) and From: 150°C/W To: 201.9°C/W (SOIC) ... 5
- Changed Thermal Resistance, $R_{\theta JA}$, in *Thermal Information: TLV3492* From: 200°C/W To: 135.4°C/W (SOT-23) and From: 150°C/W To: 201.9°C/W (SOIC) ... 5
- Changed Thermal Resistance, $R_{\theta JA}$, in *Thermal Information: TLV3494* From: 100°C/W To: 83.8°C/W (SOIC) and From: 100°C/W To: 120.8°C/W (TSSOP) ... 6

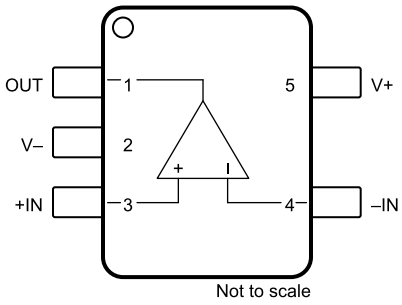

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## 5 Device Comparison Table

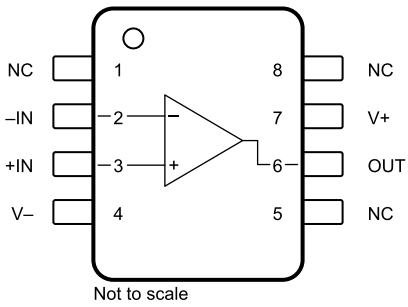
| PRODUCT | FEATURES |
|---|---|
| TLV370x | 560-nA, 2.5-V to 16-V, push-pull CMOS output stage comparators |
| TLV340x | 550-nA, 2.5-V to 16-V, open-drain output stage comparators |

## 6 Pin Configuration and Functions

**TLV3491 DBV Package**
**5-Pin SOT-23**
**Top View**



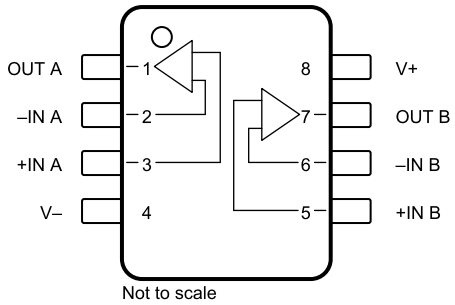

**TLV3491 D Package**
**8-Pin SOIC**
**Top View**




**Pin Functions: TLV3491**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOT-23 | SOIC | | |
| –IN | 4 | 2 | I | Inverting input |
| +IN | 3 | 3 | I | Noninverting input |
| NC | — | 1, 5, 8 | — | No internal connection (can be left floating) |
| OUT | 1 | 6 | O | Output |
| V+ | 5 | 7 | — | Positive (highest) power supply |
| V– | 2 | 4 | — | Negative (lowest) power supply |

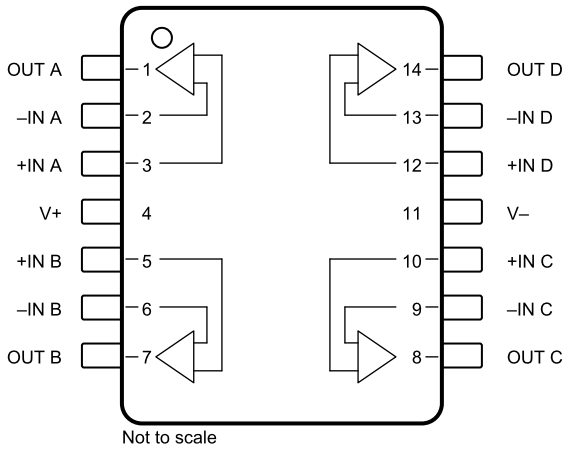
**TLV3492 DCN and D Packages**
**8-Pin SOT-23 and SOIC**
**Top View**



## Pin Functions: TLV3492

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V– | 4 | — | Negative (lowest) power supply |
| V+ | 8 | — | Positive (highest) power supply |

**TLV3494 D and PW Packages**
**14-Pin SOIC and TSSOP**
**Top View**




Not to scale

## Pin Functions: TLV3494

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –In A | 2 | I | Inverting input, channel A |
| –In B | 6 | I | Inverting input, channel B |
| –In C | 9 | I | Inverting input, channel C |
| –In D | 13 | I | Inverting input, channel D |
| +In A | 3 | I | Noninverting input, channel A |
| +In B | 5 | I | Noninverting input, channel B |
| +In C | 10 | I | Noninverting input, channel C |
| +In D | 12 | I | Noninverting input, channel D |
| Out A | 1 | O | Output, channel A |
| Out B | 7 | O | Output, channel B |
| Out C | 8 | O | Output, channel C |
| Out D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) power supply |
| V+ | 4 | — | Positive (highest) power supply |


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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply | | 5.5 | V |
| | Signal input pin | (V–) – 0.5 | (V+) + 0.5 | V |
| Current | Signal input pin | –10 | 10 | mA |
| | Output short circuit | Continuous | | |
| Temperature | Operating, $T_A$ | –40 | 125 | °C |
| | Junction, $T_J$ | | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±3000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | Supply voltage | 1.8 | 5.5 | V |
| $T_A$ | Specified temperature | –40 | 125 | °C |

## 7.4 Thermal Information: TLV3491

| THERMAL METRIC(1) | | TLV3491 | | UNIT |
|---|---|---|---|---|
| | | DBV (SOT-23) | D (SOIC) | |
| | | 5 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 237.8 | 201.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 108.7 | 92.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 64.1 | 123.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 12.1 | 23 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 63.3 | 212.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Thermal Information: TLV3492

| THERMAL METRIC(1) | | TLV3492 | | UNIT |
|---|---|---|---|---|
| | | DCN (SOT-23) | D (SOIC) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 135.4 | 201.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 68.1 | 92.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 48.9 | 123.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.9 | 23 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.4 | 212.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 7.6 Thermal Information: TLV3494

| THERMAL METRIC[1] | | TLV3494 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 83.8 | 120.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 70.7 | 34.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 59.5 | 62.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 11.6 | 1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 37.7 | 56.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.7 Electrical Characteristics: $V_S$ = 1.8 V to 5.5 V

at $T_A$ = 25°C and $V_S$ = 1.8 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C, $V_{CM}$ = 0 V, $I_O$ = 0 V | | ±3 | ±15 | mV |
| $dV_{OS}/dT$ | Input offset voltage versus temperature | $T_A$ = –40°C to 125°C | | ±12 | | µV/°C |
| PSRR | Input offset voltage versus power supply | $V_S$ = 1.8 V to 5.5 V | | 350 | 1000 | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $V_{CM}$ = $V_{CC}$/2 | | ±1 | ±10 | pA |
| $I_{OS}$ | Input offset current | $V_{CM}$ = $V_{CC}$/2 | | ±1 | ±10 | pA |
| **INPUT VOLTAGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage | | (V–) – 0.2 V | | (V+) + 0.2 V | V |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = –0.2 V to (V+) – 1.5 V | 60 | 74 | | dB |
| | | $V_{CM}$ = –0.2 V to (V+) + 0.2 V | 54 | 62 | | |
| **INPUT CAPACITANCE** | | | | | | |
| | Common-mode | | | 2 | | pF |
| | Differential | | | 4 | | pF |
| **OUTPUT ($V_S$ = 5 V)** | | | | | | |
| $V_{OH}$ | Voltage output high from rail | $I_{OUT}$ = 5 mA | | 90 | 200 | mV |
| $V_{OL}$ | Voltage output low from rail | $I_{OUT}$ = 5 mA | | 160 | 200 | mV |
| $I_{SC}$ | Short-circuit current | | See *Typical Characteristics* | | | |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage | | 1.8 | | 5.5 | V |
| | Operating voltage | | 1.8 | | 5.5 | V |
| $I_Q$ | Quiescent current[1] | $V_O$ = 5 V, $V_O$ = high | | 0.85 | 1.2 | µA |

(1) $I_Q$ per channel

## 7.8 Switching Characteristics

at f = 10 kHz, $V_{STEP}$ = 1 V, $T_A$ = 25°C, and $V_S$ = 1.8 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(PLH)}$ | Propagation delay time, low-to-high | Input overdrive = 10 mV | | 12 | | µs |
| | | Input overdrive = 100 mV | | 6 | | |
| $t_{(PLH)}$ | Propagation delay time, high-to-low | Input overdrive = 10 mV | | 13.5 | | µs |
| | | Input overdrive = 100 mV | | 6.5 | | |
| $t_R$ | Rise time | $C_L$ = 10 pF | | 100 | | ns |
| $t_F$ | Fall time | $C_L$ = 10 pF | | 100 | | ns |


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## 7.9 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 1.8 V to 5.5 V, and input overdrive = 100 mV (unless otherwise noted)

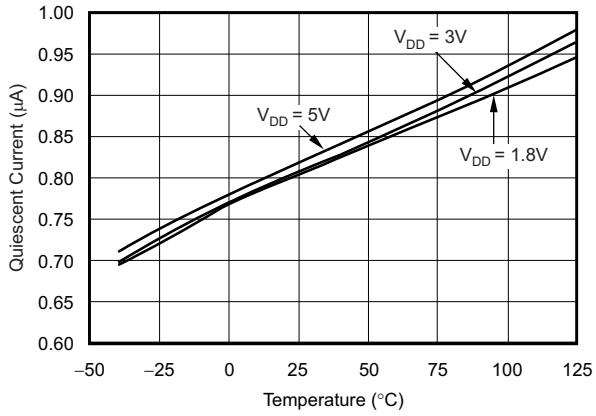



**Figure 1. Quiescent Current vs Temperature**

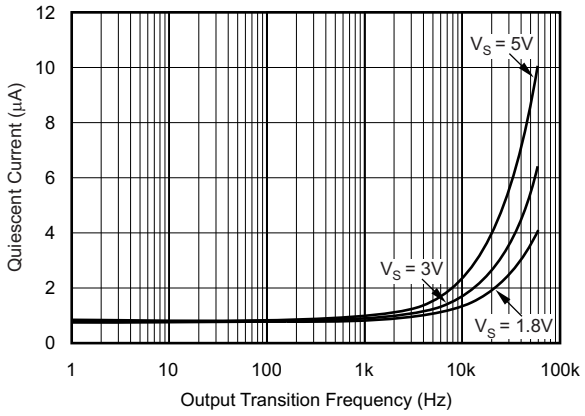



**Figure 2. Quiescent Current vs Output Switching Frequency**

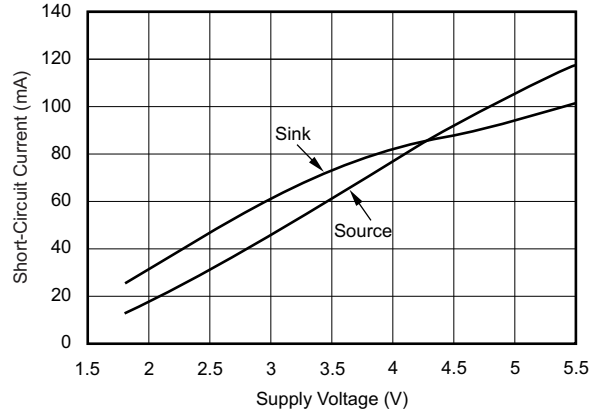



**Figure 3. Short-Circuit Current vs Supply Voltage**

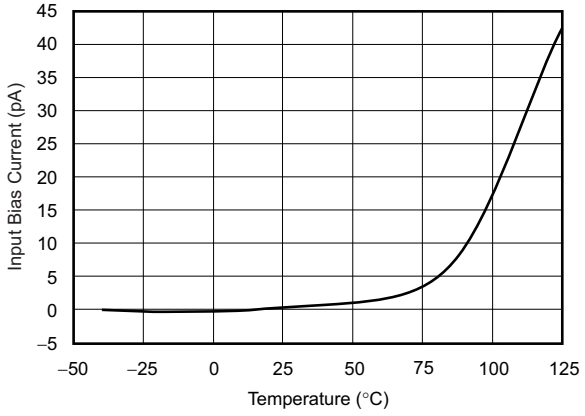



**Figure 4. Input Bias Current vs Temperature**

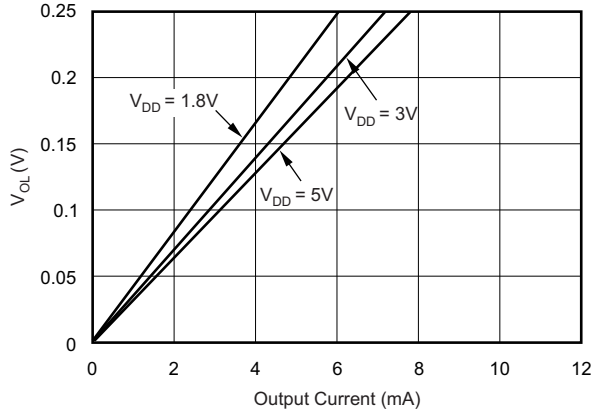



**Figure 5. Output Low vs Output Current**

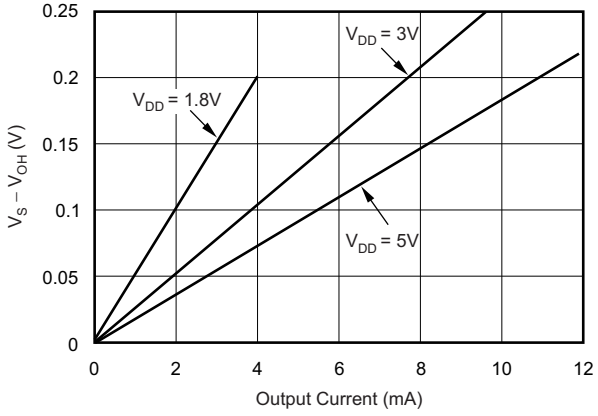



**Figure 6. Output High vs Output Current**

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## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 1.8 V to 5.5 V, and input overdrive = 100 mV (unless otherwise noted)

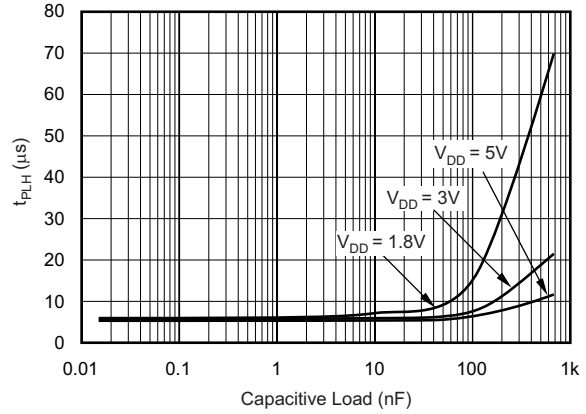



**Figure 7. Propagation Delay ($t_{PLH}$) vs Capacitive Load**

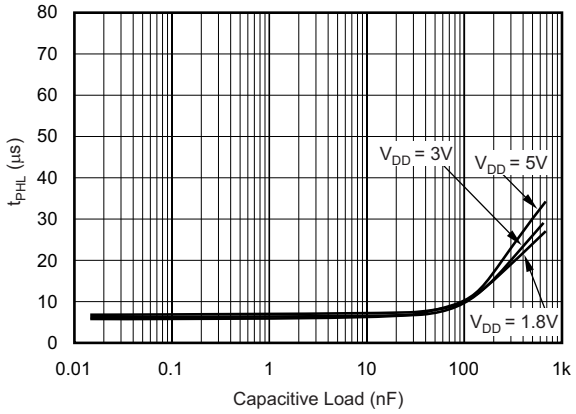



**Figure 8. Propagation Delay ($t_{PHL}$) vs Capacitive Load**

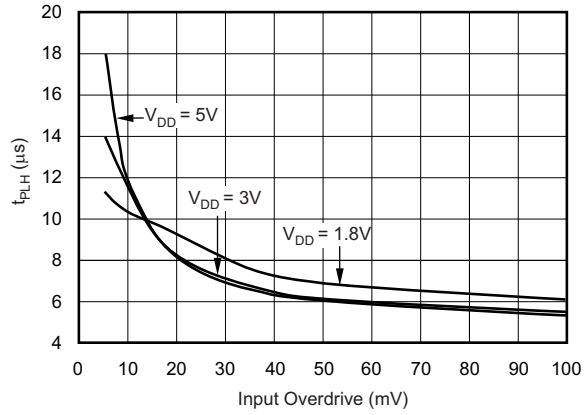



**Figure 9. Propagation Delay ($t_{PLH}$) vs Input Overdrive**

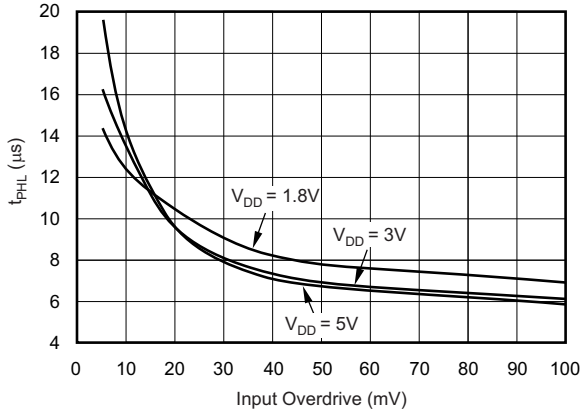



**Figure 10. Propagation Delay ($t_{PHL}$) vs Input Overdrive**

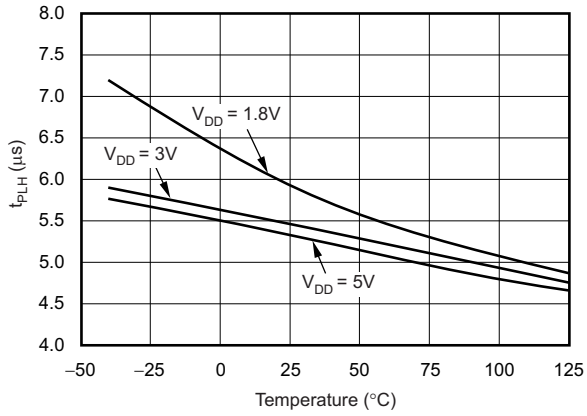



**Figure 11. Propagation Delay ($t_{PLH}$) vs Temperature**

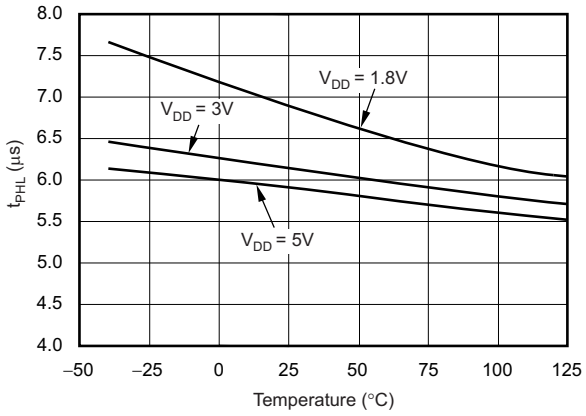



**Figure 12. Propagation Delay ($t_{PHL}$) vs Temperature**


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## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 1.8 V to 5.5 V, and input overdrive = 100 mV (unless otherwise noted)

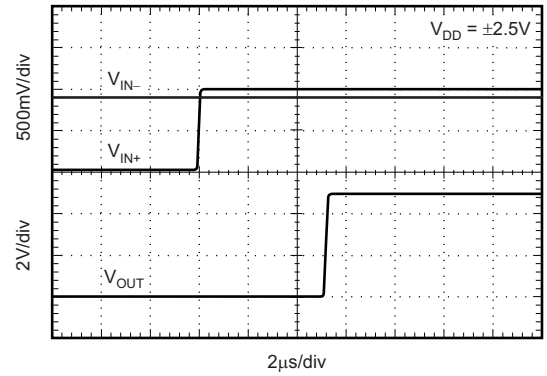



**Figure 13. Propagation Delay ($t_{PLH}$)**

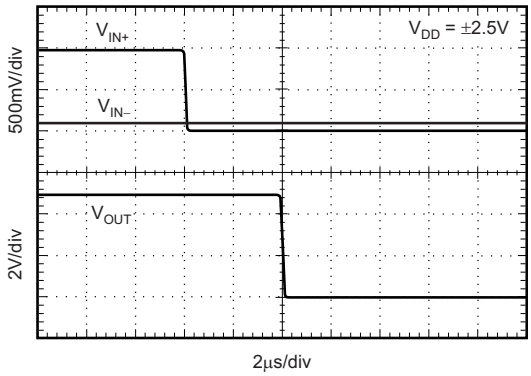



**Figure 14. Propagation Delay ($t_{PHL}$)**

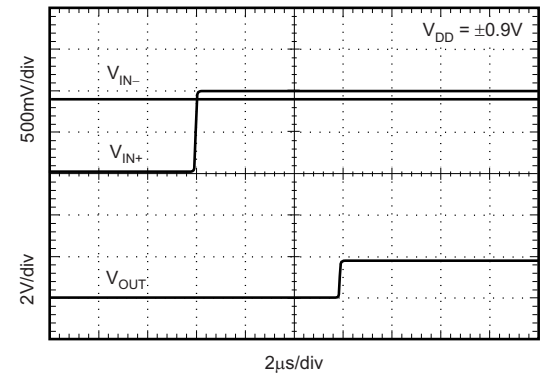



**Figure 15. Propagation Delay ($t_{PLH}$)**

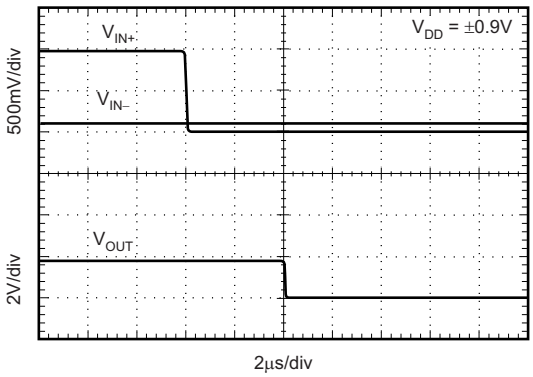


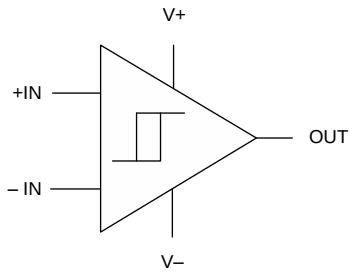

**Figure 16. Propagation Delay ($t_{PHL}$)**

# 8 Detailed Description

## 8.1 Overview

The TLV349x family of comparators features rail-to-rail input and output on supply voltages as low as 1.8 V. The push-pull output stage is optimal for reduced power budget applications and features no shoot-through current. Low supply voltages, common-mode input range beyond supply rails, and a typical supply current of 0.8 µA make the TLV349x family an excellent candidate for battery-powered applications with single-cell operation as well as a wide range of low-voltage applications. The devices are available in a selection of micro-sized packages for space-constrained and portable applications.

## 8.2 Functional Block Diagram




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## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLV349x comparators are specified for use on a single supply from 1.8 V to 5.5 V (or a dual supply from ±0.9 V to ±2.75 V) over a temperature range of −40°C to 125°C.

### 8.3.2 Input Overvoltage Protection

The device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 500 mV. Momentary voltages greater than 500 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the input to the comparator.

### 8.3.3 Setting Reference Voltage

It is important to use a stable reference when setting the transition point for the TLV349x. The REF1004 provides a 1.25-V reference voltage with low drift and only 8 µA of quiescent current.

### 8.3.4 External Hysteresis

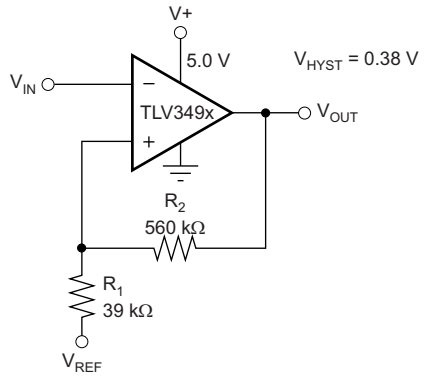
Comparator inputs have no noise immunity within the range of specified offset voltage (±15 mV). For noisy input signals, the comparator output typically displays multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV349x is ±15 mV. To prevent multiple switching within the comparator threshold of the TLV349x, external hysteresis must be added by connecting a small amount of feedback to the positive input. Figure 17 shows a typical topology used to introduce hysteresis, described in Equation 1.

$$V_{HYST} = \frac{V^{+} \times R_1}{R_1 + R_2} \quad (1)$$

$V_{HYST}$ sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.


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## Feature Description (continued)




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**Figure 17. Adding Hysteresis to the TLV349x**

## 8.4 Device Functional Modes

The TLV349x has a single functional mode and is operational when the power-supply voltage is between 1.8 V and 5.5 V.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLV349x family of comparators features rail-to-rail input and output on supply voltages as low as 1.8 V. The push-pull output stage is optimal for reduced power budget applications and features no shoot-through current. Low supply voltages, common-mode input range beyond supply rails, and a typical supply current of 0.8 µA make the TLV349x family an excellent candidate for battery-powered applications with single-cell operation.

## 9.2 Typical Applications

### 9.2.1 TLV3491 Configured as an AC-Coupled Comparator

One of the benefits of AC coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 18 shows the TLV3491 configured as an AC-coupled comparator.

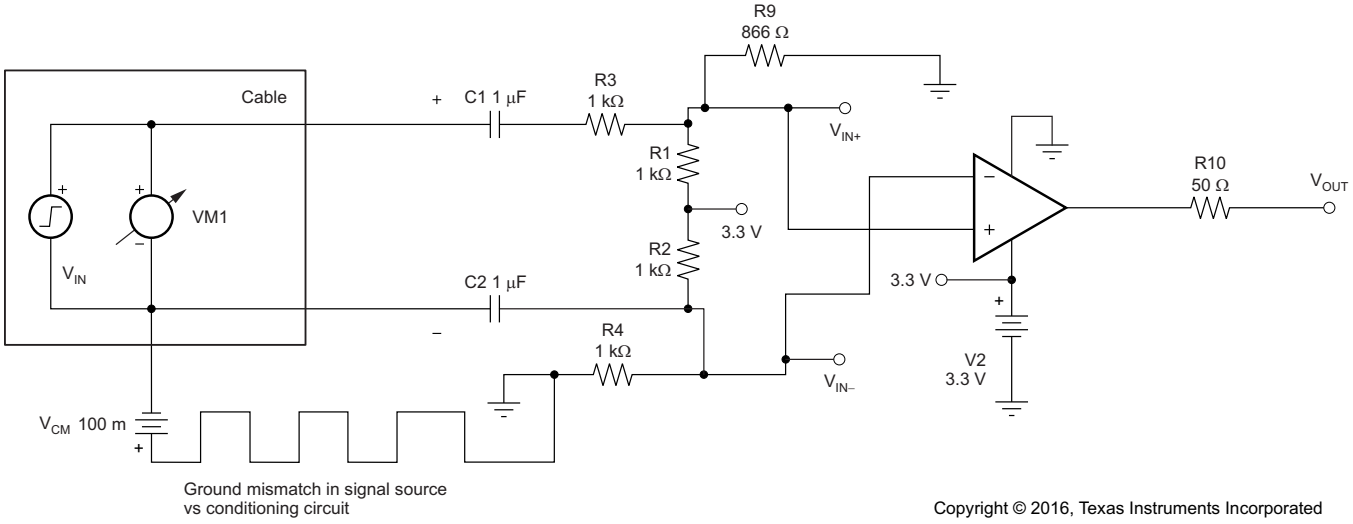



**Figure 18. TLV3491 Configured as an AC-Coupled Comparator (Schematic)**

#### *9.2.1.1 Design Requirements*

Design requirements include:

1. Ability to tolerate up to ±100 mV of common-mode signal.
2. Trigger only on AC signals (such as zero-cross detection).


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## Typical Applications (continued)

### 9.2.1.2 Detailed Design Procedure

Design analysis:

- AC-coupled, high-pass frequency
- Large capacitors require longer start-up time from device power on
- Use 1-µF capacitor to achieve high-pass frequency of approximately 159 Hz
- For high-pass equivalent, use $C_{IN}$ = 0.5 µF, $R_{IN}$ = 2 kΩ

1. Set up input dividers initially for one-half supply (to be in center of acceptable common-mode range).
2. Adjust either divider slightly upwards or downwards as desired to establish quiescent output condition.
3. Select coupling capacitors based on lowest expected frequency.

### 9.2.1.3 Application Curve

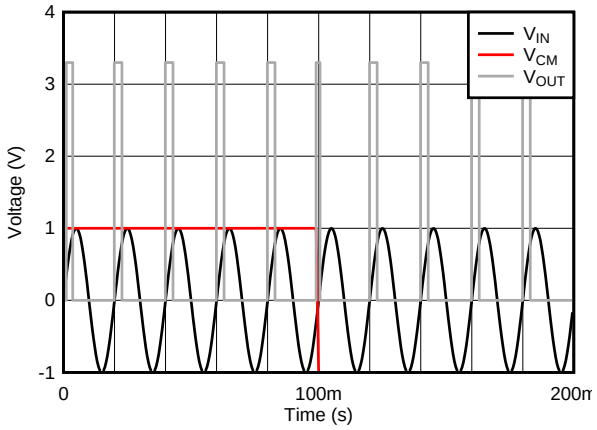



**Figure 19. AC-Coupled Comparator Results**

### 9.2.2 Relaxation Oscillator

The TLV349x can be configured as a relaxation oscillator to provide a simple and inexpensive clock output, as Figure 20 shows. The capacitor is charged at a rate of 0.69 RC. It also discharges at a rate of 0.69RC. Therefore, the period is 1.38 RC. $R_1$ may be a different value than $R_2$.

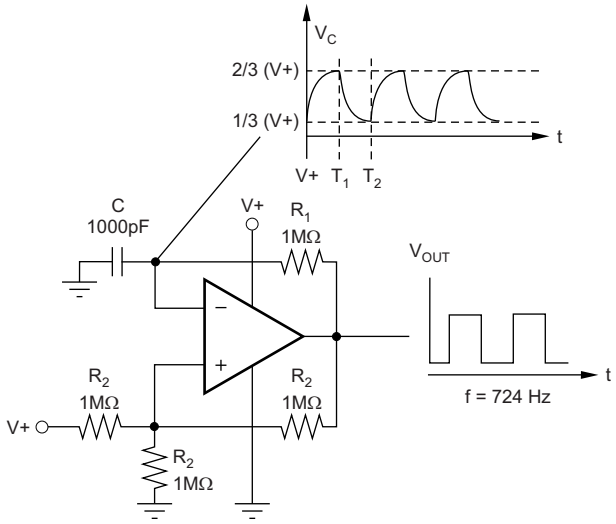



**Figure 20. TLV349x Configured as a Relaxation Oscillator**

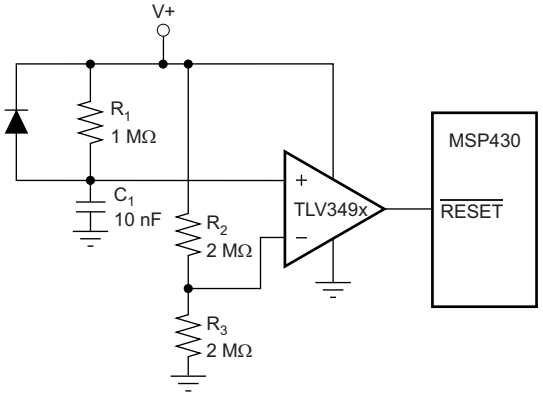
## Typical Applications (continued)

### 9.2.3 Power-On Reset

The reset circuit shown in Figure 21 provides a time-delayed release of reset to the MSP430 microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by a simple resistor divider.

These resistor values must be relatively high to reduce the current consumption of the circuit. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state and releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values.

Use of a lower-valued resistor in this portion of the circuit does not increase current consumption because no current flows through the RC circuit after the supply has stabilized. The required reset delay time depends on the power-up characteristics of the system power supply. $R_1$ and $C_1$ are selected to allow enough time for the power supply to stabilize. $D_1$ provides rapid reset if power is lost. In this example, the $R_1 \times C_1$ time constant is 10 ms.




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**Figure 21. The TLV349x Configured as a Reset Circuit for the MSP430**


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# 10 Power Supply Recommendations

The TLV349x family of devices is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in *Typical Characteristics*.

# 11 Layout

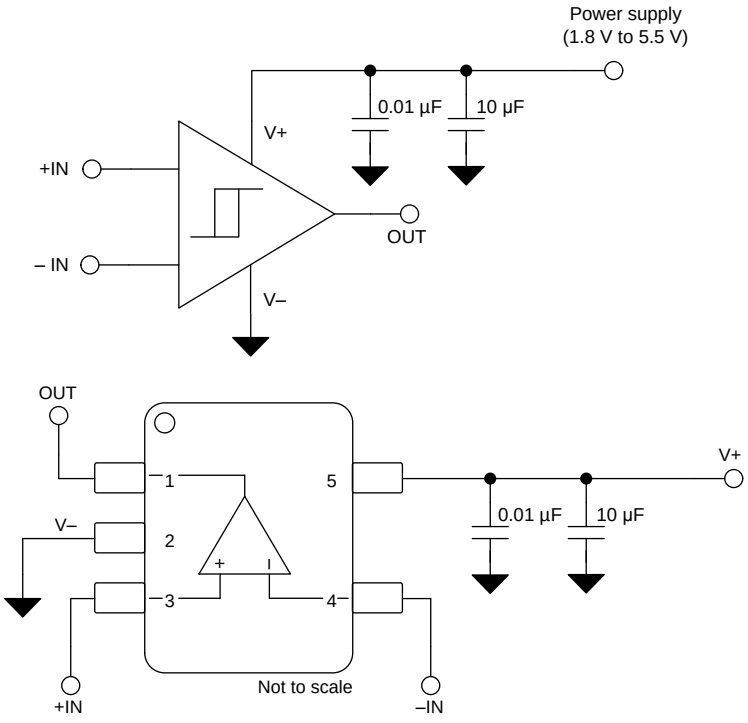
## 11.1 Layout Guidelines

Figure 22 shows the typical connections for the TLV349x. To minimize supply noise, power supplies must be capacitively decoupled by a 0.01-µF ceramic capacitor in parallel with a 10-µF electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (the use of a ground plane) helps to maintain the specified performance of the TLV349x family.

For best results, maintain the following layout guidelines:

1. Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to $V_{CC}$.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

## 11.2 Layout Example




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**Figure 22. Basic Connections of the TLV349x**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Development Support

#### *12.1.1.1 TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

#### *12.1.1.2 DIP Adapter EVM*

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

#### *12.1.1.3 Universal Op Amp EVM*

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

**NOTE**

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

#### *12.1.1.4 TI Precision Designs*

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

#### *12.1.1.5 WEBENCH® Filter Designer*

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.


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## 12.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV3491 | Click here | Click here | Click here | Click here | Click here |
| TLV3492 | Click here | Click here | Click here | Click here | Click here |
| TLV3494 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

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## 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV3491AID | Last Time Buy | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3491 |
| TLV3491AID.B | Last Time Buy | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3491 |
| TLV3491AIDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDBVRG4 | Last Time Buy | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDBVRG4.B | Last Time Buy | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDBVT | Last Time Buy | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDBVT.B | Last Time Buy | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDBVTG4 | Last Time Buy | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | VBNI |
| TLV3491AIDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3491 |
| TLV3491AIDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3491 |
| TLV3492AID | Last Time Buy | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3492 |
| TLV3492AID.B | Last Time Buy | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3492 |
| TLV3492AIDCNR | Active | Production | SOT-23 (DCN) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 |
| TLV3492AIDCNR.B | Active | Production | SOT-23 (DCN) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 |
| TLV3492AIDCNRG4 | Last Time Buy | Production | SOT-23 (DCN) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 |
| TLV3492AIDCNRG4.B | Last Time Buy | Production | SOT-23 (DCN) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 |
| TLV3492AIDCNT | Last Time Buy | Production | SOT-23 (DCN) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV3492AIDCNT.B | Last Time Buy | Production | SOT-23 (DCN) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBO1 |
| TLV3492AIDG4 | Last Time Buy | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3492 |
| TLV3492AIDG4.B | Last Time Buy | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3492 |
| TLV3492AIDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3492 |
| TLV3492AIDR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3492 |
| TLV3494AID | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV3494 |
| TLV3494AID.B | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV3494 |
| TLV3494AIPWR | Active | Production | TSSOP (PW) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3494 |
| TLV3494AIPWR.B | Active | Production | TSSOP (PW) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3494 |
| TLV3494AIPWT | Last Time Buy | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3494 |
| TLV3494AIPWT.B | Last Time Buy | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3494 |
| TLV3494AIPWTG4 | Last Time Buy | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3494 |
| TLV3494AIPWTG4.B | Last Time Buy | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 3494 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

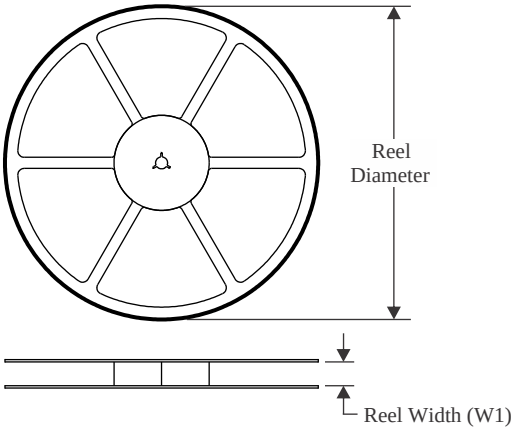
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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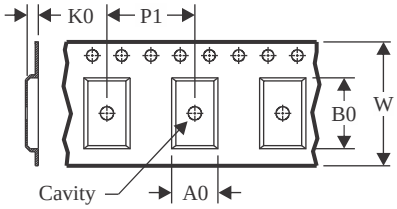
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

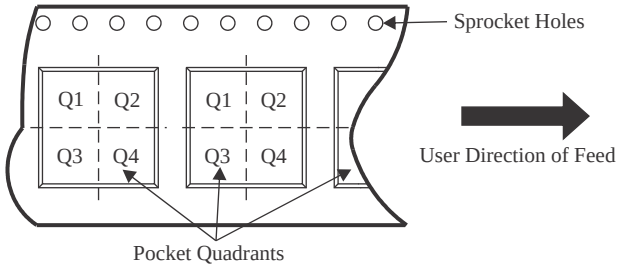



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

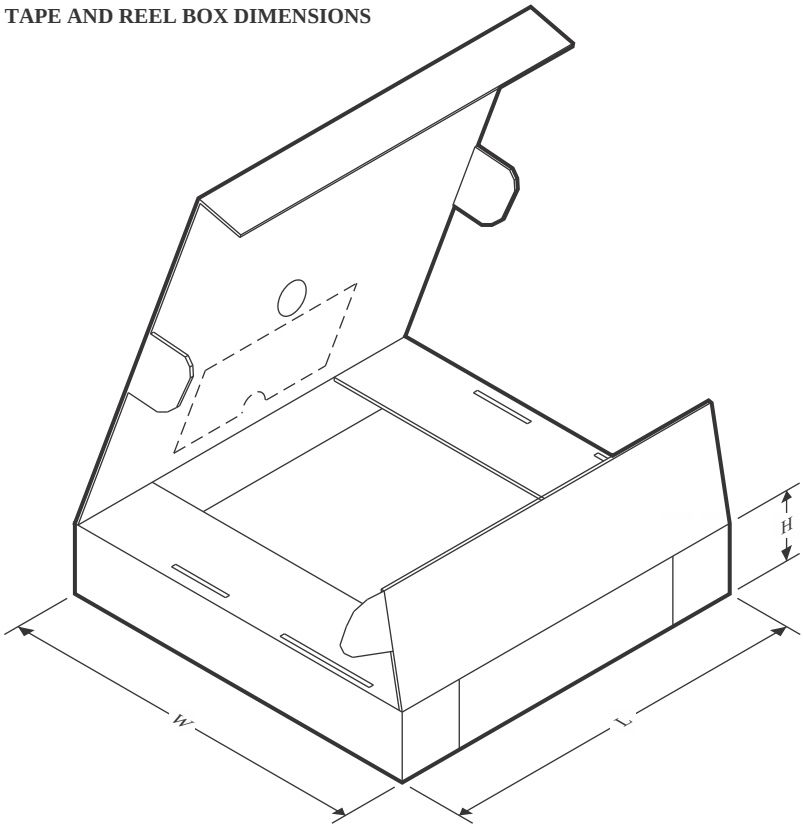
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3491AIDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3491AIDBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3491AIDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3491AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3492AIDCNR | SOT-23 | DCN | 8 | 3000 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| TLV3492AIDCNRG4 | SOT-23 | DCN | 8 | 3000 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| TLV3492AIDCNT | SOT-23 | DCN | 8 | 250 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |
| TLV3492AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3494AIPWR | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV3494AIPWT | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV3494AIPWTG4 | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

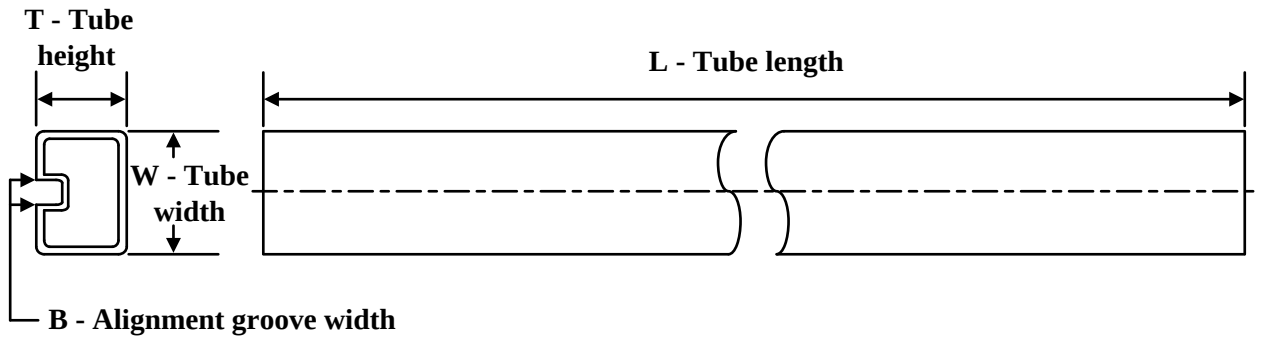
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV3491AIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV3491AIDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV3491AIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TLV3491AIDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV3492AIDCNR | SOT-23 | DCN | 8 | 3000 | 213.0 | 191.0 | 35.0 |
| TLV3492AIDCNRG4 | SOT-23 | DCN | 8 | 3000 | 213.0 | 191.0 | 35.0 |
| TLV3492AIDCNT | SOT-23 | DCN | 8 | 250 | 213.0 | 191.0 | 35.0 |
| TLV3492AIDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV3494AIPWR | TSSOP | PW | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV3494AIPWT | TSSOP | PW | 14 | 250 | 213.0 | 191.0 | 35.0 |
| TLV3494AIPWTG4 | TSSOP | PW | 14 | 250 | 213.0 | 191.0 | 35.0 |

## TUBE




*All dimensions are nominal

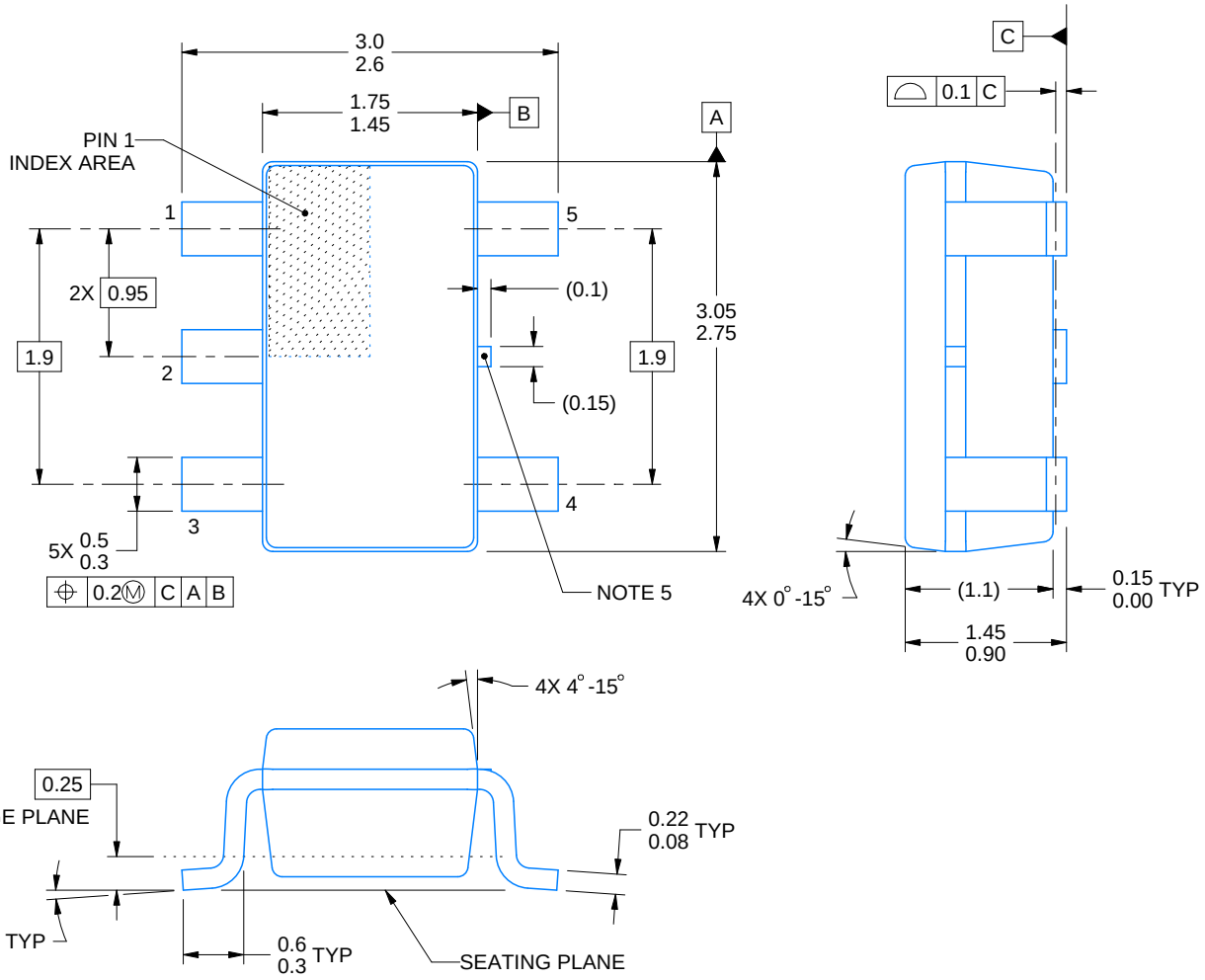
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TLV3491AID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV3491AID.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV3492AID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV3492AID.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV3492AIDG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV3492AIDG4.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| TLV3494AID | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TLV3494AID.B | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

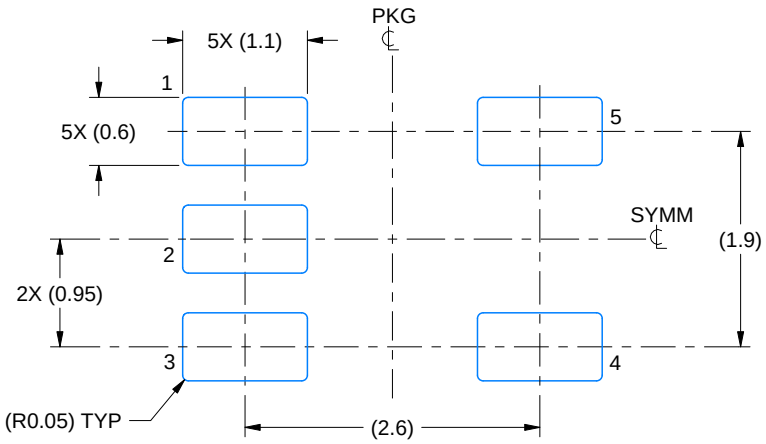
SMALL OUTLINE TRANSISTOR



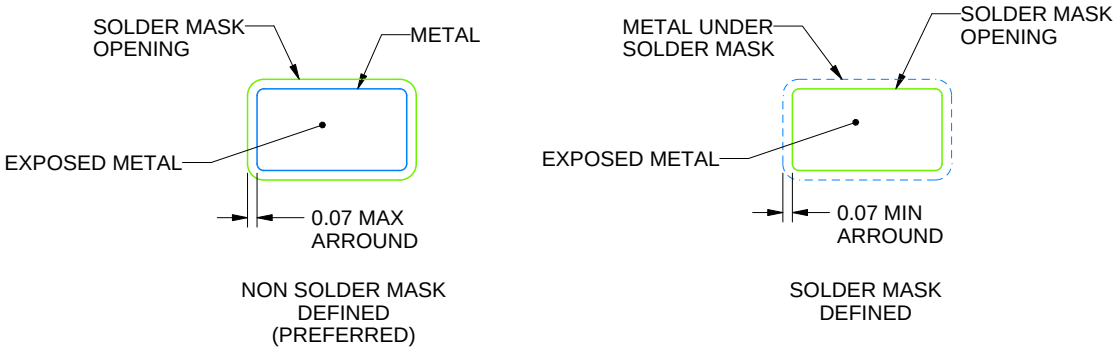

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

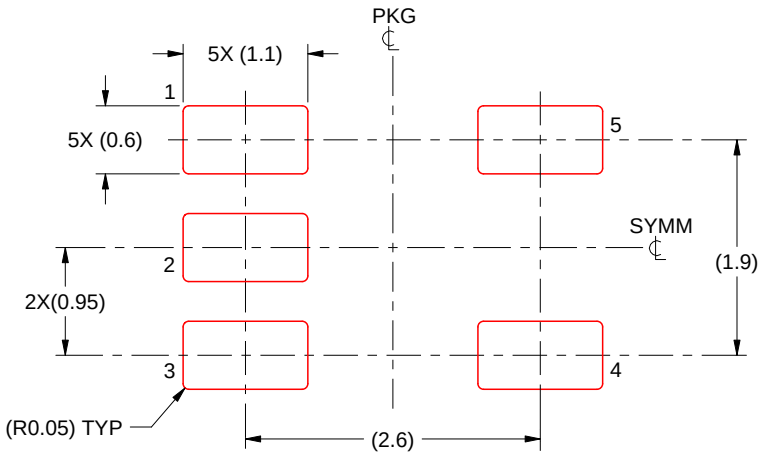



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



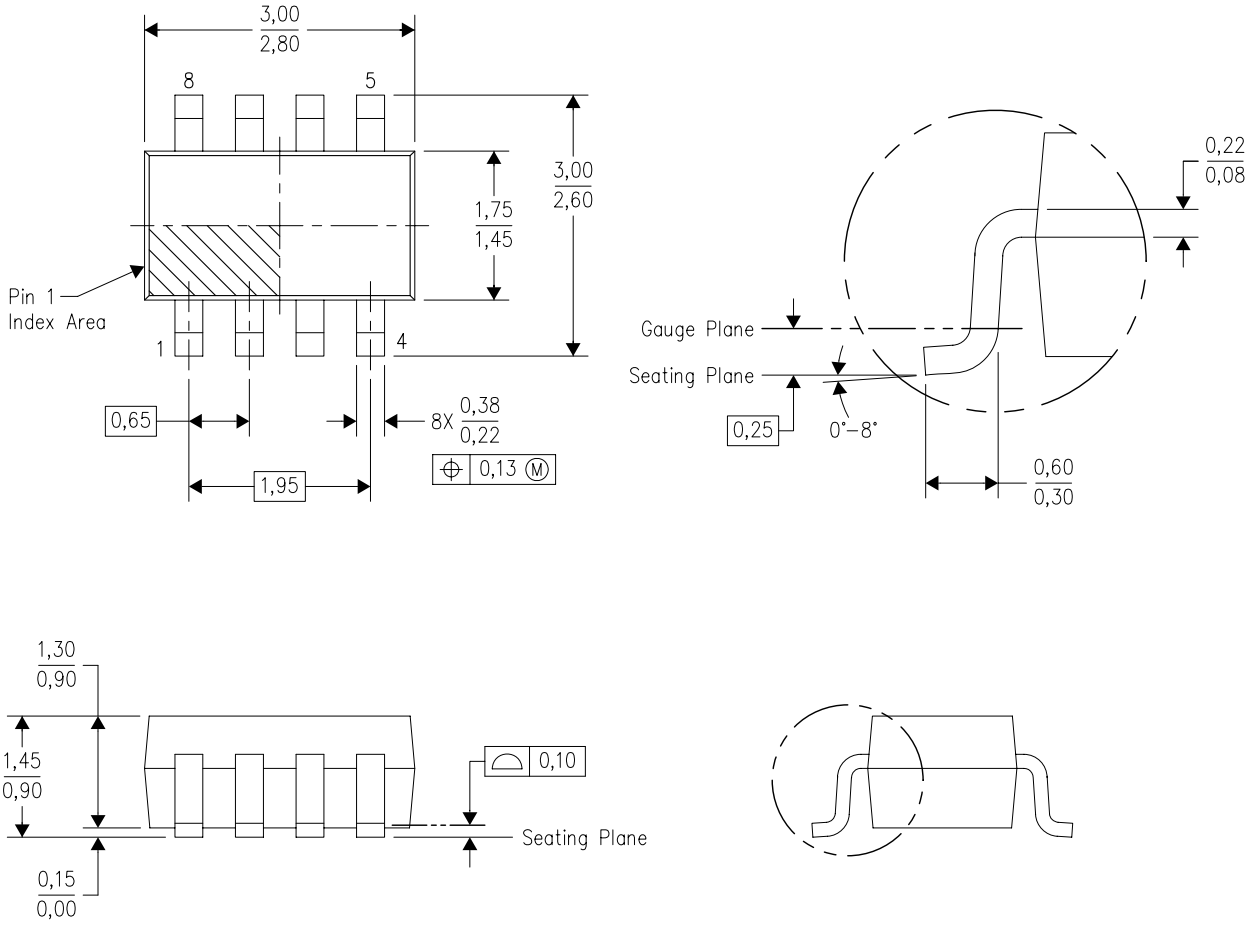

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

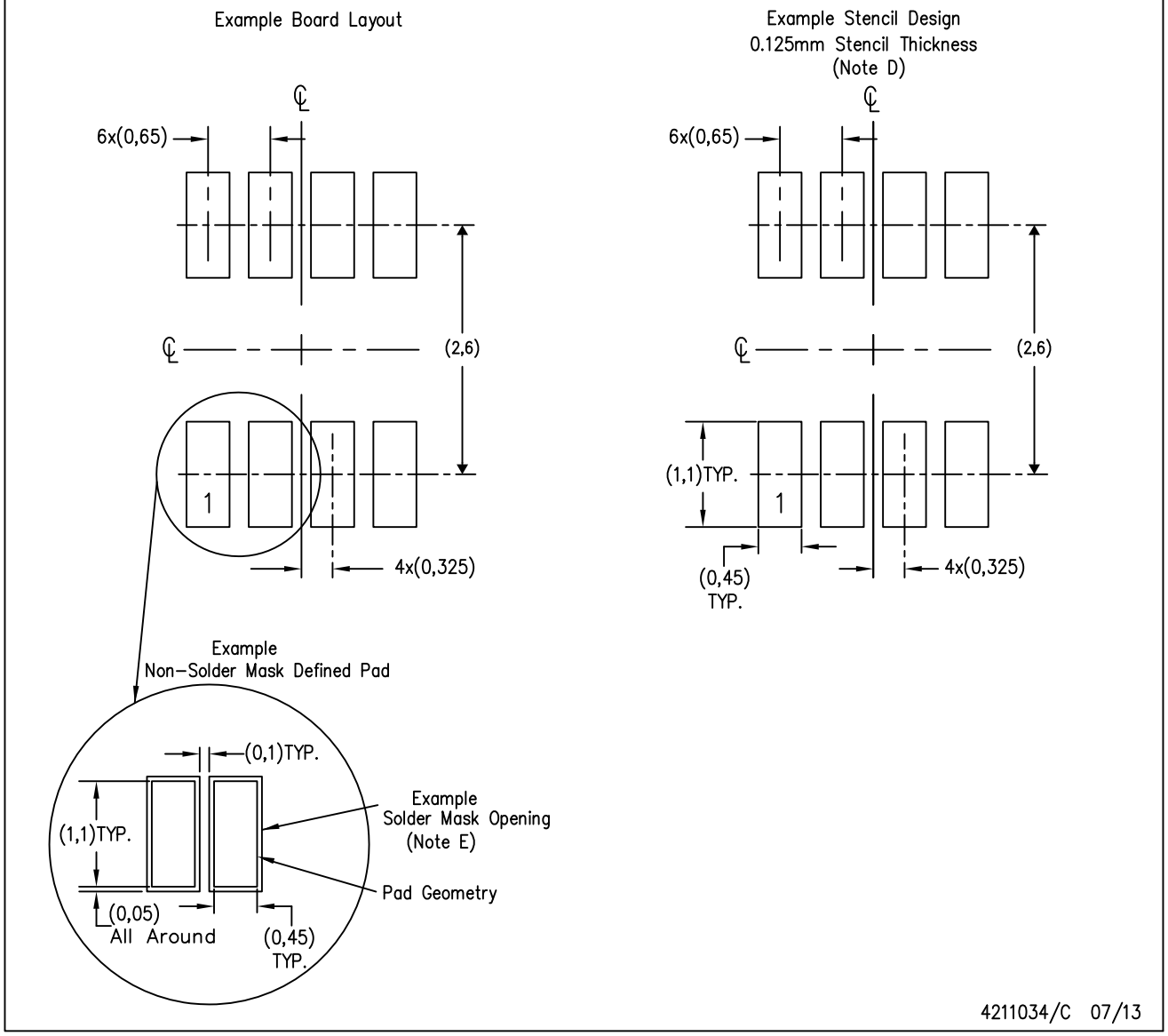
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

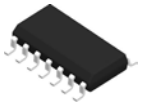



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

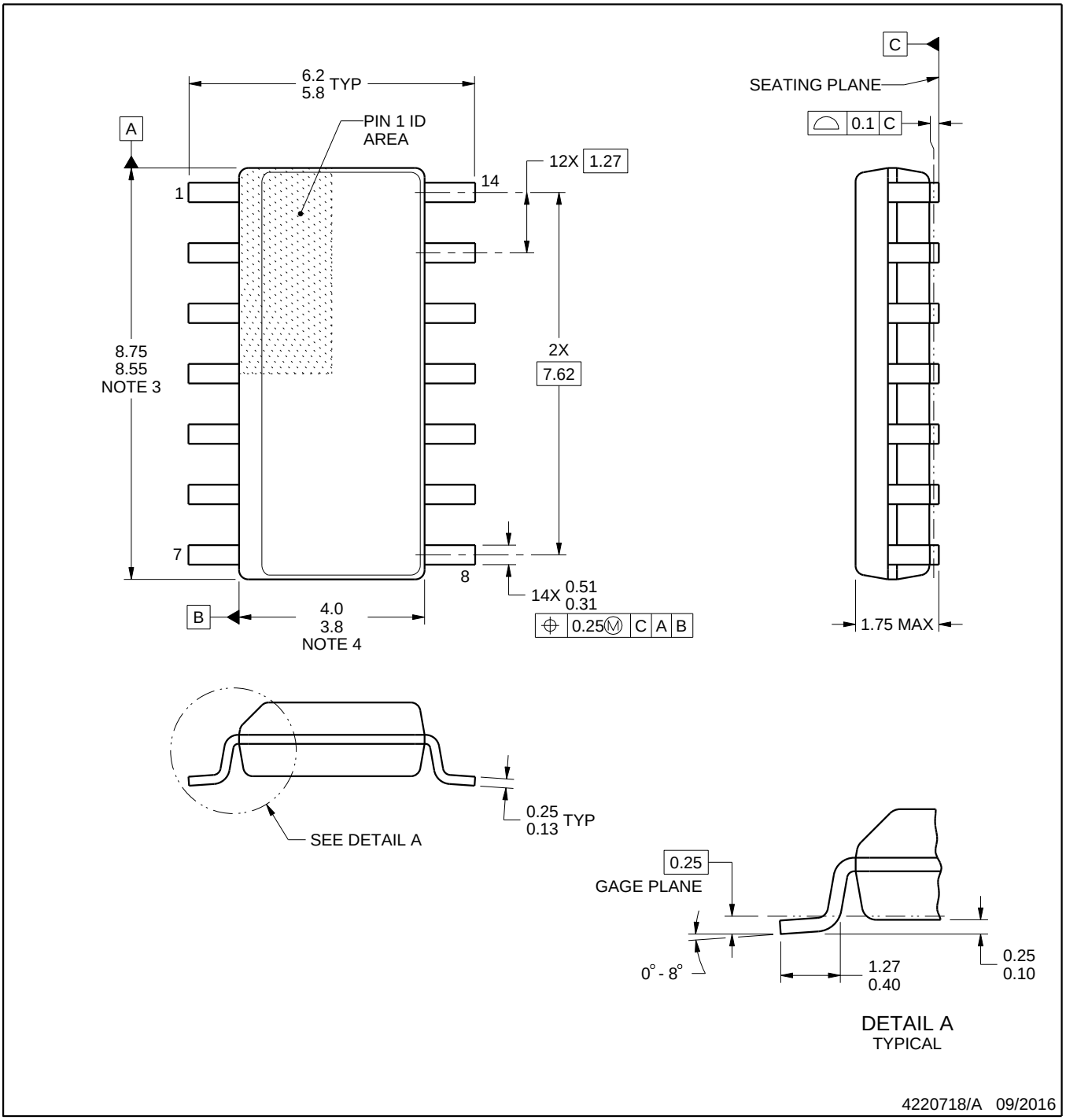


# PACKAGE OUTLINE

## D0014A

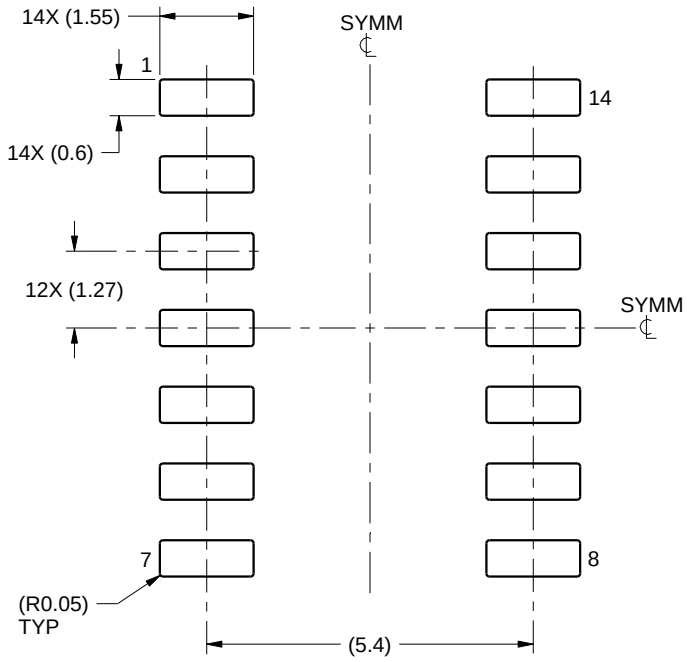
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

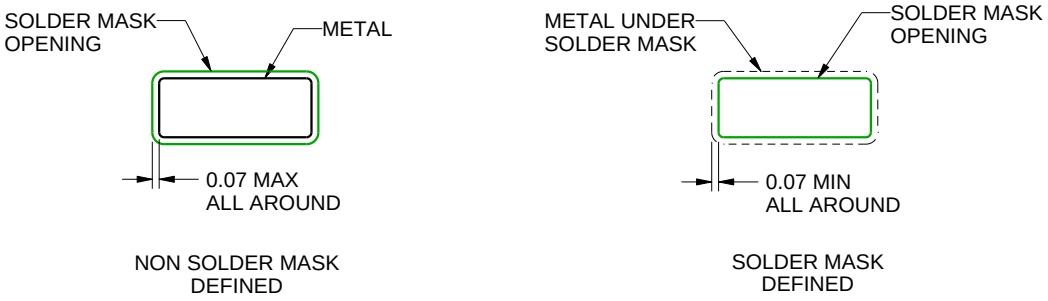



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

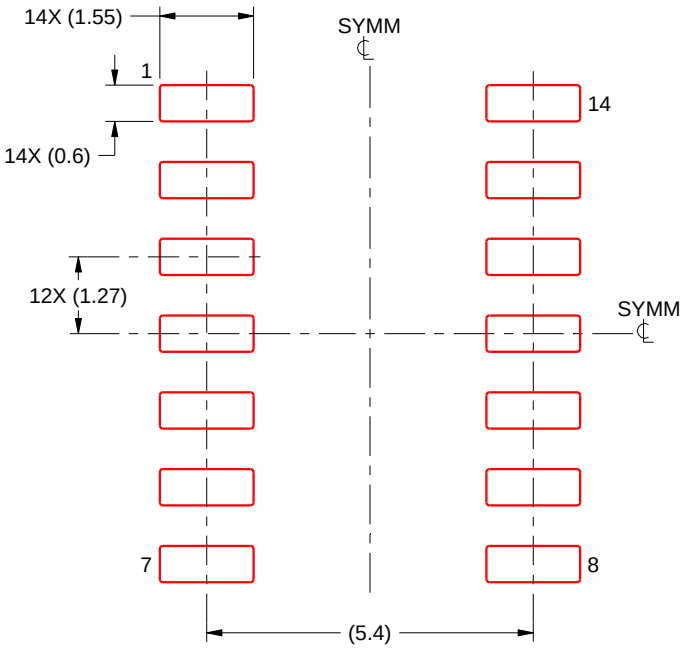
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

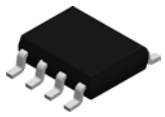



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

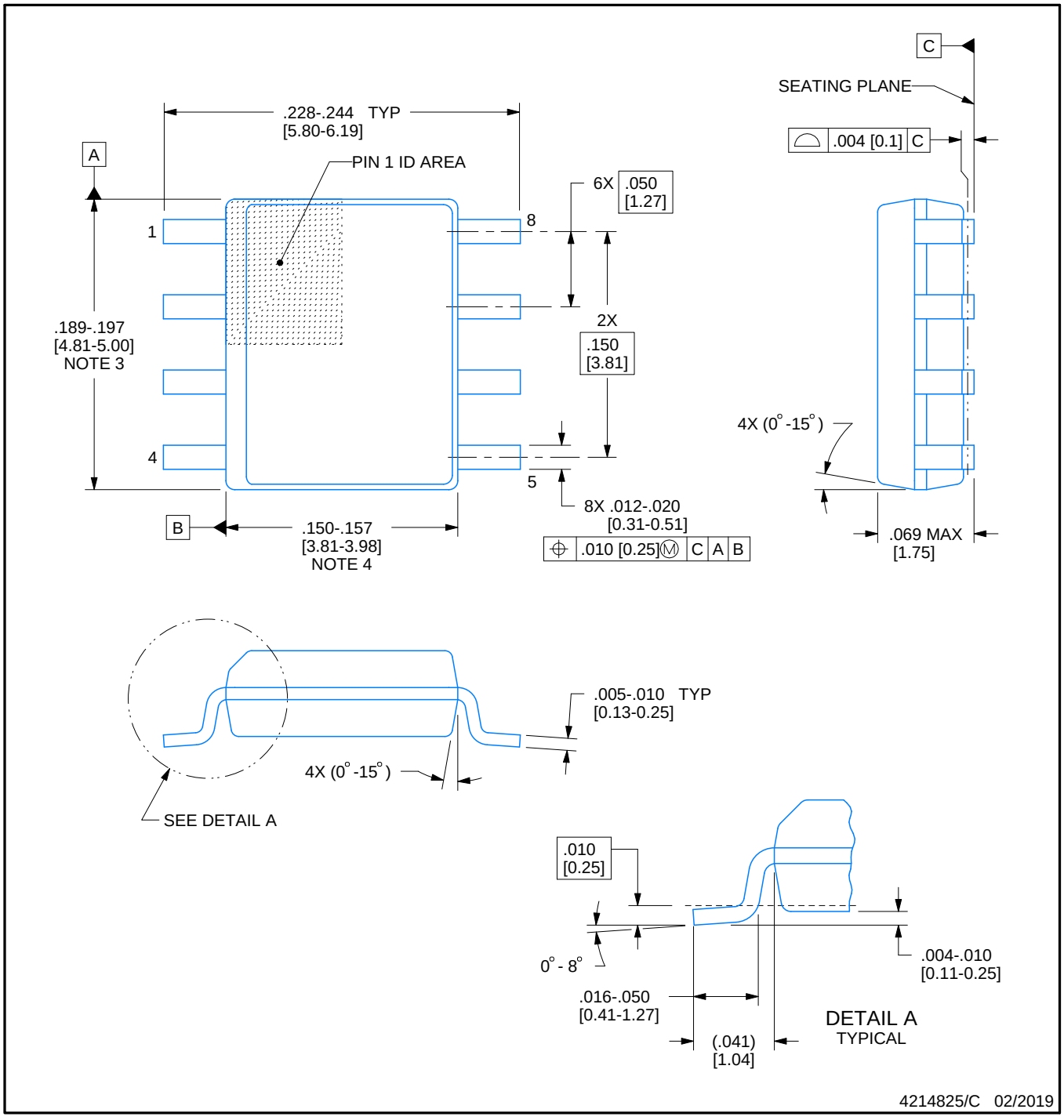


# PACKAGE OUTLINE

## D0008A

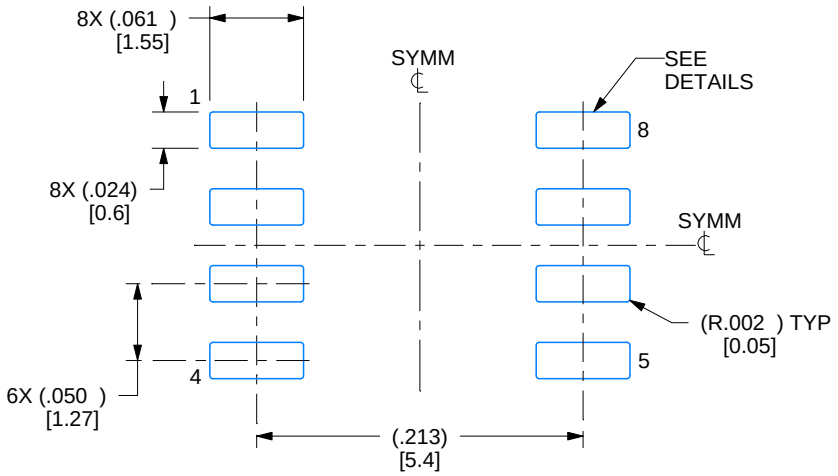
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

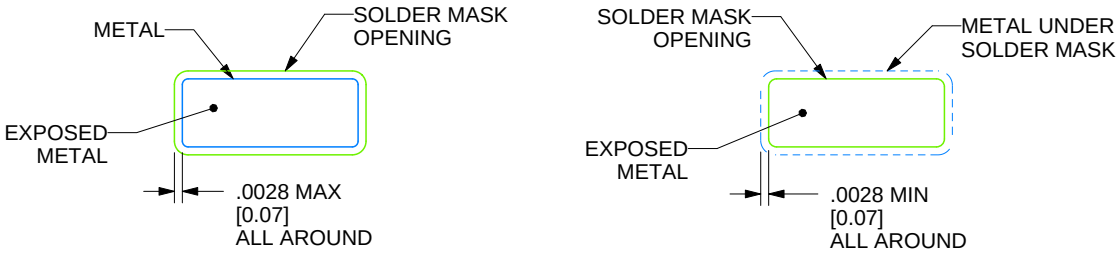



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

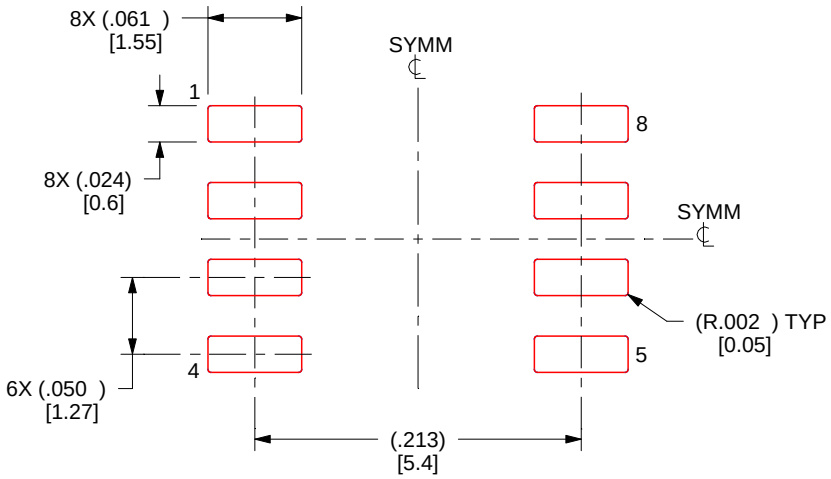
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

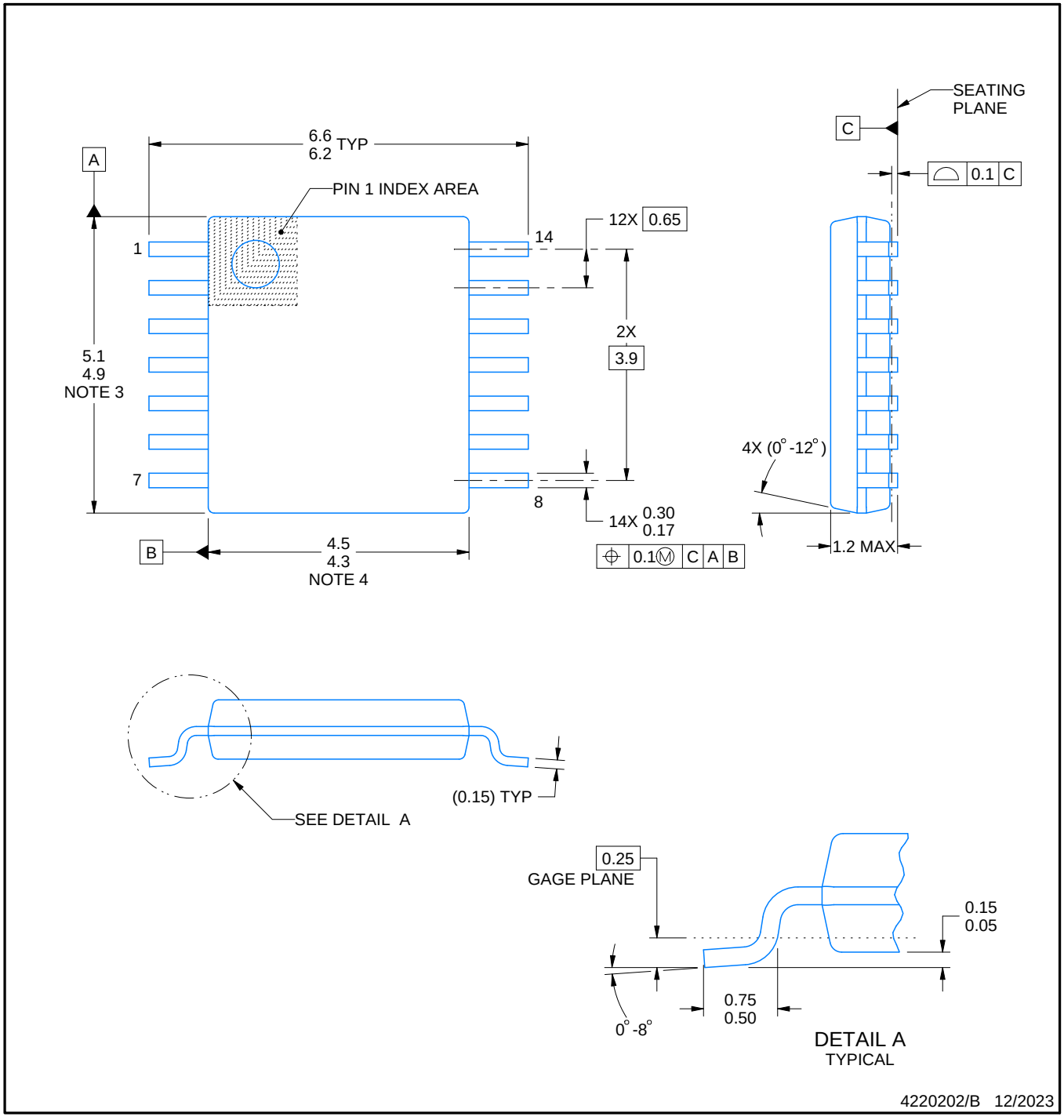
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## PW0014A

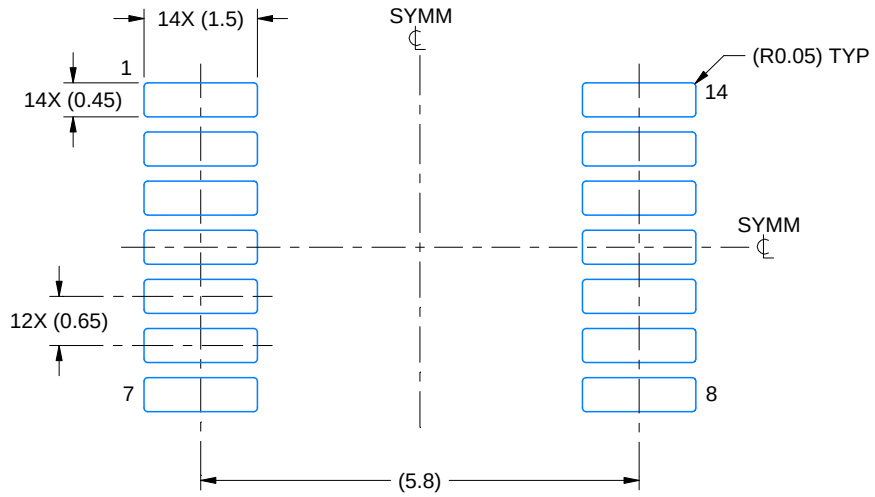
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

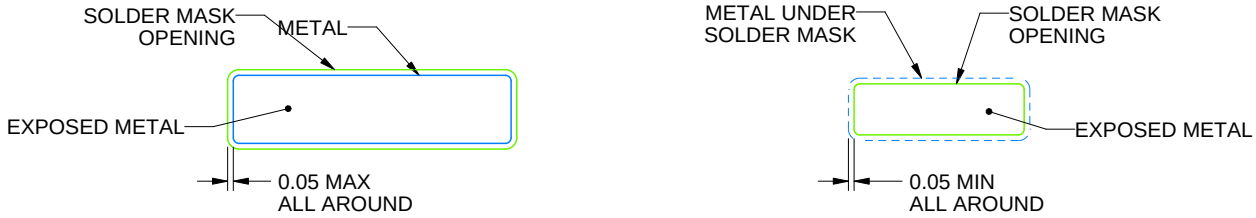



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

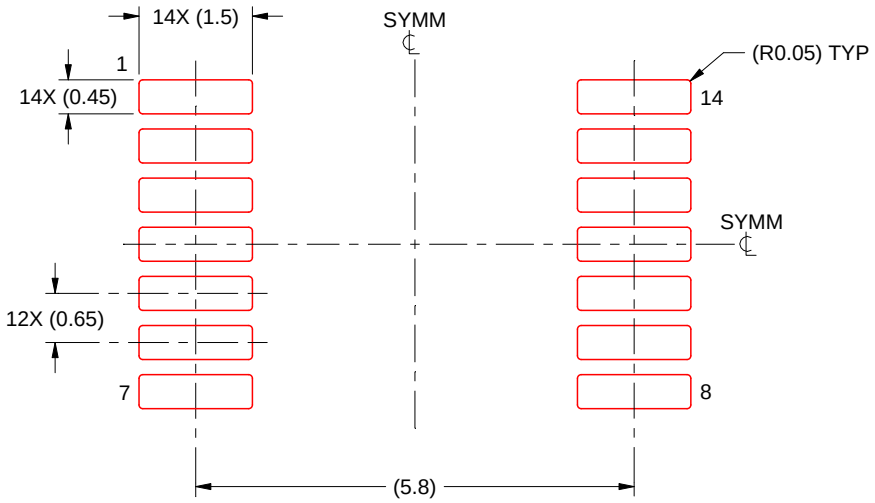



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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