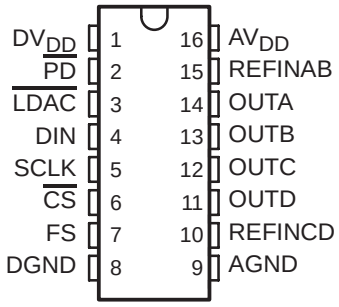
- **Four 8-Bit D/A Converters**
- **Programmable Settling Time of 2.5 μs or 8.5 μs Typ**
- **TMS320, (Q)SPI™, and Microwire™ Compatible Serial Interface**
- **Low Power Consumption:**
  7 mW, Slow Mode − 5-V Supply
  3 mW, Slow Mode − 3-V Supply
- **Reference Input Buffers**
- **Monotonic Over Temperature**
- **Dual 2.7-V to 5.5-V Supply (Separate Digital and Analog Supplies)**
- **Hardware Power Down**
- **Software Power Down**
- **Simultaneous Update**

applications

- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Controls**
- **Machine and Motion Control Devices**
- **Arbitrary Waveform Generation**

D OR PW PACKAGE
(TOP VIEW)



description

The TLV5627 is a four channel, 8-bit voltage output digital-to-analog converter (DAC) with a flexible 4-wire serial interface. The 4-wire serial interface allows glueless interface to TMS320, SPI, QSPI, and Microwire serial ports. The TLV5627 is programmed with a 16-bit serial word comprised of a DAC address, individual DAC control bits, and an 8-bit DAC value.

The device has provision for two supplies: one digital supply for the serial interface (via pins DV_{DD} and DGND), and one for the DACs, reference buffers and output buffers (via pins AV_{DD} and AGND). Each supply is independent of the other, and can be any value between 2.7 V and 5.5 V. The dual supplies allow a typical application where the DAC will be controlled via a microprocessor operating on a 3-V supply (also used on pins DV_{DD} and DGND), with the DACs operating on a 5-V supply. The digital and analog supplies can be tied together.

The resistor string output voltage is buffered by an x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. A rail-to-rail output stage and a power-down mode make it ideal for single voltage, battery based applications. The settling time of the DAC is programmable to allow the designer to optimize speed versus power dissipation. The settling time is chosen by the control bits within the 16-bit serial input string. A high-impedance buffer is integrated on the REFINAB and REFINCD terminals to reduce the need for a low source impedance drive to the terminal. REFINAB and REFINCD allow DACs A and B to have a different reference voltage than DACs C and D.

The device, implemented with a CMOS process, is available in 16-terminal SOIC and TSSOP packages. The TLV5627C is characterized for operation from 0°C to 70°C. The TLV5627I is characterized for operation from −40°C to 85°C.

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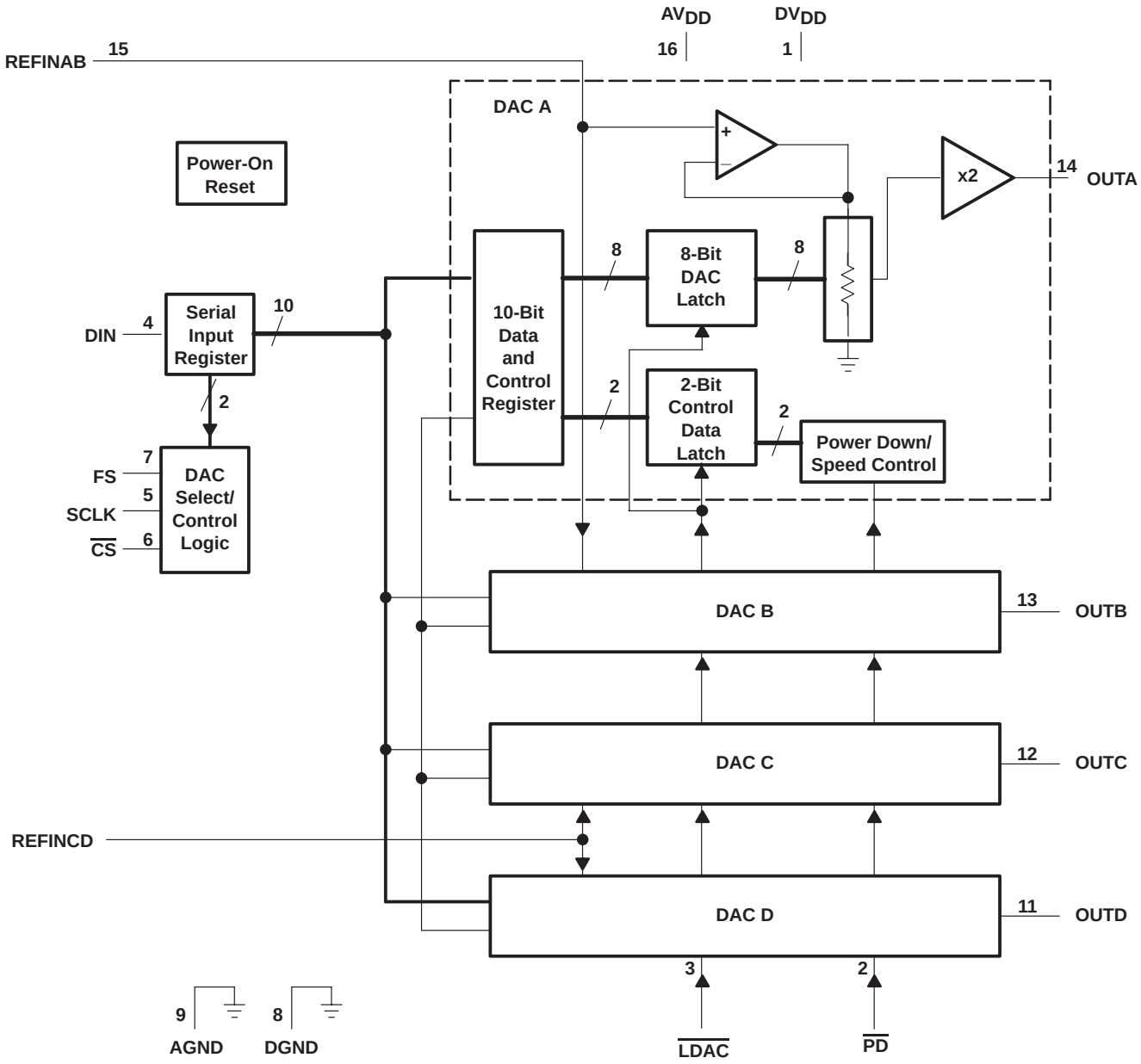
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AVAILABLE OPTIONS

T_A	PACKAGE	
	SOIC (D)	TSSOP (PW)
0°C to 70°C	TLV5627CD	TLV5627CPW
−40°C to 85°C	TLV5627ID	TLV5627IPW

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	9		Analog ground
AV_{DD}	16		Analog supply
$\overline{CS}$	6	I	Chip select. This terminal is active low.
DGND	8		Digital ground
DIN	4	I	Serial data input
DV_{DD}	1		Digital supply
FS	7	I	Frame sync input. The falling edge of the frame sync pulse indicates the start of a serial data frame shifted out to the TLV5627.
$\overline{PD}$	2	I	Power-down pin. Powers down all DACs (overriding their individual power down settings), and all output stages. This terminal is active low.
$\overline{LDAC}$	3	I	Load DAC. When the $\overline{LDAC}$ signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when $\overline{LDAC}$ is low.
REFINAB	15	I	Voltage reference input for DACs A and B.
REFINCD	10	I	Voltage reference input for DACs C and D.
SCLK	5	I	Serial clock input
OUTA	14	O	DAC A output
OUTB	13	O	DAC B output
OUTC	12	O	DAC C output
OUTD	11	O	DAC D output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, (DV_{DD}, AV_{DD} to GND) . . . . . 7 V
Supply voltage difference, (AV_{DD} to DV_{DD}) . . . . . −2.8 V to 2.8 V
Digital input voltage range . . . . . −0.3 V to DV_{DD} + 0.3 V
Reference input voltage range . . . . . −0.3 V to AV_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5627C . . . . . 0°C to 70°C
TLV5627I . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, AV_{DD}, DV_{DD}	5-V supply	4.5	5	5.5	V
	3-V supply	2.7	3	3.3	
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V	2			V
	DV_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V			0.6	V
	DV_{DD} = 5.5 V			1	
Reference voltage, V_{ref} to REFINAB, REFINCD terminal	5-V supply (see Note 1)	0	2.048	AV_{DD}−1.5	V
	3-V supply (see Note 1)	0	1.024	AV_{DD}−1.5	
Load resistance, R_L		2	10		kΩ
Load capacitance, C_L				100	pF
Serial clock rate, SCLK				20	MHz
Operating free-air temperature	TLV5627C	0		70	°C
	TLV5627I	−40		85	

NOTE 1: Voltages greater than $AV_{DD}/2$ will cause output saturation for large DAC codes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

static DAC specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8			bits
	Integral nonlinearity (INL), end point adjusted	See Note 2		±0.3	±0.5	LSB
	Differential nonlinearity (DNL)	See Note 3		±0.03	±0.5	LSB
E_{ZS}	Zero scale error (offset error at zero scale)	See Note 4			±10	mV
	Zero scale error temperature coefficient	See Note 5		10		ppm/°C
E_G	Gain error	See Note 6			±0.6	%of FS voltage
	Gain error temperature coefficient	See Note 7		10		ppm/°C

NOTES: 2. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
3. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
4. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
5. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.
6. Gain error is the deviation from the ideal output ($2V_{ref}$ − 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
7. Gain temperature coefficient is given by: E_G TC = $[E_G(T_{max}) - E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

individual DAC output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output	R_L = 10 kΩ	0		AV_{DD}−0.4	V
	Output load regulation accuracy	R_L = 2 kΩ vs 10 kΩ		0.1	0.25	% of FS voltage

reference input (REFINAB, REFINCD)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range	See Note 8		0		AV_{DD}−1.5	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference feed through	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 9)			−75		dB
	Reference input bandwidth	REFIN = 0.2 V_{pp} + 1.024 V dc	Slow		0.5		MHz
			Fast		1		

NOTES: 8. Reference input voltages greater than V_{DD}/2 will cause output saturation for large DAC codes.
9. Reference feedthrough is measured at the DAC output with an input code = 000 hex and a $V_{ref(REFINAB\ or\ REFINCD)}$ input = 1.024 Vdc + 1 V_{pp} at 1 kHz.

digital inputs (D0−D11, $\overline{CS}$, WEB, $\overline{LDAC}$, $\overline{PD}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = DV_{DD}$			±1	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±1	µA
C_I	Input capacitance			3		pF

power supply

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current		5-V supply, No load, Clock running	Slow		1.4	2.2	mA
				Fast		3.5	5.5	
			3-V supply, No load, Clock running	Slow		1	1.5	mA
				Fast		3	4.5	
	Power down supply current, See Figure 12					1		µA
PSRR	Power supply rejection ratio	Zero scale gain	See Notes 10 and 11			−68		dB
		Gain				−68		

10. Zero-scale-error rejection ratio (EZS−RR) is measured by varying the AV_{DD} from 5 ±0.5 V and 3 ±0.3 V dc, and measuring the proportion of this signal imposed on the zero-code output voltage.
11. Gain-error rejection ratio (EG-RR) is measured by varying the AV_{DD} from 5 ±0.5 V and 3 ±0.3 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

analog output dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Output slew rate	C_L = 100 pF, R_L = 10 kΩ, V_O = 10% to 90%, V_{ref} = 2.048 V, 1024 V	Fast		5		V/µs
			Slow		1		V/µs
t_S	Output settling time	To ± 0.1 LSB, C_L = 100 pF, R_L = 10 kΩ, See Notes 12 and 14	Fast		2.5	4	µs
			Slow		8.5	18	
$t_{s(c)}$	Output settling time, code to code	To ± 0.1 LSB, C_L = 100 pF, R_L = 10 kΩ, See Notes 13 and 14	Fast		1		µs
			Slow		2		
	Glitch energy	Code transition from 7F0 to 800			10		nV-sec
SNR	Signal-to-noise ratio	Sinewave generated by DAC, Reference voltage = 1.024 at 3 V and 2.048 at 5 V, f_S = 400 KSPS, f_{OUT} = 1.1 kHz sinewave, C_L = 100 pF, R_L = 10 kΩ, BW = 20 kHz			57		dB
S/(N+D)	Signal to noise + distortion				49		
THD	Total harmonic distortion				−50		
SFDR	Spurious free dynamic range				60		

NOTES: 12. Settling time is the time for the output signal to remain within ± 0.1 LSB of the final measured value for a digital input code change of 0x020 to 0xFF0 or 0xFF0 to 0x020.
13. Settling time is the time for the output signal to remain within ± 0.1 LSB of the final measured value for a digital input code change of one count.
14. Limits are ensured by design and characterization, but are not production tested.

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su(CS-FS)}$	Setup time, $\overline{CS}$ low before FS↓	10			ns
$t_{su(FS-CK)}$	Setup time, FS low before first negative SCLK edge	8			ns
$t_{su(C16-FS)}$	Setup time, sixteenth negative SCLK edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
$t_{su(C16-CS)}$	Setup time. The first positive SCLK edge after D0 is sampled before $\overline{CS}$ rising edge. If FS is used instead of the SCLK positive edge to update the DAC, then the setup time is between the FS rising edge and $\overline{CS}$ rising edge.	10			ns
t_{wH}	Pulse duration, SCLK high	25			ns
t_{wL}	Pulse duration, SCLK low	25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	Pulse duration, FS high	20			ns

PARAMETER MEASUREMENT INFORMATION

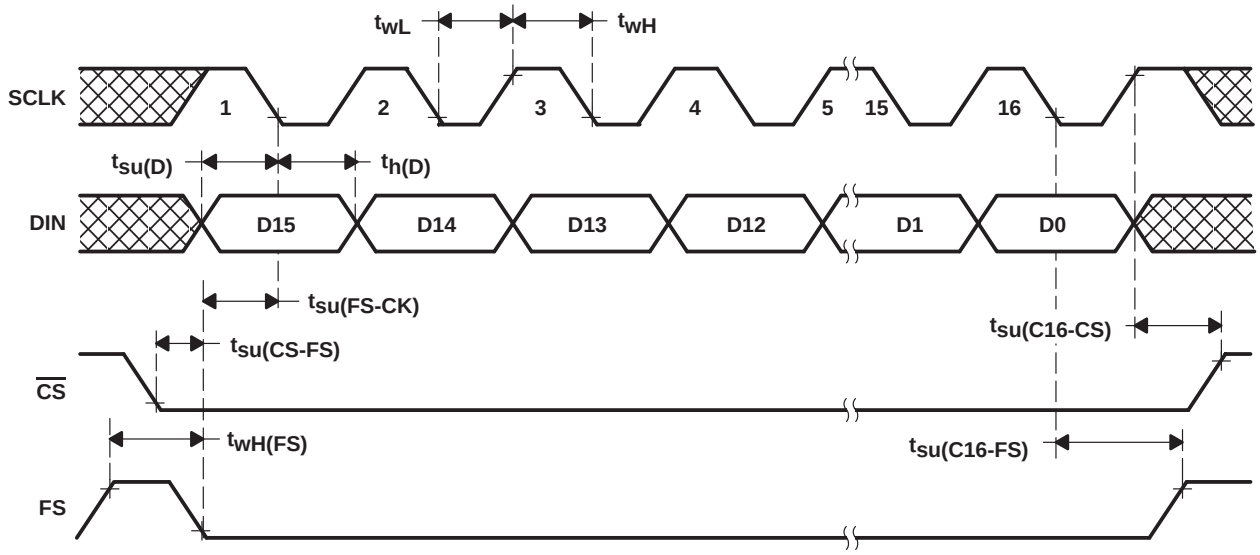


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

LOAD REGULATION

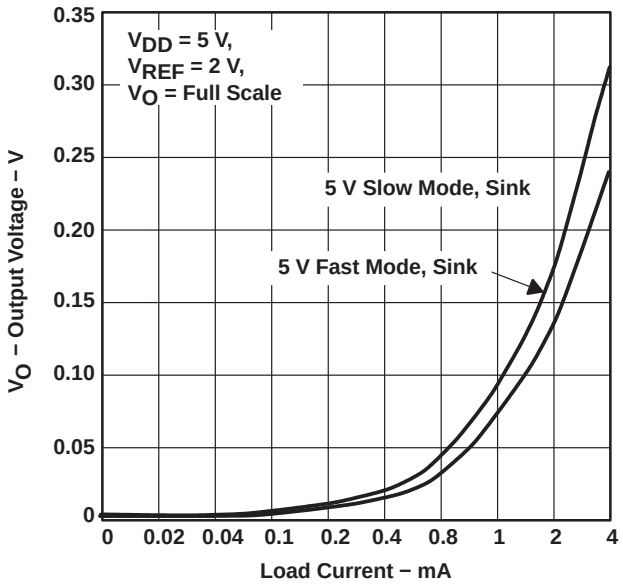


Figure 2

LOAD REGULATION

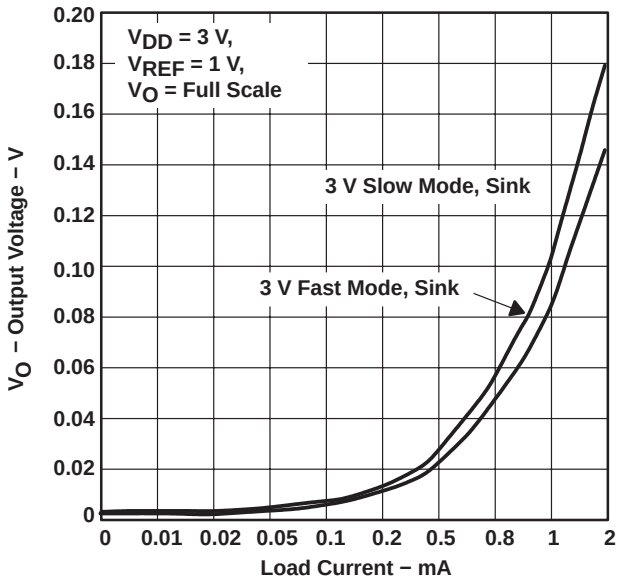


Figure 3

LOAD REGULATION

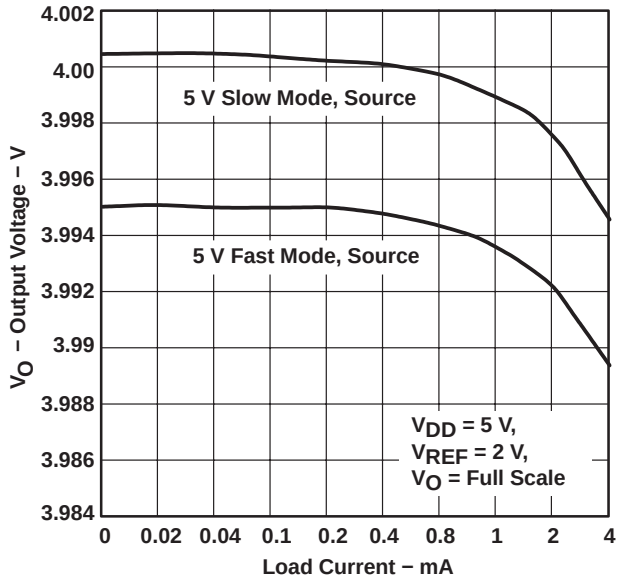


Figure 4

LOAD REGULATION

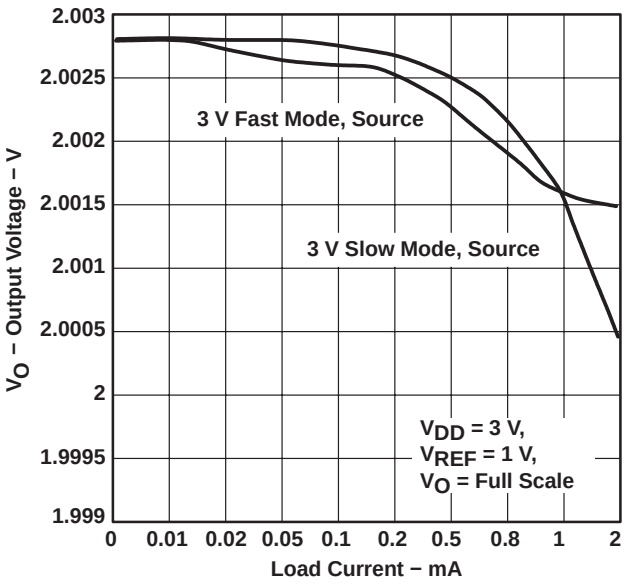


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE

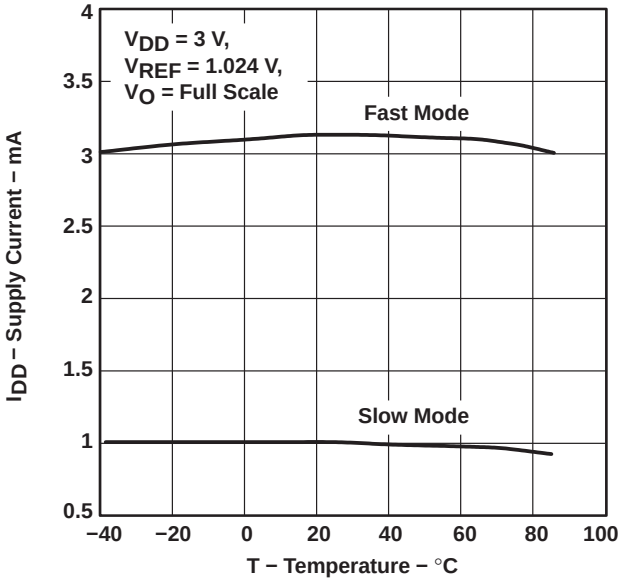


Figure 6

SUPPLY CURRENT vs TEMPERATURE

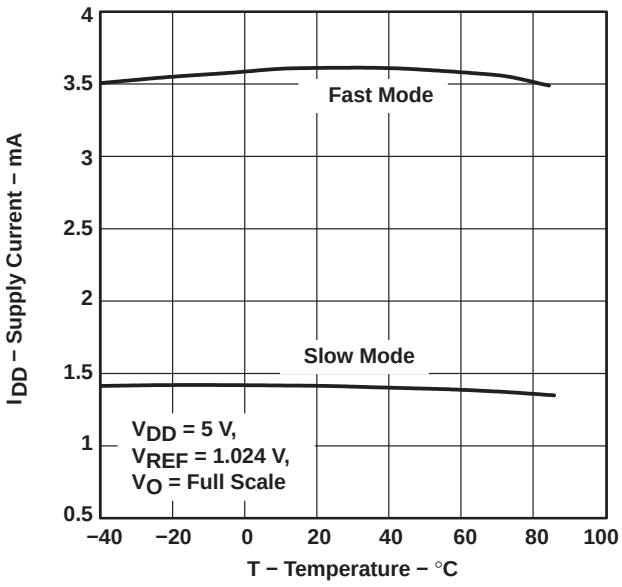


Figure 7

TOTAL HARMONIC DISTORTION vs FREQUENCY

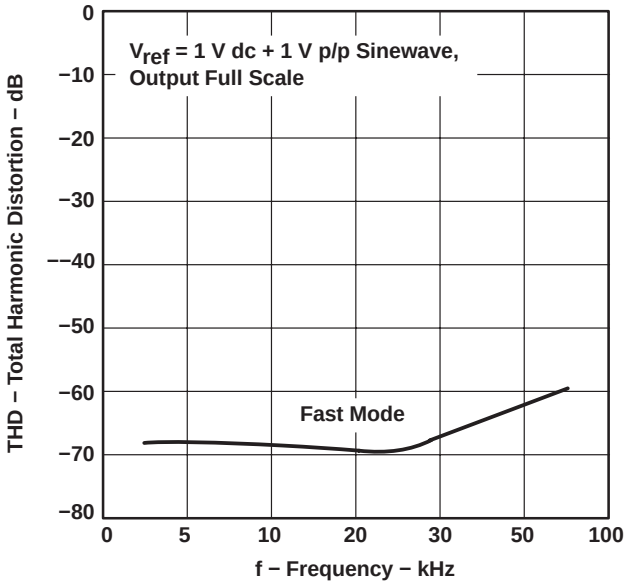


Figure 8

TOTAL HARMONIC DISTORTION vs FREQUENCY

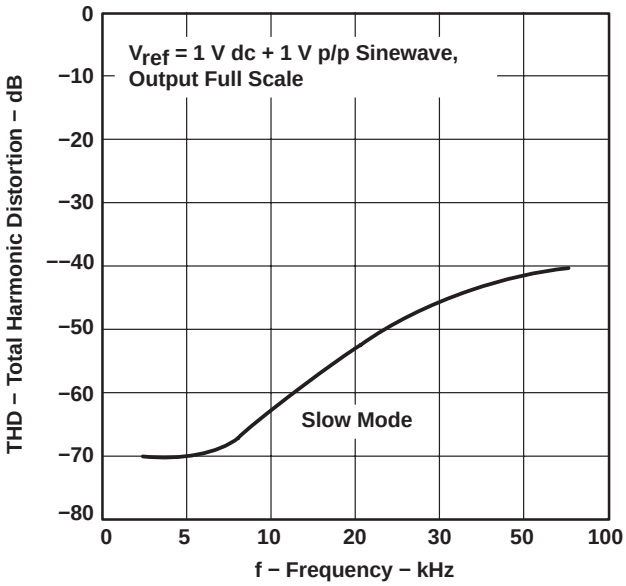


Figure 9

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

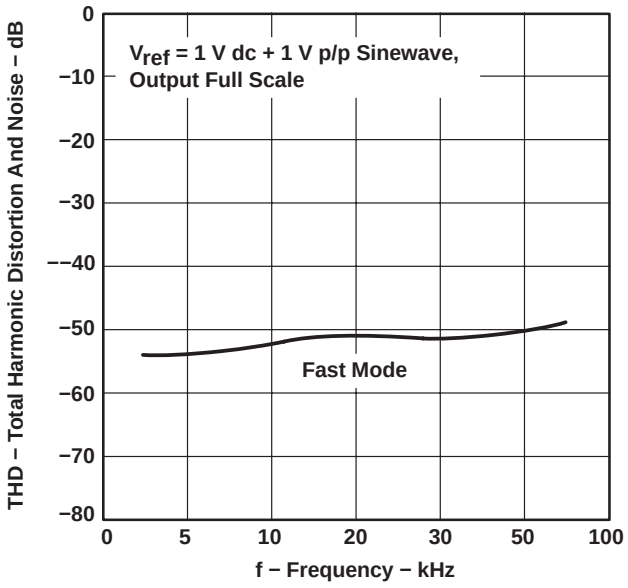


Figure 10

TOTAL HARMONIC DISTORTION AND NOISE
vs
FREQUENCY

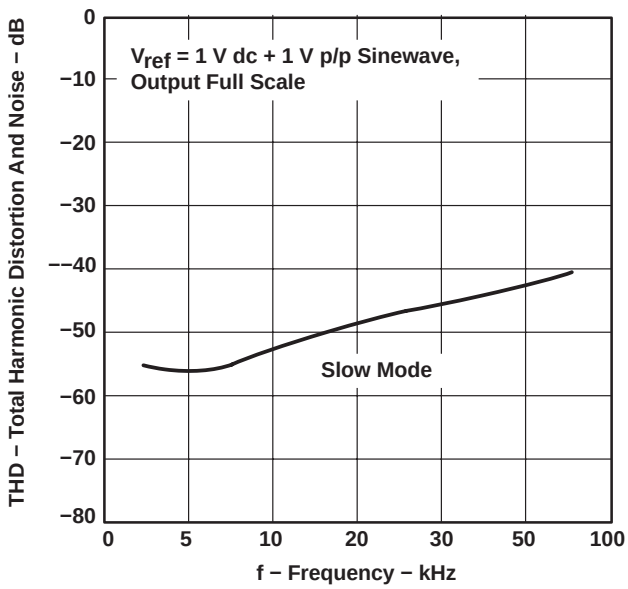


Figure 11

SUPPLY CURRENT
vs
TIME
(WHEN ENTERING POWER-DOWN MODE)

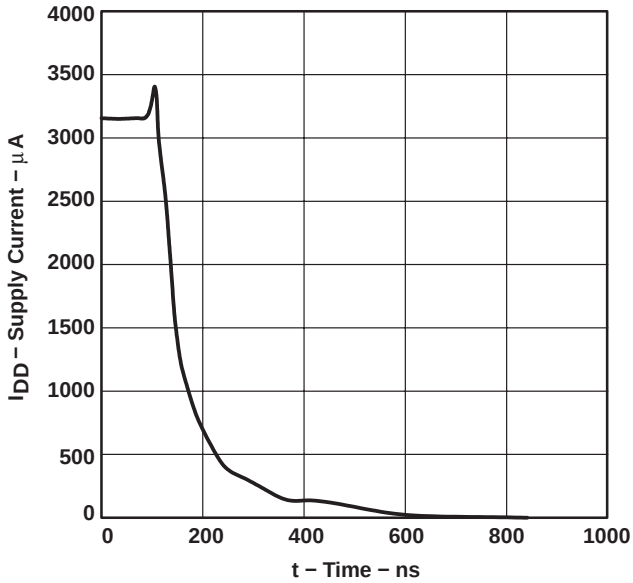


Figure 12

TYPICAL CHARACTERISTICS

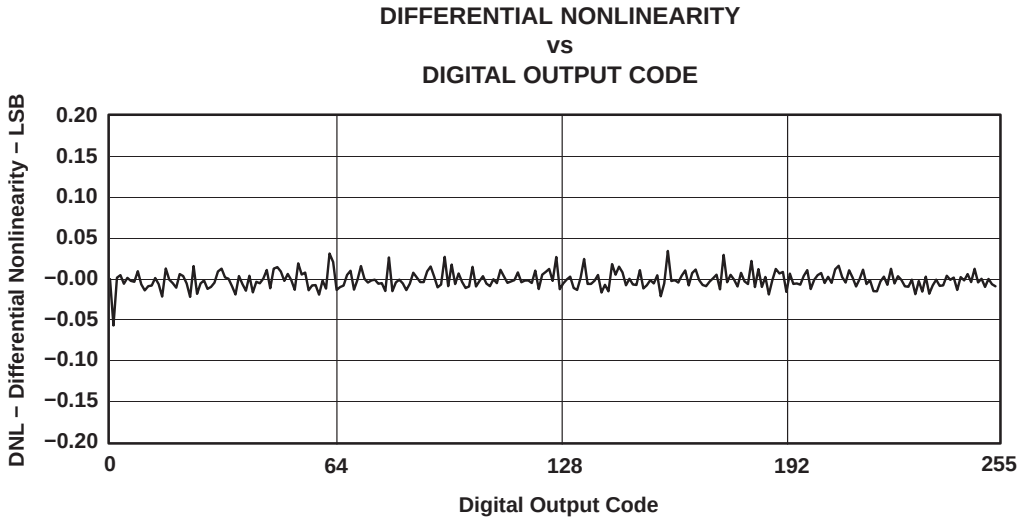


Figure 13

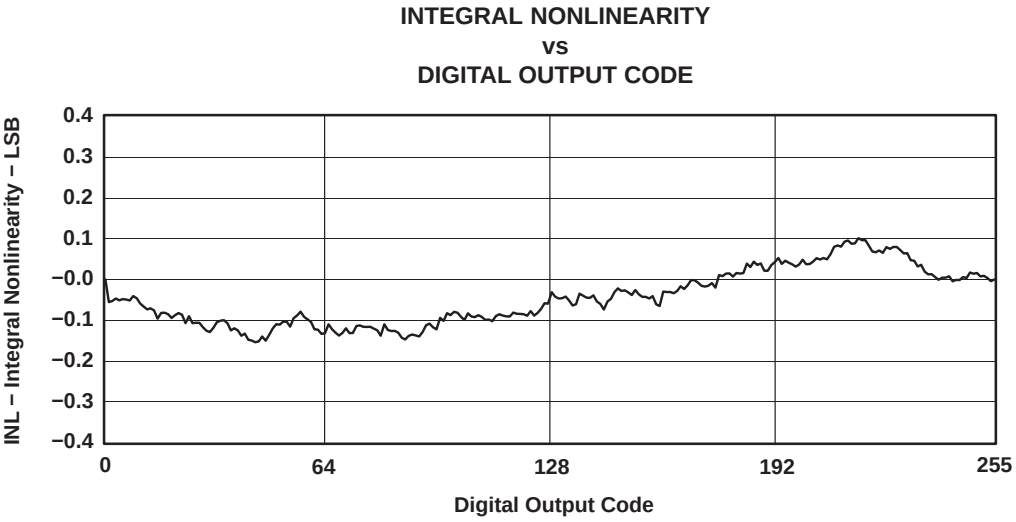


Figure 14

APPLICATION INFORMATION

general function

The TLV5627 is an 8-bit single supply DAC based on a resistor string architecture. The device consists of a serial interface, speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{2^n}\ [\mathrm{V}]$$

Where REF is the reference voltage and CODE is the digital input value within the range of 0_{10} to 2^n-1, where n=8 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

The device has to be enabled with $\overline{\mathrm{CS}}$ set to low. A falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch, which updates the voltage output to the new level.

The serial interface of the TLV5627 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four-wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). The interface is compatible with the TMS320 family. Figure 15 shows an example with two TLV5627s connected directly to a TMS320 DSP.

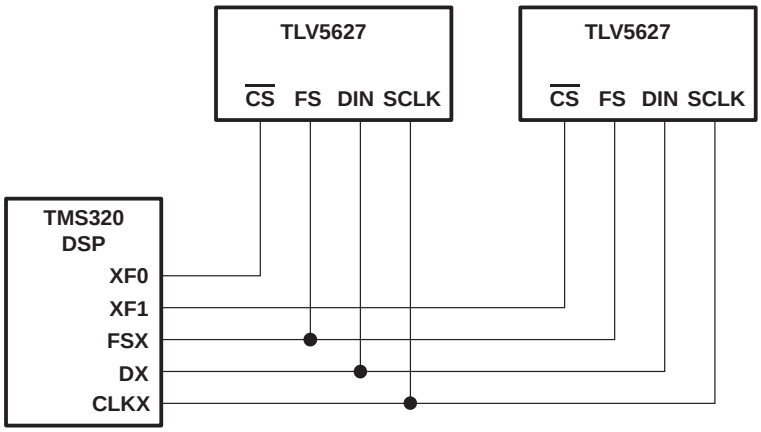


Figure 15. TMS320 Interface

APPLICATION INFORMATION

serial interface (continued)

If there is no need to have more than one device on the serial bus, then $\overline{CS}$ can be tied low. Figure 16 shows an example of how to connect the TLV5627 to a TMS320, SPI, or Microwire port using only three pins.

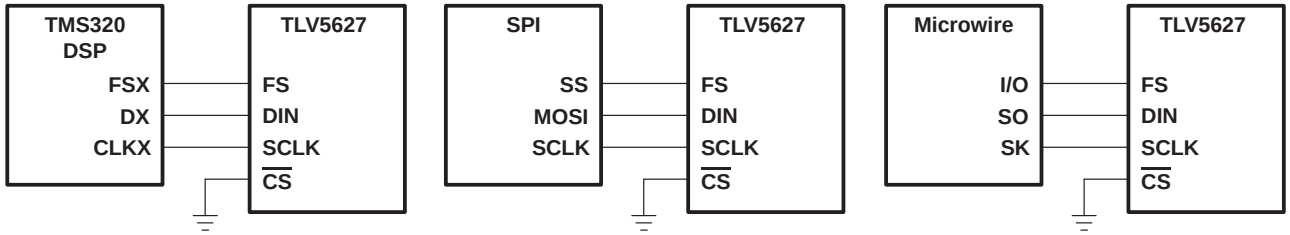


Figure 16. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5627. After the write operation(s), the DAC output is updated automatically on the next positive clock edge following the sixteenth falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{SCLKmax} = \frac{1}{t_{wH(min)} + t_{wL(min)}} = 20\ \text{MHz}$$

The maximum update rate is:

$$f_{UPDATEmax} = \frac{1}{16\left(t_{wH(min)} + t_{wL(min)}\right)} = 1.25\ \text{MHz}$$

The maximum update rate is a theoretical value for the serial interface since the settling time of the TLV5627 has to be considered also.

data format

The 16-bit data word for the TLV5627 consists of two parts:

- Control bits (D15 . . . D12)
- New DAC value (D11 . . . D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A1	A0	PWR	SPD	New DAC value (8 bits)								0	0	0	0

SPD: Speed control bit. 1 → fast mode 0 → slow mode
PWR: Power control bit. 1 → power down 0 → normal operation

APPLICATION INFORMATION

In power-down mode, all amplifiers within the TLV5627 are disabled. A particular DAC (A, B, C, D) of the TLV5627 is selected by A1 and A0 within the input word.

A1	A0	DAC
0	0	A
0	1	B
1	0	C
1	1	D

TLV5627 interfaced to TMS320C203 DSP

hardware interfacing

Figure 17 shows an example of how to connect the TLV5627 to a TMS320C203 DSP. The serial port is configured in burst mode, with FSX generated by the TMS320C203 to provide the frame sync (FS) input to the TLV5627. Data is transmitted on the DX line, with the serial clock input on the CLKX line. The general-purpose input/output port bits IO0 and IO1 are used to generate the chip select ($\overline{CS}$) and DAC latch update ($\overline{LDAC}$) inputs to the TLV5627. The active low power down ($\overline{PD}$) is pulled high all the time to ensure the DACs are enabled.

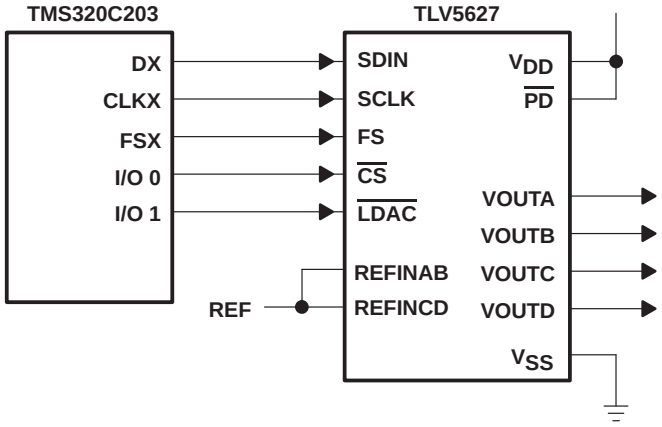


Figure 17. TLV5627 Interfaced with TMS320C203

APPLICATION INFORMATION

TLV5627 interfaced to MCS®51 microcontroller

hardware interfacing

Figure 18 shows an example of how to connect the TLV5627 to an MCS®51 Microcontroller. The serial DAC input data and external control signals are sent via I/O Port 3 of the controller. The serial data is sent on the RxD line, with the serial clock output on the TxD line. Port 3 bits 3, 4, and 5 are configured as outputs to provide the DAC latch update ($\overline{\text{LDAC}}$), chip select ($\overline{\text{CS}}$) and frame sync (FS) signals for the TLV5627. The active low power down pin ($\overline{\text{PD}}$) of the TLV5627 is pulled high to ensure that the DACs are enabled.

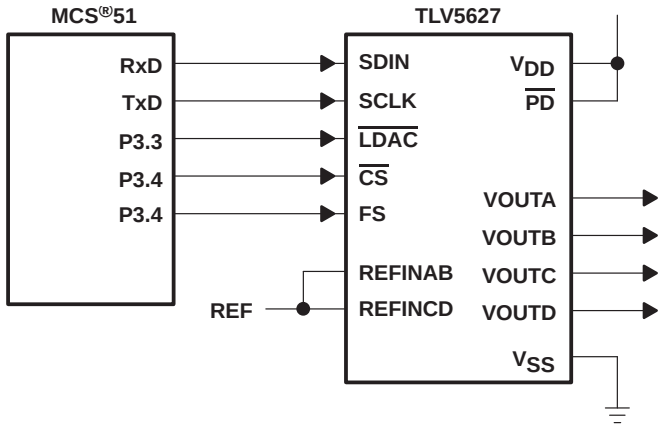


Figure 18. TLV5627 Interfaced with MCS®51

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 19.

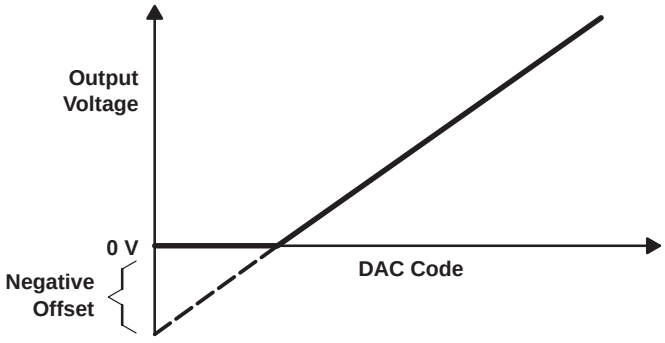


Figure 19. Effect of Negative Offset (single supply)

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APPLICATION INFORMATION

linearity, offset, and gain error using single ended supplies (continued)

The offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well-managed and there are negligible voltage drops across the ground plane.

A 0.1-μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 20 shows the ground plane layout and bypassing technique.

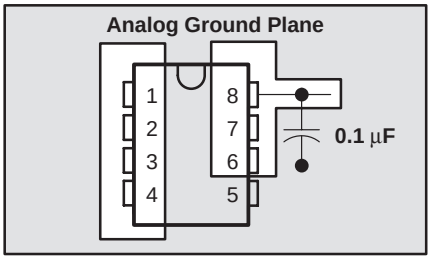
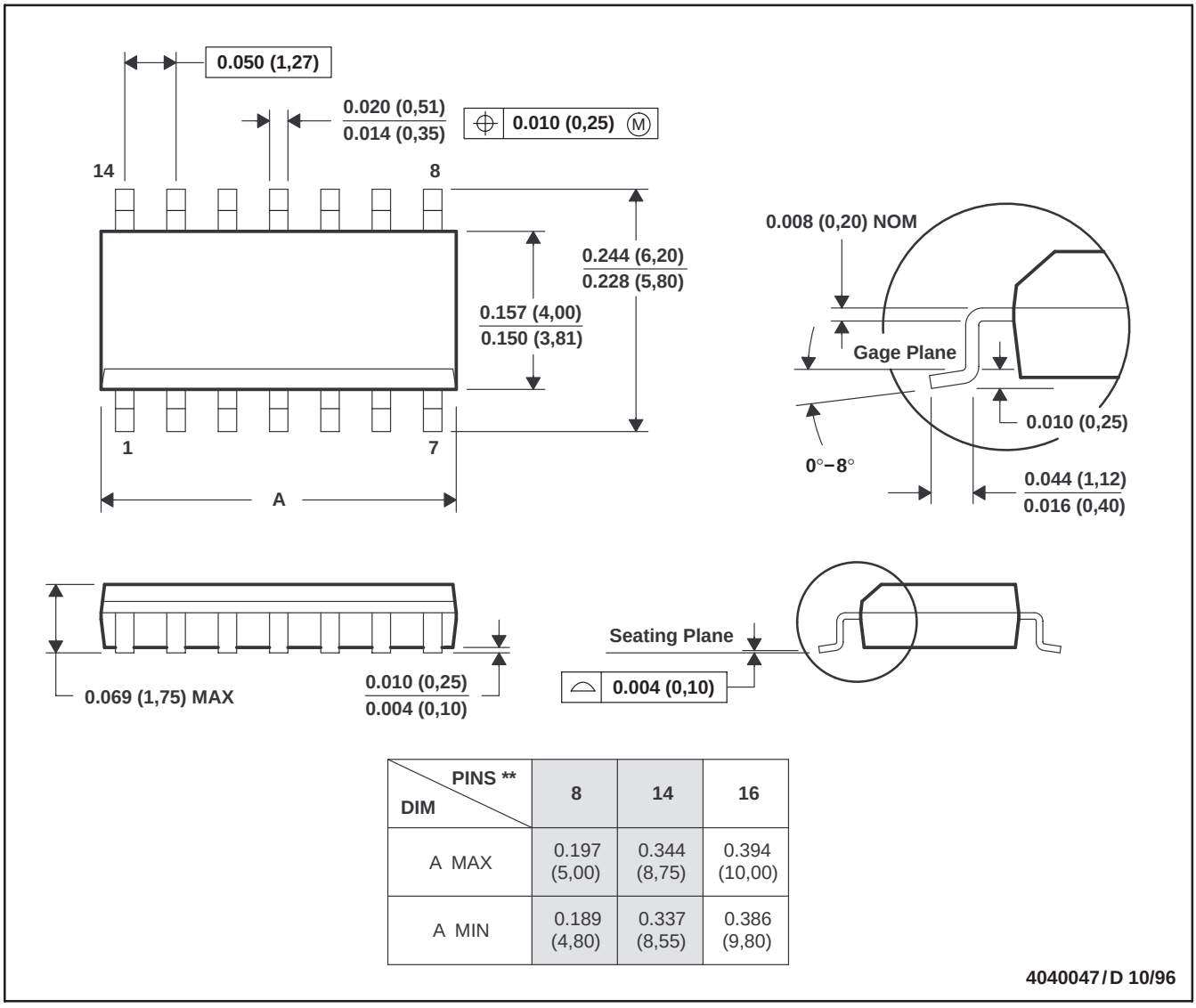


Figure 20. Power-Supply Bypassing

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

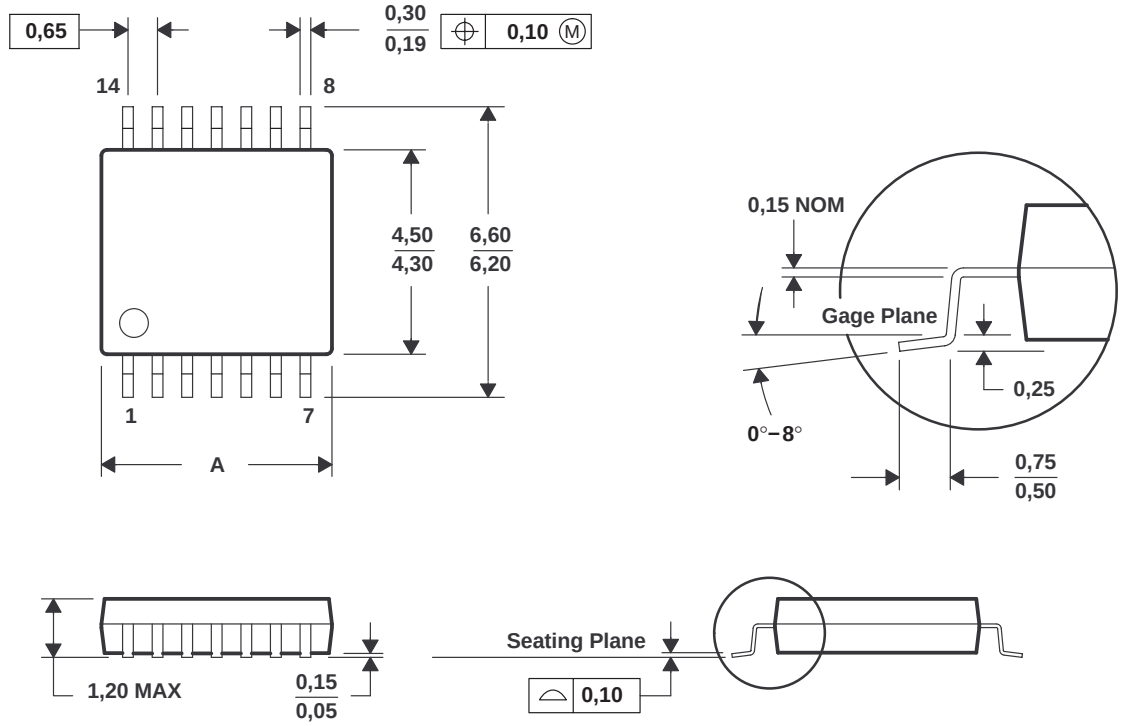
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV5627CD	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5627C
TLV5627CD.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5627C
TLV5627CDG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5627C
TLV5627CDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5627C
TLV5627CDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5627C
TLV5627CPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5627
TLV5627CPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5627
TLV5627CPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5627
TLV5627CPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5627
TLV5627ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5627I
TLV5627ID.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5627I
TLV5627IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5627
TLV5627IPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5627
TLV5627IPWG4	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5627
TLV5627IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5627
TLV5627IPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5627

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

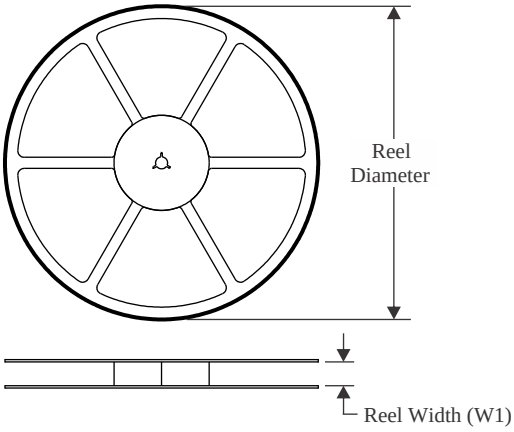
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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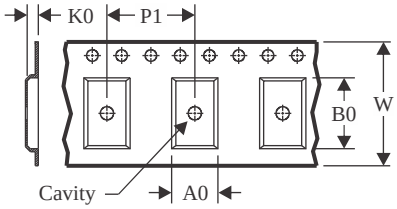
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

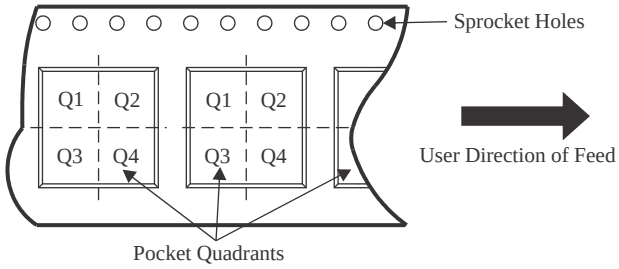


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

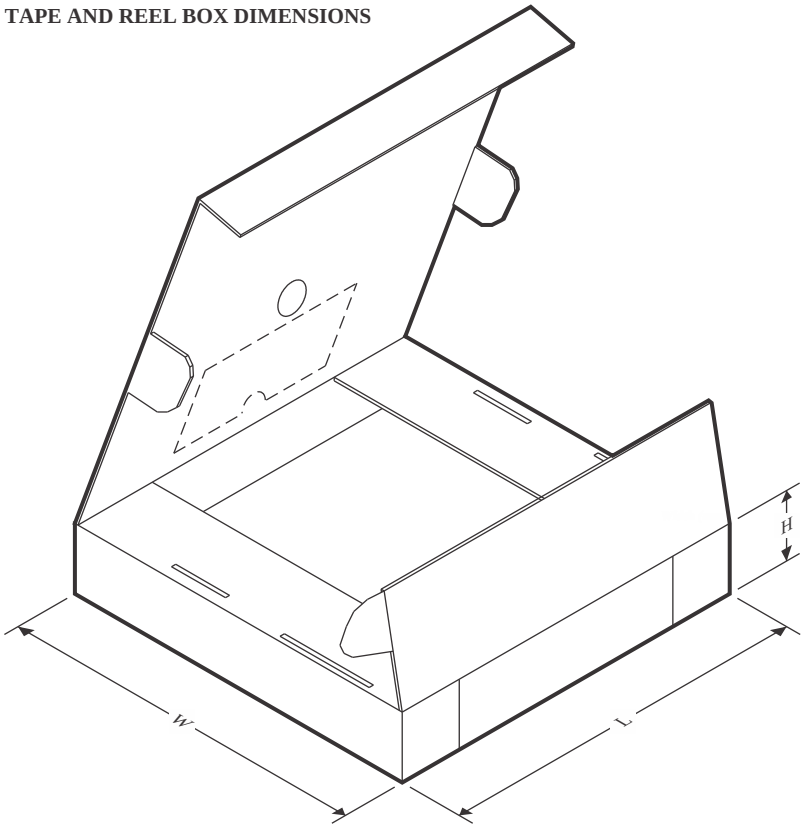
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5627CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV5627CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV5627IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

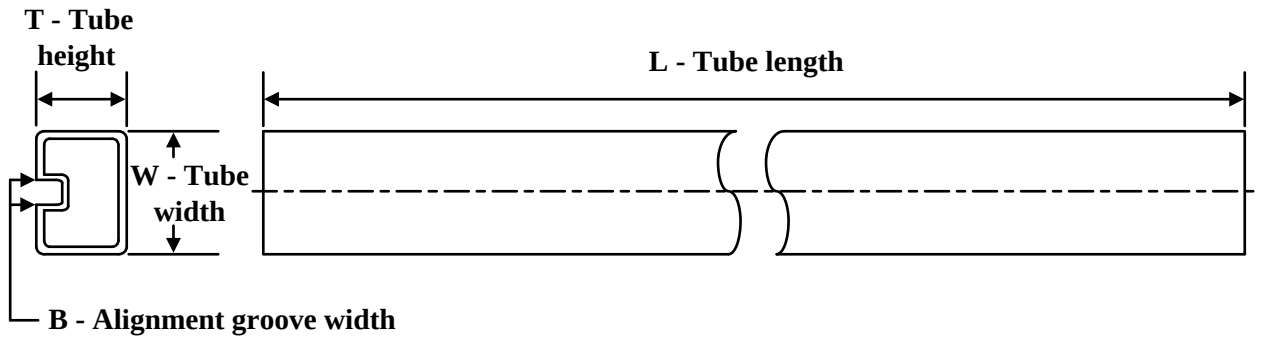
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5627CDR	SOIC	D	16	2500	350.0	350.0	43.0
TLV5627CPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
TLV5627IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5627CD	D	SOIC	16	40	505.46	6.76	3810	4
TLV5627CD.A	D	SOIC	16	40	505.46	6.76	3810	4
TLV5627CDG4	D	SOIC	16	40	505.46	6.76	3810	4
TLV5627CPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV5627CPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV5627ID	D	SOIC	16	40	505.46	6.76	3810	4
TLV5627ID.A	D	SOIC	16	40	505.46	6.76	3810	4
TLV5627IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV5627IPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5
TLV5627IPWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

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