TLV713P-Q1 Capacitor-Free, 150-mA, Low-Dropout Regulator With Foldback Current Limit for Portable Devices

1 Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range: 1.4 V to 5.5 V
- Stable Operation With or Without Capacitors
- Foldback Overcurrent Protection
- Package: 5-Pin SOT-23
- Very Low Dropout: 230 mV at 150 mA
- Accuracy: 1%
- Low I_Q: 50 µA
- Available in Fixed-Output Voltages:
  - 1 V to 3.3 V
- High PSRR: 65 dB at 1 kHz
- Active Output Discharge

2 Applications

- Automotive Head Units
- Audio Amplifiers
- DI Clusters
- ADAS ECUs
- Microprocessor Rails
- USBs
- Body Electronics

3 Description

The TLV713P-Q1 series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%.

The TLV713P-Q1 series of devices is designed to be stable without an output capacitor. The removal of the output capacitor allows for a very small solution size. However, the TLV713P-Q1 series is also stable with any output capacitor if an output capacitor is used.

The TLV713P-Q1 also provides inrush current control during device power-up and enabling. The TLV713P-Q1 limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

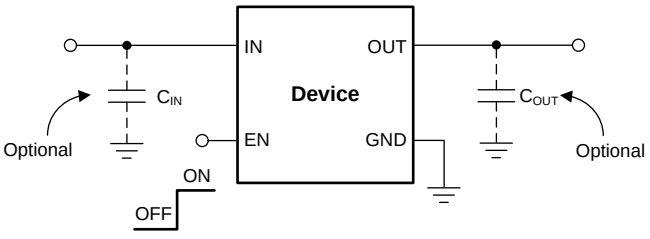
The TLV713P-Q1 series is available in a standard DBV package and provides an active pulldown circuit to quickly discharge output loads. The TLV713P-Q1 is suited for automotive applications because the device is qualified for AEC-Q100 grade 1.

Device Information(1)

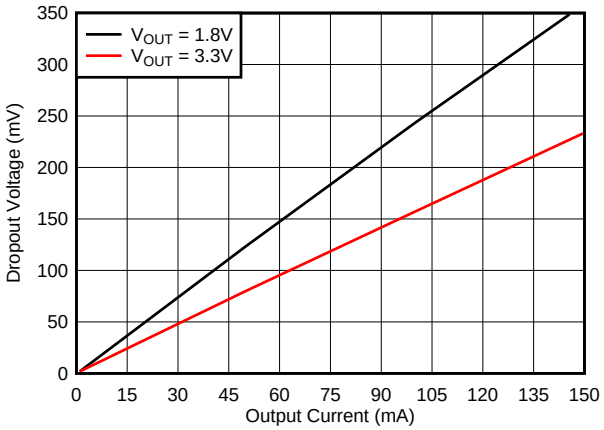
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV713P-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Dropout Voltage vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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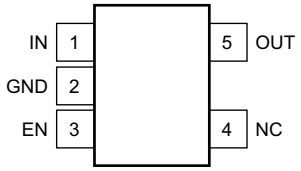
4 Revision History

DATE	REVISION	NOTES
May 2015	*	Initial release.

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5 Pin Configurations and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO. SOT-23		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	—	Ground pin
IN	1	I	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Considerations* section in the *Feature Description* for more details.
NC	4	—	No internal connection
OUT	5	O	Regulated output voltage pin. For best transient response, a small 1-µF ceramic capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Considerations* section in the *Feature Description* for more details.
Thermal pad		—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (T_J = 25°C), unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	V
	Output, V_{OUT}	–0.3	3.6	V
Current	Maximum output, $I_{OUT(max)}$	Internally limited		
Output short-circuit duration		Indefinite		
Total power dissipation	Continuous, $P_{D(tot)}$	See the *Thermal Information*		
Temperature	Storage, T_{stg}	–55	150	°C
	Junction, T_J	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V_{EN}	Enable range	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
C_{IN}	Input capacitor	0	1		µF
C_{OUT}	Output capacitor	0	0.1	100	µF
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		TLV713P-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	249	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	172.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

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6.5 Electrical Characteristics

Over operating temperature range (T_J, T_A = –40°C to 125°C), $V_{IN(nom)}$ = $V_{OUT(nom)}$ + 0.5 V or $V_{IN(nom)}$ = 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{OUT} = 0.47 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.4		5.5	V
V_{OUT}	Output voltage range			1		3.3	V
	DC output accuracy	V_{OUT} ≥ 1.8 V; T_J, T_A = 25°C		–1%		1%	
		V_{OUT} < 1.8 V; T_J, T_A = 25°C		–20		20	mV
		V_{OUT} ≥ 1.2 V; –40°C ≤ T_J, T_A ≤ 125°C		–1.5%		1.5%	
		V_{OUT} < 1.2 V; –40°C ≤ T_J, T_A ≤ 125°C		–50		50	mV
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	Max [$V_{OUT(nom)}$ + 0.5 V, V_{IN} = 2.0 V] ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(nom)}$; T_J, T_A = –40°C to 85°C	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	900	mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 30 mA		70		mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	575	mV
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 30 mA		50		mV
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 150 mA		246	445	mV
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 30 mA		46		mV
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	420	mV
		V_{OUT} = 0.98 × $V_{OUT(nom)}$; T_J, T_A = –40°C to 125°C	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	1020	mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	695	mV
			2.5 V ≤ V_{OUT} < 3 V, I_{OUT} = 150 mA		246	600	mV
			3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	560	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			50	75	µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V; 2.0 V ≤ V_{IN} ≤ 5.5 V; T_J, T_A = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 100 Hz		70		dB
			f = 10 kHz		55		dB
			f = 1 MHz		55		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			73		μV_{RMS}
t_{STR}	Start-up time	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 4 V			120		Ω
I_{LIM}	Output current limit	V_{IN} = 3.8 V, V_{OUT} = 3.3 V		175			mA
		V_{IN} = 3.0 V, V_{OUT} = 2.5 V		175			mA
		V_{IN} = 2.3 V, V_{OUT} = 1.8 V		175			mA
		V_{IN} = 2.0 V, V_{OUT} = 1.2 V		175			mA
		V_{IN} = 2.0 V, V_{OUT} = 1.0 V		175			mA
I_{SC}	Short-circuit current	V_{OUT} = 0 V			40		mA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			158		°C
		Reset, temperature decreasing			140		°C

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6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

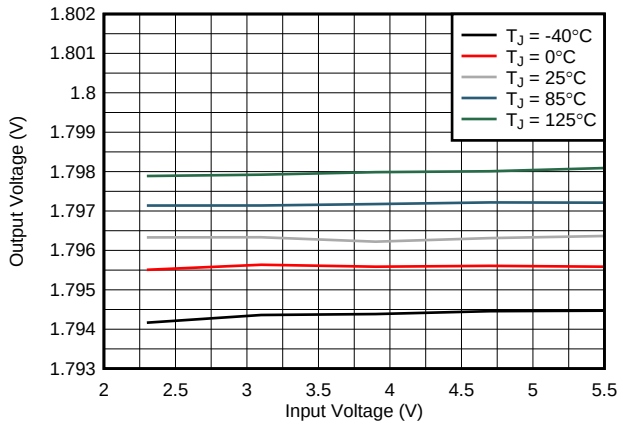


Figure 1. 1.8-V Line Regulation vs V_{IN} and Temperature

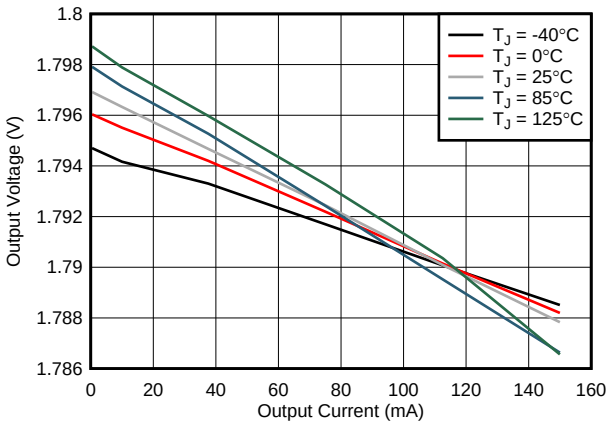


Figure 2. 1.8-V Load Regulation vs I_{OUT} and Temperature

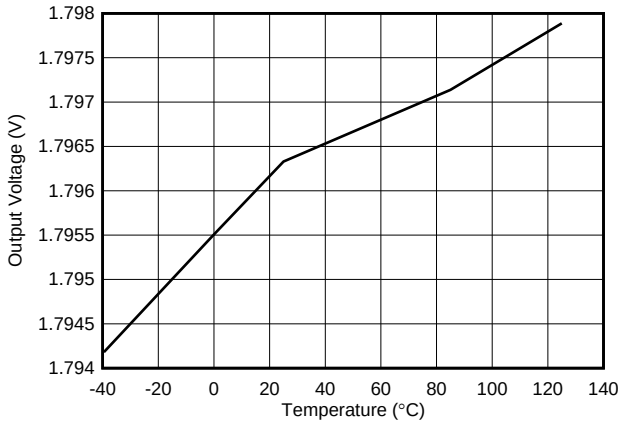


Figure 3. 1.8-V Output Voltage vs Temperature

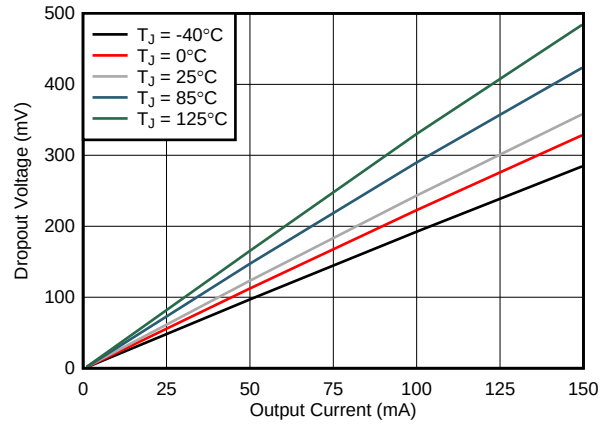


Figure 4. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

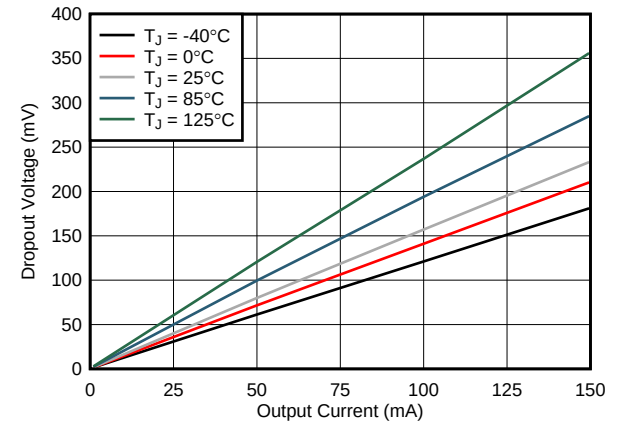


Figure 5. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

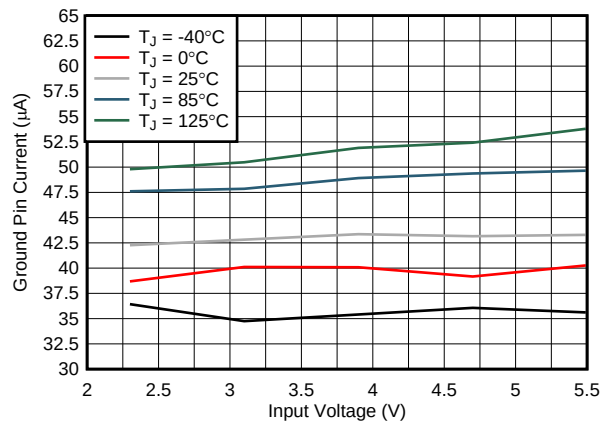


Figure 6. Ground Pin Current vs V_{IN} and Temperature

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.

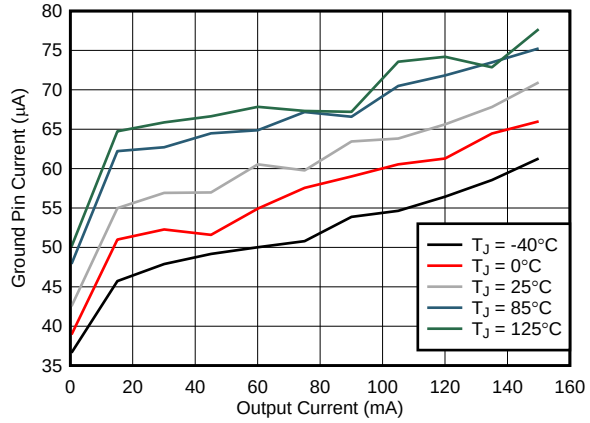


Figure 7. Ground Pin Current vs I_{OUT} and Temperature

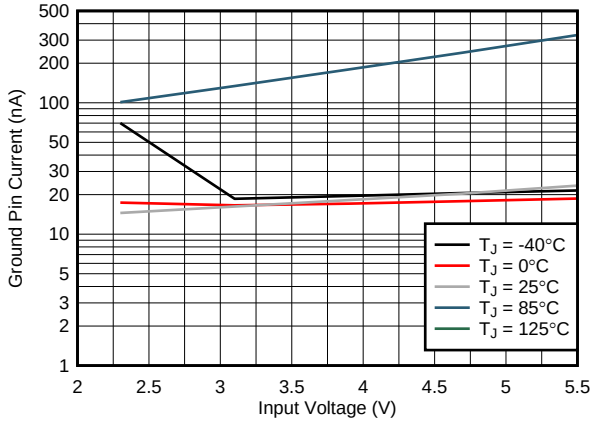


Figure 8. Shutdown Current vs V_{IN} and Temperature

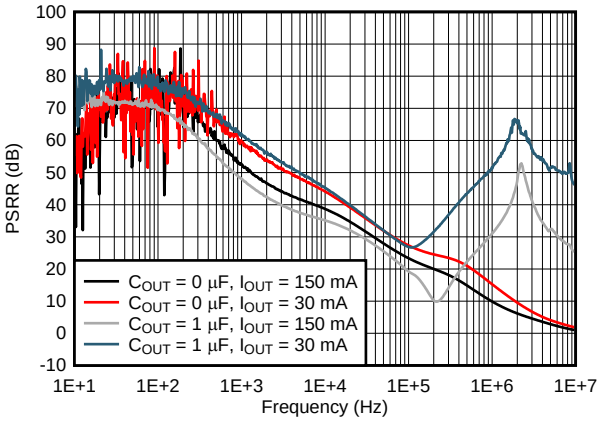


Figure 9. Power-Supply Rejection Ratio vs Frequency and C_{OUT}

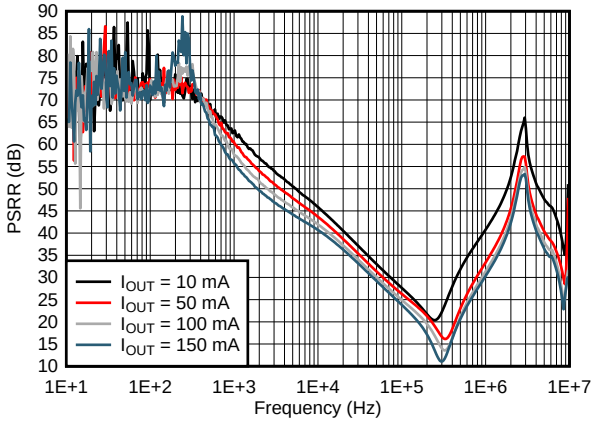


Figure 10. Power-Supply Rejection Ratio vs Frequency and I_{OUT}

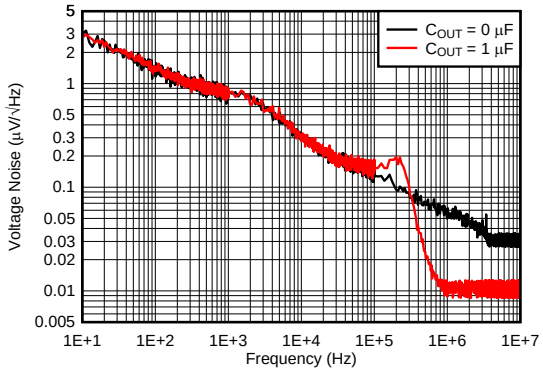
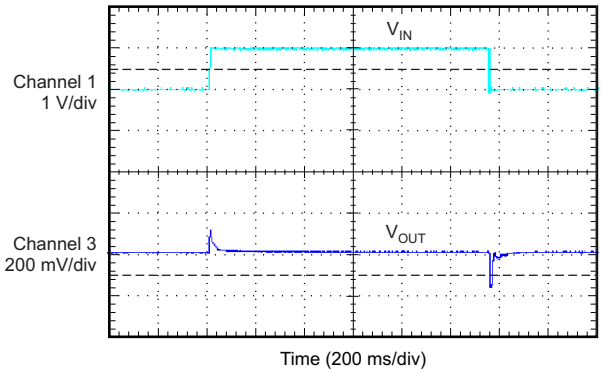


Figure 11. Output Spectral Noise Density



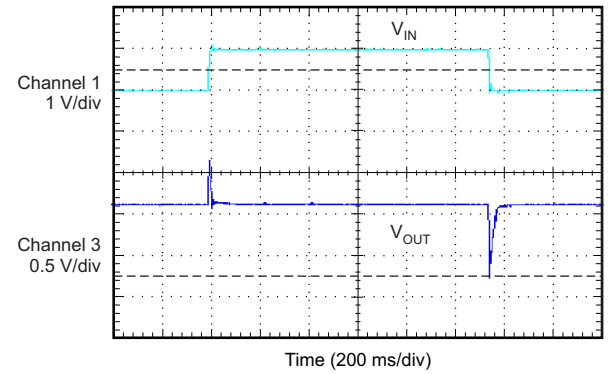
V_{IN} = 3 V to 4 V , I_{OUT} = 0 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 12. Line Transient

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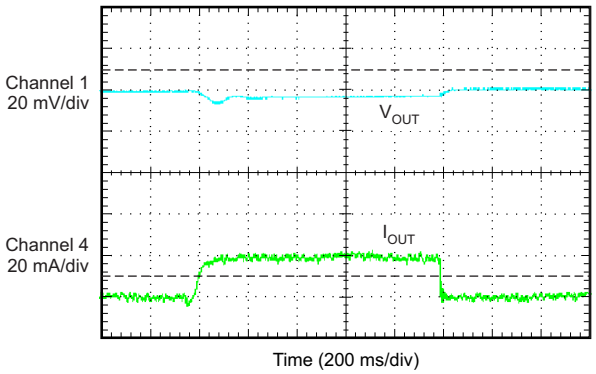
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.



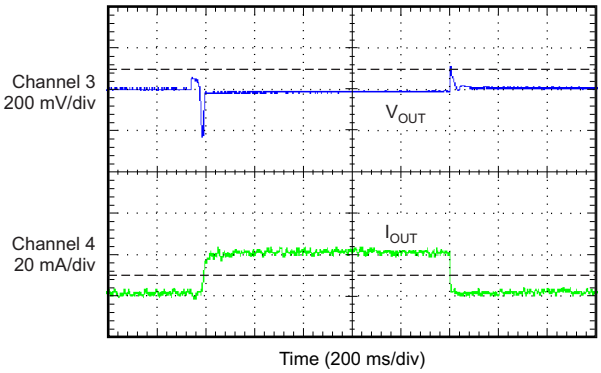
V_{IN} = 3 V to 4 V, I_{OUT} = 150 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 13. Line Transient



V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 1 µF

Figure 14. 0-mA to 20-mA Load Transient



V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 15. 0-mA to 20-mA Load Transient

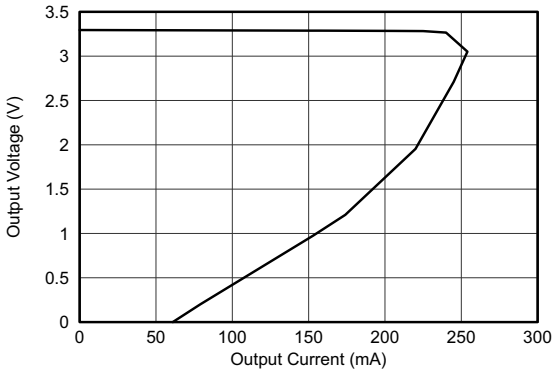
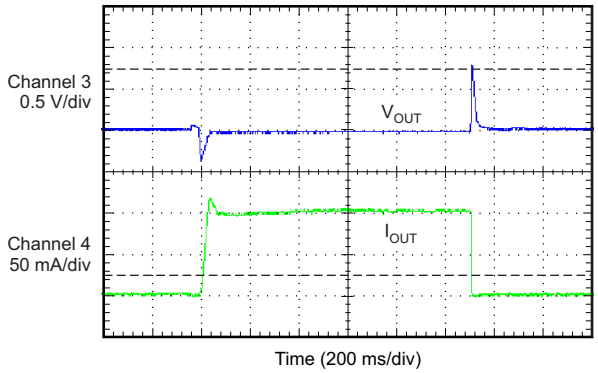


Figure 16. 3.3-V Output Voltage vs Output Current (Foldback Current Limit)



V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 17. 0-mA to 100-mA Load Transient

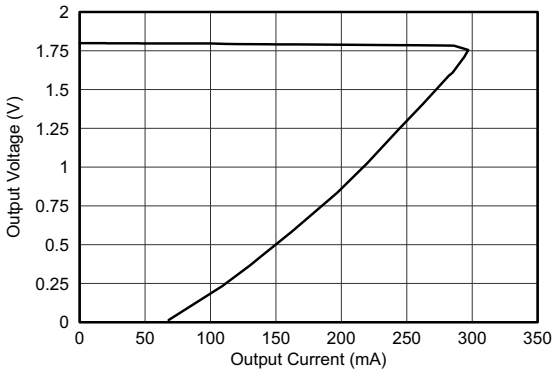
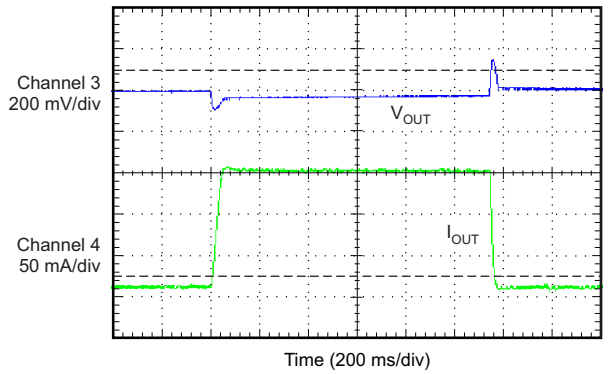


Figure 18. 1.8-V Output Voltage vs Output Current (Foldback Current Limit)

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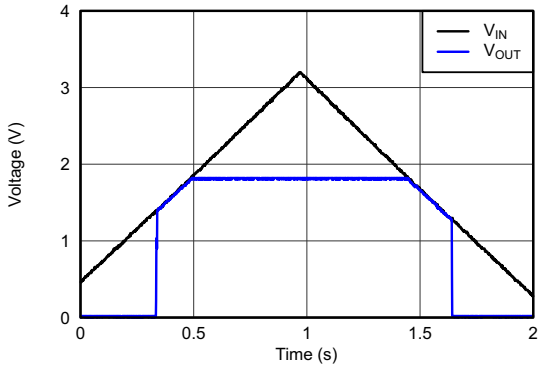
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and $V_{OUT(nom)}$ = 1.8 V, unless otherwise noted. Typical values are at T_J = 25°C.



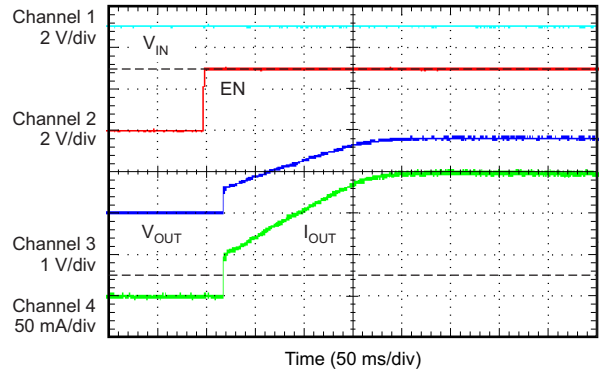
V_{IN} = 5 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 19. 10-mA to 150-mA Load Transient



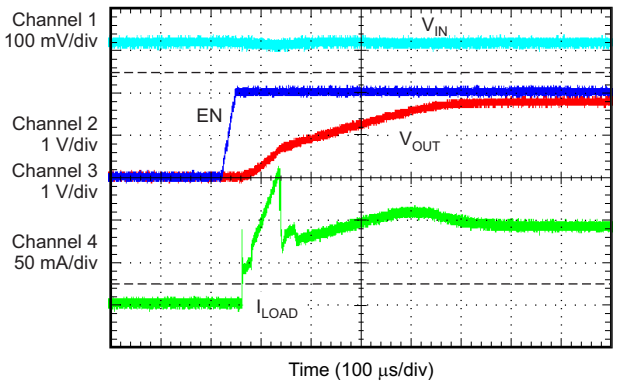
I_{OUT} = 150 mA

Figure 20. V_{IN} Power-Up and Power-Down



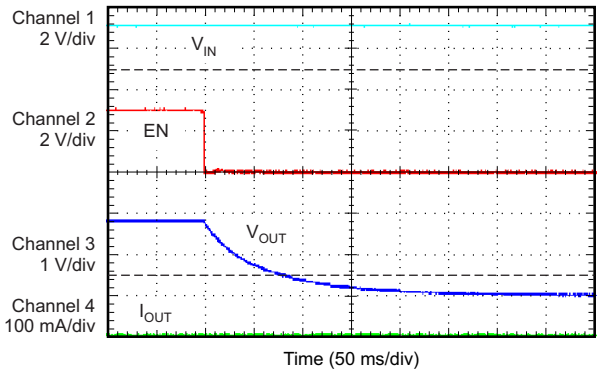
V_{IN} = 3 V, I_{OUT} = 150 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 0 µF

Figure 21. Start-Up With EN



V_{IN} = 2.3 V, I_{OUT} = 90 mA, C_{OUT} = 10 µF, V_{OUT} = 1.8 V, C_{IN} = 1 µF

Figure 22. Start-Up With EN



V_{IN} = 3 V, I_{OUT} = 0 mA, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 1 µF

Figure 23. Shutdown Response With Enable

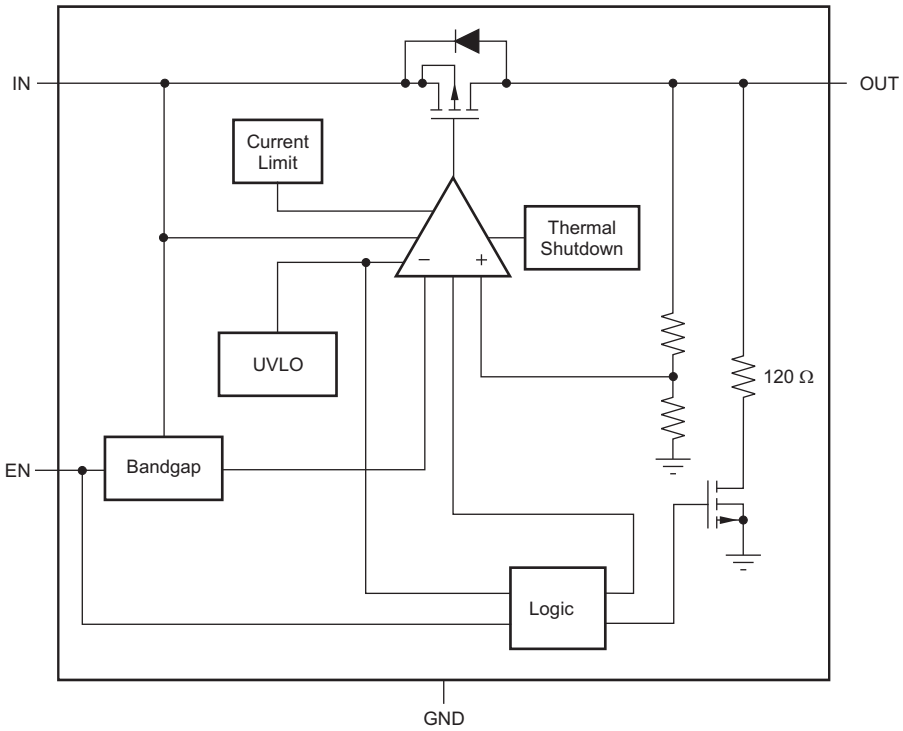
7 Detailed Description

7.1 Overview

These devices belong to a family of low-dropout (LDO) regulators that consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current limit and thermal protection. Device operating junction temperature is –40°C to 125°C.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV713P-Q1 uses a UVLO circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$. During UVLO disable, the output of the TLV713P-Q1 is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V. If shutdown capability is not required, connect EN to IN.

The TLV713P-Q1 has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1.

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

7.3.3 Foldback Current Limit

The TLV713P-Q1 has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device is gradually reduced when the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is calculated by Equation 2:

$$V_{OUT} = I_{LIMIT} \times R_{LOAD} \quad (2)$$

The PMOS pass transistor dissipates $[(V_{IN} – V_{OUT}) \times I_{LIMIT}]$ until thermal shutdown is triggered and the device turns off. The device is turned on by the internal thermal shutdown circuit during cool down. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The TLV713P-Q1 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV713P-Q1 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TLV713P-Q1 into thermal shutdown degrades device reliability.

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7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 158°C$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Considerations

The TLV713P-Q1 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. The TLV713P-Q1 dynamic performance is improved with the use of an output capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV713P-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded when (V_{IN} – V_{OUT}) approaches dropout.

8.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

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8.2 Typical Application

Several versions of the TPS713P-Q1 are ideal for powering the MSP430 microcontroller.

Figure 24 shows a diagram of the TLV713P-Q1 powering an MSP430 microcontroller. Table 2 shows potential applications of some voltage versions.

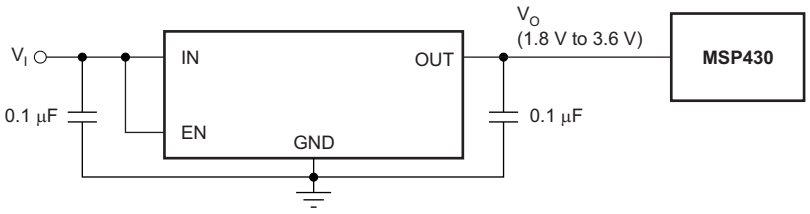


Figure 24. TLV713P-Q1 Powering a Microcontroller

Table 2. Typical MSP430 Applications

DEVICE	V_{OUT} (Typ)	APPLICATION
TLV71318P-Q1	1.8 V	Allows for lowest power consumption with many MSP430s
TLV71325P-Q1	2.5 V	2.2-V supply required by many MSP430s for flash programming and erasing

8.2.1 Design Requirements

Table 3 lists the design requirements.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, ±1%
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

An input capacitor is not required for this design because of the low impedance connection directly to the battery.

No output capacitor allows for the minimal possible inrush current during start-up, ensuring the 180-mA maximum input current limit is not exceeded.

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8.2.3 Application Curves

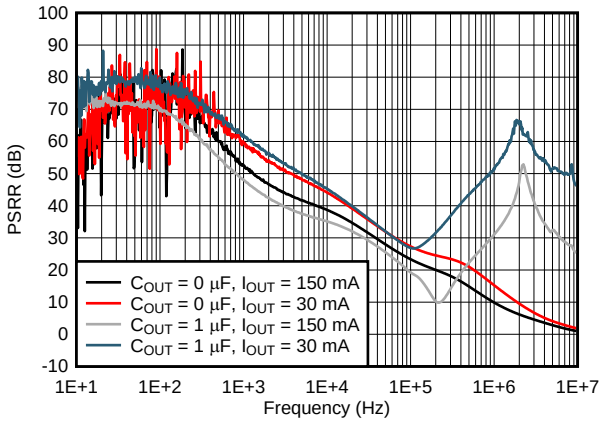


Figure 25. Power-Supply Rejection Ratio vs Frequency

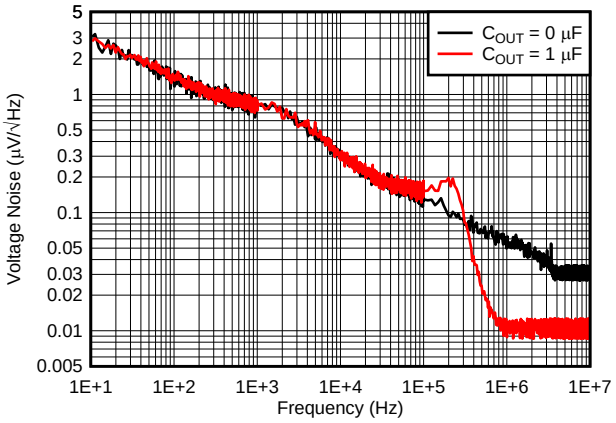


Figure 26. Output Spectral Noise Density

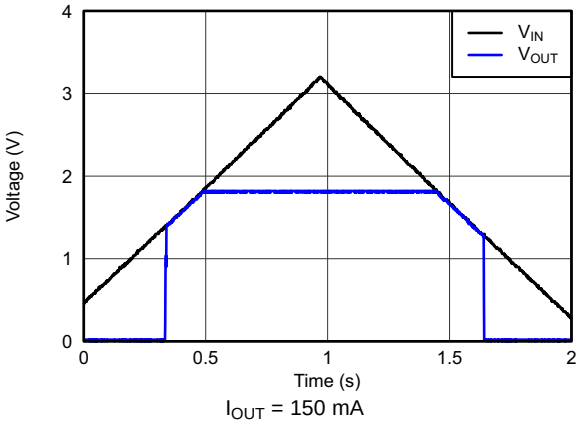


Figure 27. V_{IN} Power Up and Power Down

8.3 Do's and Don'ts

For best transient performance, place at least one 0.1-µF ceramic capacitor as close as possible to the OUT pin of the regulator and at least one 1-uF capacitor as close as possible to the IN pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.

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9 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.4 V to 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

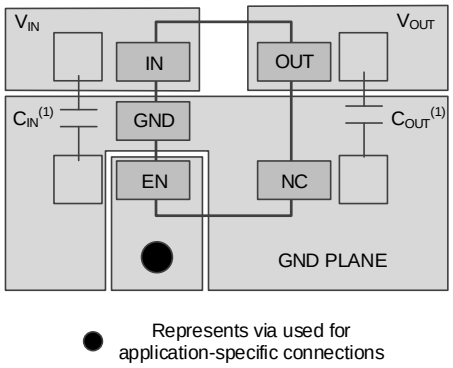
10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High-ESR capacitors may degrade PSRR performance.

10.2 Layout Example



(1) Not required.

Figure 28. SOT-23 Layout Example

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10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 3.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (3)$$

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, as discussed in the table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 4.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \quad (4)$$

where

- P_D is the power dissipation shown by Equation 3,
- T_T is the temperature at the center-top of the device package,
- T_B is the PCB temperature measured 1 mm away from the device package *on the PCB surface*.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

Three evaluation modules (EVMs) are available to assist in the initial circuit performance evaluation using the TLV713P-Q1:

- TLV71312PEVM-171
- TLV71318PEVM-171
- TLV71333PEVM-171

These EVMs come populated with the commercial version of the device in the DQN package; however, they can be used for parametric evaluation. These EVMs can be requested at the Texas Instruments website through the device product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV713P-Q1 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 4. Ordering Information(1) (2)

PRODUCT	V_{OUT}
TLV713P**xx**P**Q**yyyz**Q1**	**xx** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number (for example, 28 = 2.8 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, SBVA025
- *TLV713xxEVM-171 User's Guide*, SLVU771

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV71310PQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBGW
TLV71310PQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBGW
TLV71312PQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBHW
TLV71312PQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBHW
TLV71318PQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBIW
TLV71318PQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBIW
TLV71318PQDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBIW
TLV71318PQDBVRQ1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBIW
TLV71325PQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBJW
TLV71325PQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBJW
TLV71333PQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBKW
TLV71333PQDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBKW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV713P-Q1 :

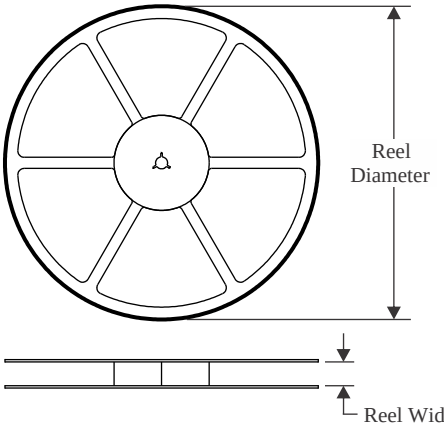
- Catalog : TLV713P

NOTE: Qualified Version Definitions:

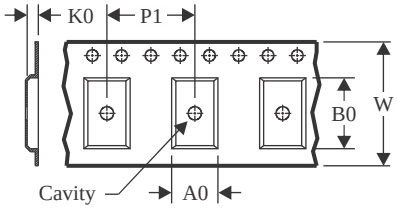
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

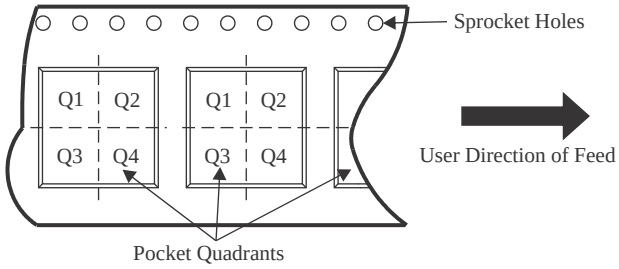


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

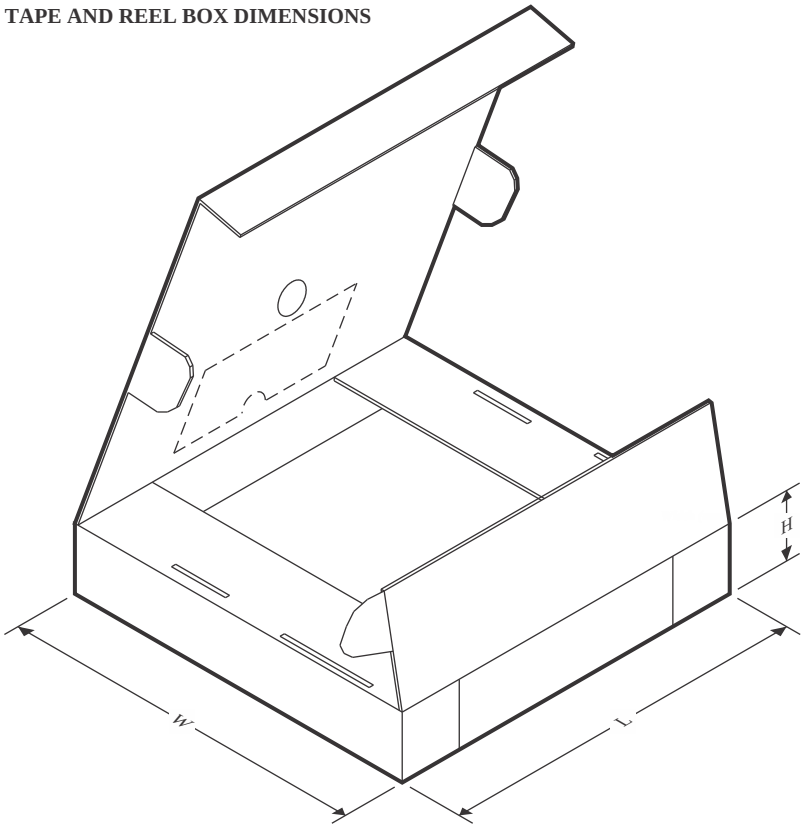
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71310PQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV71310PQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71312PQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV71312PQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71318PQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71318PQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV71318PQDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71325PQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV71325PQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71333PQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV71333PQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

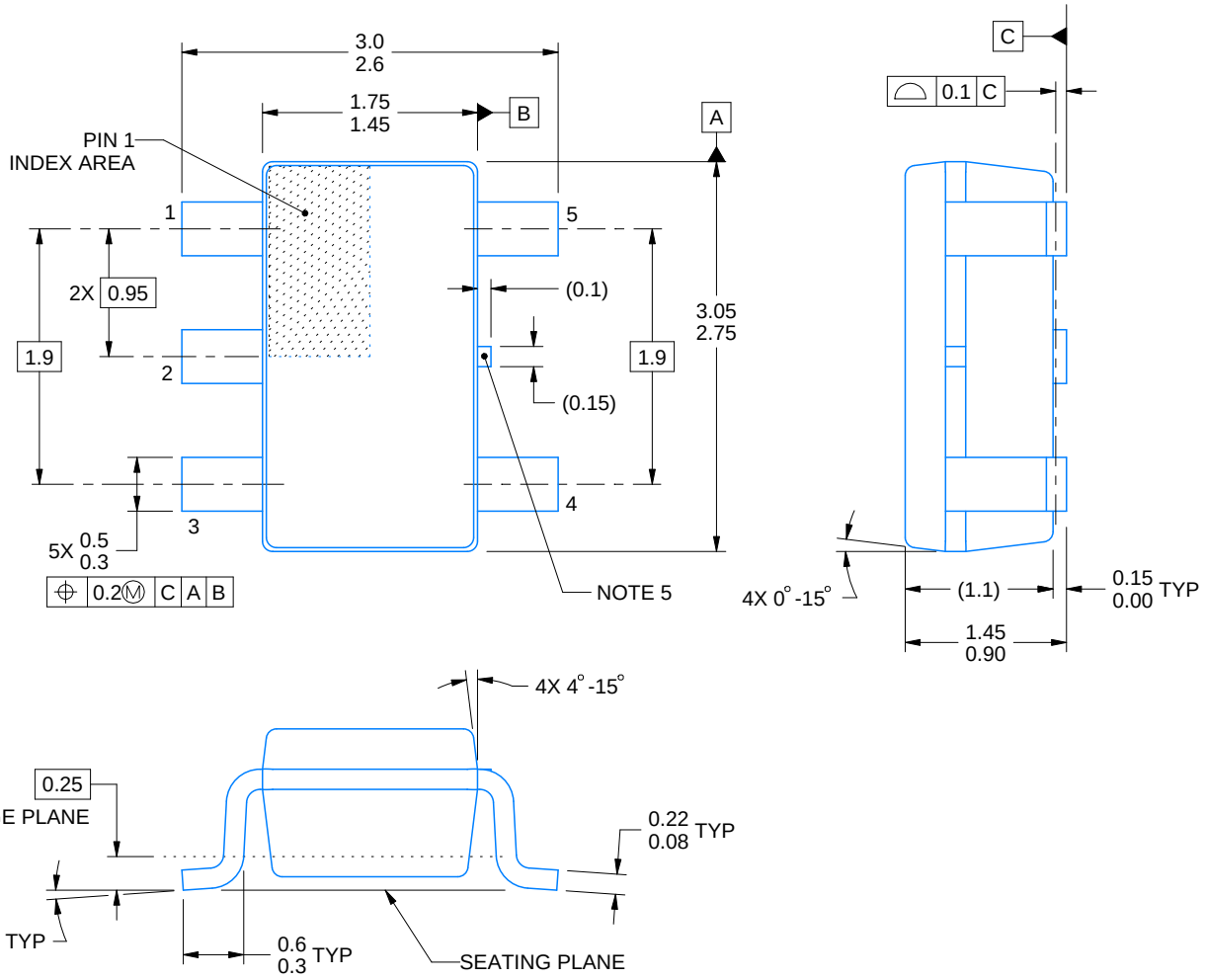
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71310PQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV71310PQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71312PQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV71312PQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71318PQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71318PQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV71318PQDBVRQ1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71325PQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV71325PQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71333PQDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV71333PQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

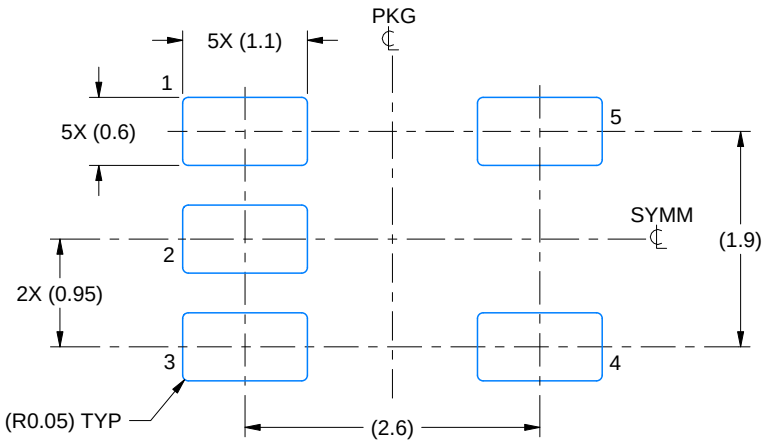
SMALL OUTLINE TRANSISTOR



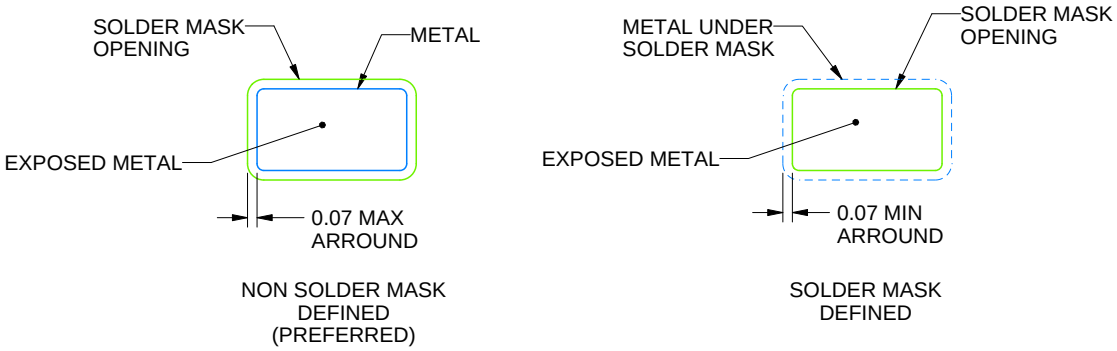
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

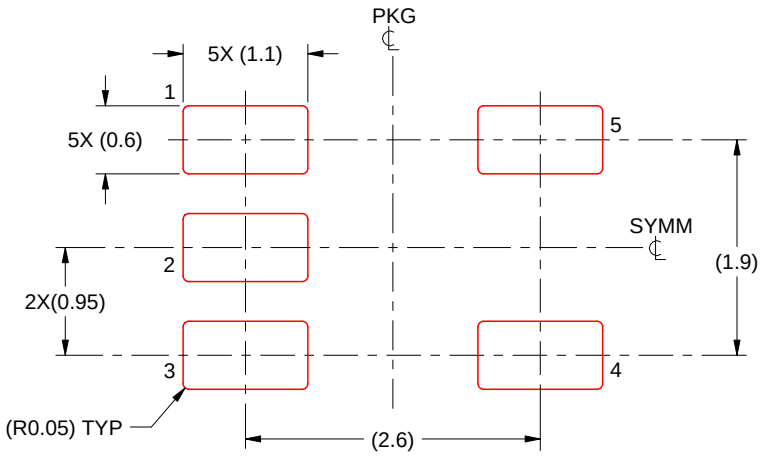


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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