CMOS Comparators with Rail-to-Rail Input and Push-Pull Output

1 Features

- Parameters specified at 2.7V, 5V, and 15V supplies
- Supply current 7µA (typical) at 5V
- Response time 420ns (typical) at 5V
- Push-pull output
- Input common-mode range beyond V_{CC-} and V_{CC+}
- Low input current

2 Applications

- Battery-powered products
- Notebooks and PDAs
- Mobile communications
- Alarm and security circuits
- Direct sensor interface
- Replaces amplifiers used as comparators with better performance and lower current

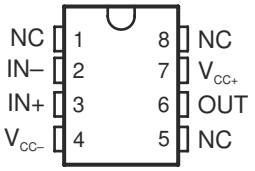
3 Description

The TLV7211 and TLV7211A are micropower CMOS comparators available in the space-saving SOT-23-5 package. This makes the comparators designed for space- and weight-critical designs. The TLV7211A features an input offset voltage of 5mV, and the TLV7211 features an input offset voltage of 15mV.

The main benefits of the SOT-23-5 package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the TLV7211 or TLV7211A a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

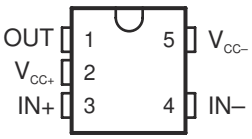
The small size of the SOT-23-5 package allows the device to fit into tight spaces on PC boards.

D PACKAGE (TOP VIEW)

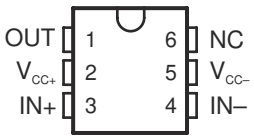


NC – No internal connection

DBV PACKAGE (TOP VIEW)



DCK PACKAGE (TOP VIEW)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Ordering Information

T_A	V_{OS} (MAX)	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	5mV	SOIC – D	Reel of 2500	TLV7211AIDR	7211AI
			Tube of 75	TLV7211AID	
		SOT-23-5 – DBV	Reel of 3000	TLV7211AIDBVR	YBN_
		SOT (SC-70) – DCK	Reel of 3000	TLV7211AIDCKR	Y8_
	15mV	SOIC – D	Reel of 2500	TLV7211IDR	TY7211
			Tube of 75	TLV7211ID	
		SOT-23-5 – DBV	Reel of 3000	TLV7211IDBVR	YBK_
		SOT (SC-70) – DCK	Reel of 3000	TLV7211IDCKR	Y7_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

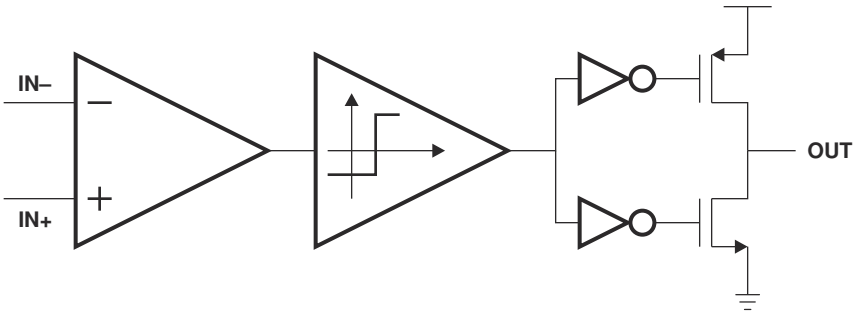

Figure 4-1. Functional Block Diagram

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage[1]			16	V
V_{ID}	Differential input voltage[2]			±Supply voltage	V
V_I	Input voltage range (any input)		$V_{CC–} – 0.3$	$V_{CC+} + 0.3$	V
V_O	Output voltage range		$V_{CC–} – 0.3$	$V_{CC+} + 0.3$	V
I_{CC}	Supply current			40	mA
I_I	Input current			±5	mA
I_O	Output current			±30	mA
θ_{JA}	Package thermal impedance[3] [4]	D package		97	°C/W
		DBV package		206	
		DCK package		259	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(2) Differential voltages are at IN+ with respect to IN–.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Protection

	TYP	UNIT
Human-Body Model	2000	V

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage	2.7	15	V
T_J	Operating virtual junction temperature	–40	85	°C

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5.4 2.7V Electrical Characteristics

V_{CC+} = 2.7V, V_{CC-} = GND, V_{CM} = V_O = V_{CC+}/2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	TLV7211A			TLV7211			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage		25°C		3	5		3	15	mV
			–40°C to 85°C			8			18	
TCV_{OS}	Input offset voltage temperature drift		25°C		1			1		μV/°C
I_B	Input current		25°C		0.04			0.04		pA
I_{OS}	Input offset current		25°C		0.02			0.02		pA
CMRR	Common-mode rejection ratio	0 ≤ V_{CM} ≤ 2.7V	25°C		75			75		dB
PSRR	Power-supply rejection ratio	2.7V ≤ V_{CC+} ≤ 15V	25°C		80			80		dB
A_V	Voltage gain		25°C		100			100		dB
CMVR	Input common-mode voltage range	CMRR > 55dB	25°C	2.9	3		2.9	3		V
			–40°C to 85°C	2.7			2.7			
		CMRR > 55dB	25°C		–0.3	–0.2		–0.3	–0.2	
			–40°C to 85°C			0			0	
V_{OH}	High-level output voltage	I_{load} = 2.5mA	25°C	2.4	2.5		2.4	2.5		V
			–40°C to 85°C	2.3			2.3			
V_{OL}	Low-level output voltage	I_{load} = 2.5mA	25°C		0.2	0.3		0.2	0.3	V
			–40°C to 85°C			0.4			0.4	
I_{CC}	Supply current	V_{OUT} = Low	25°C		7	12		7	12	μA
			–40°C to 85°C			14			14	
		V_{OUT} = High-Idle	25°C		5	10		5	10	
			–40°C to 85°C			12			12	

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5.5 5V Electrical Characteristics

V_{CC+} = 5V, V_{CC-} = GND, V_{CM} = V_O = V_{CC+}/2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	TLV7211A			TLV7211			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage		25°C		3	5		3	15	mV
			–40°C to 85°C			8			18	
TCV_{OS}	Input offset voltage temperature drift		25°C		1			1		μV/°C
I_B	Input current		25°C		0.04			0.04		pA
I_{OS}	Input offset current		25°C		0.02			0.02		pA
CMRR	Common-mode rejection ratio		25°C		75			75		dB
PSRR	Power-supply rejection ratio	5V ≤ V_{CC+} ≤ 10V	25°C		80			80		dB
A_V	Voltage gain		25°C		100			100		dB
CMVR	Input common-mode voltage range	CMRR > 55dB	25°C	5.2	5.3		5.2	5.3		V
			–40°C to 85°C	5			5			
		CMRR > 55dB	25°C		–0.3	–0.2		–0.3	–0.2	
			–40°C to 85°C			0			0	
V_{OH}	High-level output voltage	I_{load} = 5mA	25°C	4.6	4.8		4.6	4.8		V
			–40°C to 85°C	4.45			4.45			
V_{OL}	Low-level output voltage	I_{load} = 5mA	25°C		0.2	0.4		0.2	0.4	V
			–40°C to 85°C			0.55			0.55	
I_{CC}	Supply current	V_{OUT} = Low	25°C		7	14		7	14	μA
			–40°C to 85°C			18			18	
		V_{OUT} = High-Idle	25°C		5	10		5	10	
			–40°C to 85°C			13			13	
I_{OH}	Short-circuit output current	I_{source}	25°C	30			30			mA
I_{OL}	Short-circuit output current	I_{sink}, V_O < 12V(1)	25°C	45			45			mA

(1) Do not short circuit the output to V+ if V+ is >12V.

5.6 15V Electrical Characteristics

V_{CC+} = 15V, V_{CC-} = GND, V_{CM} = V_O = V_{CC+}/2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	TLV7211A			TLV7211			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input offset voltage		25°C		3	5		3	15	mV
			–40°C to 85°C			8			18	
TCV_{OS}	Input offset voltage temperature drift		25°C		4			4		µV/°C
I_B	Input current		25°C		0.04			0.04		pA
I_{OS}	Input offset current		25°C		0.02			0.02		pA
CMRR	Common-mode rejection ratio		25°C		82			82		dB
PSRR	Power-supply rejection ratio	5V ≤ V_{CC+} ≤ 10V	25°C		80			80		dB
A_V	Voltage gain		25°C		100			100		dB
CMVR	Input common-mode voltage range	CMRR > 55dB	25°C	15.2	15.3		15.2	15.3		V
			–40°C to 85°C	15			15			
		CMRR > 55dB	25°C		–0.3	–0.2		–0.3	–0.2	
			–40°C to 85°C			0			0	
V_{OH}	High-level output voltage	I_{load} = 5mA	25°C	14.6	14.8		14.6	14.8		V
			–40°C to 85°C	14.45			14.45			
V_{OL}	Low-level output voltage	I_{load} = 5mA	25°C		0.2	0.4		0.2	0.4	V
			–40°C to 85°C			0.55			0.55	
I_{CC}	Supply current	V_{OUT} = Low	25°C		7	14		7	14	µA
			–40°C to 85°C			18			18	
		V_{OUT} = High-Idle	25°C		5	12		5	12	
			–40°C to 85°C			14			14	
I_{OH}	Short-circuit output current	I_{source}	25°C	30			30			mA
I_{OL}	Short-circuit output current	I_{sink}, V_O < 12V[(1)]	25°C	45			45			mA

(1) Do not short circuit the output to V+ if V+ is >12 V.

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5.7 Switching Characteristics

T_J = 25°C, V_{CC+} = 5V, V_{CC-} = GND, V_{CM} = V_O = V_{CC+}/2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	UNIT
t_{rise}	Rise time	f = 10kHz, C_L = 50pF(1), Overdrive = 10mV		15	ns
t_{fall}	Fall time	f = 10kHz, C_L = 50pF(1), Overdrive = 10mV		15	ns
t_{PHL}	Propagation delay time, high to low	f = 10kHz, C_L = 50pF(1)	10mV	900	ns
			100mV	450	
t_{PLH}	Propagation delay time, low to high	f = 10kHz, C_L = 50pF(1)	10mV	900	ns
			100mV	420	

(1) C_L includes probe and jig capacitance.

5.8 Typical Characteristics

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

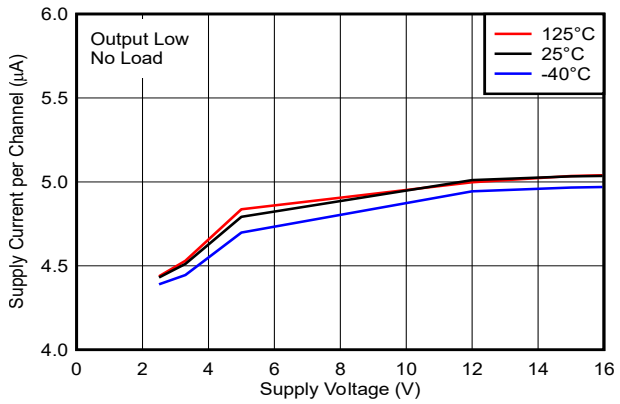

Figure 5-1. Supply Current per Channel vs. Supply Voltage, Output Low

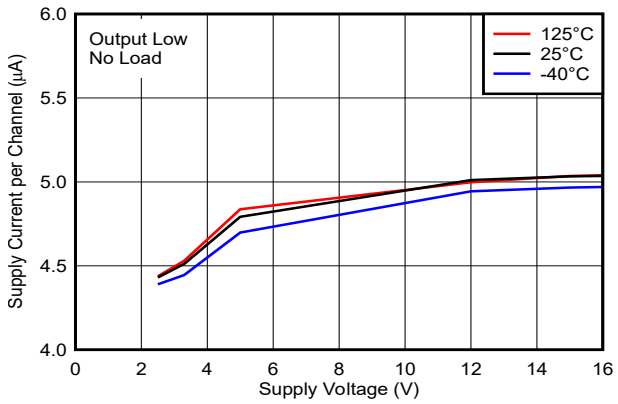

Figure 5-2. Supply Current per Channel vs. Supply Voltage, Output High

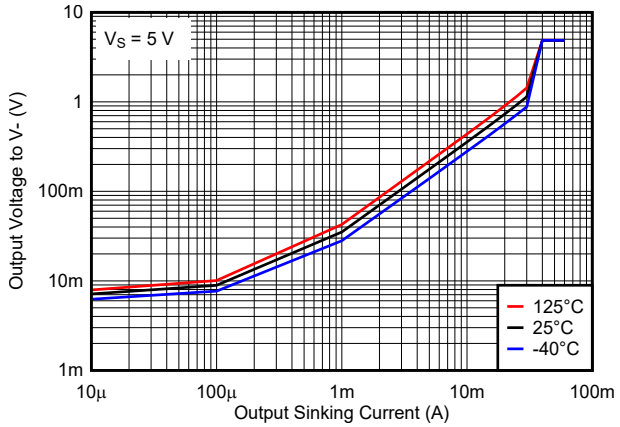

Figure 5-3. Output Voltage vs. Output Sinking Current, 5V

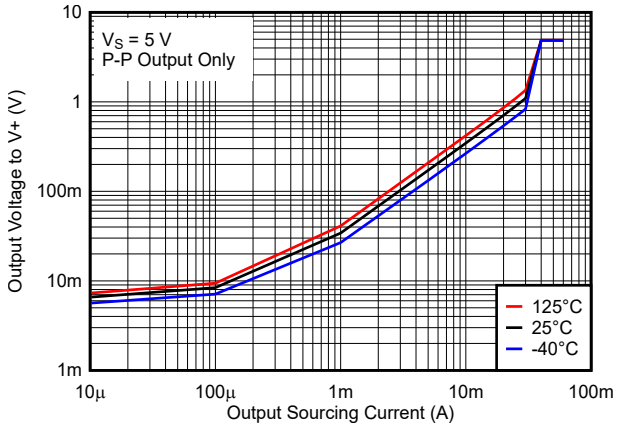

Figure 5-4. Output Voltage vs. Output Sourcing Current, 5V

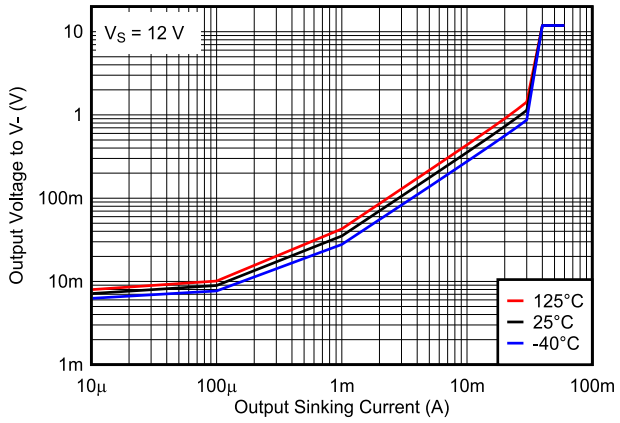

Figure 5-5. Output Voltage vs. Output Sinking Current, 12V

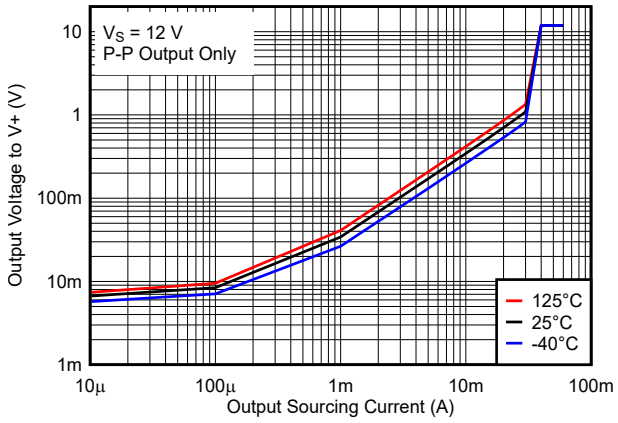

Figure 5-6. Output Voltage vs. Output Sourcing Current, 12V

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5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

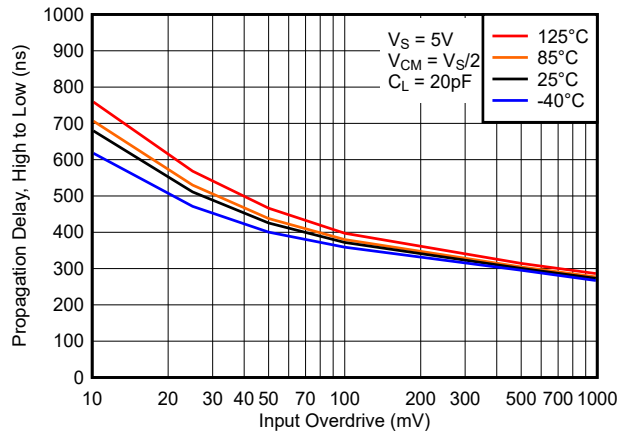


Figure 5-7. Propagation Delay, High to Low, 5V

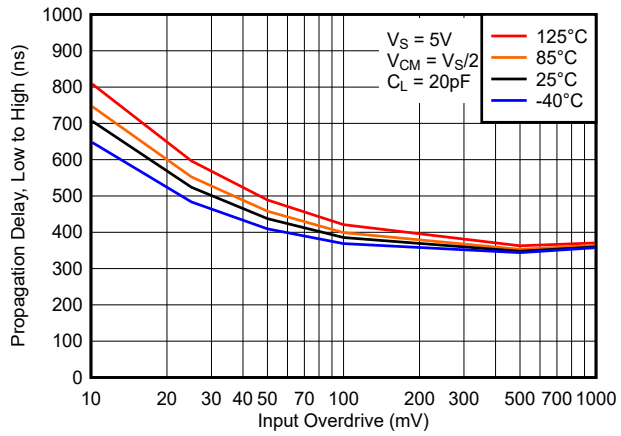


Figure 5-8. Propagation Delay, Low to High, 5V

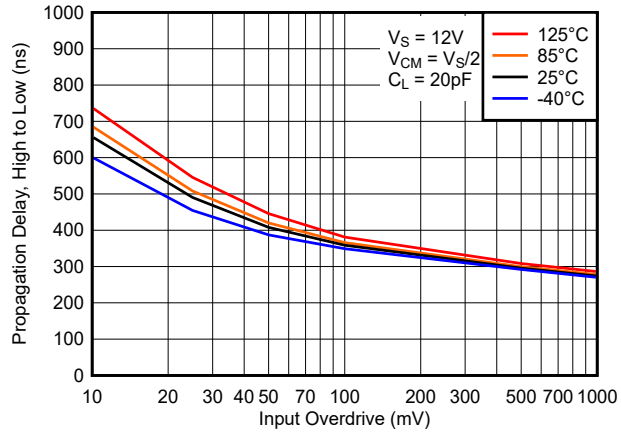


Figure 5-9. Propagation Delay, High to Low, 12V

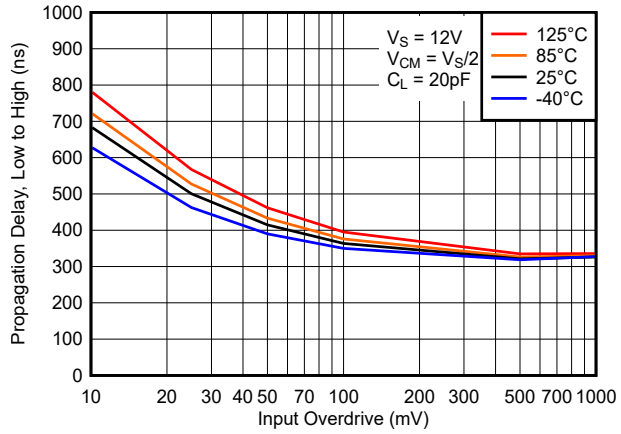


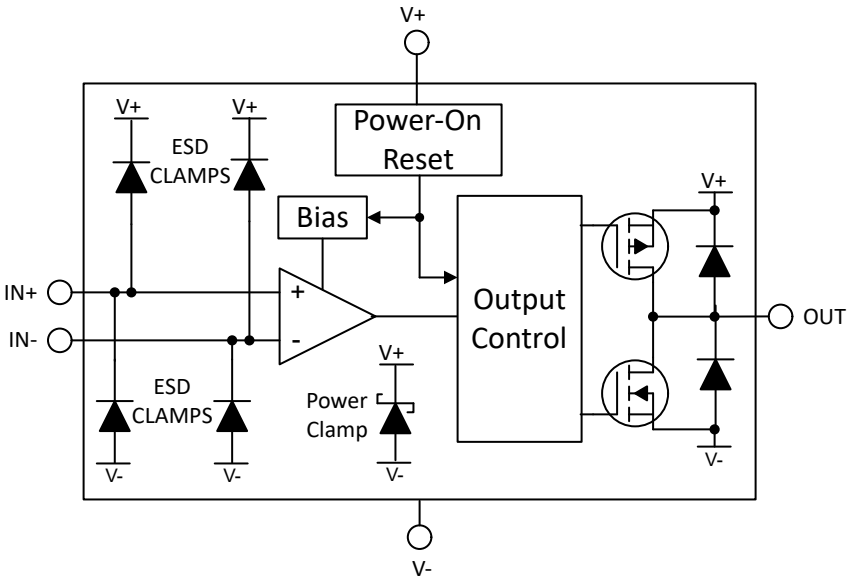
Figure 5-10. Propagation Delay, Low to High, 12V

6 Detailed Description

6.1 Overview

The TLV7211 push-pull output comparator features a low quiescent current 7uA and operation from 2.7V to 15V. The push-pull CMOS output stage drives capacitive loads directly without a power consuming pull-up resistor to achieve the stated response time. Likewise, an internal power-on reset circuit is integrated so the outputs remain in a known state during power-up and power-down.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Functional Modes

The TLV7211 is powered on when the supply is connected. The device can operate with single or dual supply, depending on the application. The device is in the full performance once the supply is above the recommended value.

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6.3.2 Power-On Reset (POR)

The TLV7211 has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 200µs after 1.7V is crossed, or immediately when the supply voltage drops below 1.7V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV7211 push-pull output devices, the output is held low during the POR period (t_{on}).

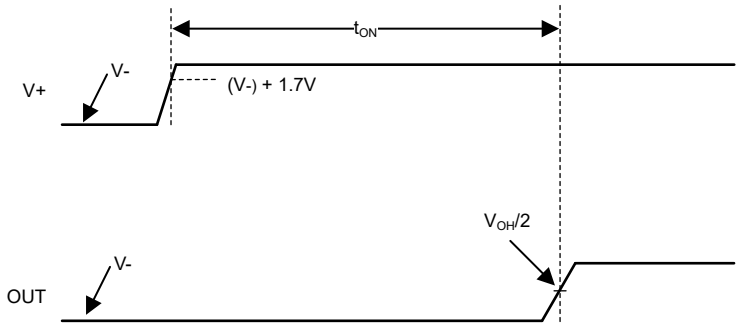

Figure 6-1. Power-On Reset Timing Diagram

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2007) to Revision C (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated propagation delay and rise and fall times specifications throughout document	1
• Removed typical input offset voltage average drift in the *Electrical Characteristics* tables	4
• Updated the Typical Performance Characteristics curves	8
• Added Power-on-Reset (POR) description	11

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7211AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YBNM
TLV7211AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YBNM
TLV7211AIDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y8A
TLV7211AIDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y8A
TLV7211AIDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV7211AIDCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	Y8A
TLV7211AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	YBKM
TLV7211IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YBKM
TLV7211IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y7A
TLV7211IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y7A
TLV7211IDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV7211IDCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	Y7A
TLV7211IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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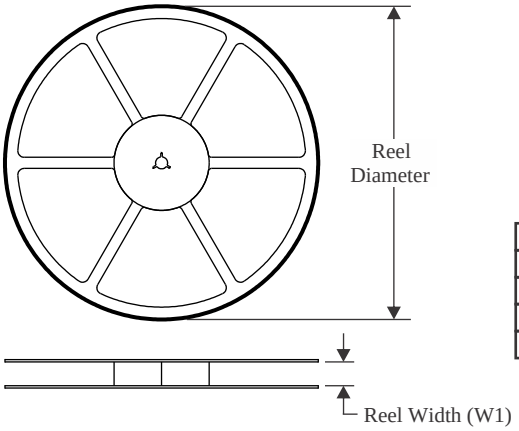
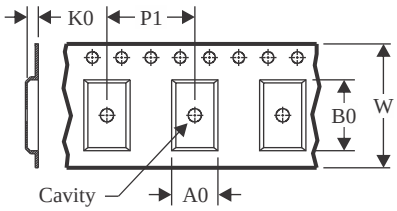
TAPE AND REEL INFORMATION

REEL DIMENSIONS

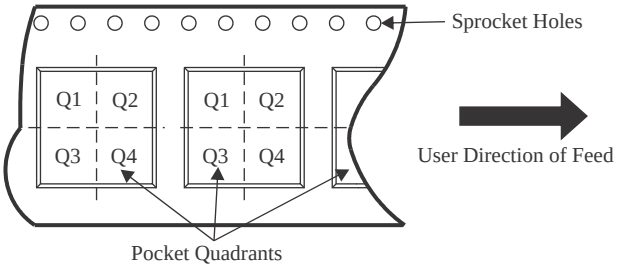


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

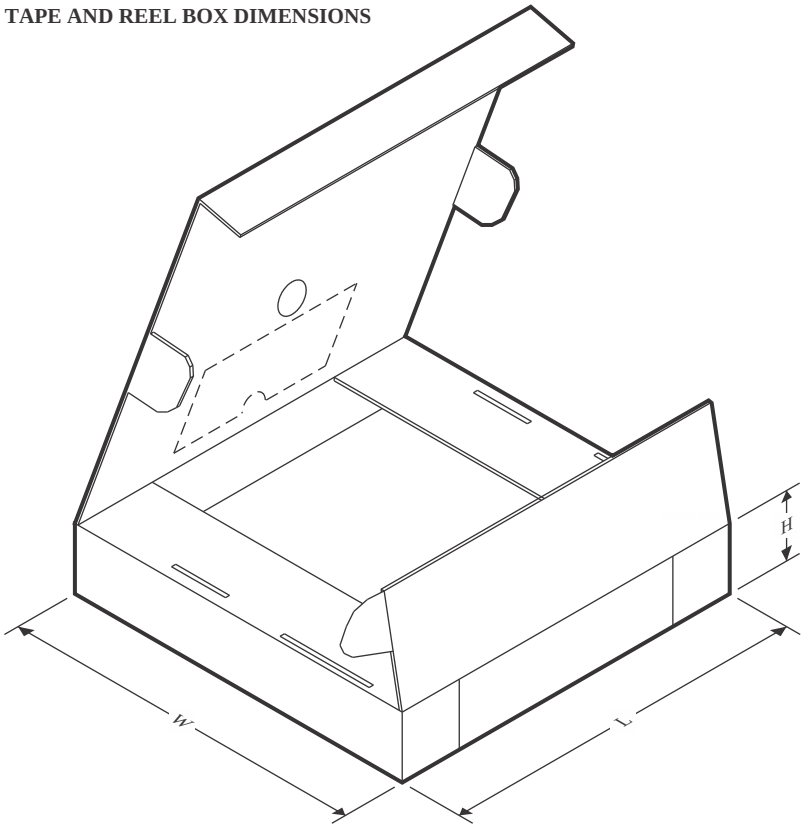
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7211AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV7211IDBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV7211IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

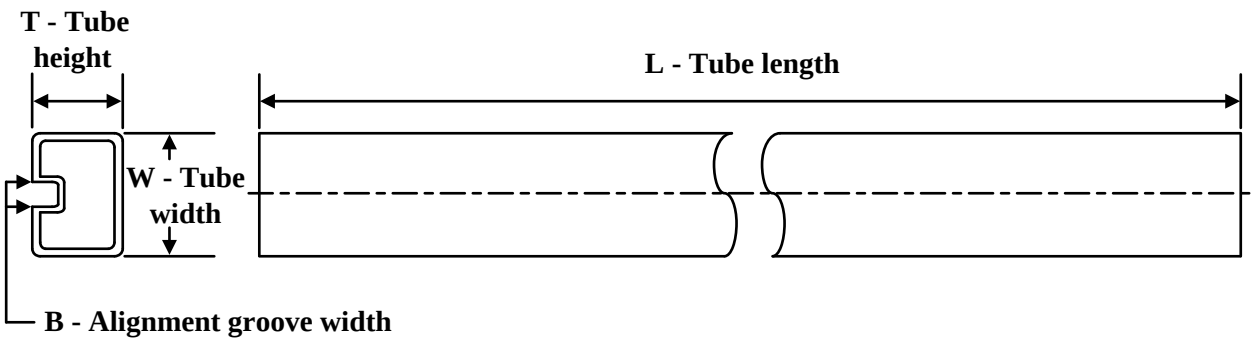
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

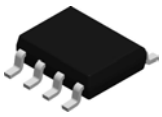
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7211AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7211AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV7211AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV7211IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7211IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV7211IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV7211IDRG4	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV7211AID	D	SOIC	8	75	507	8	3940	4.32
TLV7211AID.A	D	SOIC	8	75	507	8	3940	4.32
TLV7211ID	D	SOIC	8	75	507	8	3940	4.32
TLV7211ID.A	D	SOIC	8	75	507	8	3940	4.32

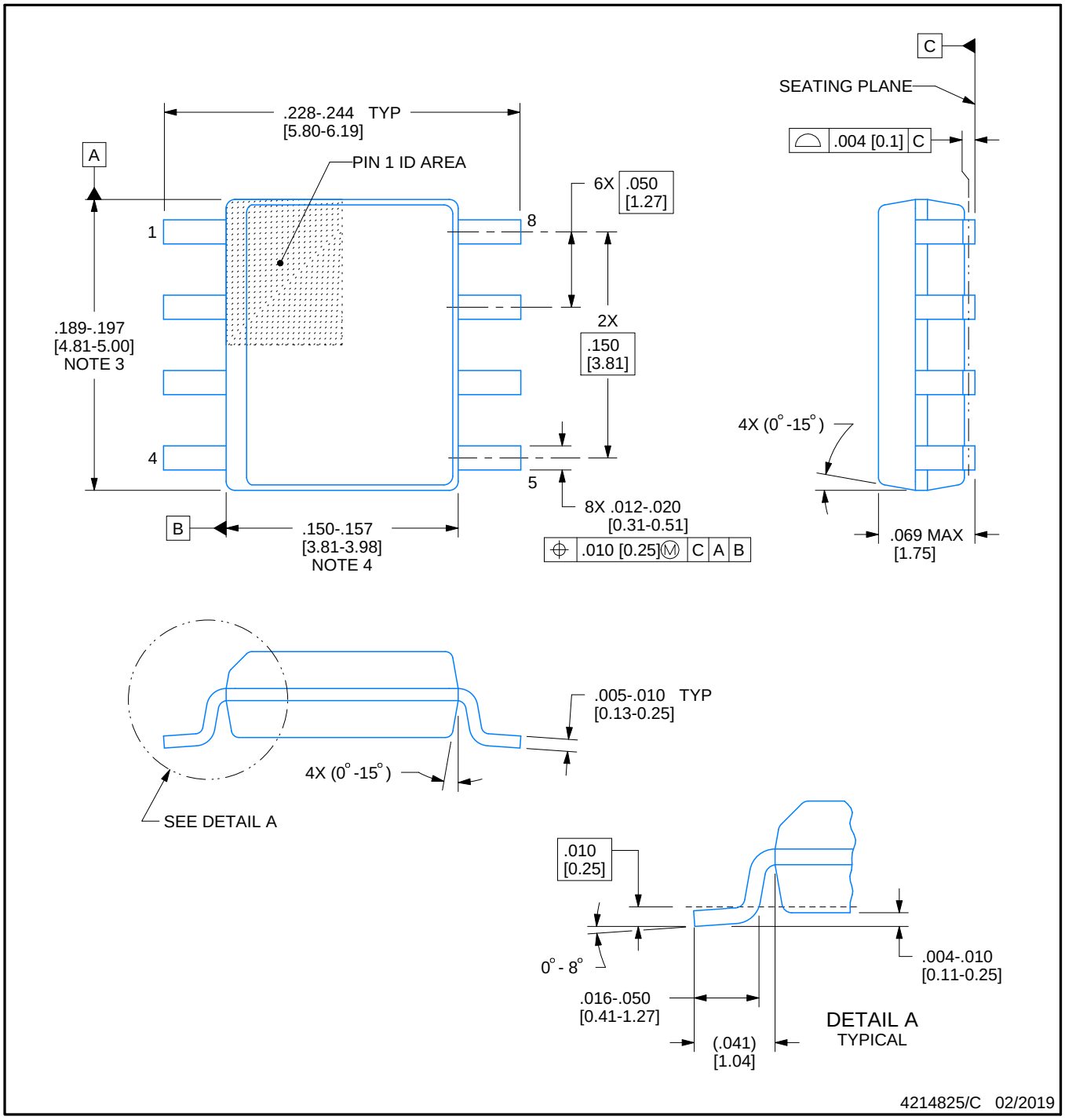


PACKAGE OUTLINE

D0008A

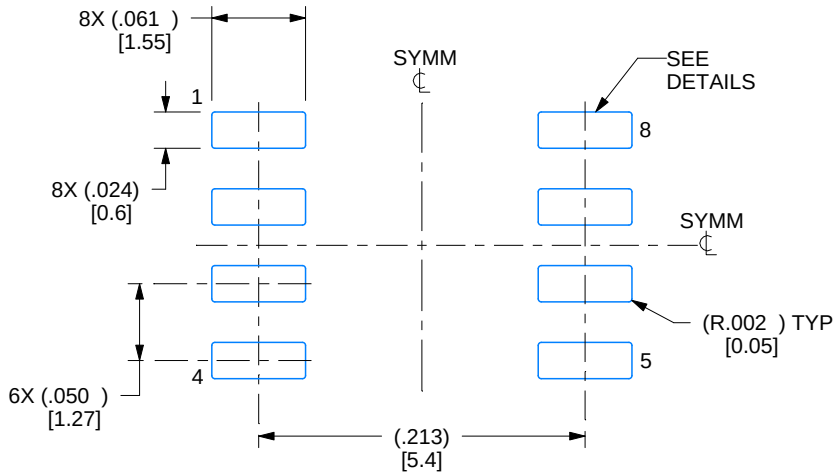
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

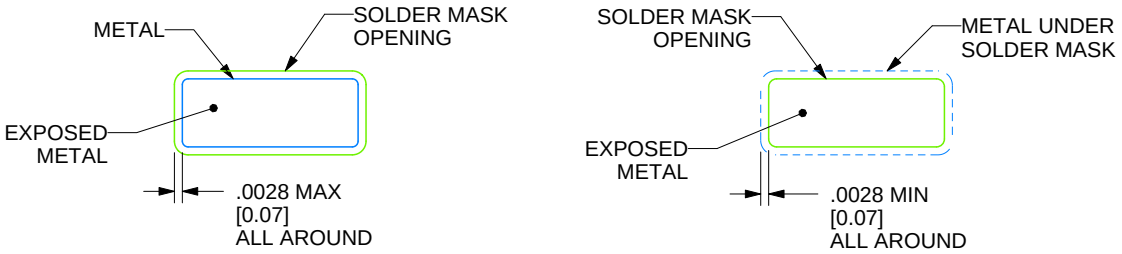


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

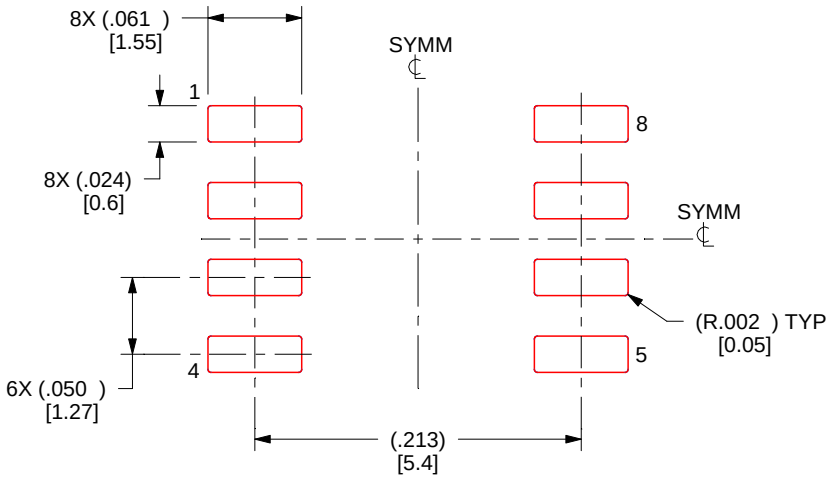


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

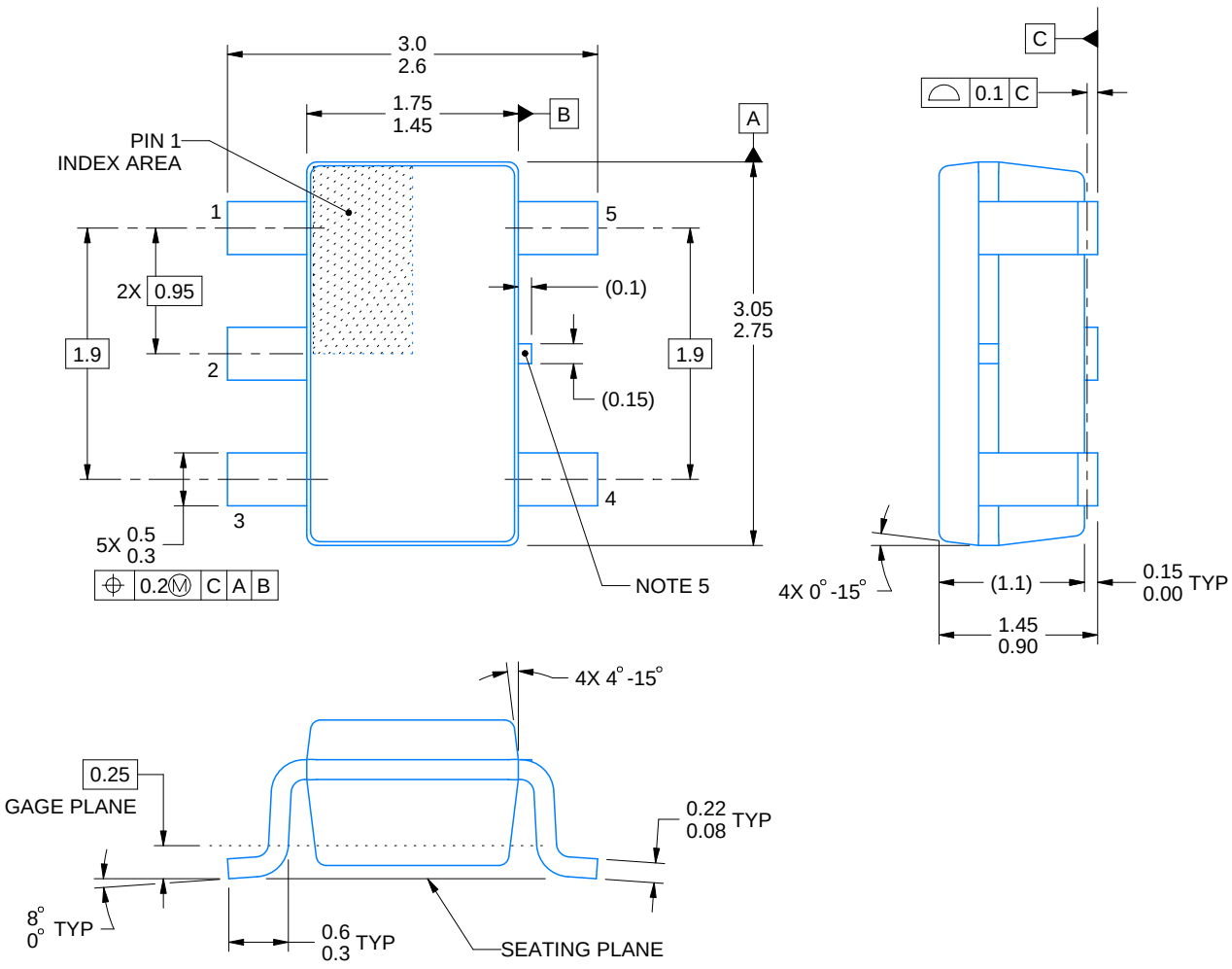


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

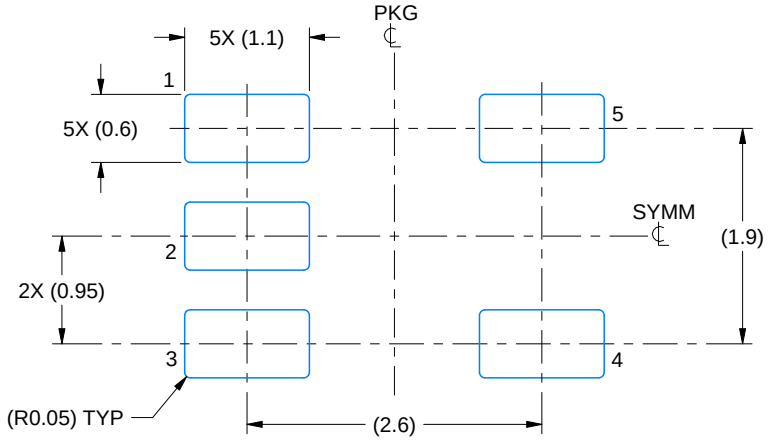
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



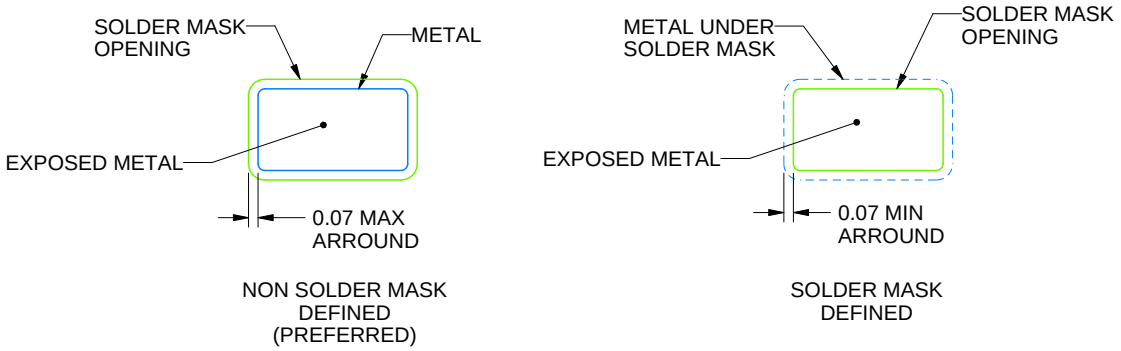
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

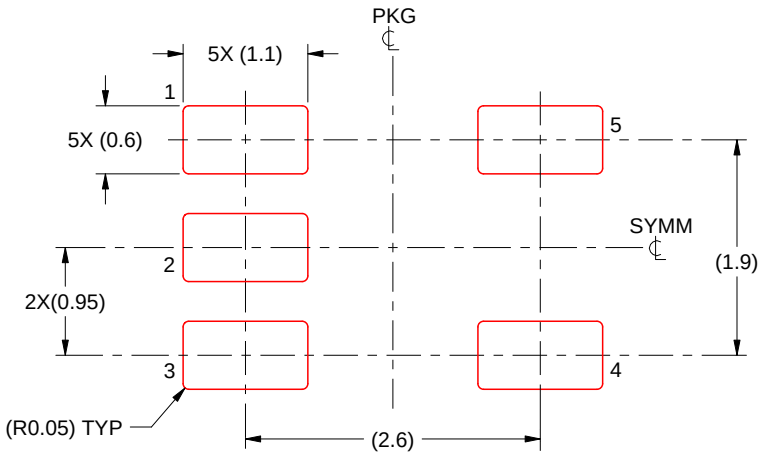


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

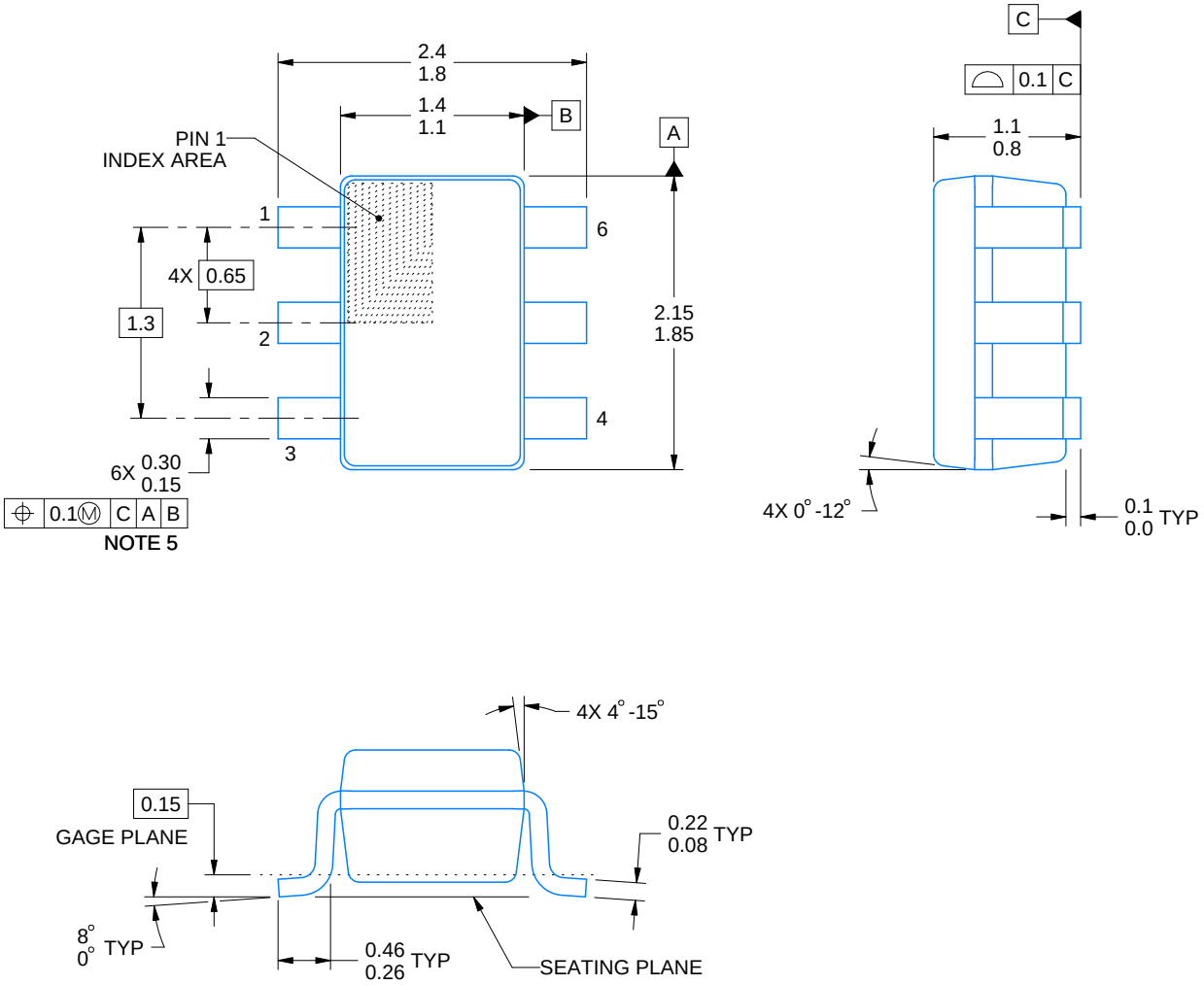


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

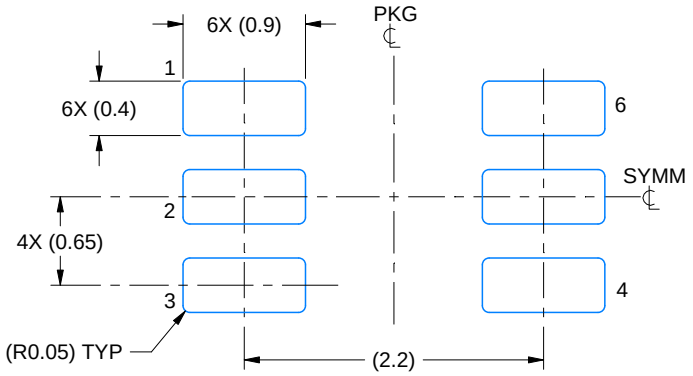
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



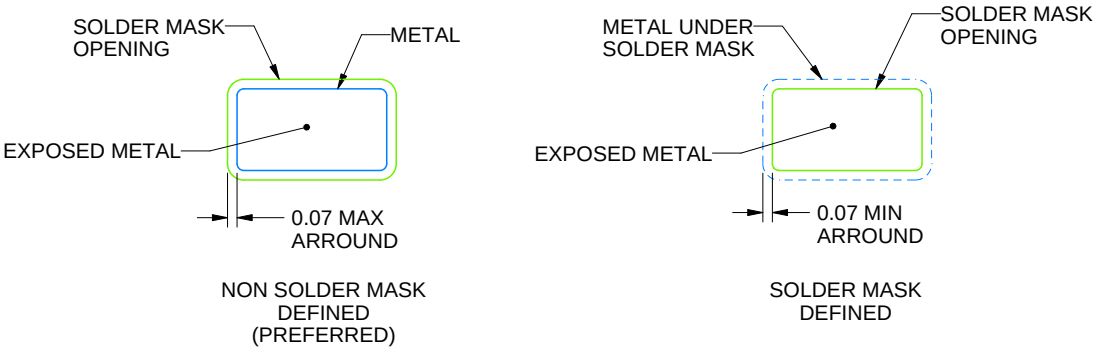
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

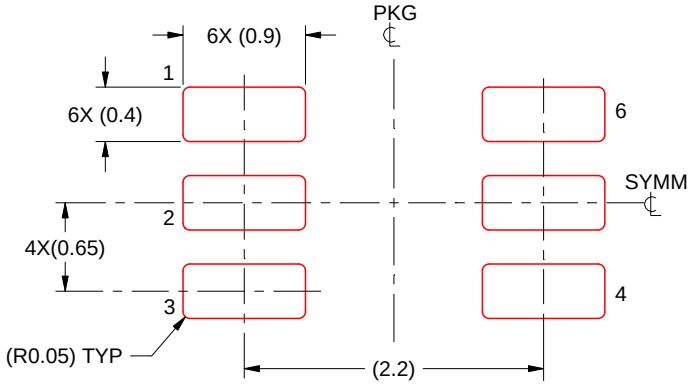


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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